Power Pulsing using Saltro16 and future power pulsing possibilities with the GDSP.

The Present

The Saltro16 – overview

Power Pulsing with the SAltro16

Ideas for the Future

Industrial Trends in Microelectronics

Projections and ideas for the future – The GDSP.

GDSP Power Pulsing possibilities

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Saltro16

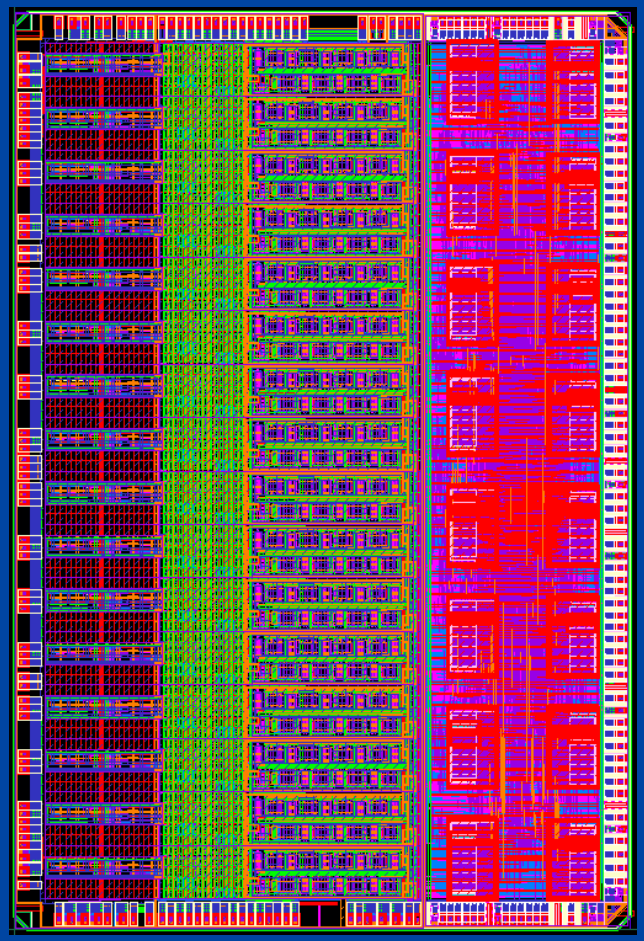
Goal :

To demonstrate integration per channel of an analog front-end, an ADC and digital signal processing in a single chip.

Data processing of 100us of data sampled at 10MHz.

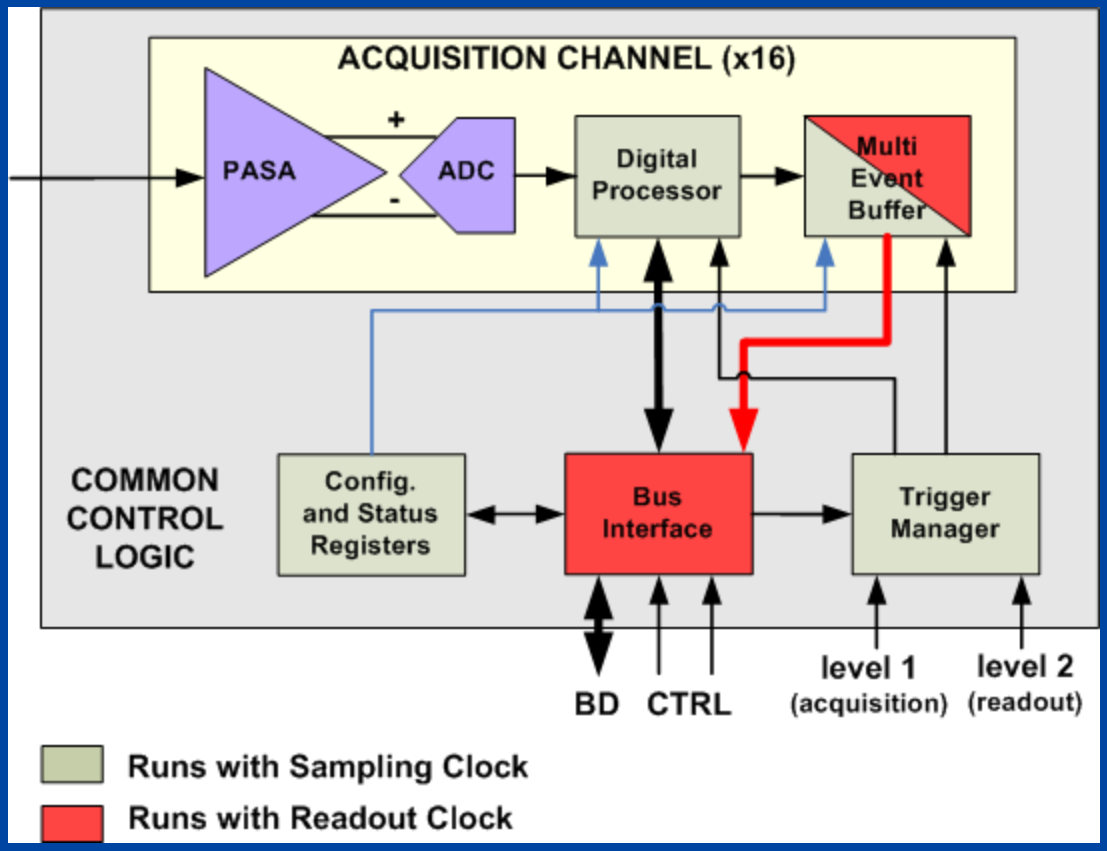
Prepare ideas for TPC readout in the ILC & CLIC

16 channel demonstrator chip designed in 2009-2010, recently received back from the foundry awaiting test.



Luciano Musa …… **S-Altro Specifications and Architecture**
Paul Aspell …… **Coordinator of design team.**
Massimiliano De Gaspari ……. **Front-end + ADC**
Hugo França-Santos ……... **ADC core**
Eduardo Garcia …… **Data Processing & Control**

SAltro16 Architecture



Technology :
IBM 130nm CMOS 8RFDM

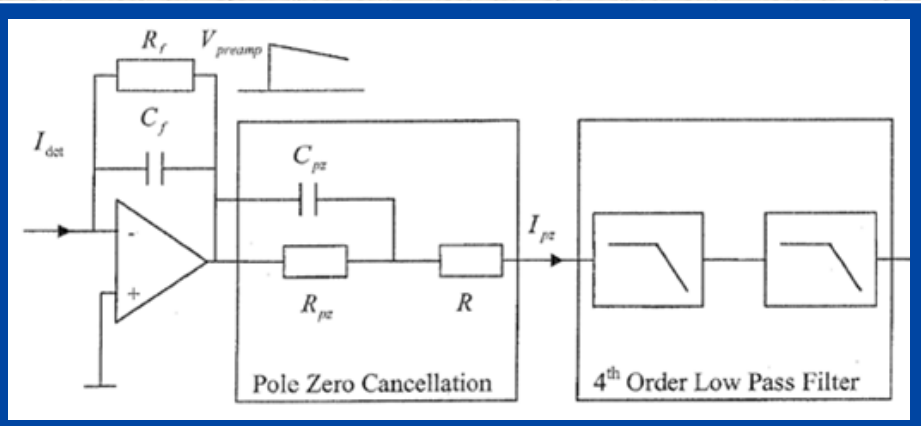
- 16 Channels.
- Sampling : 25us @ 40MHz, 100us @10MHz.
- ADC : 10 bits per sample.
- Level 1 commences sampling of a data-stream.
- 1008 (max) samples per data-stream.
- DSP for zero suppression.
- 40 bit word data packets containing timestamp and length.
- Possibility to by-pass DSP to have raw data.
- MEB (1024*40 RAM).
- Max. storage of 4 non-zero suppressed data-streams.

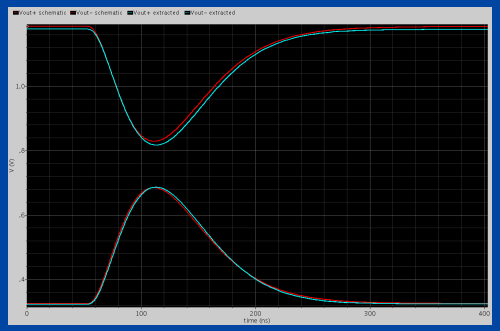
or

- Max. storage of 8 zero suppressed data-streams and/or with reduced data-stream length.
- Level 2 must arrive before next Level 1 in order to keep the data.
- <80 MHz readout on 40 bit CMOS bus.

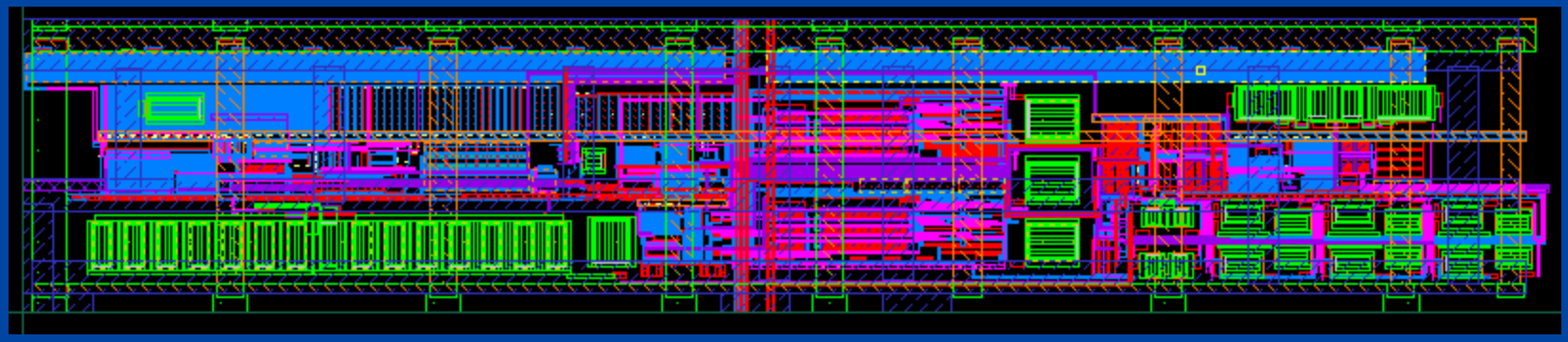
Saltro demonstrator Preamplifier/Shaper

- Single-ended input, differential output
  - Dual polarity
  - 4 Gain options : 12, 15, 19 & 27mV/fC
  - 4 Shaping times : 30, 60, 90 & 120ns.
  - Linearity <1% to 150 fC
  - Shutdown mode (for power pulsing via a duty cycle clock)
  - Preamplifier enable (bypass shaper)





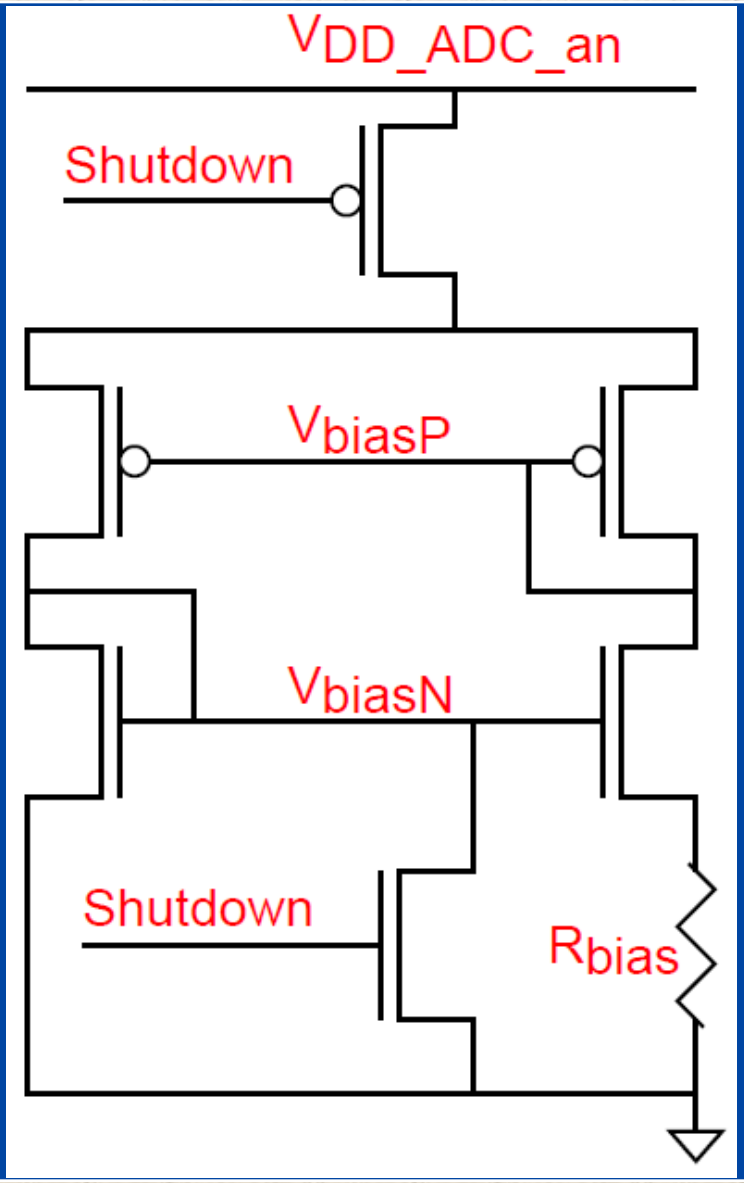
Size: 1100um X 210um Power: 8.4mW/channel Supply: 1.5V



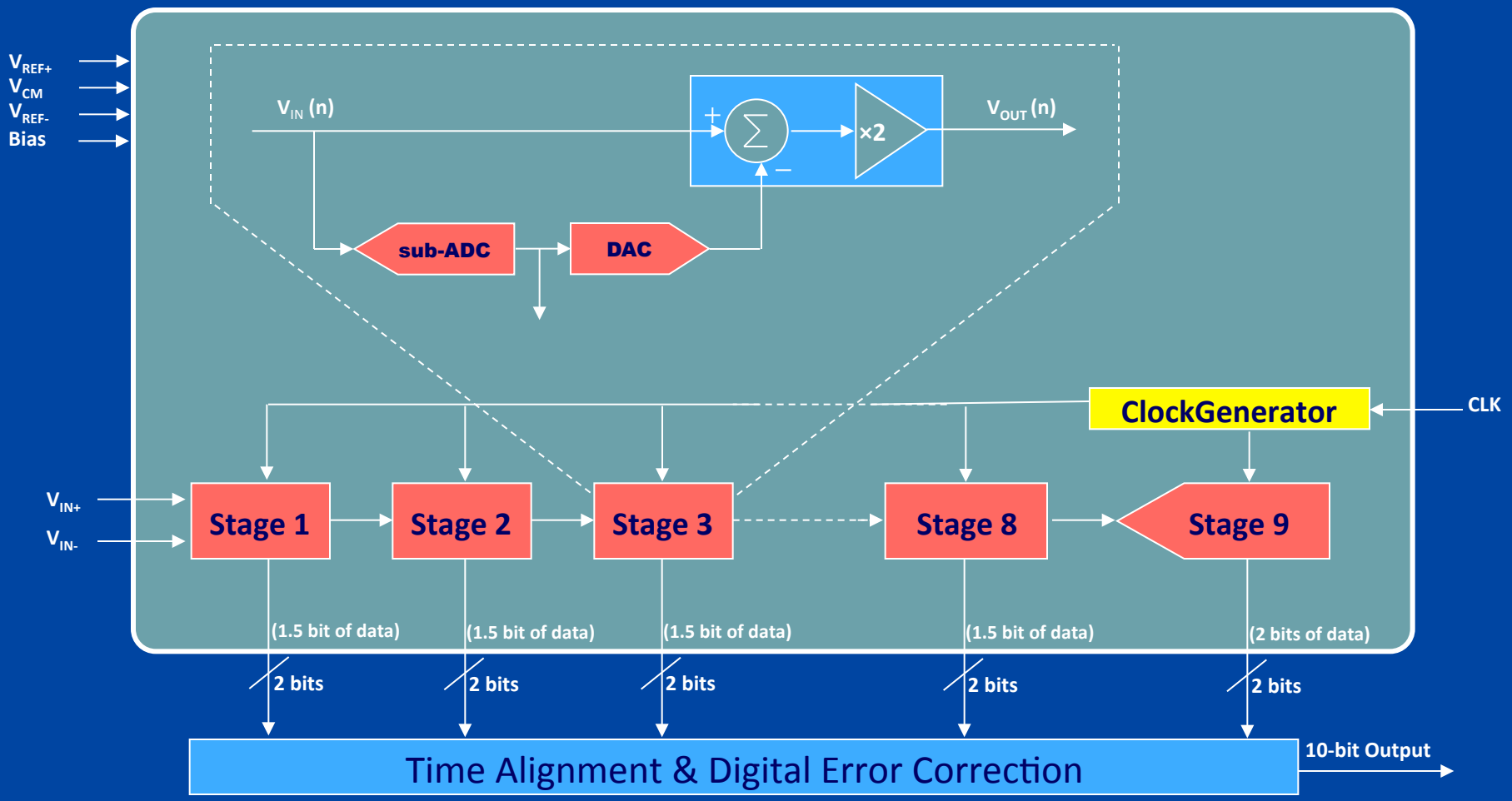
Original PASA design from G.Trampitsch

PASA: Shutdown switch

- The shutdown line controls the main beta-multiplier.
- VbiasP and VbiasN are later replicated by several current mirrors, in order to provide biasing to each stage of the PASA.
- Therefore, the shutdown line can remove the biasing to the whole PASA.



Pipeline ADC



9 ENOB, 40MHz, 1.5V supply, 34mW power , 0.7mm² area

Power pulsing possible through bias pin.

A 10-bit 40MS/s Pipelined ADC in a 0.13µm CMOS Process – TWEPP 2009

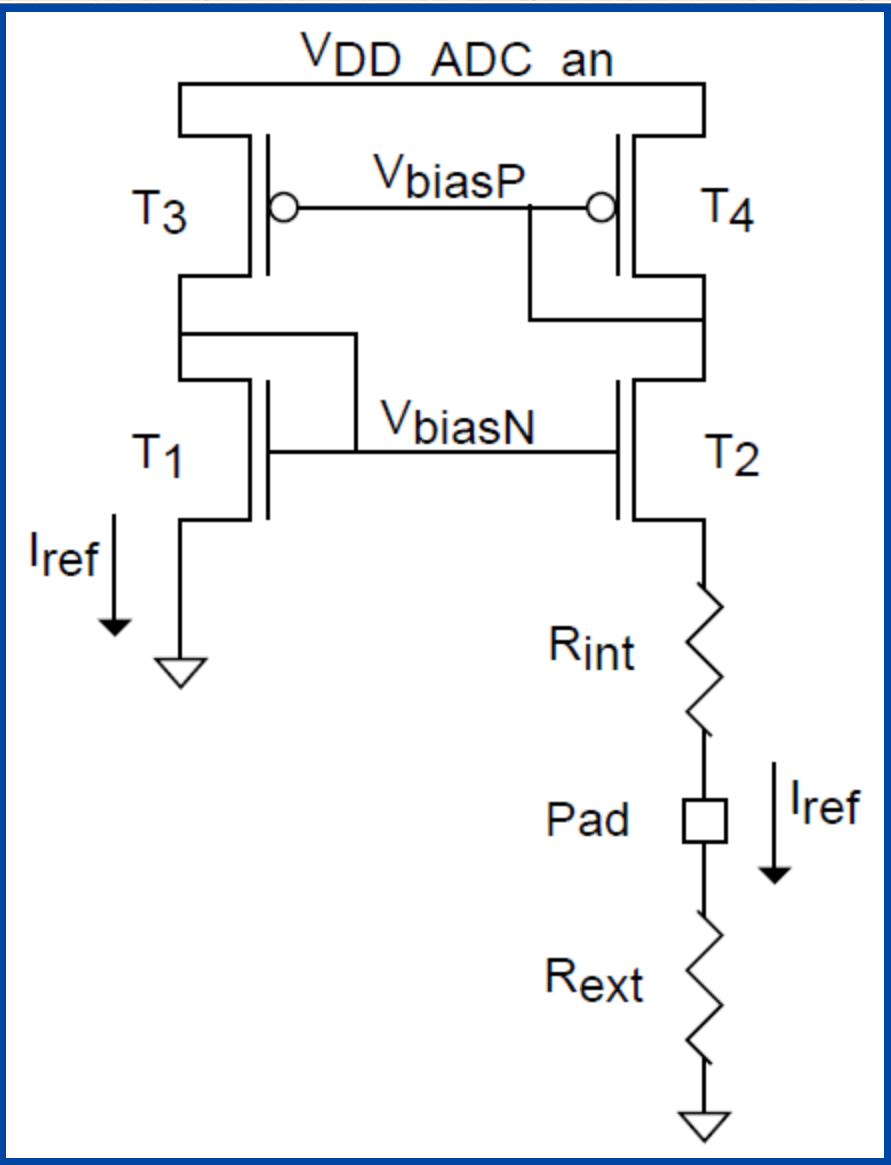
Hugo França-Santos

ADC bias circuitry (beta-multiplier)

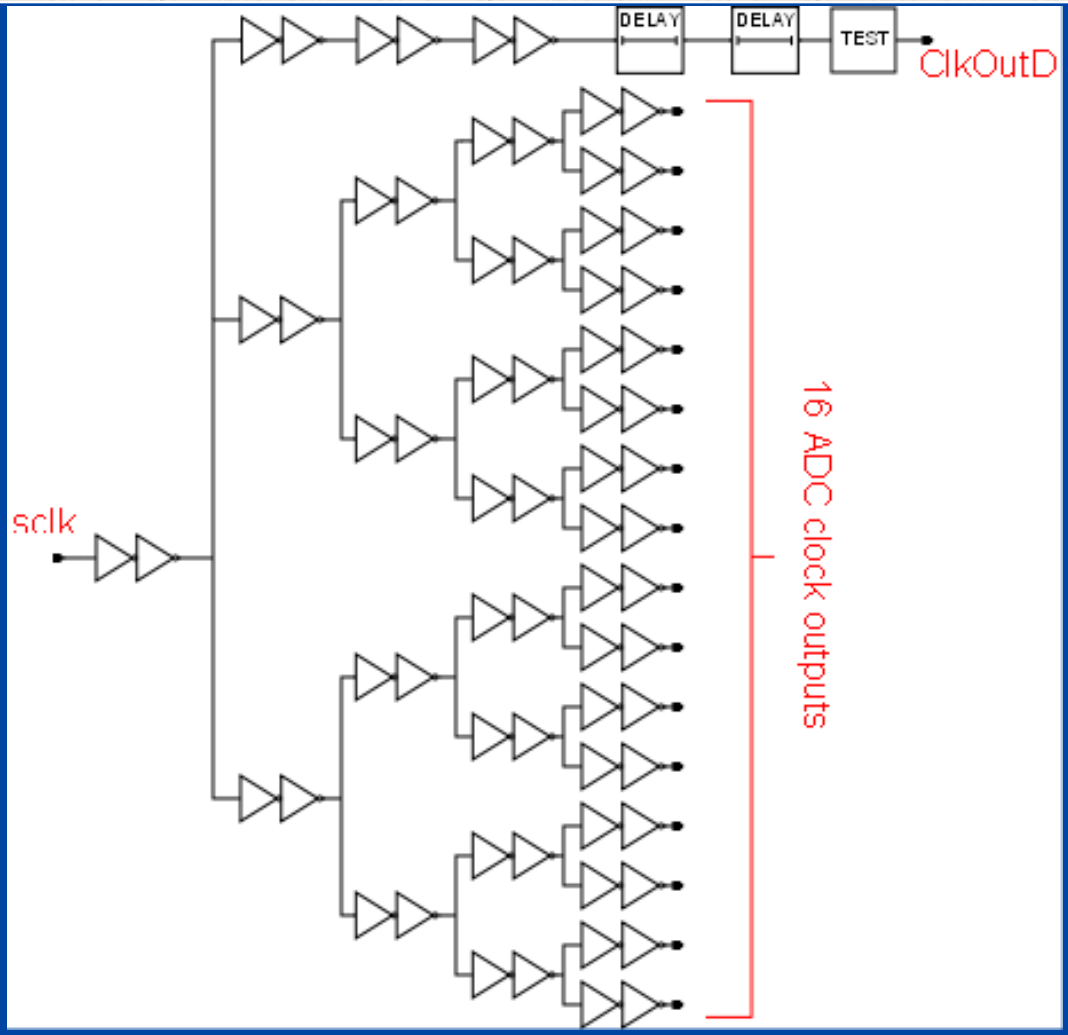
The off-chip resistor is meant to adjust externally the power consumption of the ADC,

Different sampling frequencies ➔ change resistance to adapt the power consumption

Power-pulsing ➔ disconnect the external resistor to stop the biasing current



Saltro Clock Tree



Buffer the clock to the 16 channels, deliver a delayed clock (typical: 600ps) to the digital block. Fully symmetrical structure (also in layout).

PASA + ADC + Clock Tree

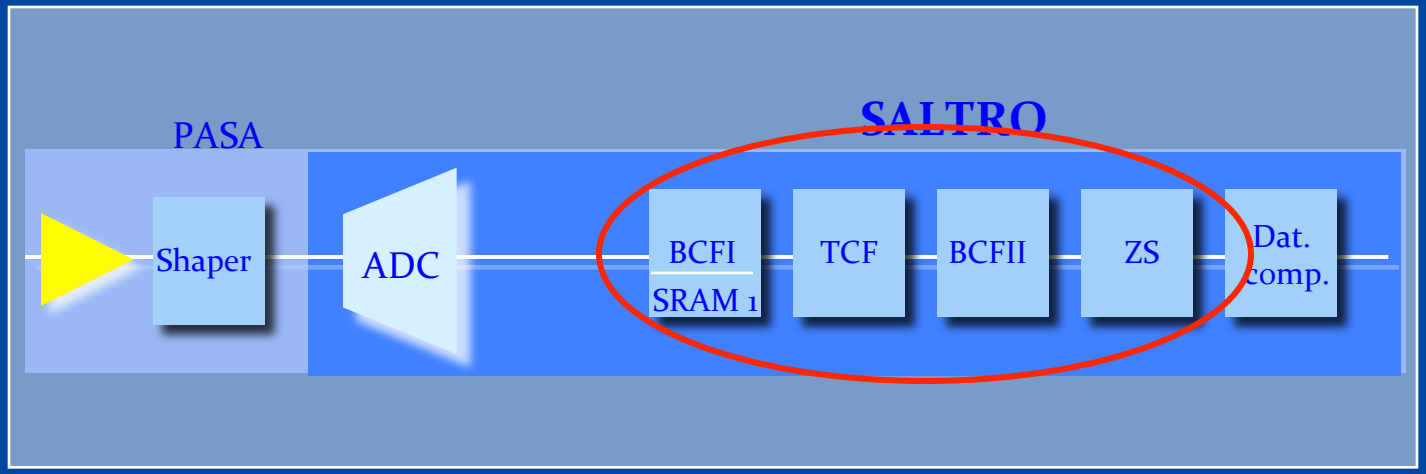
	40MHz	Shutdown
PASA	8.4mW	120uW
ADC Analog	36mW	1.2mW
ADC Digital	580uW	3.2uW
Error Correction	180uW	1.2uW
Clock Tree	383uW	0.8uW

Power consumption per channel (except clock tree).

@ 40MHz: 3kΩ ADC bias resistor
@ Shutdown: PASA shutdown switch, ADC bias resistor disconnected, no clock

1.2mW ADC analog power in shutdown mode: due to the start-up circuitry in the beta multiplier, which sets the lower limit to the bias current.

DP functions



Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to very long ion tails.
Baseline correction 2	Reduces baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.

Eduardo Garcia

DSP

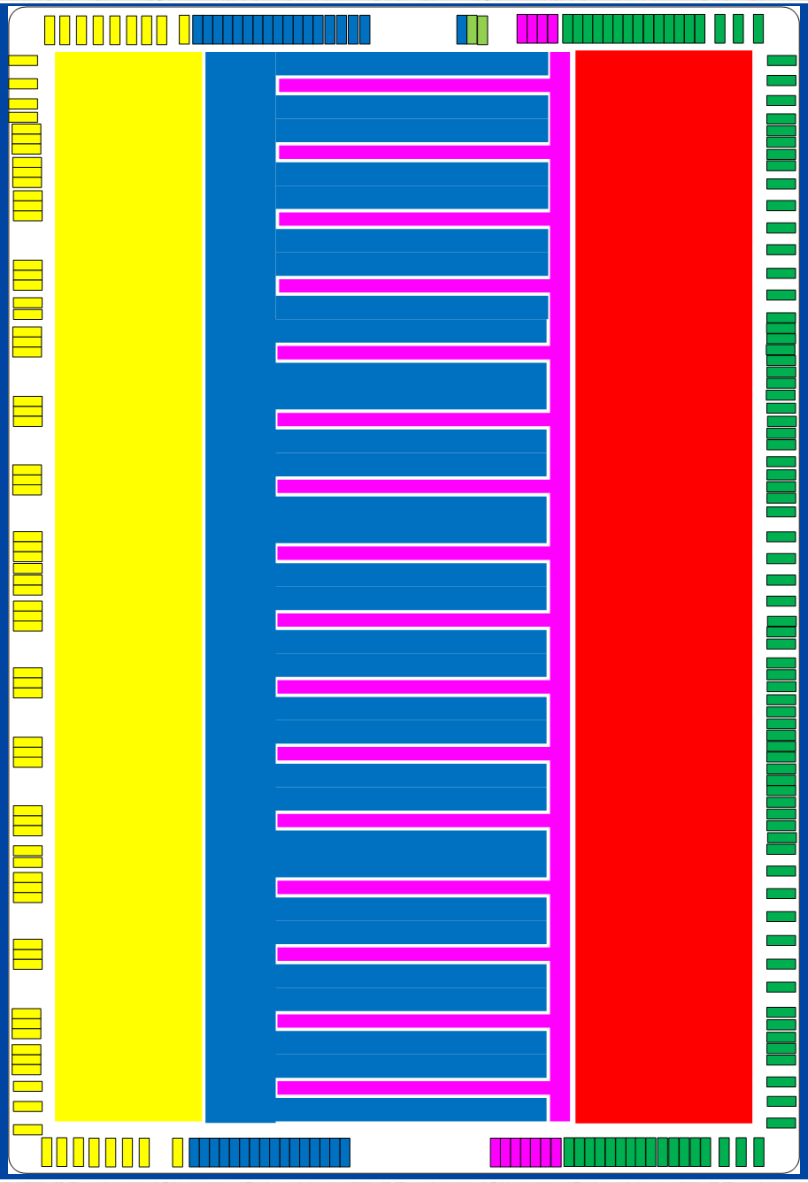
Sclk = 50MHz
Rdoclk = 90Mhz
Toggle probability: 0.3

VSupply	50MHz	0MHz
1.5V	118.6mW	0.41mW
1.2V	49.8mW	0.17mW
1.0V	34.4mW	0.12mW
0.8V	21.3mW	0.07mW

Power consumption of the DSP block , including pads and memories.
The value @1.5V,50MHz is simulated by encounter. All other values are calculated using the simulation of a NAND gate as reference.

Eduardo Garcia

SAltro16 Power & Power Domains



Power domains:

PASA analog

ADC analog

ADC digital

Digital core

Digital Pads

PASA ~8mW/ch,

ADC 36mW/ch @40MHz

Digital functions ~118mW

Total power ~ 800mW

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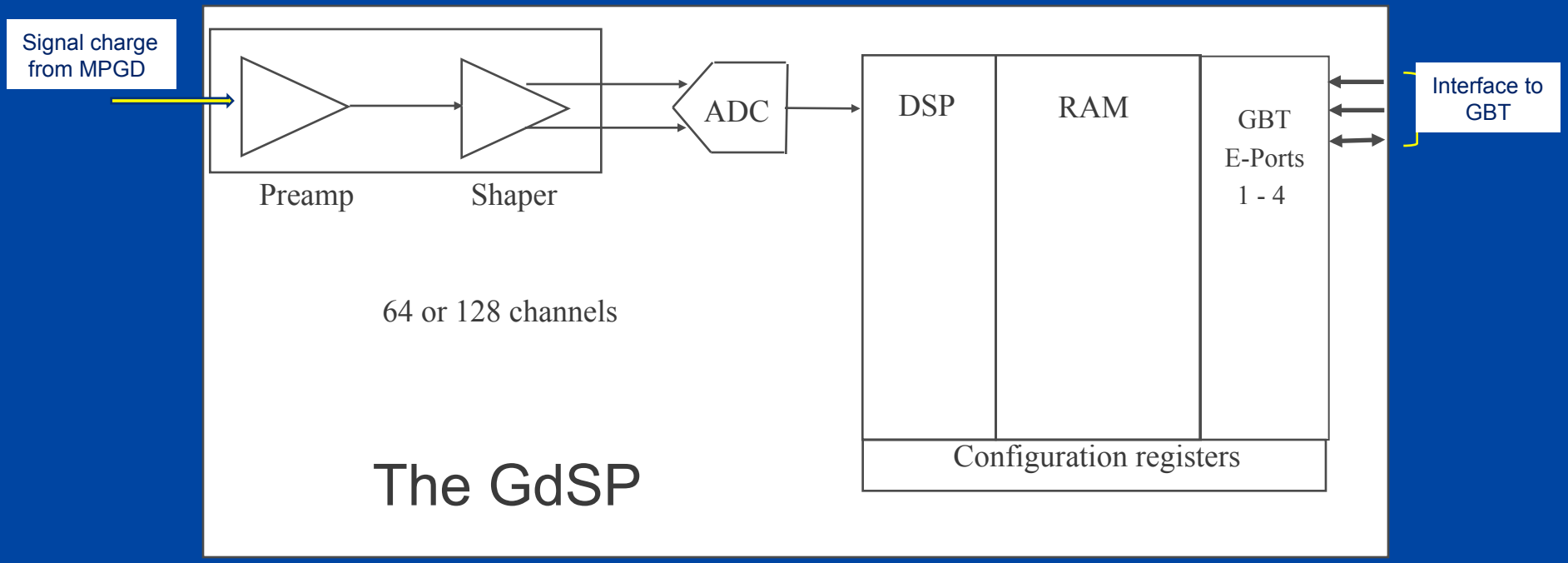
Projections and ideas for the future – The GDSP.

GDSP Power Pulsing possibilities

The GdSP (a possibility)

(Gas Detector Signal Processor)

The GdSP, a 64 – 128 channel front-end ASIC designed specifically to tackle the needs of MPGD readout in the next decade.
A natural evolution of the SAltro architecture.



The GdSP is a possibility due to :

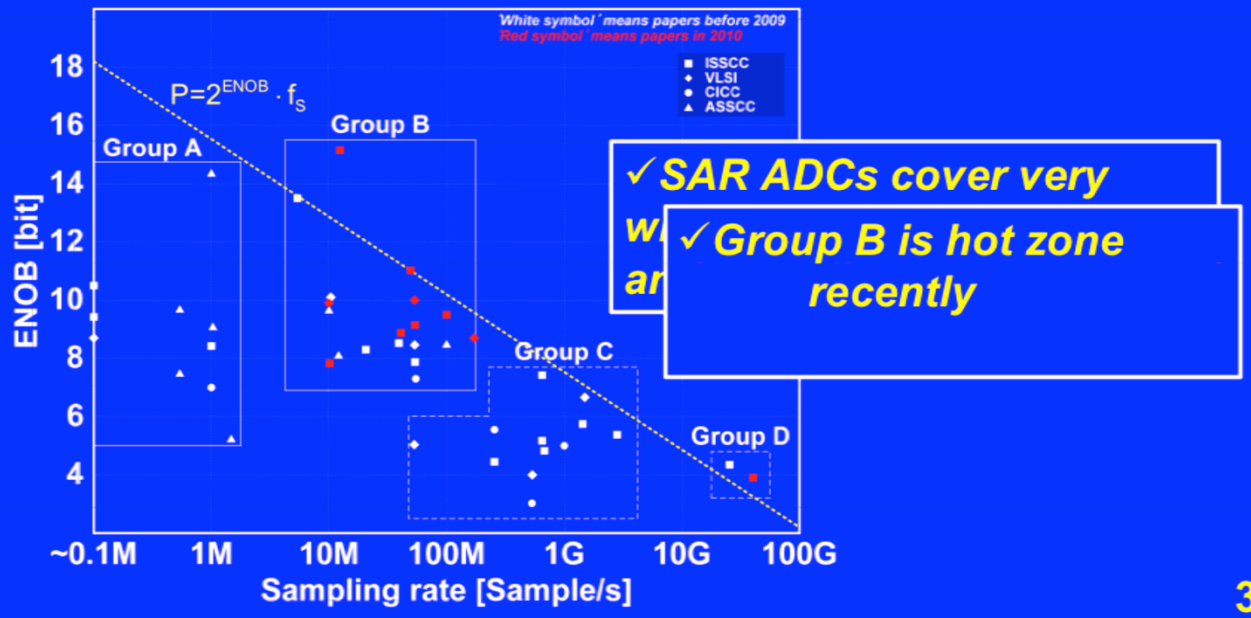
i) Very rapid IC trends in ADC power efficiency and Power Management techniques.

ii) Optimising the the full chip for static power consumption before applying power pulsing.

ADC Trends

Trend II : Applications

- Group-A. Sensor network, Bio-medical
- Group-B. Video, Substitute for 'Pipeline & $\Delta\sum$ ADC'
- Group-C. UWB, SERDES, OFDM receiver, Magnetic recording
- Group-D. Optical Communication



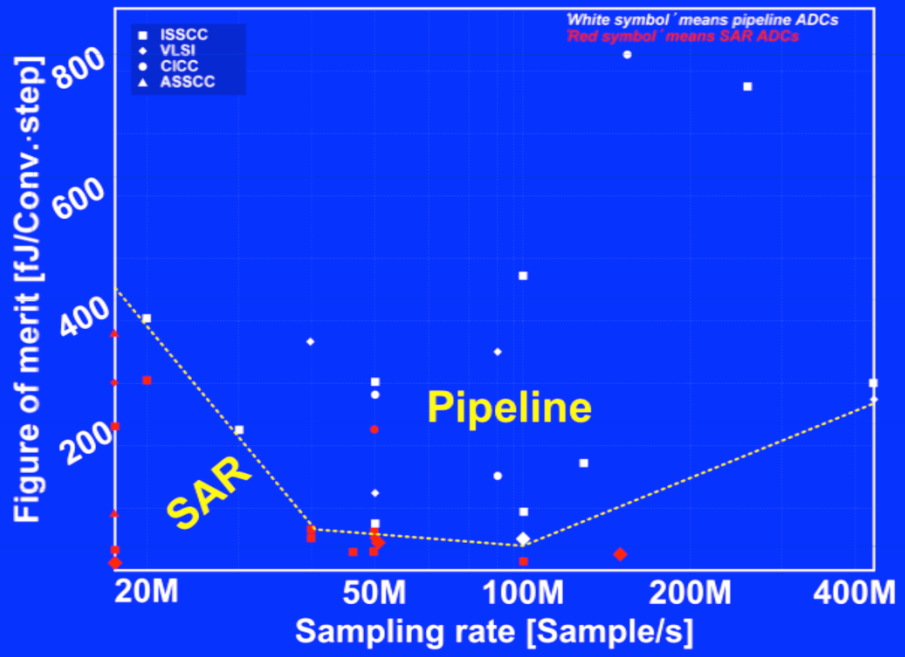
3

Source : A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.* CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

ADC Trends

Trend III : FOM Comparison

- SAR ADCs → from Group B : 18 papers
- Pipeline ADCs → 8-12b, 20-500MS/s



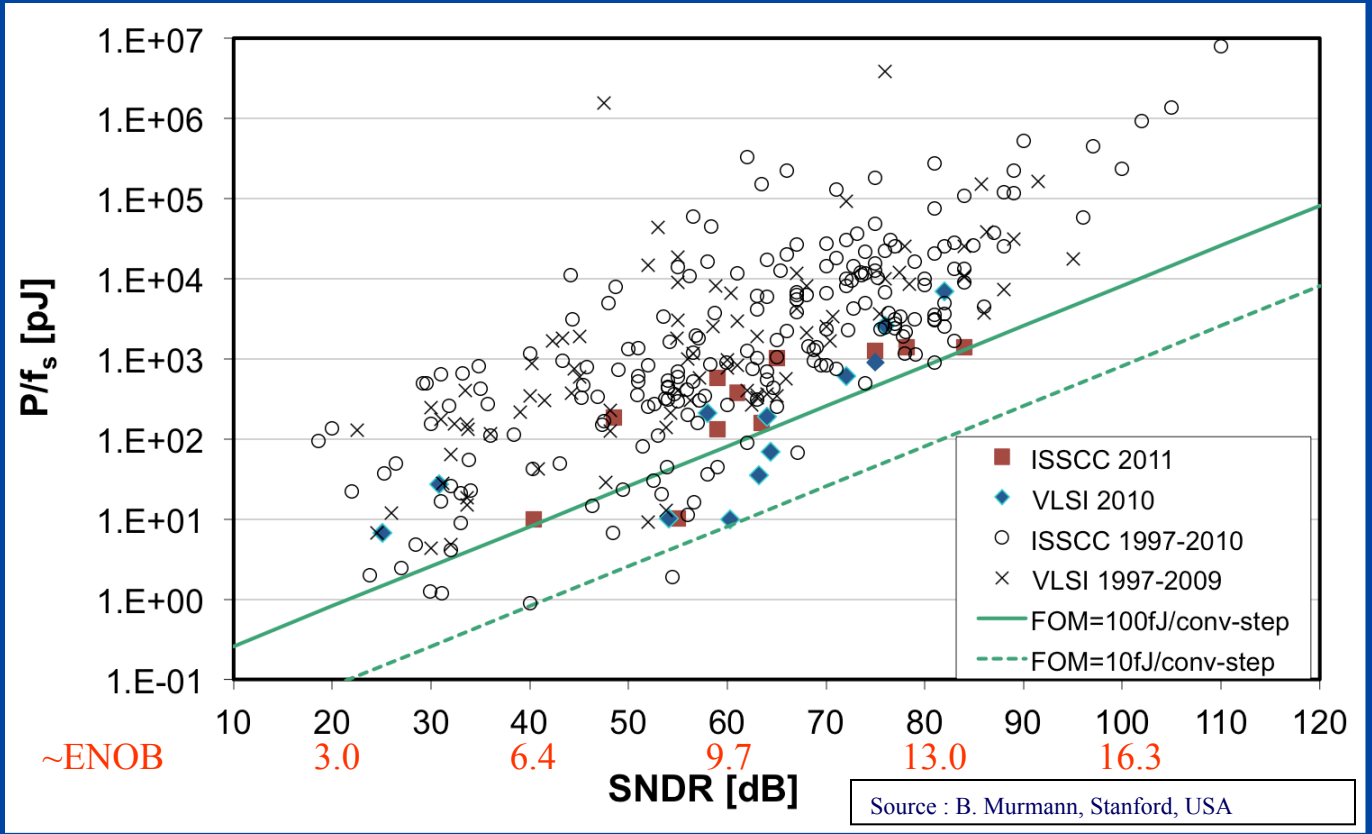
4

Source : A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.* CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

ADC Trends

- FOM ~ P / (2^{ENOB}. 2BW)

- 1pJ is high
- (~40mW @ ENOB 9, 40MS/s)
- 100fJ is good
- (~4mW @ ENOB 9, 40MS/s)
- 50fJ excellent
- (~2mW @ ENOB 9, 40MS/s)



State of the art :

A 30fJ/conversion 8b 0 to 10MS/s Asynchronous SAR ADC in 90nm CMOS. P. Harp et. al. IMEC ISSCC 2010
[They measured 69uW at 10MS/s,]

A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.*
CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

ADC Specifications

Sampling rate	**40Msps**
ENOB	9
Power Consumption	4mW/channel

4mW/channel corresponds to a FOM ~ 100fJ/conversion

Either :

Buy an IP block to satisfy these specifications.
Collaborate with an institute who is able to design to these spec.s.
Design in house an ADC (very challenging)

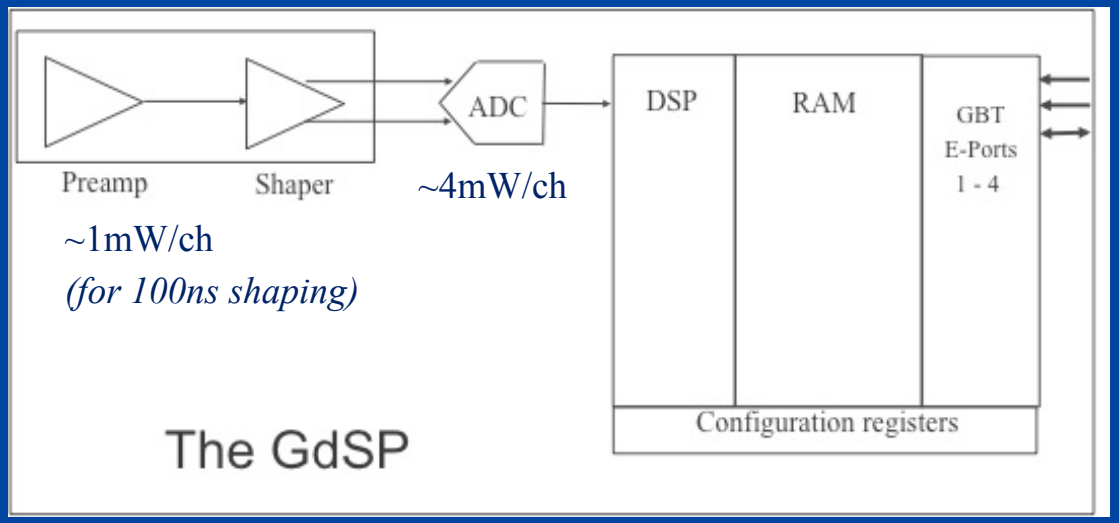
Note : An ADC satisfying these specifications is extremely challenging and exists, as yet, only in publications. Hence it is not expected to be available in the form of an IP block immediately. However it is expected in the near future.

Front-End power optimisation

- Front-end power can be very finely tuned but requires detailed knowledge of the sensor characteristics.
  - » Total input capacitance (sensor + coupling to neighbours + board) is required to optimise the input transistor current.
  - » Charge collection properties are required to make the correct choice of shaping time. If the shaping time is too small ballistic deficit will degrade S/N.
- Input transistor current scales with detector capacitance and charge collection time. Approx. 10μA/pF for 25ns shaping and ~ 2.5μA/pF for 100ns shaping .

Rough estimate of front-end power budgets		
Electrode capacitance	for 100ns shaping	for 25ns shaping
1pF	12μW ??	48μW
10pF	120μW	480μW
20pF	240μW	1.6mW
50pF	800μW	3.2mW

Estimate for optimal future power (static)



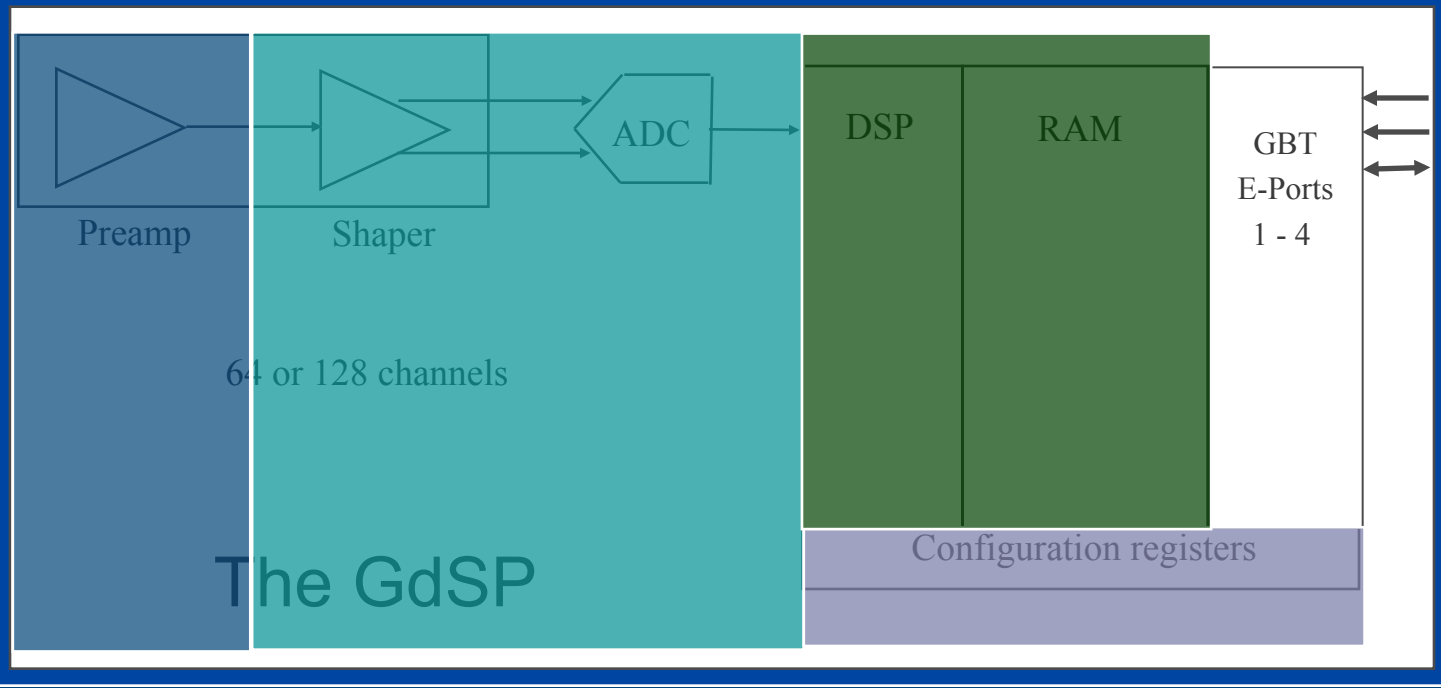
64 channels = Analog power ~ 320mW + Digital power ~ a few hundred mW.
Approx. ~500mW / chip.

128 channels = Analog power 640mW + Digital power ~ some hundreds mW.
Approx. ~900mW / chip.

Should be possible to get 7-8 mW/ch for everything on a 128 ch chip.

Power management & pulsing may then be applied to reduce power further.

Power Pulsing : Power Management with multiple power domains



Preamp > Reduce current via bias control, important to maintain a low impedance on the electrode.

Shaper > Reduce current to approx. zero via bias control. Vdd could be maintained.

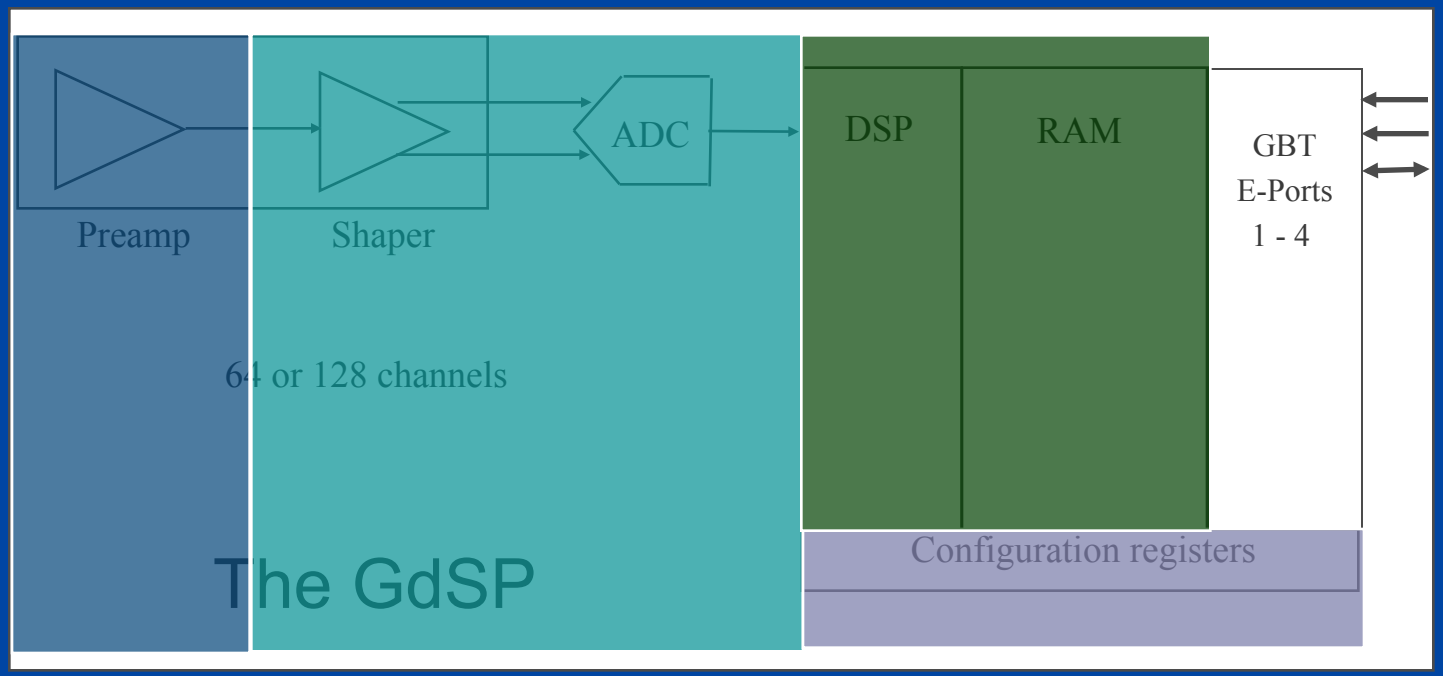
ADC > Stop clock and reduce current to approx. zero via bias control. Vdd could be maintained.

Configuration reg.s > Reduce Vdd to minimum voltage necessary to hold data. Current consumption limited to leakage currents.

Digital logic > Switched off by reducing Vdd to 0V.

Power Pulsing Phases

"Sampling", "Read" and "Sleep" phases controlled by fast synchronous commands through the E-port.



"Sampling" Phase = All modules "Up".

"Non Sampling" Phase = Preamp, Shaper and ADC "Down",

"Read" Phase = Preamp, Shaper and ADC "Down", DSP RAM Configuration Reg.s and E-ports "Up"
"Sleep" Phase = Preamp, Shaper, ADC, DSP, RAM "Down", Configuration Registers and E-port "Up".

Summary

- The SAltro16 demonstrator chip exists and is awaiting test..
  - » Comprises 16 channels of Front-end + ADC + DSP on the same chip.
  - » Chip return back from foundry for beginning of 2011.
  - » Many things can be studied using the SAltro demonstrator :
    - – Internal power pulsing on front-end and ADC via clock and bias control.
    - – The power consumption of the present 16 channel chip is about the same absolute value as future chips with more channels. This makes the demonstrator useful for groups studying external power pulsing.
    - – GEM properties : capacitance, charge collection time, optimal shaping, channel to channel coupling etc.

- The future looks favourably on the SAltro architecture, see GDSP.
  - » The industrial trend is with us continually looking for ways to reduce power.
  - » The ADC remains the critical element w.r.t. power, however state of the art ADCs are becoming more and more power efficient.
  - » Power management within a chip is now common place in modern industrial chips and could be a useful tool for power pulsing.

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Both the SAltro16 and the GDSP will be presented in more detail as 2 separate talks in the Saltro meeting this afternoon.