KPiX - An Array of Self Triggered Charge Sensitive Cells Generating Digital Time and Amplitude Information

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Introduction

* KPiX is a multi-channel system-on-chip, for self triggered detection and processing of low level charge signals. It is motivated by the Silicon Detector (SiD) for the International Linear Collider (ILC).
* A digital core controls all operations according to parameters stored during set-up. This allows to match the chip to signals from a variety of sources. A variety of options, selectable by register settings, have been added over several prototype cycles.
* The only external control signals are system clock, reset and command. Data output is serial.
* Low average power consumption (<20 µW per channel) for ILC operation is obtained by lowering currents by a factor 1/100 between beam spills while keeping the supply voltage fixed. This is achieved by changing the currents in the bias generator. The current is made to drop slowly, with a decay time-constant ~10 us, to limit voltage spikes caused by the cable impedance.
* The chip is designed to be bump bonded to a Si-sensor, or to a hybrid for large area detectors (RPC's, GEM's). This avoids an extensive cable plant for the detector signals, resulting in significant savings in cost for large systems and a reduction in detector mass. The absence of cables to the detector elements also simplifies the task of eliminating pick-up noise.
* Range- and Noise-Specifications:

  Peak Signal (Dual Range) 10 pC.

  Range Switching (selectable) ~400 fC.

  Noise Floor 0.15 fC (1000 electrons).

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Full System power

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System	Count	Channels	Power [W]
Tracker	29,630	1024	607
EM-Cal	105,863	1024	2168
H-Cal	37,222	1024	762
Muons	9049	64	12
Total	181,764		3549

* The assumption for this table is 20 uW average power per pixel, which is an upper limit for KPiX.
* The plan is to bring power to KPiX through the Yale DC-DC converter, with a step-down ratio of at least 8. With KPiX running at 2.5 V, the total average current is about 150-200 A, depending on conversion efficiency. With a higher step-down ratio the current would drop further.
* The conductors will be sized for a substantially higher peak current. The resulting cable plant would still be quite modest.
* An important feature of the current profile in KPiX is a controlled drop with a time constant of ~10 us, perhaps longer. This is required to limit the peaking due to the cable inductance. Satish Dhawan at Yale tested this with a model setup of cable and current profile and found peaking of ~0.5 V.

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Prototypes and Special Features

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* Prototypes of 64, 256, 512 and 1024 pixels (cost)
* Option for a common external trigger.
* On-chip temperature sensor
* Allow DC operation
* Choice of 8 front end currents
* Choice of 4 differentiation times in shaper
* Choice of 8 hold times
* Choice of 2 integration time constants (0.5 and 0.2 us)
* Factory installed solder bump-bonding pads
* Lay-out improvements to achieve good uniformity of response for all pixels and buckets

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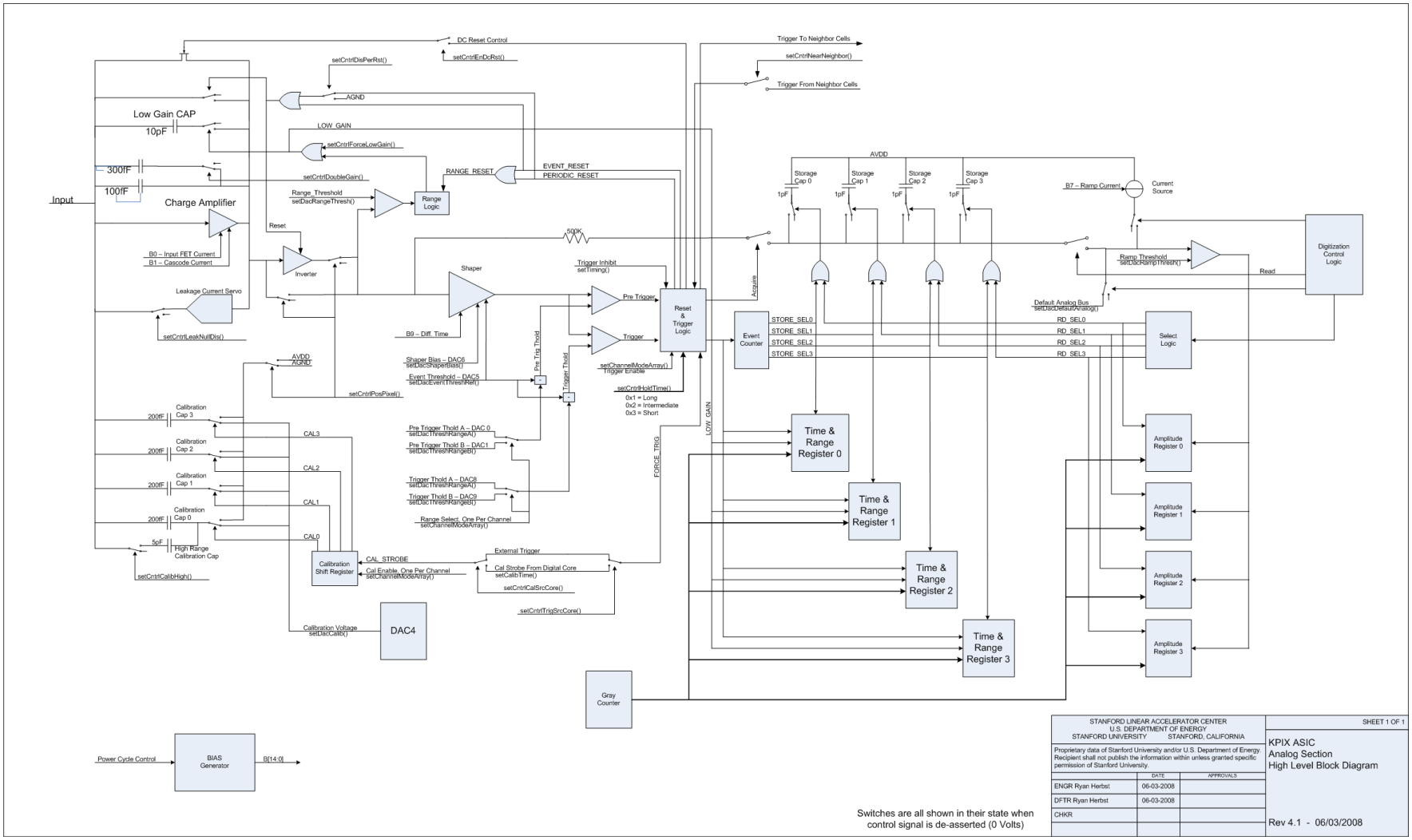
Simplified Block Diagram



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Charge Amplifier Block

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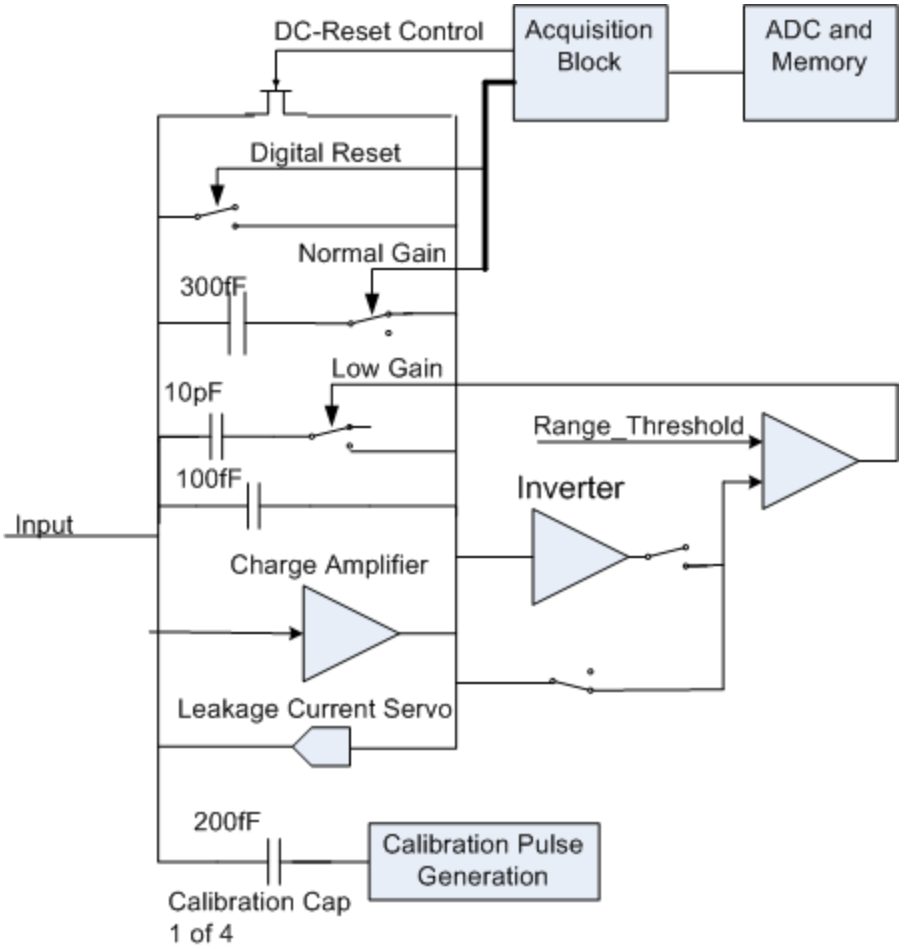
* The incoming signal is picked up by the charge amplifier and stored in the feedback capacitor (default ranges 100 fF and 400 fF).
* If the default range is exceeded, a 10 pF capacitor is automatically added to the feedback to extend the range to 10 pC.
* For negative-polarity signals, an inverter is inserted after the charge amplifier. The polarity of the calibration signal is reversed too.
* For DC-coupled signals, the leakage is compensated by a servo circuit. The amount of leakage is determined with no signal present and held during the signal period.
* A precision calibrator sends up to four signals with amplitudes and timings as defined during the set-up cycle.
* Digital reset during power-up and after each triggered event. Can be executed before each beam bunch for ILC operation.
* Option for DC reset for non-bunched signals, e.g. cosmic rays, radioactive source data.
* Periodic and digital resets are inhibited immediately after each trigger (controlled by the acquisition block)..



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Data Acquisition Logic

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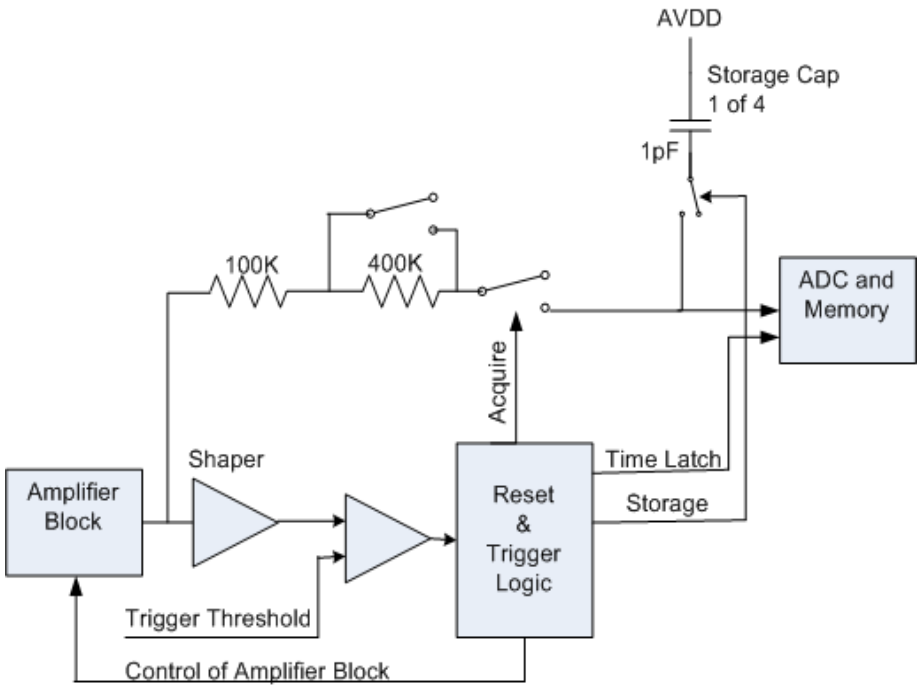
* The charge amplifier signal is amplified, shaped and sent to the trigger stage.
* For signals above trigger threshold, the digitally controlled acquisition cycle is started. After a wait period, the signal is acquired in the storage capacitor. The coupling elements form a low pass filter. Two integration constants (0.5 us and 0.2 us) can be selected.
* One of two threshold levels is selectable in each cell. High-low discrimination system to catch potential triggers early to inhibit digital and DC resets.
* For the tracker application, the trigger is carried over to the neighboring cells to catch low level spill-over signals below trigger threshold.
* After a programmable time interval, the signal amplitude is held in the capacitor and control passed to the next storage capacitor.
* The integration interval is thus precisely controlled, resulting in a stored amplitude proportional to the signal, even if the asymptotic value is not reached.
* A strobe signal is sent to the memory block to record event time.
* Amplitude and time information for up to four events can be stored for each data cycle.



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ADC and Digital Storage

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* The analog information previously stored in 4x1024 capacitors is digitized in four cycles, each for 1024 capacitors in parallel.

* The Wilkinson method is used for the conversion, with a current mirrored into each cell running down the charge in the storage capacitor. A ramp-threshold discriminator detects the transition through zero and causes the content of a common Gray counter to be stored in memory.

* The ADC has 13 bits resolution.

* This method of digitization could proceed independently in each cell, offering the possibility of continuous operation. The four buffers in each cell could be filled and read out on a rotating basis. This would require a major upgrade of the digital core.

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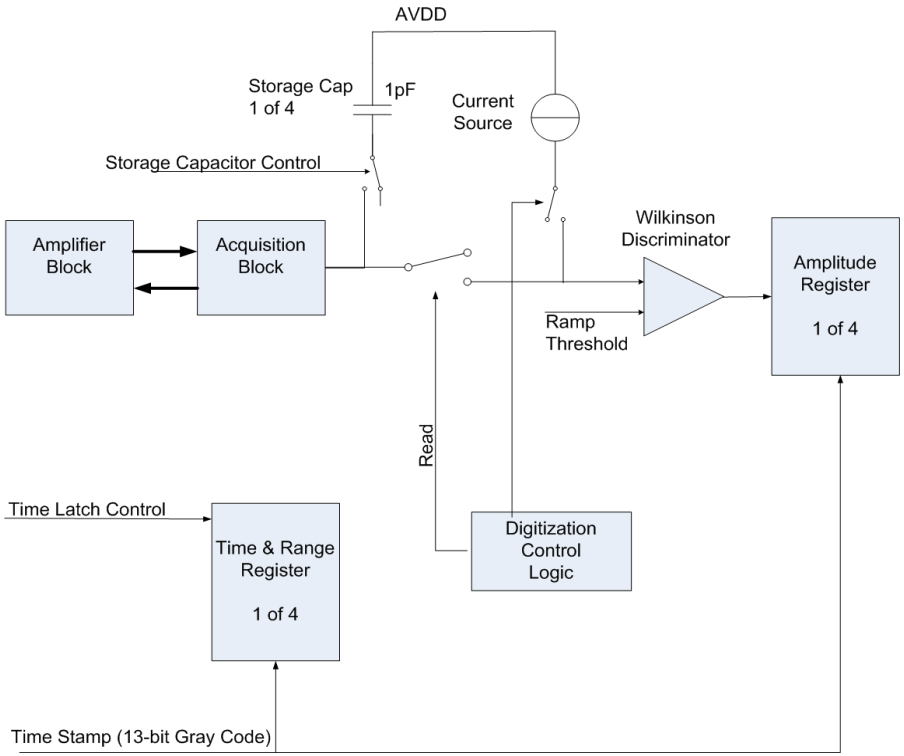

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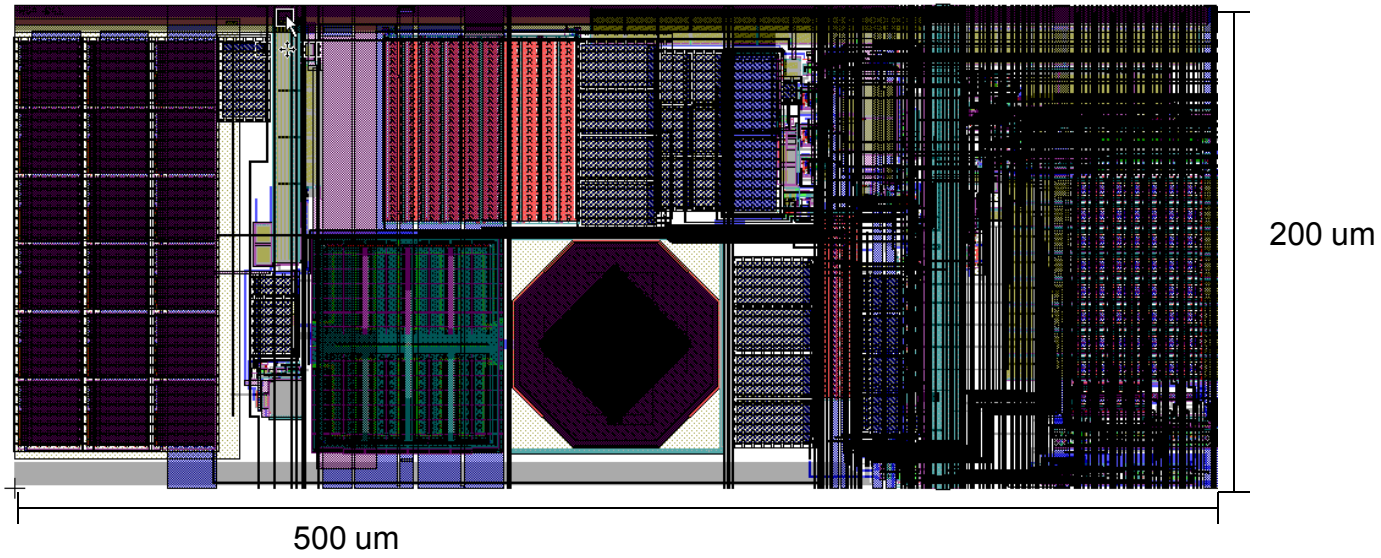
Single Pixel Lay-out



* The leftmost ¾ is the analog section, dominated by signal pad, pad-protection and capacitors, resistors for signal processing. The last quarter is the digital section.

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Measurement Results

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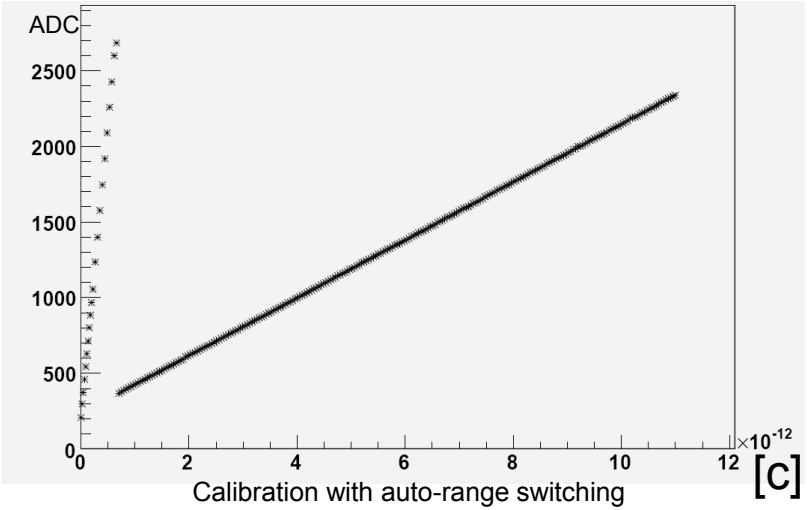
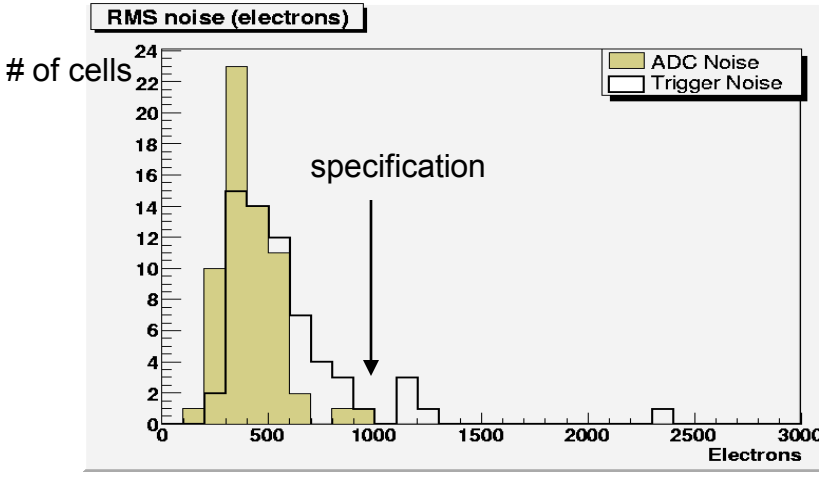
* The figure shows ADC counts as a function of internal high-level calibration signals.
* The automatic range switch takes place at ~0.5 fC (determined by the range threshold).
* RMS values to the linear fit in the two branches are 1 fC for normal gain, 10 fC for low gain.
* The normal-gain noise in high-cal mode is dominated by the 12-bit accuracy of the calibration DAC.



* Measured noise in 64 cells set to high gain mode. ADC branch high-lighted in yellow, trigger branch open boxes.
* The noise in the trigger branch is determined by recording the trigger rate as function of threshold in each of 64 cells and fitting an error function to the data points.
* Most cells are below the specification of 1000 electrons (0.15 fC).



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Si-Tracker and KPiX in SLAC Test-Beam

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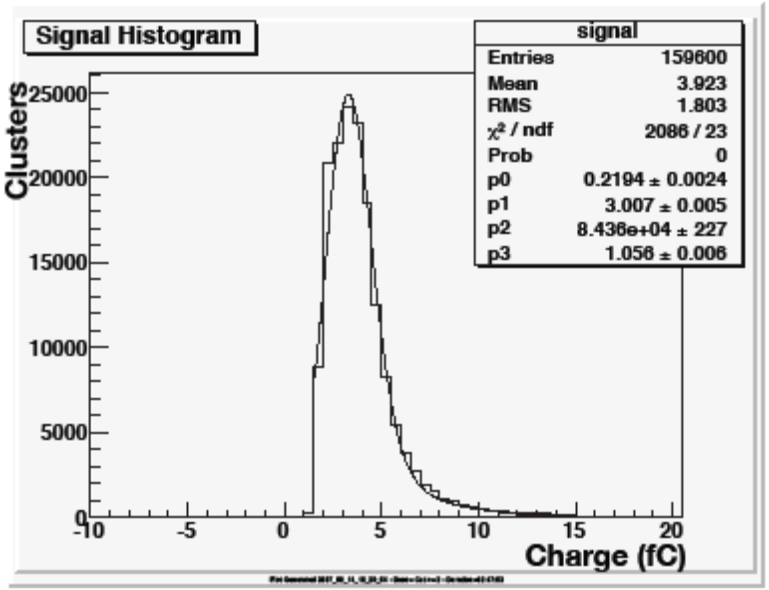
* Three CDF sensors (128 channel) were arranged in layers of vertically oriented strips.
* The data were taken in a SLAC test-beam of 10 GeV e-.
* A synchronous trigger signal 1 ms before beam pulse was used to power-up KPiX.
* An external forced trigger at the correct beam time served as a common data strobe.
* Plotted are double-coincidence clusters of strips (only 15% >1 strip).
* The fitted curve is a Landau distribution convoluted with a Gaussian (noise).



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Signals from Resistive Plate Chambers in KPiX

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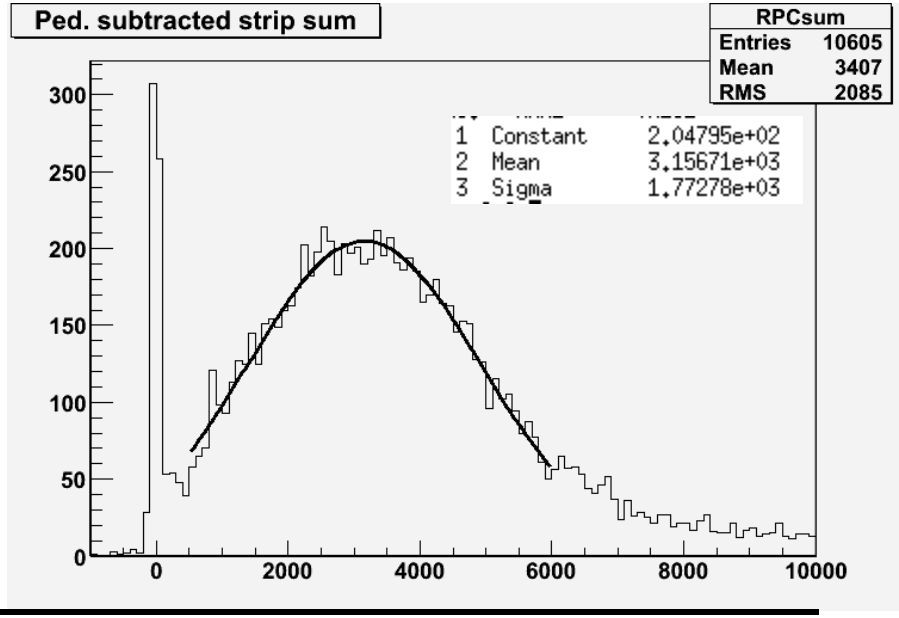
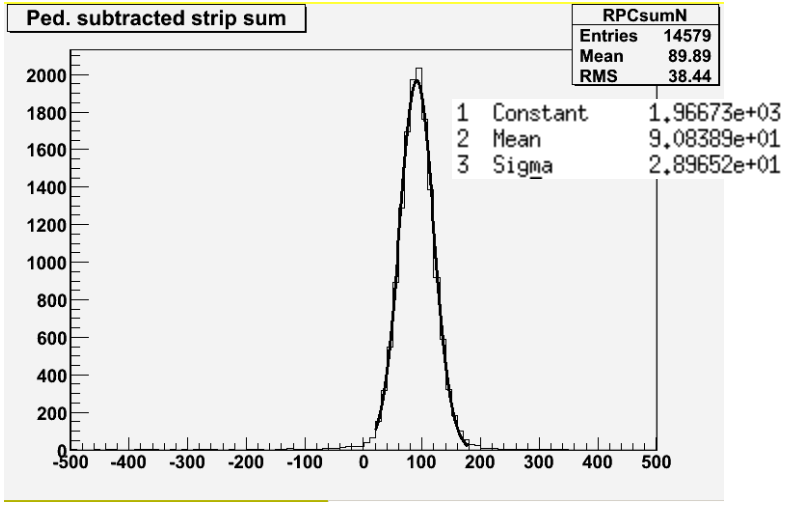
* The plot shows Cosmic Ray data in an RPC connected to KPiX.
* Data taken by H. Band of the Univ. of Wisconsin.
* The RPC's are running in avalanche mode.
* The signal peaks at 3 pC.
* The spike at zero is attributed to tracks missing the RPC.



* The plot shows the noise distribution without a signal in the RPC.
* The variance is 29 fC, to be compared to the expected noise of <10 fC.
* The difference may be due to pick-up.



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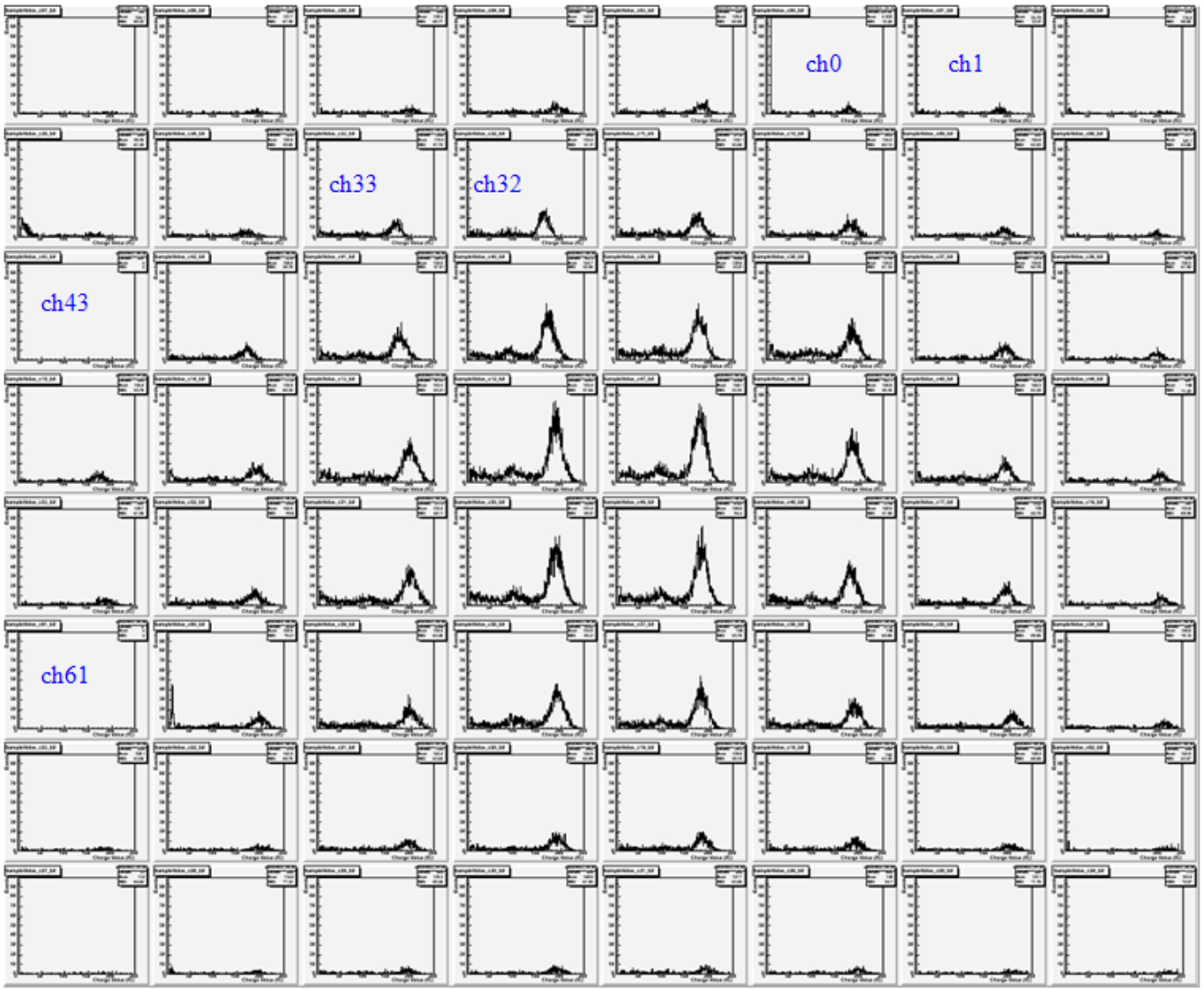
Fe55 into GEM (Seongtae Park UTA)



2010_10_05_14_47_28 Horizontal scale to 250 fC, peak 180 fC

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Version A: 1024 pixels

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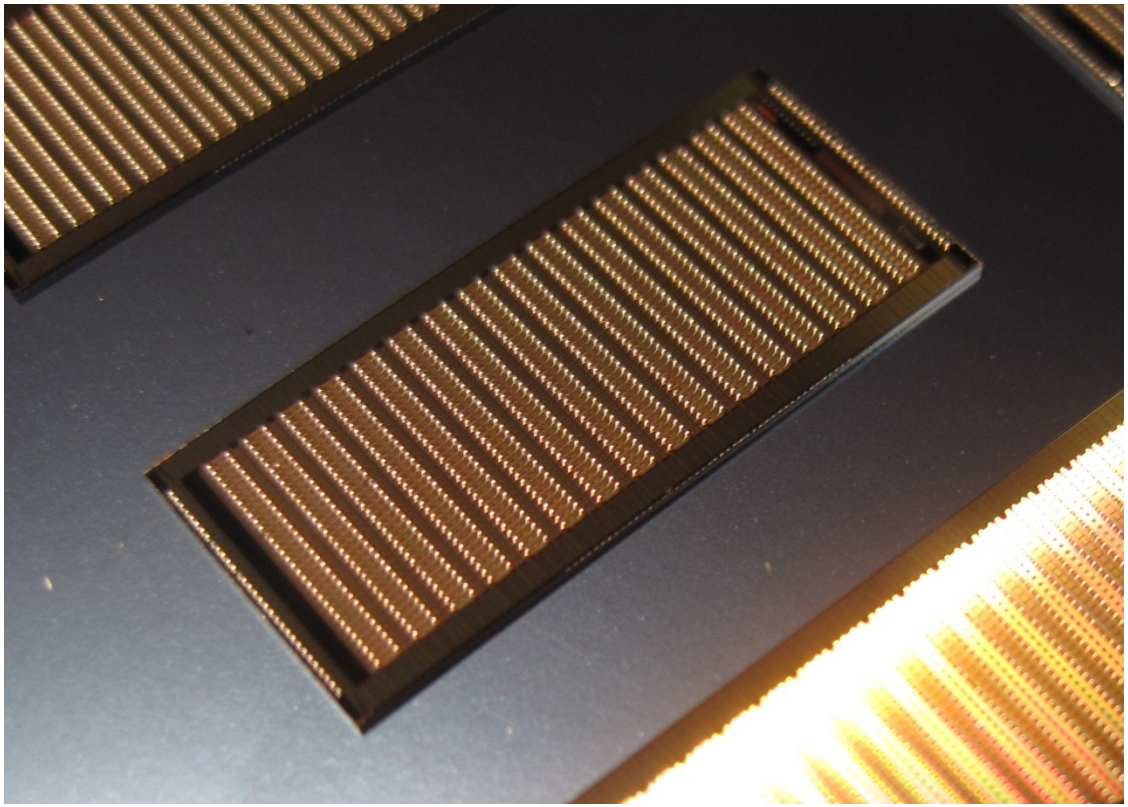

7 mm

18 mm

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Internal Calibration Data for KPiX_A

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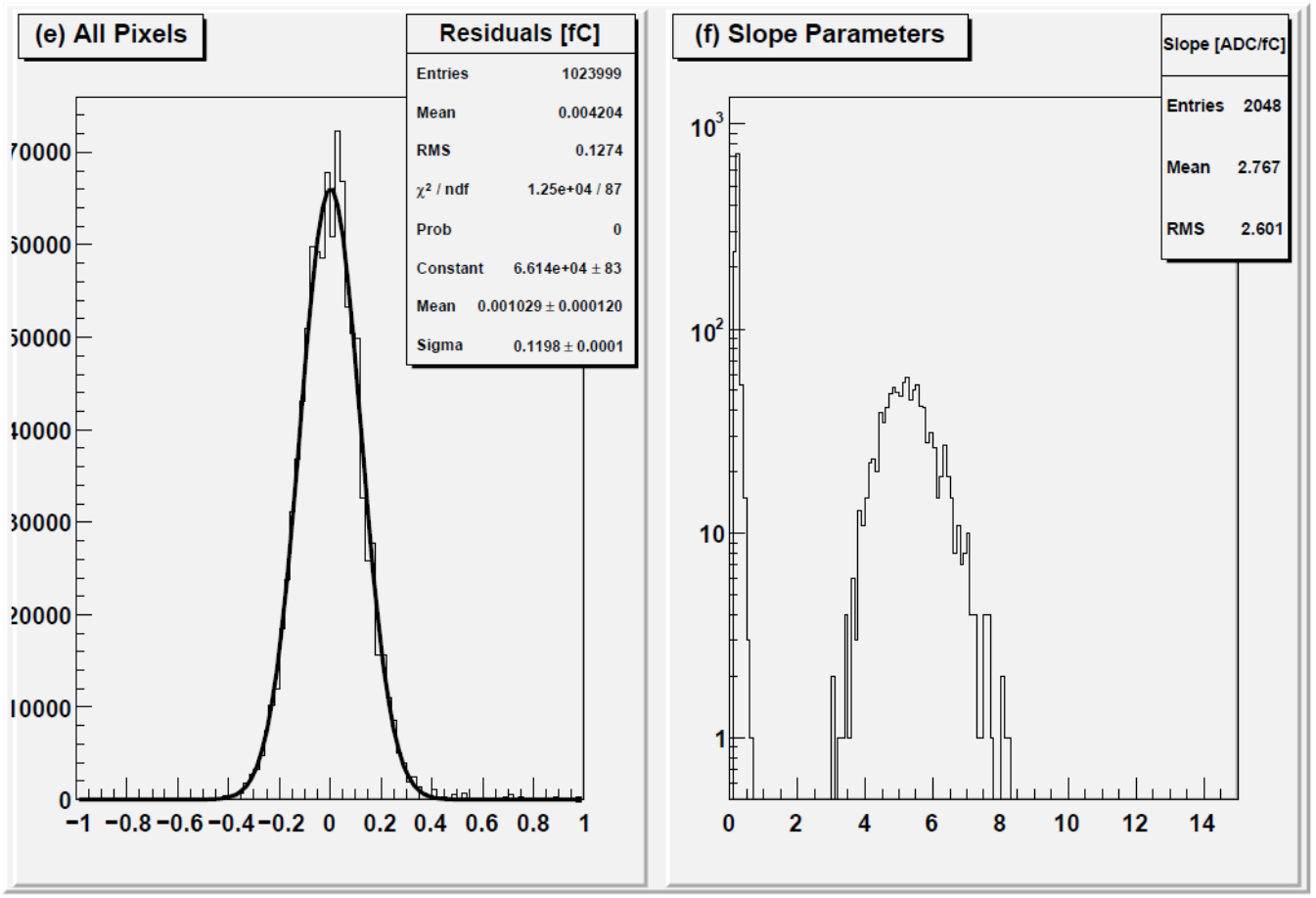

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Summary

* Prototypes of 64, 256, 512 and 1024 pixels have been fabricated and tested.
* A number of new features have been added to the original design to make it useful for other than ILC applications. Testing with signals like cosmic rays or radioactive sources, which by nature are not synchronized with the system clock, relies on these added features.
* The prototypes with 64 and 512 pixels have been used on detectors using wire-bond connections.
* Bump bonding for the prototype quantities presents a challenge. KPiX_A has factory produced solder bumps.
* We hope to bond KPiX_A to a calorimeter wafer in the near future.
* Internal calibration of the bare chip yielded rms-noise of 750 electrons. All 1024 pixels were functional on 4 chips tested.
* Work on powering larger numbers of KPiX is in the planning stage.

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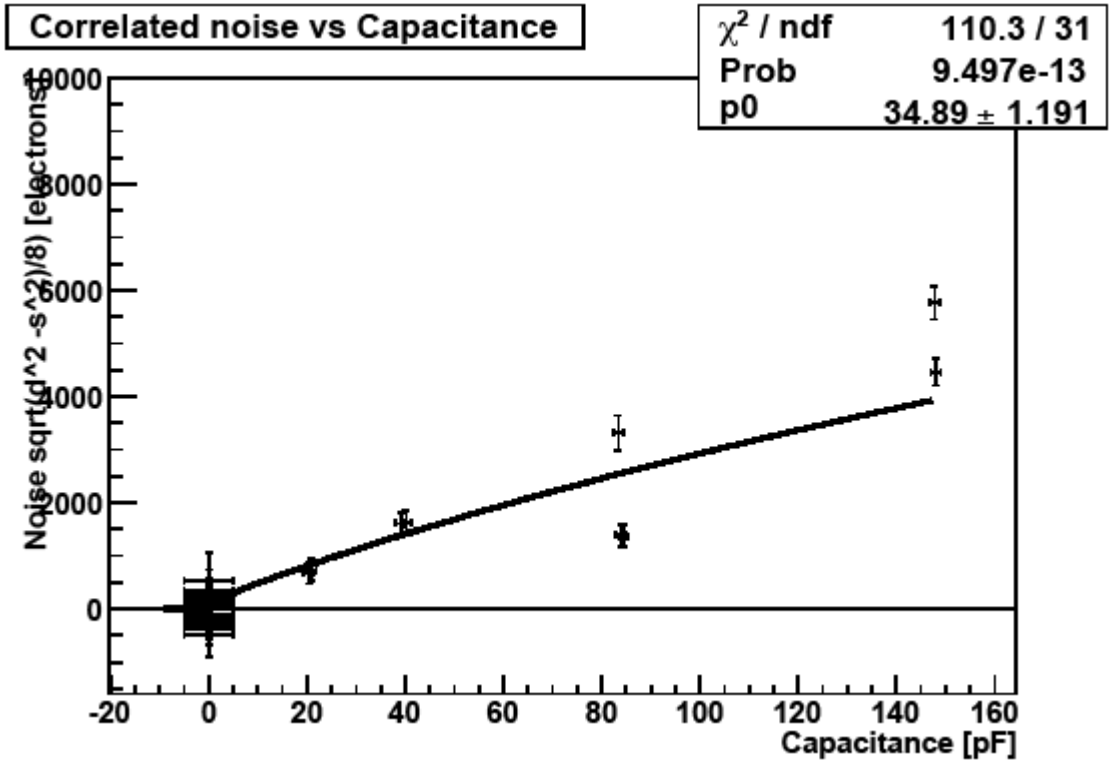
Backup: Noise vs. Capacitance



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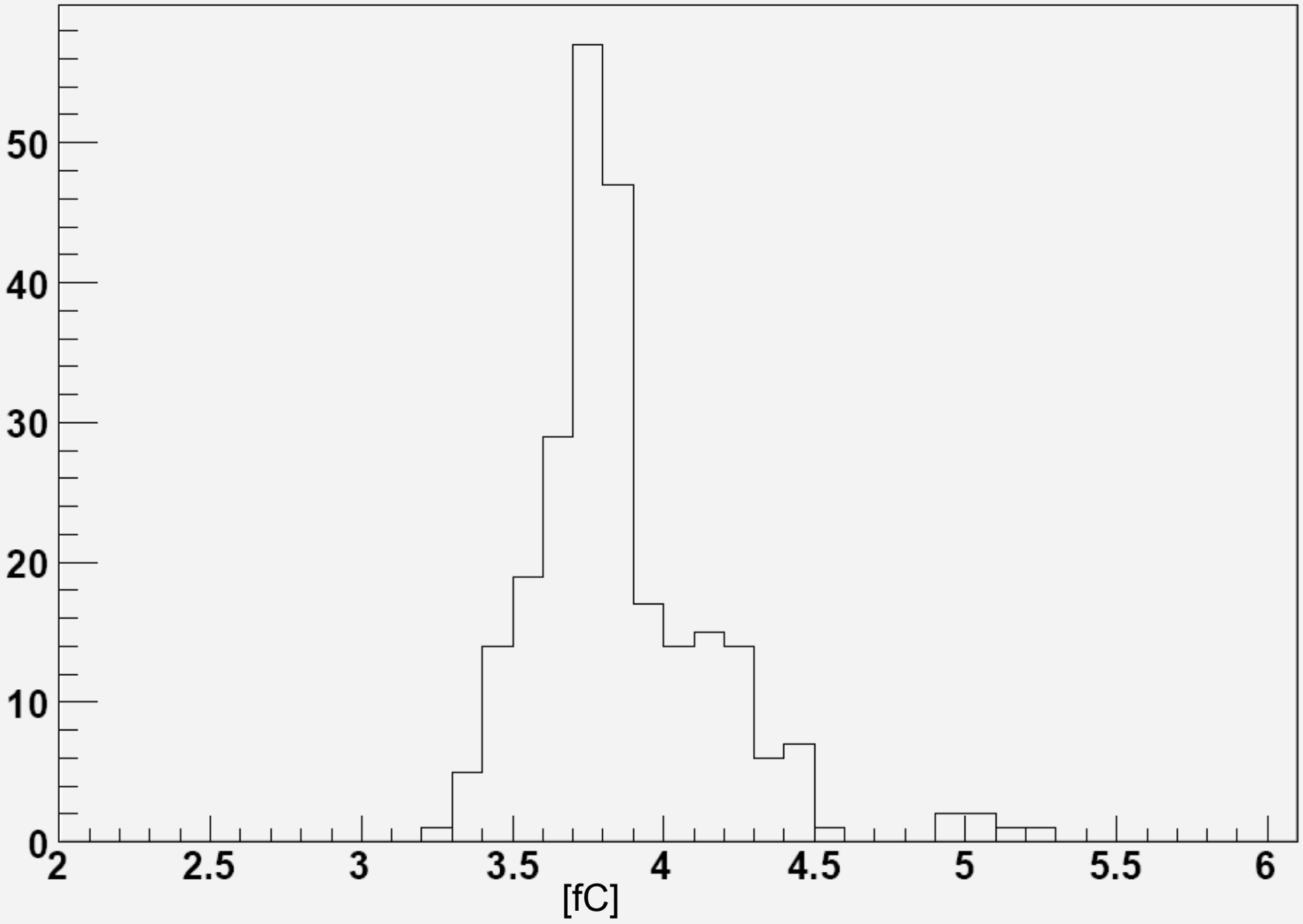
Backup: Noise in Low Gain (10 pC full scale).



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