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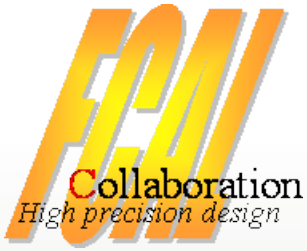


# Development of ASICs for LumiCal readout within FCAL and Power pulsing issues

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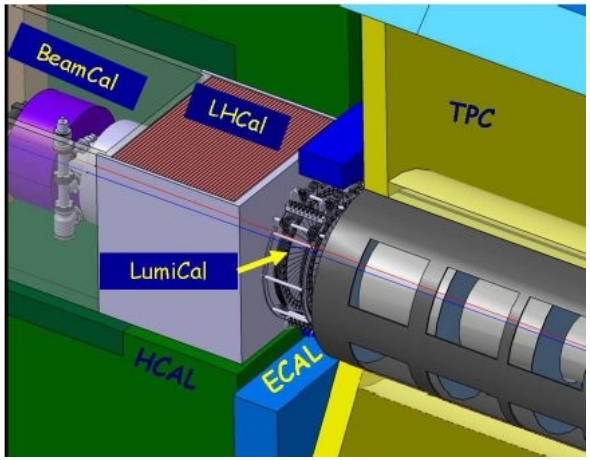
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

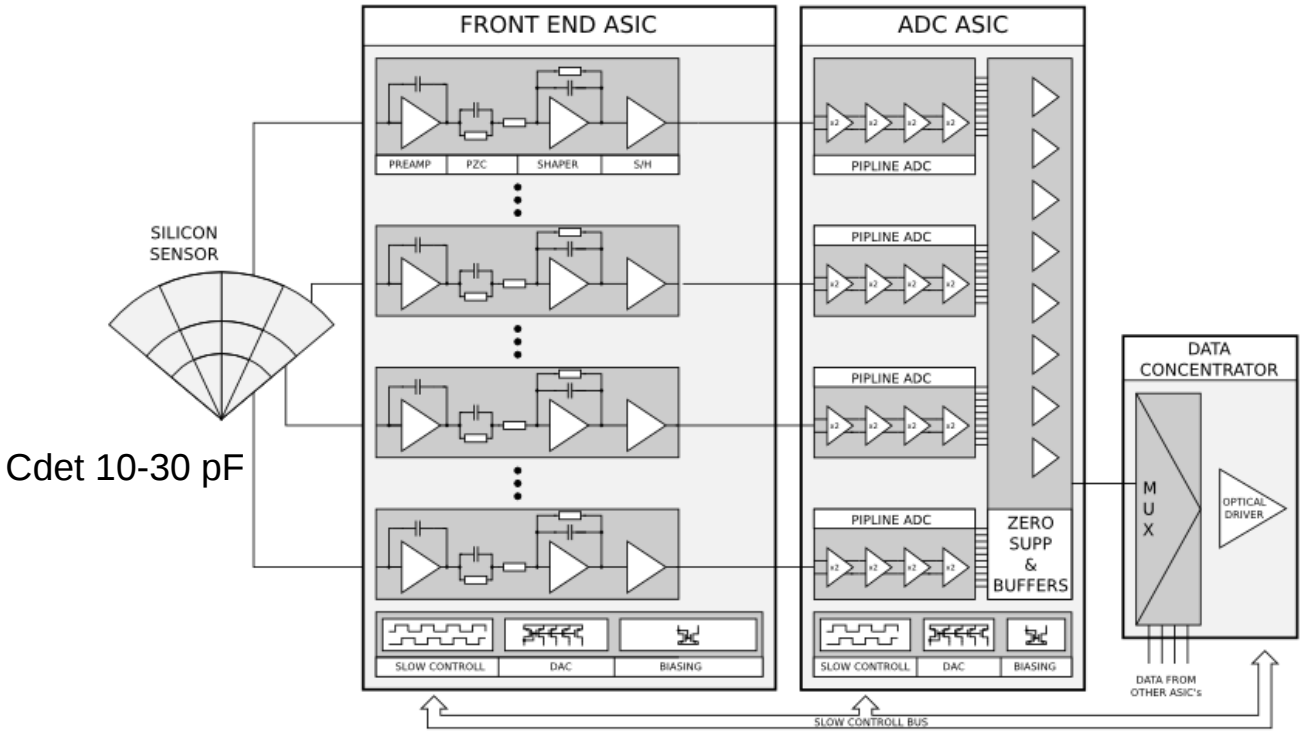
Linear Collider Power Distribution and Pulsing Workshop
LAL Orsay 9-10 May 2011

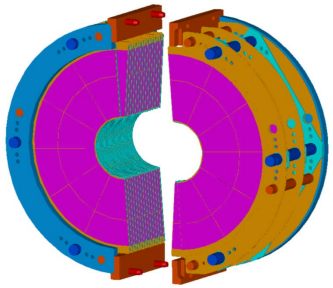
# Outline




- LumiCal readout architecture
- Front-End ASIC
- Multichannel ADC & data serialization
- Prototype multichannel LumiCal module
- Summary and future plans

# LumiCal readout architecture



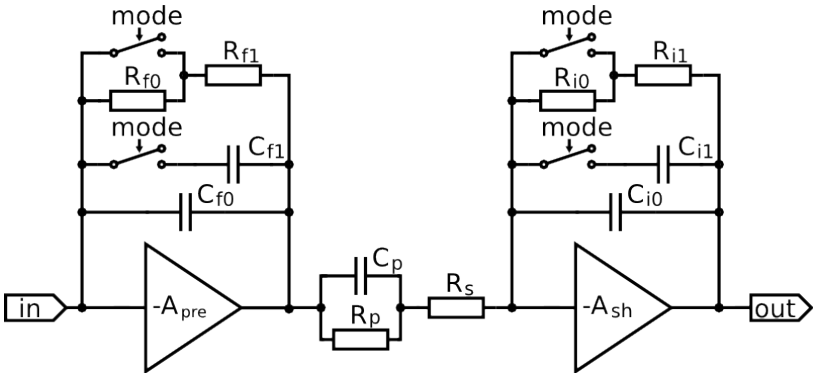



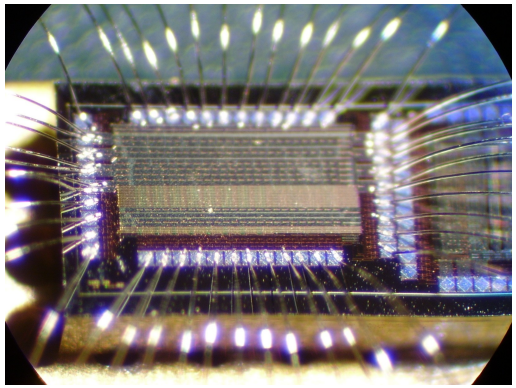
LumiCal detector:

- 2barrels * 30planes * 48sectors * 64pads
- ~200 000 channels

- Worst case peak power/current estimation for ILC: 200 000 * 15mW/chan ~ 2.8kW/850A
  - done for present AMS0.35um front-end(<9mW) and ADC&serialization(~6mW), without power pulsing
- With power pulsing (already implemented in ADC) with duty cycle 1% gives: 28W/8.5A
- Moving to smaller size technology (in view of CLIC specs., radiation hardness) we expect a huge drop of power consumption

# Front-end Electronics Status and Plans



**Existing prototypes:**

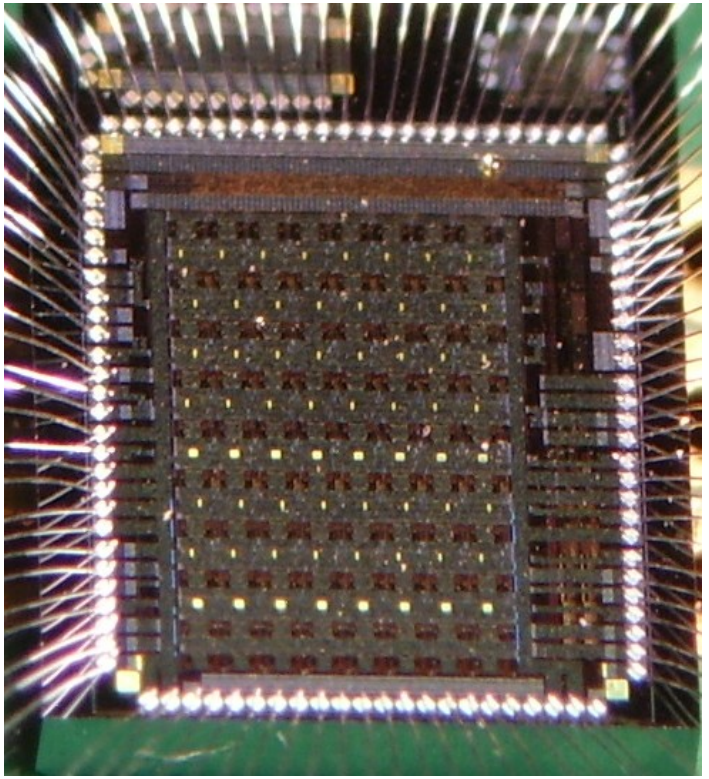
- 8 channels in AMS0.35um
- Cdet ≈ 0 ÷ 100pF (in new specs: Cdet<30pF)
- 1st order shaper (Tpeak ≈ 60 ns)
- Variable gain:
  - calibration mode - MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC
- Power switching off NOT implemented
- Designed for OLD specifications
- Prototypes fabricated and tested
  - power consumption 8.9 mW/channel
  - event rate up to 3 MHz
  - Crosstalk < 1%

**Plans:**

- Design of new front-end is just starting with updated specifications: nr channels >=8, technology probably IBM 130nm, with power pulsing. Submission expected in 2011
- Drop of power consumption expected, due to: technology, smaller Cdet, power pulsing

# First prototype of Multichannel ADC

- 8 channels of 10 bit pipeline ADC
- AMS 0.35um technology
- Layout with 200um ADC pitch
- Digital multiplexer/serializer:
  - Serial mode (~250MHz):  one data link per all channels (max fsmp ~ 3 MSps)
  - Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
  - Test mode: single channnel output  (max fsmp ~50 MSps)
- High speed LVDS drivers (<=1GHz)
- Power switching on/off
- Low power DAC voltage/current biasing
- Precise BandGap reference source
- Temperature sensor
- The only external analog signal - reference voltage (differential)

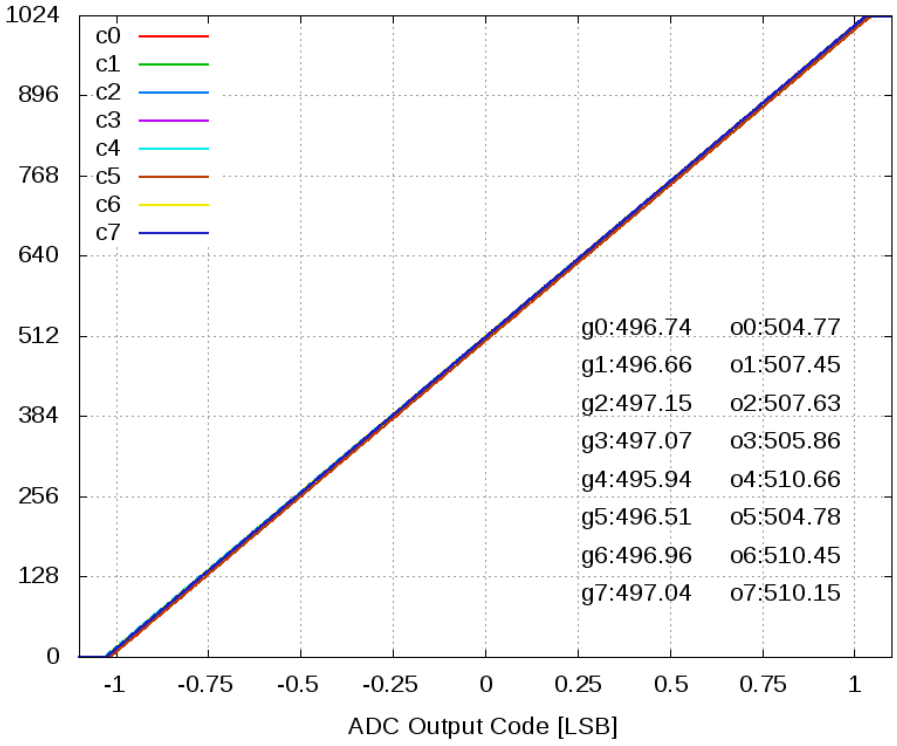


2.6mm x 3.2mm

# Multichannel ADC - Static measurements

Transfer curves for 8 ADC channels (left)

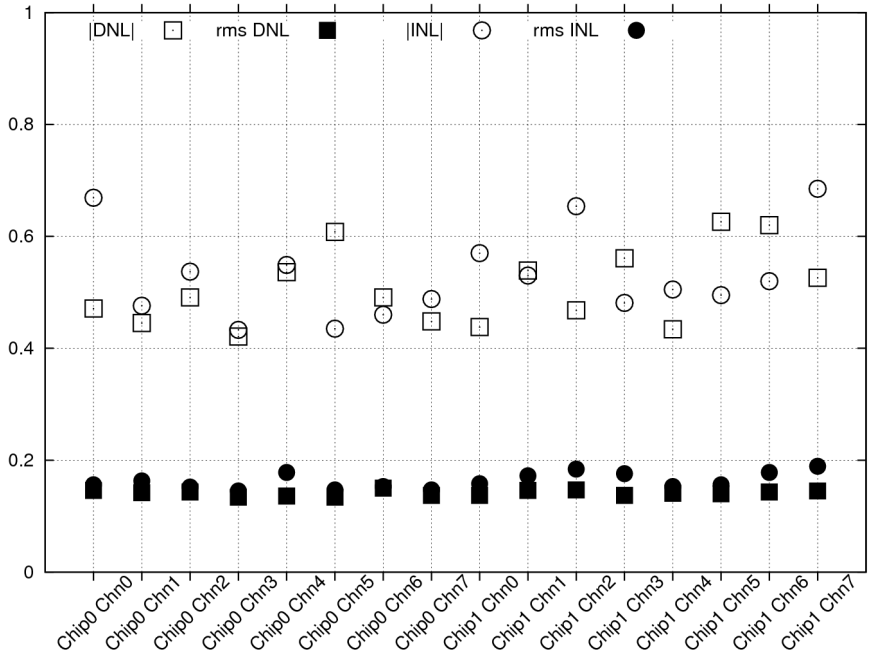
- Good uniformity of offset and gain



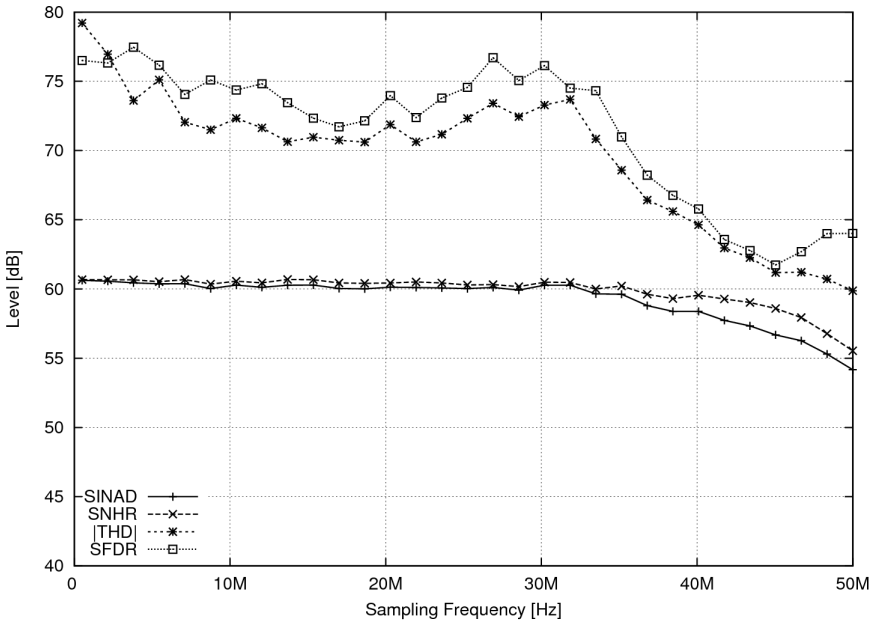

Typical INL,DNL < 0.2 LSB

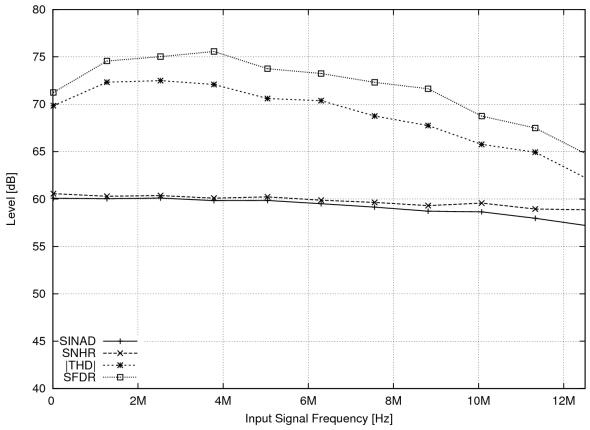
Maximum INL and DNL measured for two ASICs (16 channels) at 25MS/s:

- INL < 0.7 LSB
- DNL < 0.65 LSB



# Multichannel ADC - Dynamic measurements




- Dynamic parameters vs sampling frequency (top) and vs input frequency (bottom)
- SINAD ~60 dB corresponding to ENOB ~ 9.7 bits for sampling rates below 35 MS/s
- In test mode ADC works up to ~50 MS/s but in multichannel system two practical configurations are:
  - serialization/channel up to~25 MS/s
  - serialization/chip up to~3 MS/s

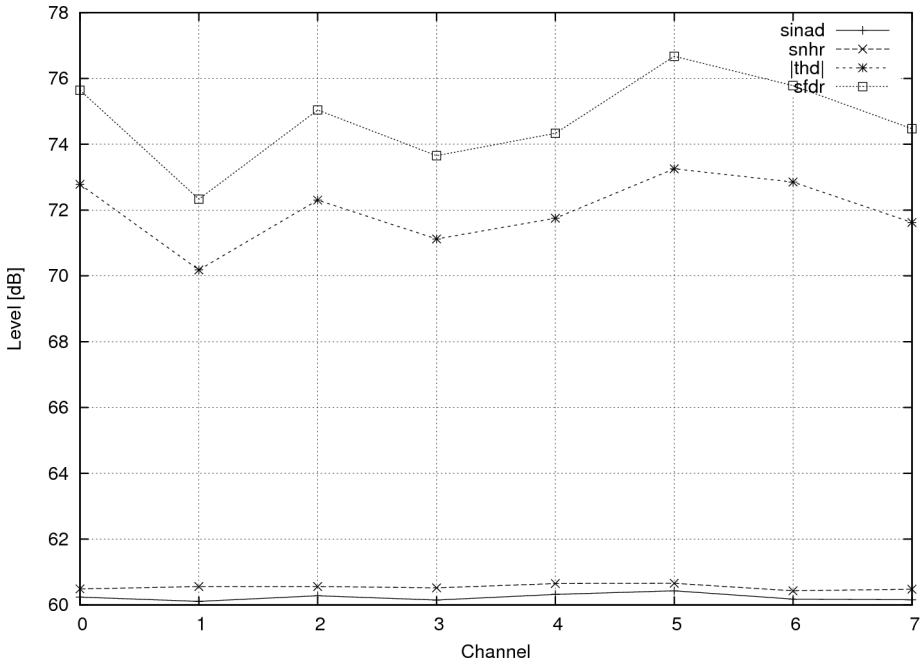
# Multichannel ADC – Dynamic uniformity/crosstalk

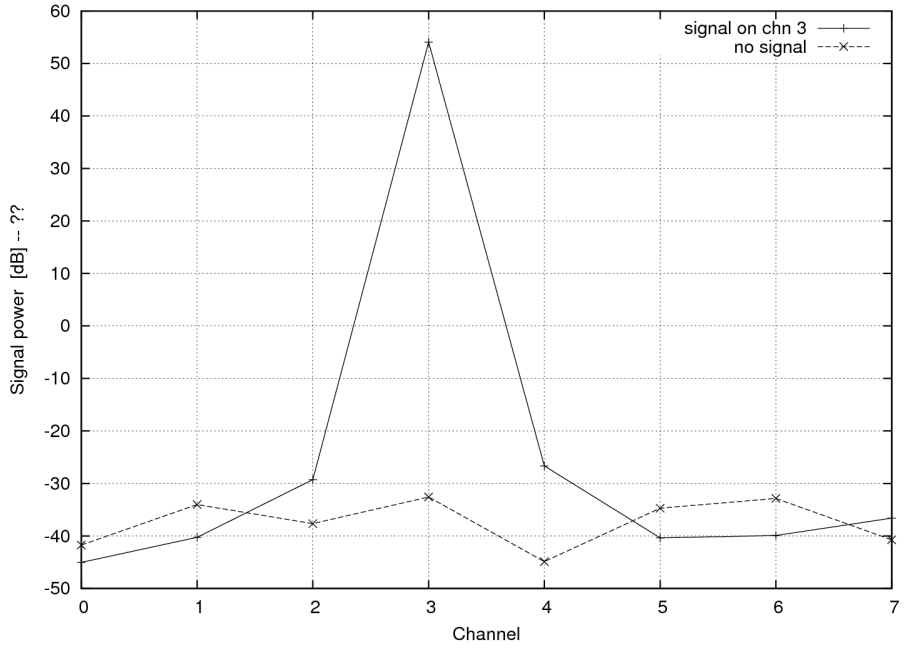
Comparison of dynamic parameters at 25MHz sampling and 1MHz signal:

- ALL channels have SINAD ~60dB corresponding to ENOB ~ 9.7 bits
- Very good uniformity!

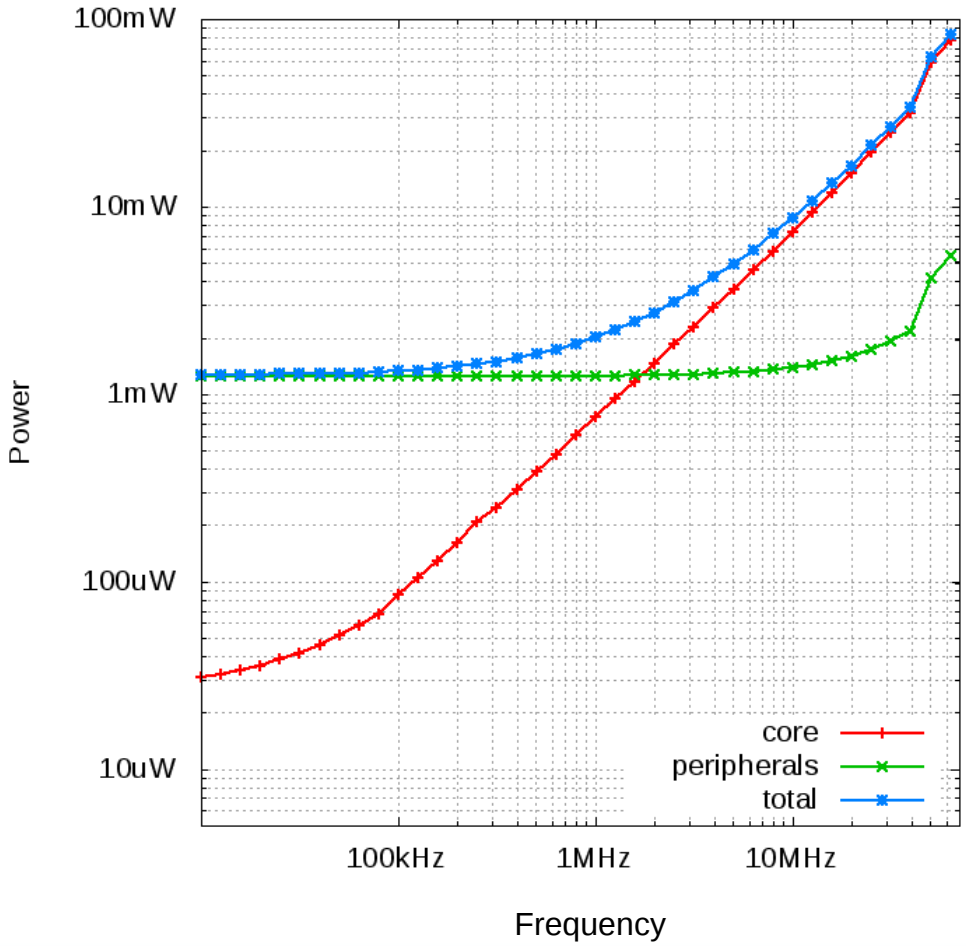
Crosstalk measured for full scale sine wave applied to channel 3:

- Crosstalk <= -80 dB
- Practically crosstalk my be neglected!



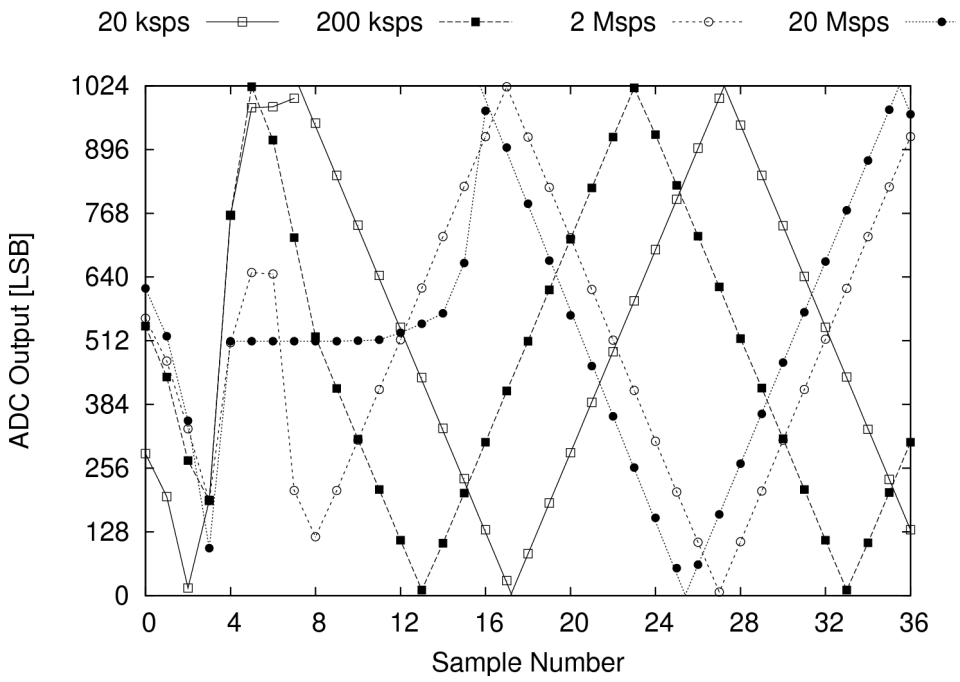



# Multichannel ADC - Power scaling/pulsing




- Measurements in progress...
- Power consumption scales linearly in large frequency range
  - ~0.85 mW/MHz per ADC core
  - MUX+LVDS needs to be measured and added
- Power pulsing not yet verified...
- Power on/off switching implemented. For previous single channel prototype ~10 clocks were needed to restart correct conversion

# Previous single channel ADC – Power pulsing




- Start-up time is measured applying triangle waveform to ADC input
- Different curves are obtained for different sampling frequences

About 8-16 clocks needed to restart correct operation

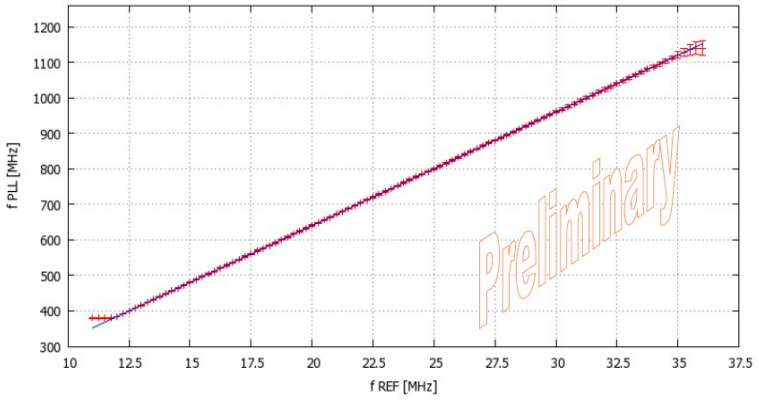
# Multichannel ADC – Status and Plans

- Multichannel ADC measurements almost completed. Very good performance (ENOB~9.7 bit) as well as channel to channel uniformity and negligible crosstalk verified, power scaling/pulsing in progress...
- Present prototype multichannel ADC fulfills ILC requests and will be used, together with front-end, in LumiCal detector prototypes during beamtests (first already in july 2011)
- For CLIC, power consumption may be still an issue as well as radiation hardness (maybe also for ILC)
- Design of lower power and radiation resistant multichannel ADC (probably in IBM 130nm) is just starting – submission expected in 2011

# Serialization and fast data transmision studies
# 1 GHz PLL based wire transceiver

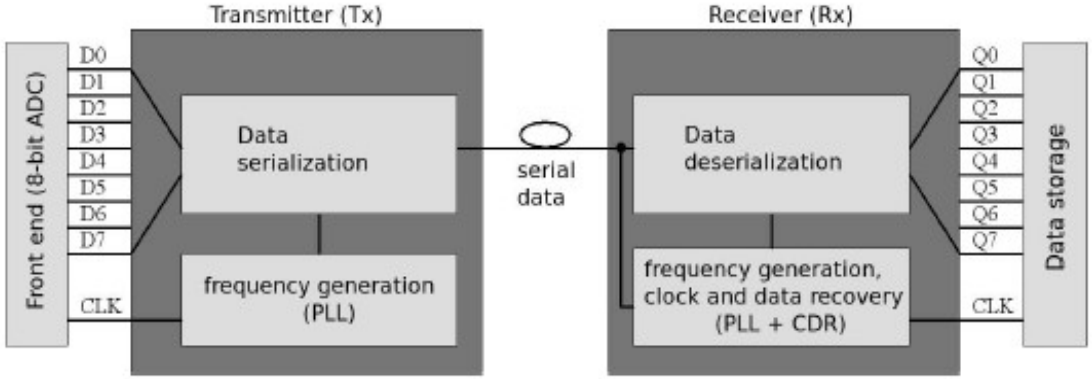
Prototype (AMS 0.35um) of PLL block fully functional

- Frequency range 380MHz-1.1GHz
- Power consumption(1GHz) 4.5mW
- Area 160um x 140um




First prototype (AMS 0.35um) of serial transceiver (PLL based), with Clock & Data Recovery, fully functional

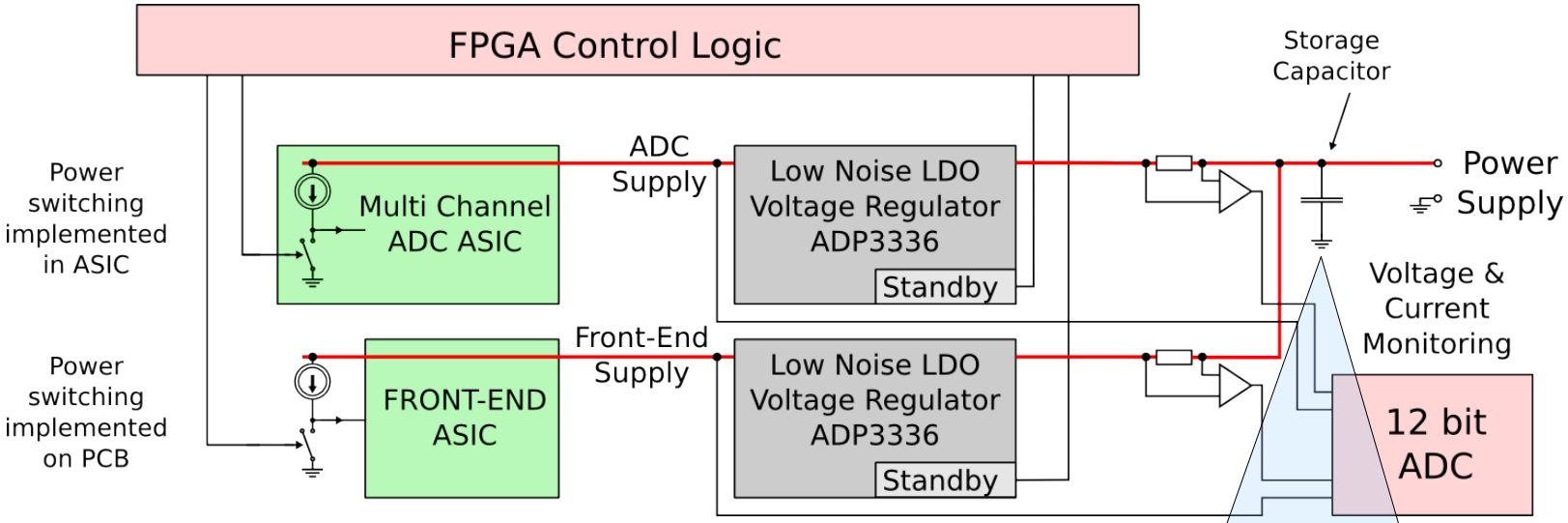
- Transmitter (with 8 bit serializer) and receiver (with 8 bit deserializer) fabricated, data coding not yet implemented
- Wide frequency range 640MHz - 980MHz




Measurements in progress ...

# Prototype detector module - Power pulsing

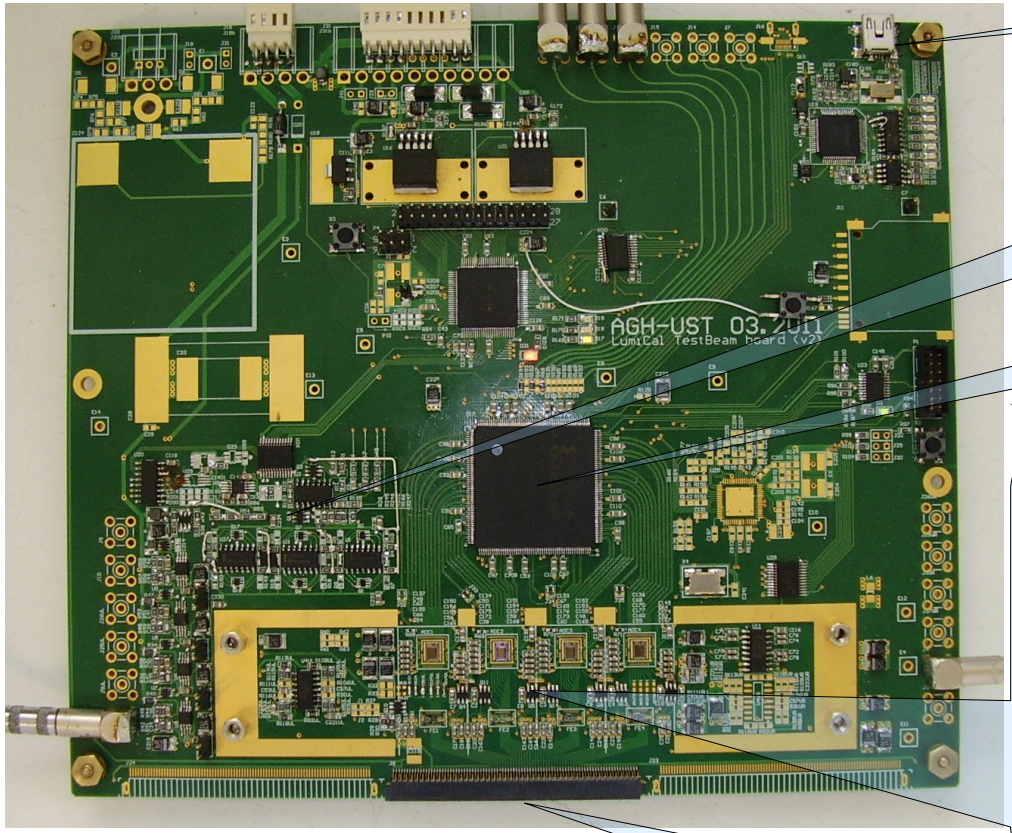
We are just developing a prototype detector system with 32 channels (comprising 4 pairs of FE+ADC chips and FPGA based data concentrator) allowing also the studies of power pulsing.




Commercial voltage regulator (ADP3336) needs about 1ms to switch on

# Prototype detector module – readout electronics

Will be used on testbeam in july 2011

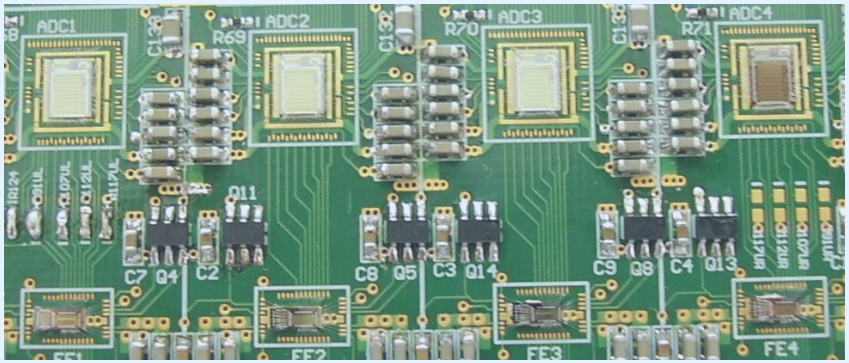



USB bridge

Power supply regulators/monitoring

Data concentrator Xilinx Spartan 3E

4 pairs of front-end + ADC




sensor connector

# Summary & future plans

- Prototypes of two ASICs (8 channel each): front-end and ADC (fulfiling ILC specifications) fabricated and fully operational.
- Prototype of 32 channels LumiCal module almost completed. Studies of performance and power pulsing should start in may.
- Different serialization and fast data transmission solutions under study.
- Testbem with prototype LumiCal module in july.
- Design of new, lower power radiation hard, multichannel front-end and ADC ASICs in smaller size technology (probably IBM 130nm) is just starting. Submission expected in 2011.
- Complete multichannel (~64) readout comprising front-end, digitization and serialization should be ready within AIDA FP7 period.