Power pulsing strategy with **Timepix3**

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Linear Collider Power Distribution and Pulsing workshop

Timepix3 Scope

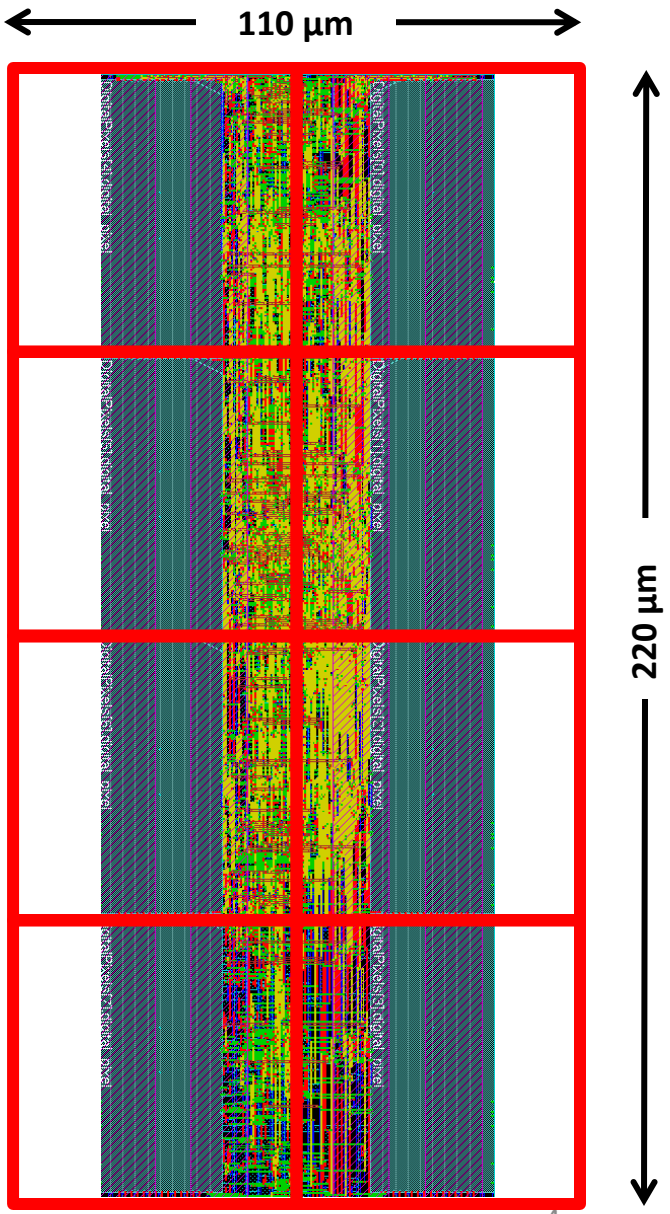
- Several groups in the Medipix3 collaboration have shown interested in a new version of the Timepix → Timepix3
- Large range of applications (HEP and non-HEP):
  - X-ray radiography, X-ray polarimetry, low energy electron microscopy
  - Radiation and beam monitors, dosimetry
  - 3D gas detectors, neutrons, fission products
  - Gas detector, Compton camera, gamma polarization camera, fast neutron camera, ion/MIP telescope, nuclear fission, astrophysics
  - Imaging in neutron activation analysis, gamma polarization imaging based on Compton effect
  - Neutrino physics
- Reuse many building blocks from Medipix3 chip (2009)
- Main Linear Collider application: pixelized TPC readout
- Timepix3 is an approved project by the Medipix3 collaboration with an assigned budget (2-engineering runs)
- Design groups: NIKHEF, BONN, CERN

Timepix3 Main Requirements

- Matrix layout: 256x256 pixels (Pixel size 55x55 µm)
- Time stamp and TOT recorded simultaneously
  - 8-10 bit Energy Measurement (TOT)
    - Standard Resolution 25ns (@40MHz)
    - Energy Dynamic range from 6.4 µs to 25.6 µs (@40MHz)
  - 10-12 bits Slow time-stamp
    - Resolution 25ns (@40MHz)
    - Dynamic range 25.6 µs (10 bit) to 102.4 µs (12 bit)
  - 4 bits Fast time-stamp
    - resolution ~1.5ns (if using on-pixel oscillator running at 640MHz)
    - Dynamic range 25ns
- Sparse Readout
- Technology choice: IBM 130nm DM 3-2-3 or 4-1

The Timepix3 Chip

Readout Chip	TIMEPIX3 (beginning of 2012)
Pixel size	55 x 55 µm^2
Pixel arrangement	256 x 256 (2x4 superpixels)
Sparse readout	YES
PC, TOA or TOT recorded simultaneously	YES (2 at a time) ~40 bit/Hit
Minimum threshold	> 500 e- (1.8keV)
TOA resolution	> 1.5ns
Peaking time	< 25 ns
TOT resolution	< 5% channel to channel spread
Technology	IBM 130nm DM 3-2-3
Power consumption ON	<700 mW (~20 µW/pixel) @1.2 V
Power consumption OFF	<10 mW (*)
Target floorplan	3 sides buttable and minimum periphery
TSVs possibility	YES. Multi-dicing scheme as Medipix3
Count Rate	~0.2 x 10^6 x-rays/mm^2/s



Timepix3 as a demonstrator for CLICpix

- Timepix3 will be a step towards CLICpix

- CLICpix main features:
  - ~20 µm square pixels → 65nm or below…
  - TOT and Arrival time (~10ns) simultaneously
  - Extremely low power (<50mV/cm^2) → Power Pulsing

- A “proper” power pulsing strategy will be included in Timepix3

Timepix1 (2006) Power Contributors

- Timepix1 (CMOS 250nm) has three power domains:
  - VDDA = 2.2V
  - VDD = 2.2V
  - VDD_LVDS = 2.2V

- (VDDA) → Analog static power consumption (~250mA) dominated by the analog pixel power consumption:
  - Preamp DAC [0-2uA] → 2uA * 256 *256 = 131mA
  - Idisc DAC [0-1.6uA] → 2uA * 256 *256 = 104mA

- (VDD) → Dynamic digital power consumption (~200mA @ 100MHz)
  - Dominated by the RefClock distribution → Idd [mA] = ~2*fRefClock[MHz]
  - Digital leakage current is minimal (<50uA/chip) → Due to the CMOS technology used

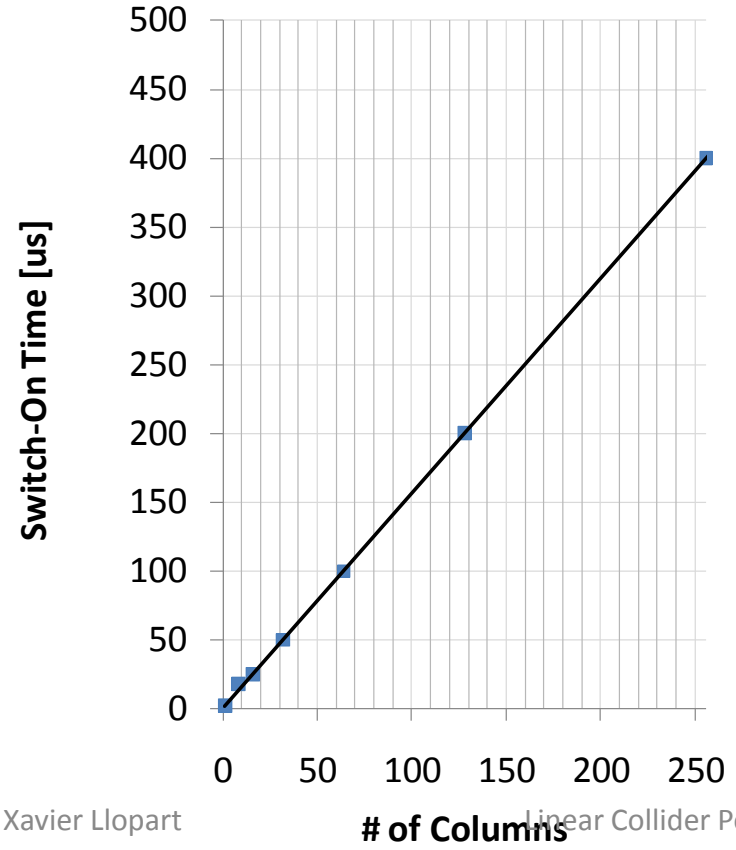
- (VDD_LVDS) → Dominated by the LVDS drivers (~12mA)

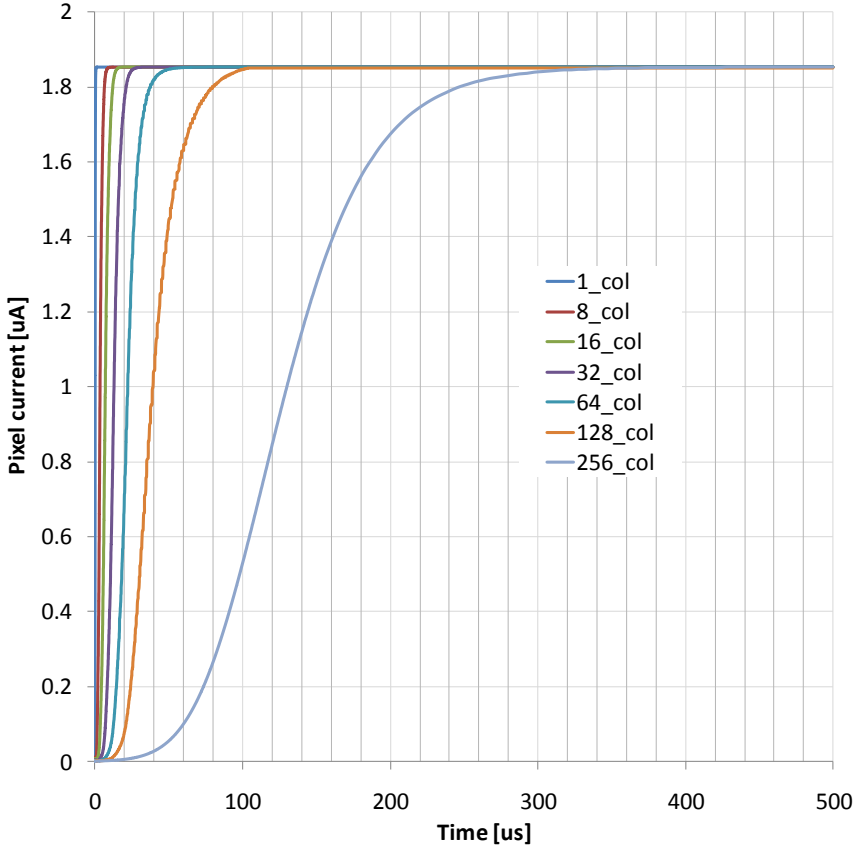
Power pulsing with Timepix1

- Timepix1 is not designed to be power pulsed
- The obvious strategy would be to gate the Preamp and Idisc DAC outputs… but:
  - The DACs are not designed to have a large current capability:
    - The DAC output are directly connected to all 65536 pixels → >2nF load capacitance → large switch on/off time
  - The IO control logic of Timepix is not prepared to switch ON/OFF multiple DACs quickly → Command controlled (software) 1 to 10ms
  - However through ExtDAC 1 DAC at a time can be power pulsed and “some” power pulsing information can be extracted

Full chip Switch-On simulation

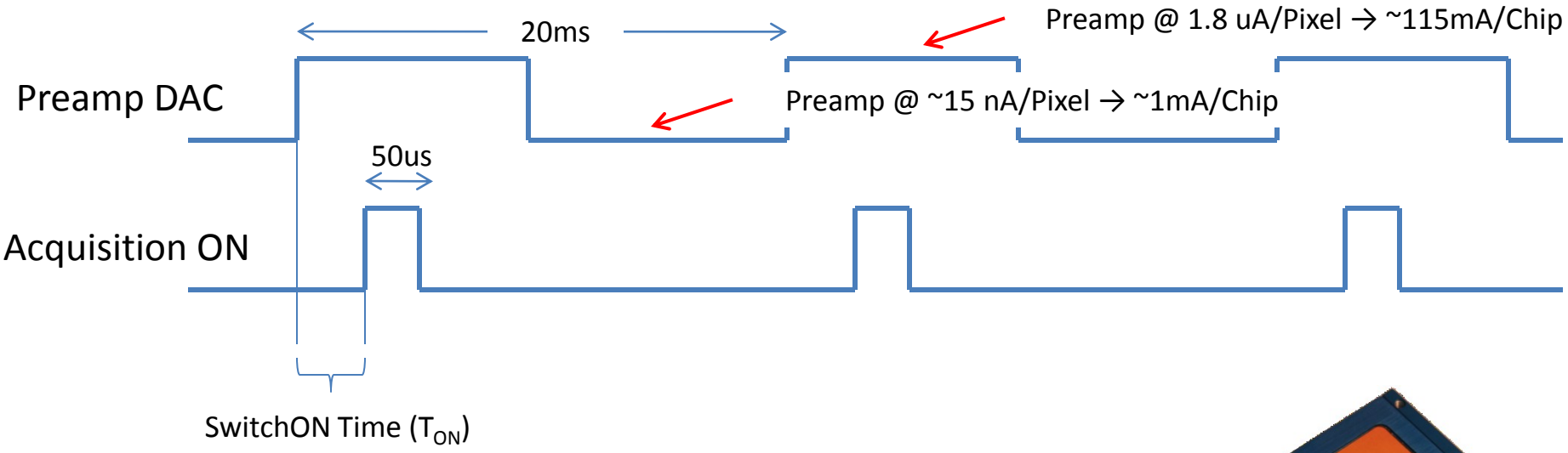
- Based in a typical output stage of a Medipix3 DAC
- Simulation includes full column power distribution: Rline, Cline and pixel target transistor but no on-pixel parasitic capacitances





Power pulsing Setup

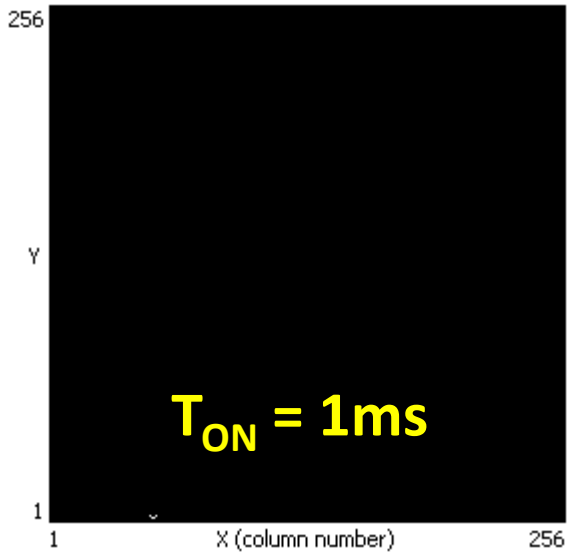
D. Dannheim
P.G. Roloff
E. Van der Kraaj

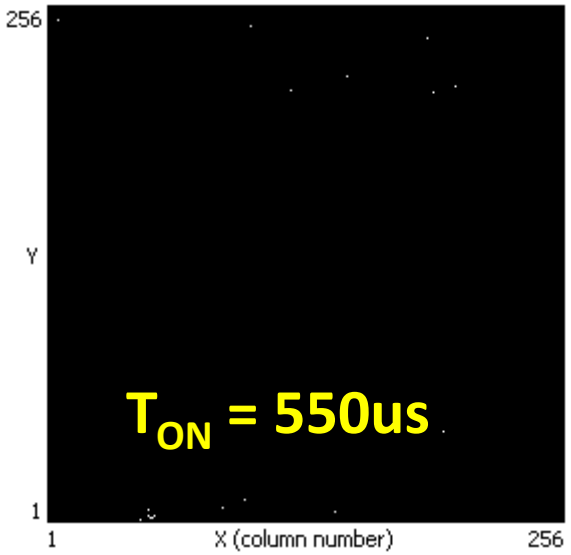


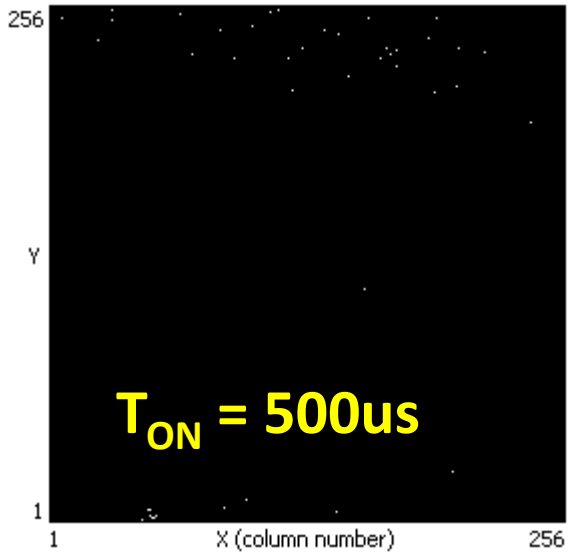
- Power Pulsing using the External DAC in pin and selecting the Preamp DAC (0.4 to 1.15 V)
- Timepix1 programmed in TOT (charge collection mode) with external triggering
- 1000 frames of 50 us acquisition time added together

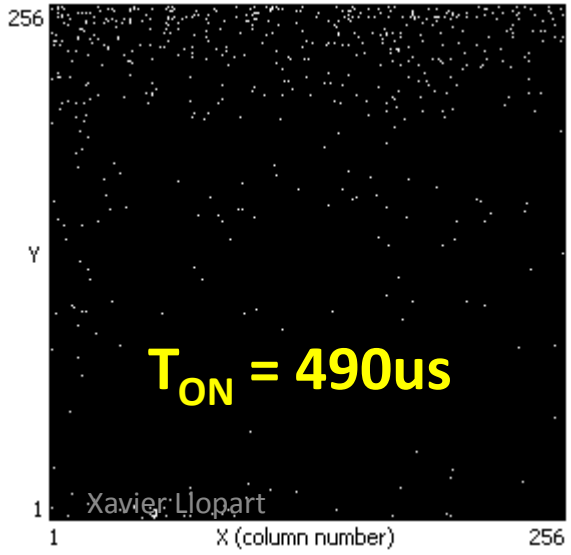
Switch ON time using Noise floor

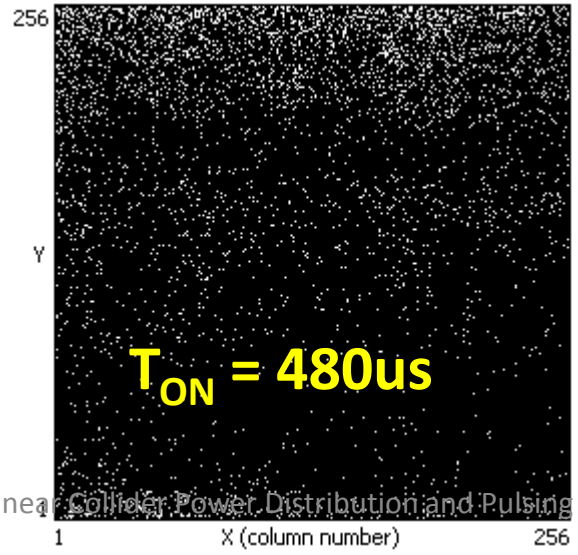
D. Dannheim
P.G. Roloff
E. Van der Kraaj

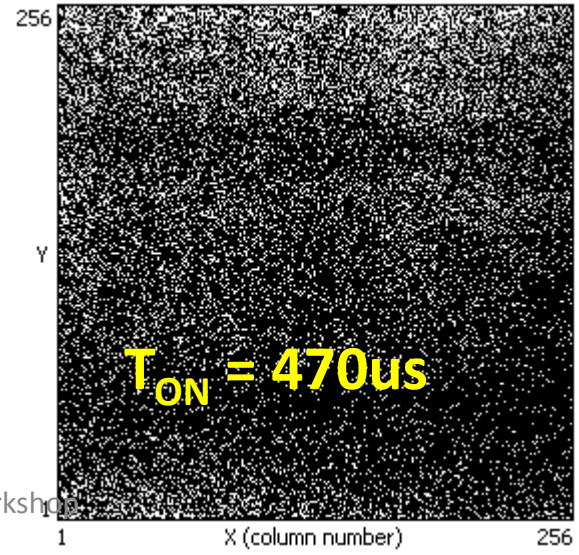












Switch ON time using Fe55 in TOT mode

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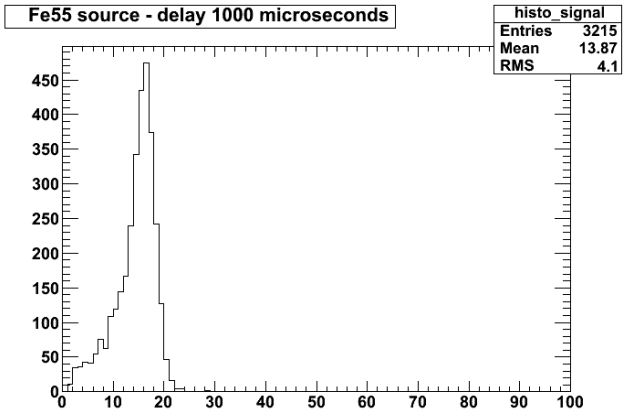
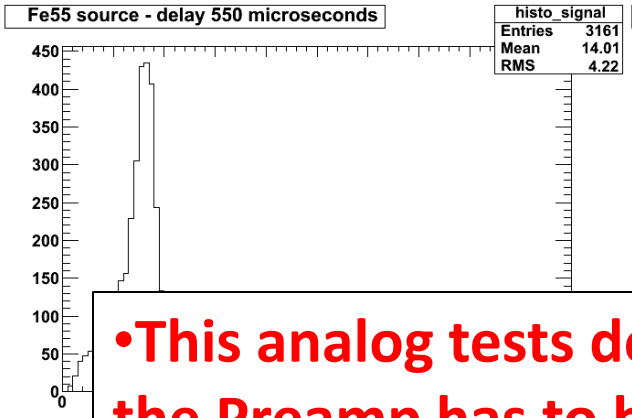
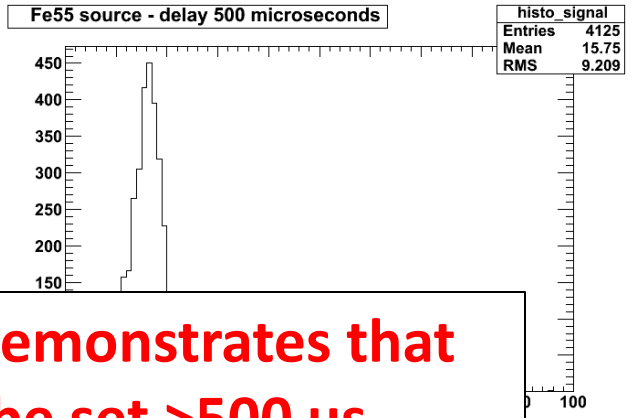
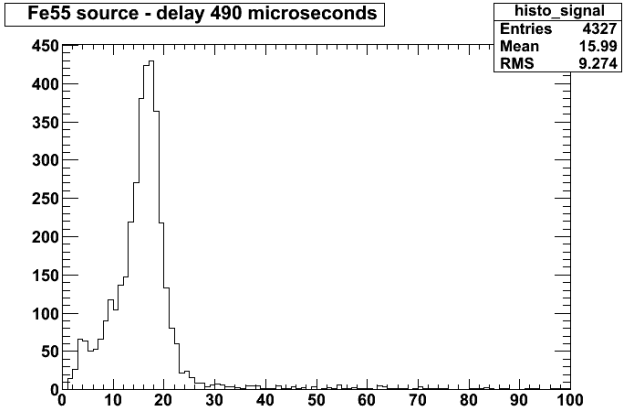
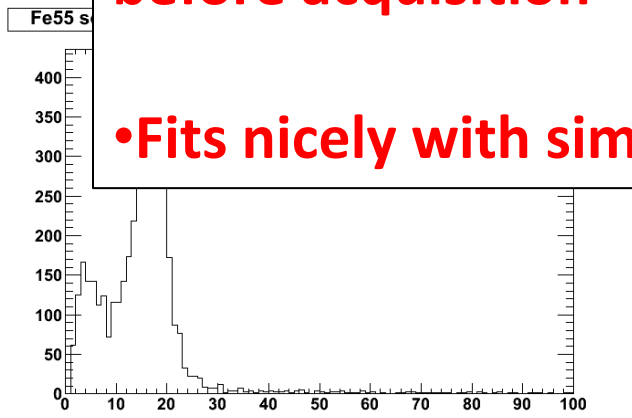


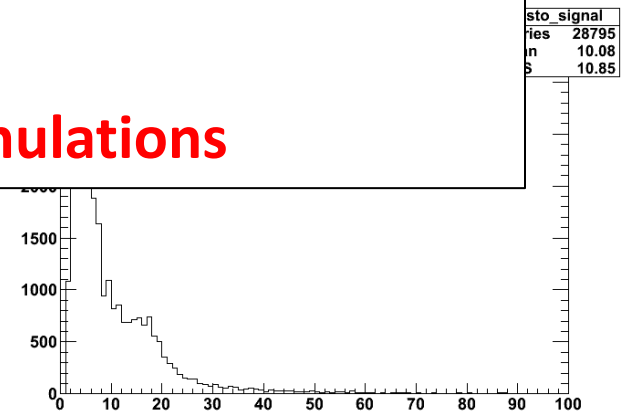




- **This analog tests demonstrates that the Preamp has to be set >500 us before acquisition**
- **Fits nicely with simulations**







Power pulsing strategy in Timepix3

- Power pulsing only in the main biasing sources of the user selected analog blocks:
  - A periphery power pulsing control logic
  - Biasing switching:
    - DAC column analog buffer
    - Sleep transistors at pixel level in required biasing nodes
- Digital blocks always on:
  - Use only HVT transistors in the digital blocks of the pixel matrix (depending on the CMOS technology might be not sufficient…)

Periphery power pulsing control logic

- Select which blocks (DACs) will be power pulsed and the ON/OFF range. 2 possible strategies:
  1) Switching the DAC output between the 2 Digital DAC values
  2) Multiplexing between 2 DAC outputs

- Configurable power pulsing strategy (3 bits)
  - 2,4,8,16,32,64,128 or 256 columns simultaneously

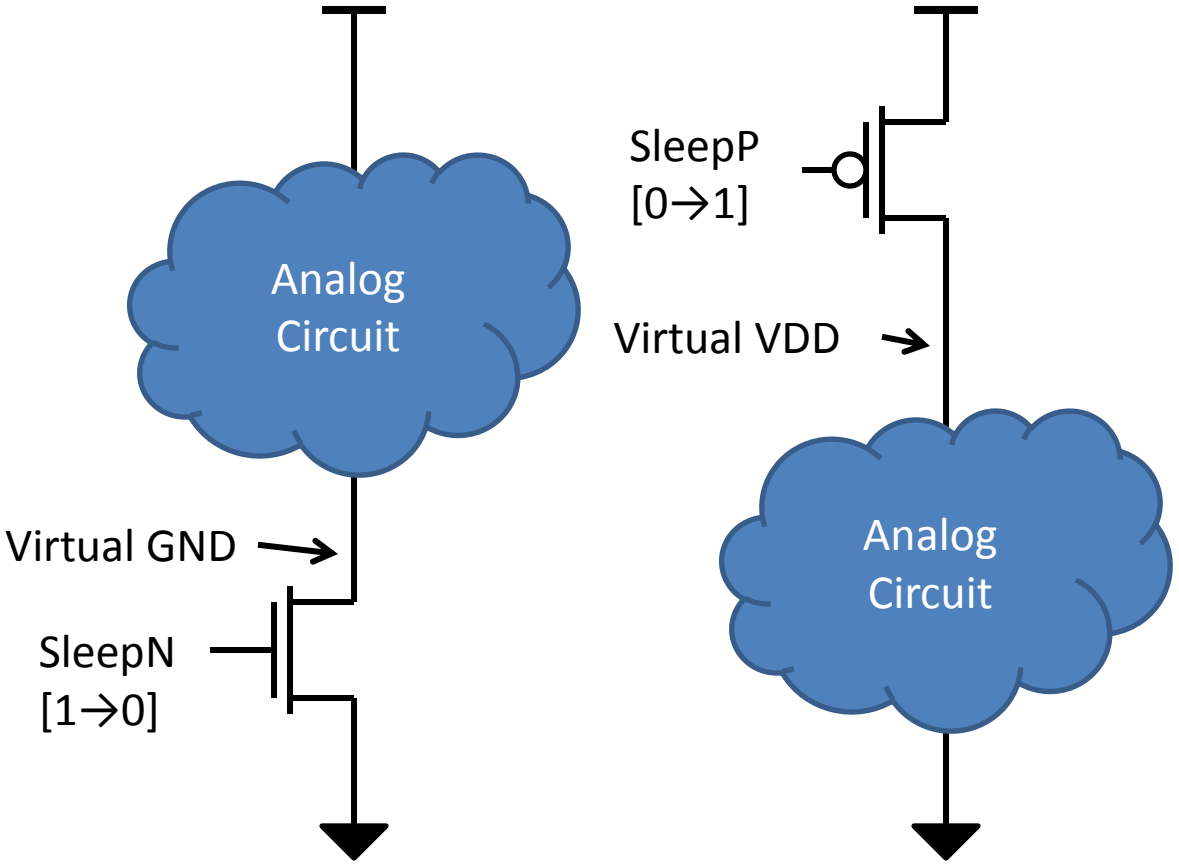
- 1 external IO Pin to apply power pulsing

DAC column analog Buffer in Timepix3?

- Advantages:
  - Faster turn-ON/OFF times
    - 1 per pixel column < 2us
    - 1 per 8 pixel column < 20us
  - Better control of gate leakage and antenna DRC rules (Medipix3 problems)

- Disadvantages:
  - Column to column mismatch !!!
    - A good buffer with little offset can take quite some area → larger periphery
  - Depending on the switching speed this buffer will take quite some power (~50 uA/Buffer)

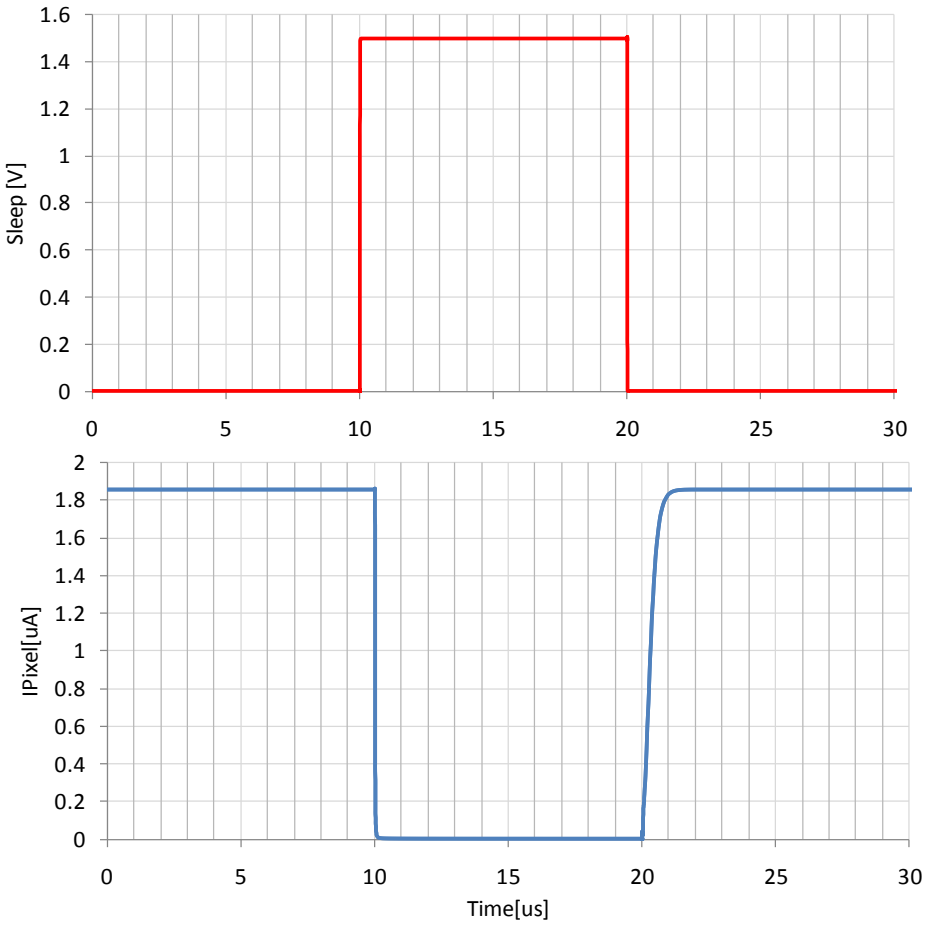
On-Pixel Sleep Transistors



- Advantages:
  - Reduces even more the switching time
  - Digital control: Easy to design (sleep/wake column patterns)
  - DAC output can go directly to all pixels
- Disadvantages:
  - More pixel logic
  - Virtual Ground/VDD in each pixel (~5mV)
  - Coupling digital to analog

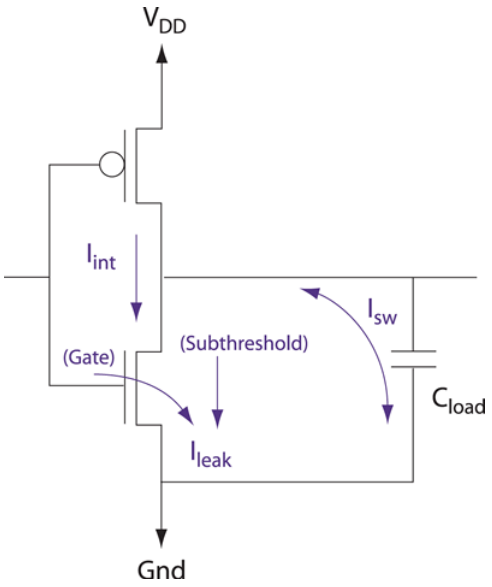
Simulation with on-pixel sleep transistors

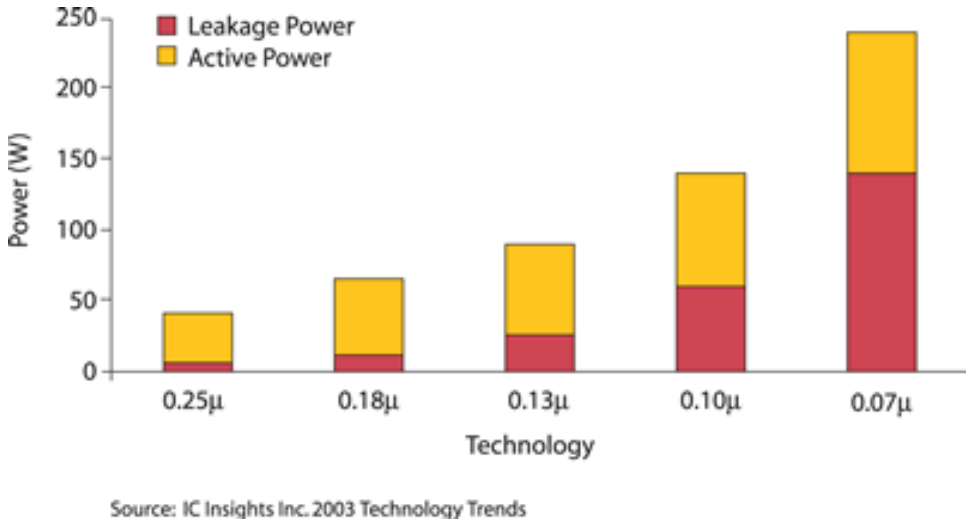
- Simulation of 1 full column (256 pixels)
- Digital column buffer is very small (minimum size buffer) → Top to bottom delay ~40ns
- Switch OFF (sleep) time ~100ns
- Switch ON (wake) time ~2us



Leakage power trend with technology scaling

- Advanced semiconductor technologies show a steady increase of leakage power (gate and sub-threshold currents)
- Power gating (sleep transistor) is widely used in order to keep fast logic and low power consumption
- Multi-Vt transistors offer different level of speed and leakage

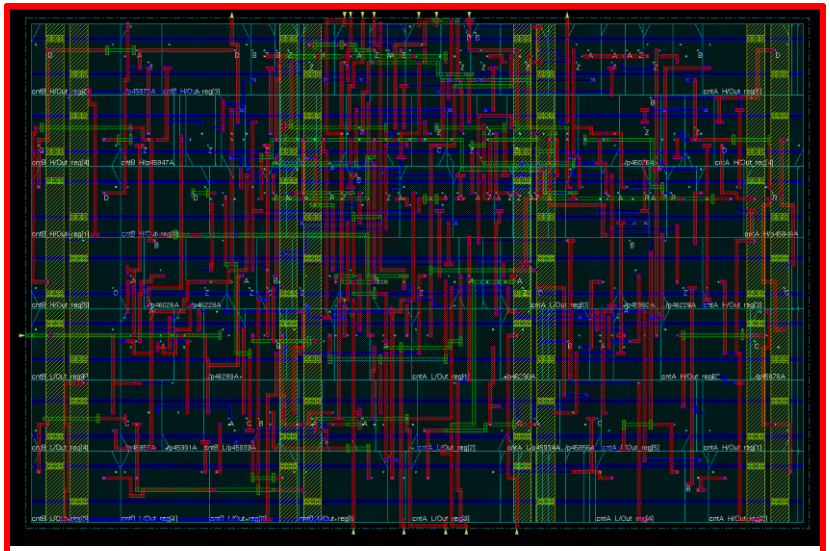




Source: IC Insights Inc. 2003 Technology Trends

Medipix3 counter synthesized with a LVT (left) and HVT (right) standard cell library

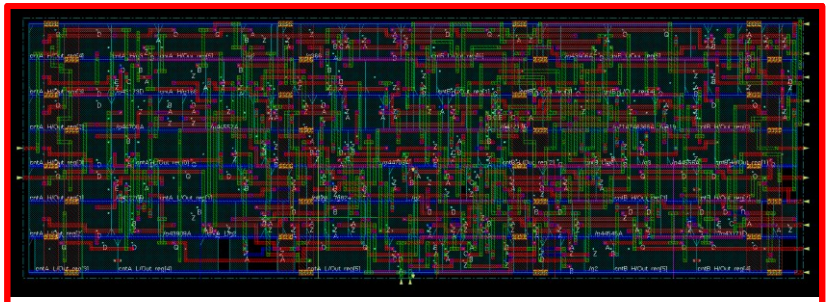
- Ultra High density and low power Standard Cell library in IBM 130nm will be used in Medipix3.1 and Timepix3



VDD	Temp	Pixel leakage	Chip leakage
1.4 V	125 C	22.5 µW	**1.5 W !!!**
1.5 V	25 C	223 nW	**14.6 mW**
1.6 V	-55 C	470 pW	**30 µW**

55 µm

X100 reduction !!!



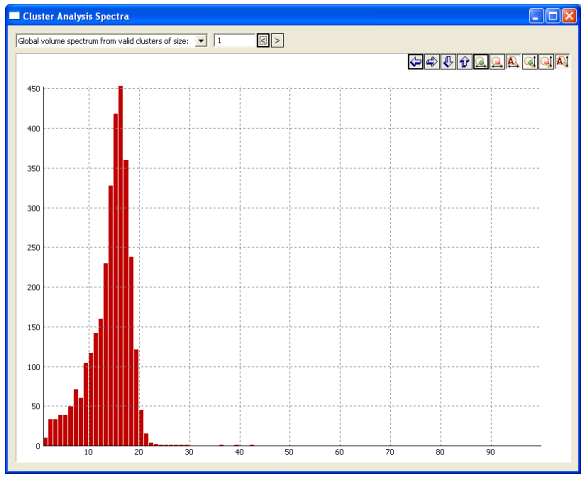
VDD	Temp	Pixel leakage	Chip leakage
1.5 V	25 C	2.5 nW	**163 µW**
1.2 V	25 C	1.15 nW	**75.3 µW**

55 µm

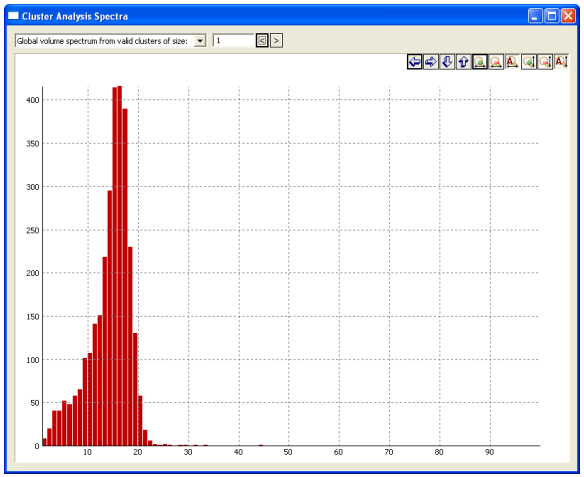
Conclusions

- Timepix1 (CMOS 250nm) is not prepared for power pulsing but still can be used to verify sleep/wake simulations
- The Timepix3 chip (130nm) will have a highly configurable power pulsing strategy:
  - An external control (IO pad) over the static analog pixel power consumption → Column DAC analog buffer and/or pixel sleep transistors
  - The expected Timepix3 pixel matrix static (sleep mode) power consumption should be <200 uA/chip if HVT transistors are used
  - Expected power consumption:
    - ON → 350 mW/cm^2
    - OFF → <5 mW/cm^2
- The Timepix3 submission is programmed to be by the beginning of 2012. First detectors should be ready in 1 year time

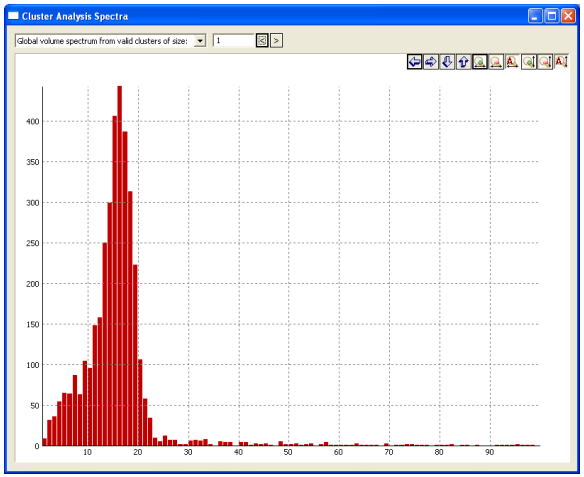

CERN



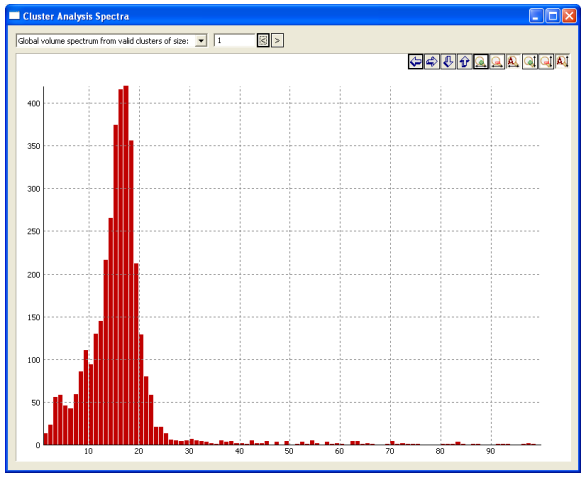
T_{ON} = 1ms



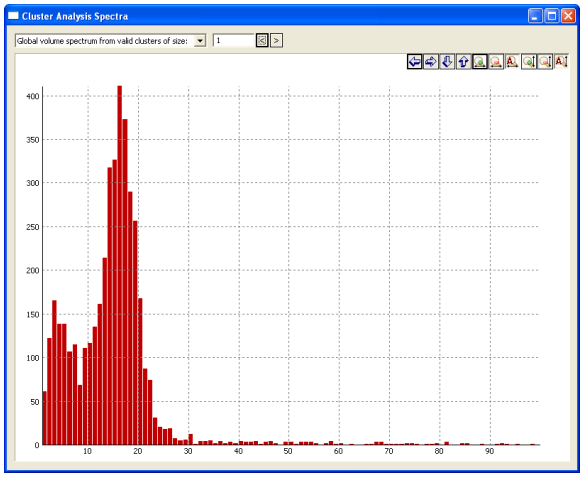
T_{ON} = 550us



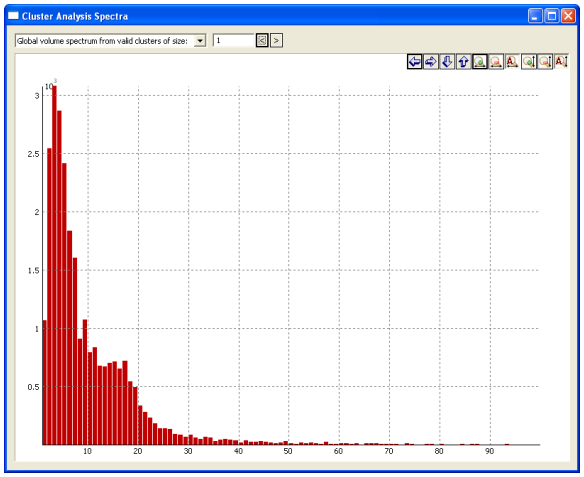
T_{ON} = 500us



T_{ON} = 490us



T_{ON} = 480us



T_{ON} = 470us

Faster response time if Cload decreases