Development of CMOS pixel sensors fully adapted to the ILD vertex detector requirements

M. Winter (PICSEL team of IPHC-Strasbourg)

- Sensor design : coll. with IRFU-Saclay -

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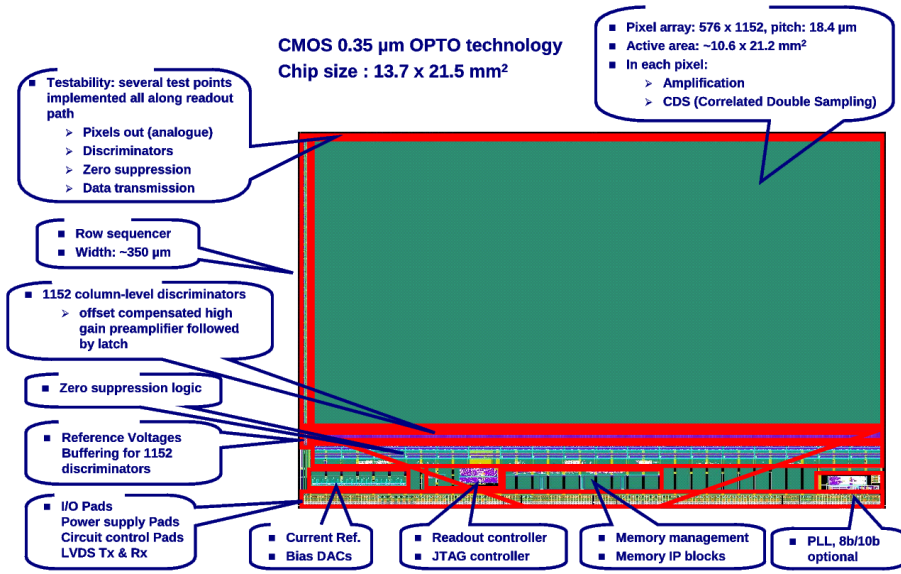
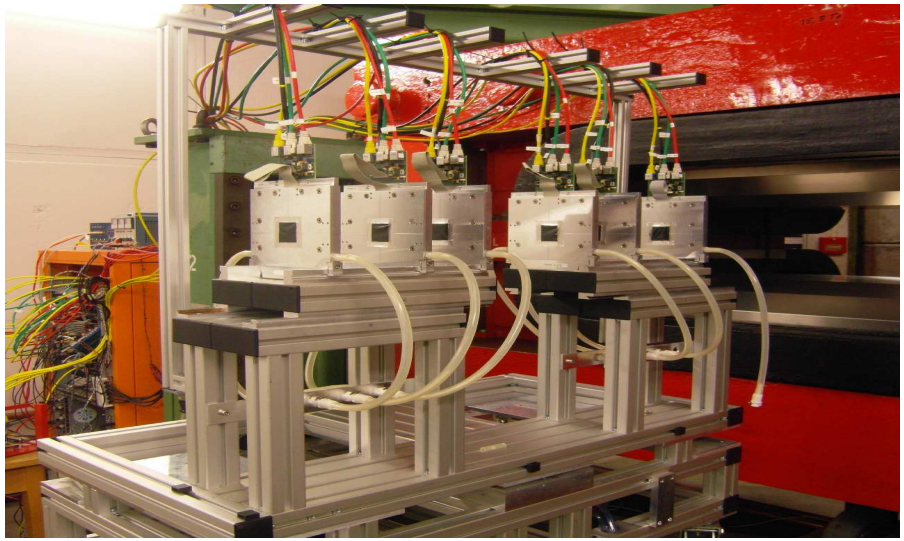
CMOS Pixel Sensors: Established Architecture

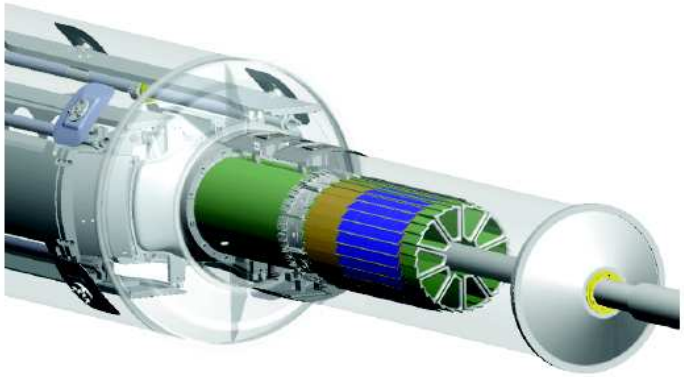
- **Main characteristics of MIMOSA sensor equipping EUDET BT:**
  - ⁕ 0.35 μm process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)
  - ⁕ column // architecture with in-pixel amplification (cDS) and end-of-column discrimination, followed by $\emptyset$
  - ⁕ binary charge encoding
  - ⁕ active area: 1152 columns of 576 pixels (21.2$\times$10.6 mm^2)
  - ⁕ pitch: 18.4 μm $\rightarrowtail$ $\sim$ 0.7 million pixels
    - ▷ charge sharing $\Rrightarrow$ $\sigma_{sp}\sim$ 3.-3.5 μm
  - ⁕ $t_{r.o.} \lesssim$ 100 μs ($\sim 10^4$ frames/s) suited to $>10^6$ part./cm^2/s
  - ⁕ JTAG programmable
  - ⁕ rolling shutter architecture
    - $\Rrightarrow$ full sensitive area dissipation $\cong$ 1 row
    - ▷ $\sim$ 250 mW/cm^2 power consumption (fct of N_{col})
  - ⁕ thinned to 50 μm
  - ⁕ various appli. : VD demonstr., NA63, oncotherapy, dosimetry, ...

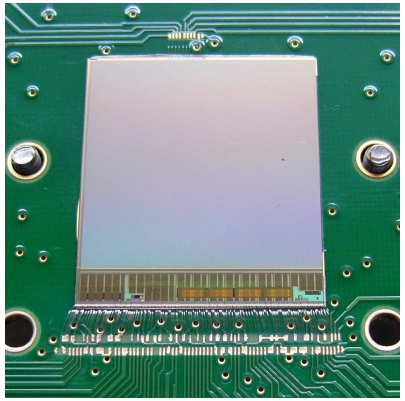




State-of-the-Art: MIMOSA-28 for the STAR-PXL

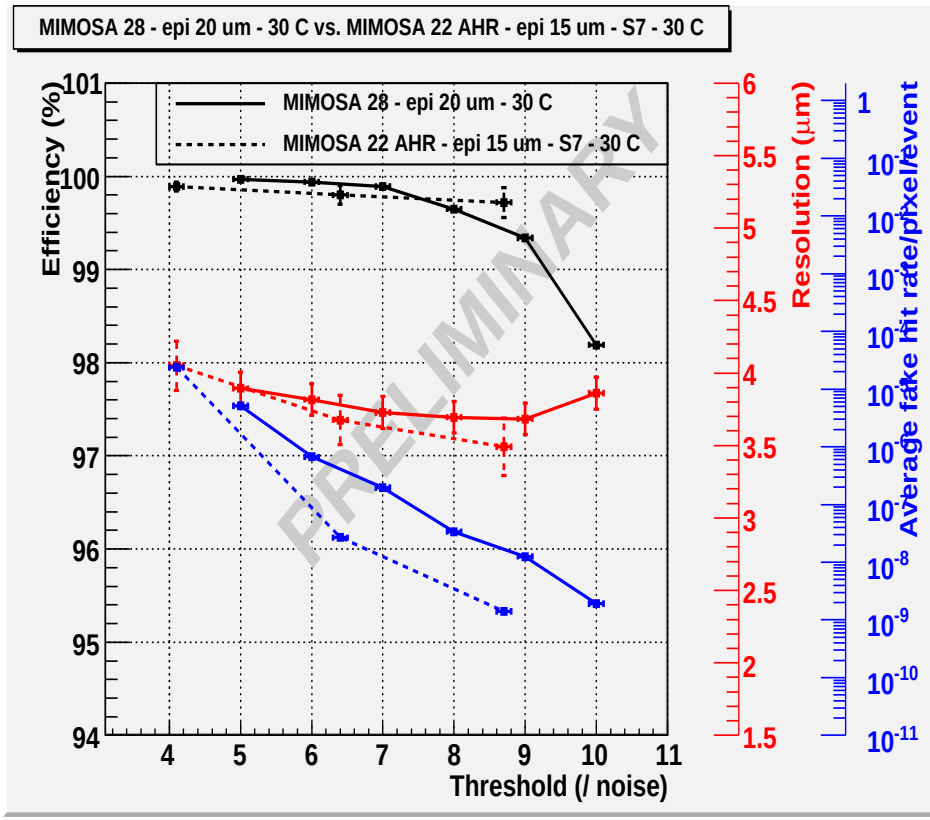
- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - ⋇ 0.35 μm process with high-resistivity epitaxial layer
  - ⋇ column // architecture with in-pixel cDS & amplification
  - ⋇ end-of-column discrimination & binary charge encoding
  - ⋇ on-chip zero-suppression
  - ⋇ **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)**
  - ⋇ **pitch: 20.7 μm $\rightarrowtail$ $\sim$ 0.9 million pixels**
    - ↪ **charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm** ▷ ▷ ▷
  - ⋇ JTAG programmable
  - ⋇ **$t_{r.o.} \lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s**
  - ⋇ 2 outputs at 160 MHz
  - ⋇ $\lesssim$ 150 mW/cm^2 power consumption





▷▷▷ **Tests under way since early April :** (50 μm thin)

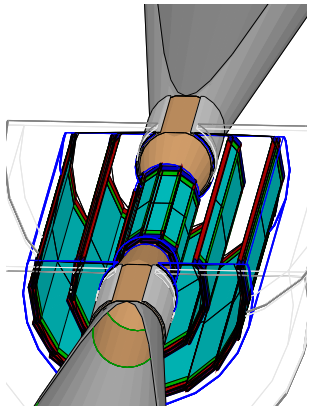
- ⋇ N $\lesssim$ 15 e$^-$ ENC at 30-35°C (as MIMOSA-22AHR)
- ⋇ CCE (^{55}Fe) similar to MIMOSA-22AHR
- —o Ionising rad. tolerance validated (150 kRad at 30°C)
- —o NI rad. tolerance validation (3$\cdot$10^{12}n$_{eq}$/cm^2 at 30°C) in Oct. 2011

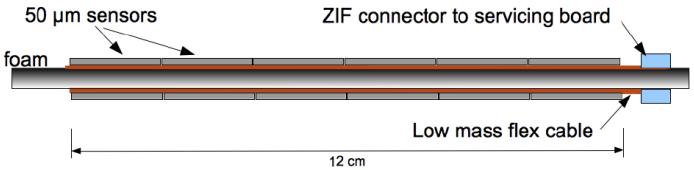


▷▷▷ **Start of data taking in FY-2012**

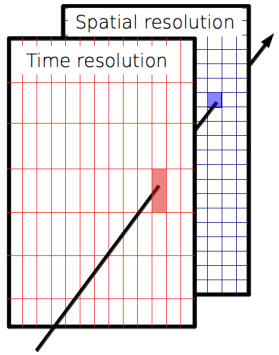
CMOS sensors for the ILD-VTX

- **Two types of sensors :**
  - ⋇ Inner layers ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ t$_{r.o.}$ $\sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 5 μm
  - ⋇ Outer layers ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ t$_{r.o.}$ $\sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⋇ Total VTX instantaneous (average) power $<$ 700 W (20 W)

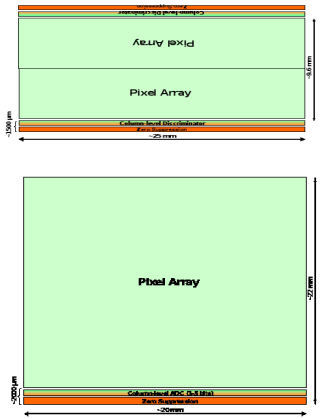




- **2-sided ladder concept for inner layer :**
  - ⋇ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} <$ 3 μm)
    & *E*longated pixels (16×80 μm^2) on external ladder face (t$_{r.o.}$ $\sim$ 10 μs)

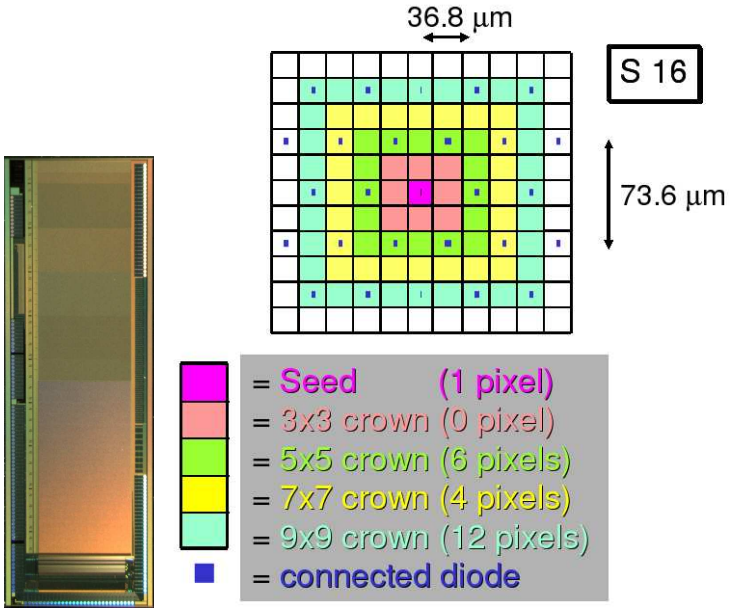


- **Sensor final prototypes :** submitted for fab. Sept. 4th, 2011
  - ⋇ MIMOSA-30: inner layer prototype with 2-sided read-out
    - ↪ one side : 256 pixels (16×16 μm^2)
      other side : 64 pixels (16×64 μm^2)
  - ⋇ MIMOSA-31: outer layer prototype
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC



Towards a Large Pitch

- **Large pitch : Motivations**
  - ⋇ elongated pixels allow faster read-out
  - ⋇ trackers (e.g. ILD-SIT) require $\sigma_{sp} \gtrsim 10\ \mu m$
  - ⇛ minimise number of pixels for the sake of power dissipation, integration time and data flow
- **Large pitch : Limitations (besides spatial resolution)**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - ⇛ particles traversing sensor "far" from sensing diodes may not be detected because of e^- recombination
  - ⋇ "fragile" detection efficiency, exposed to losses due to irradiation, high temperature operation & "slow" read-out
- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype, composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T ∼ 15°C)
    - —o $\epsilon_{det} \sim$ 99.8 %
    - —o $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)

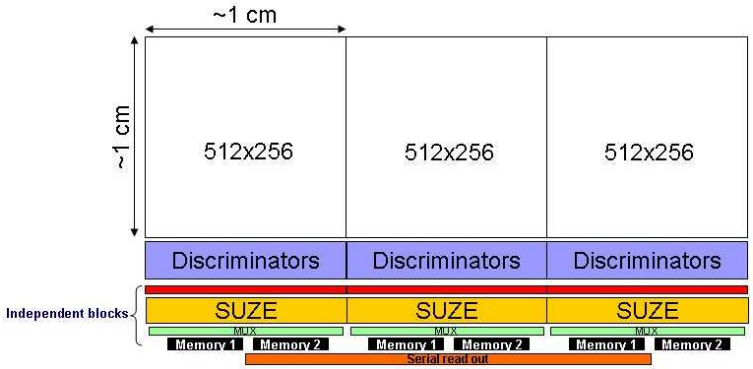


- **Square pixels : prototype back from foundry**
  - ⋇ MIMOSA-29 : fabricated on high-resistivity epitaxy in Summer '11
  - ⋇ pixels of 64×16/32/64 μm^2 and 80×16/48/80 μm^2
  - ⋇ chips back from foundry ⇛ test preparation under way

Moving to 0.18 μm CMOS Technology

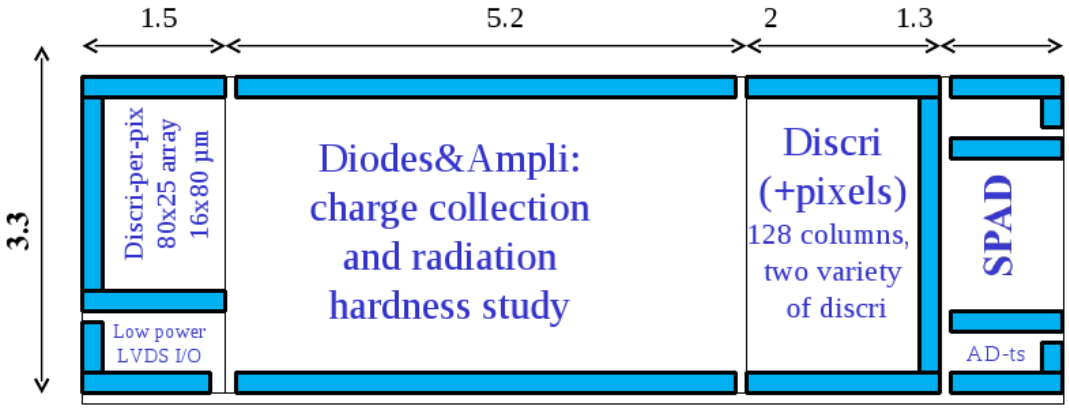
- **Evolve towards feature size $<<$ 0.35 μm :**
  - ⋇ **μcircuits :** 4-well, smaller transis., more Metal Layers, ...
  - ⋇ **sensing :** depleted epitaxy, low noise diode, ...
- **Benefits :**
  - ⋇ higher μcircuit density ⇛ higher data reduction capability
  - ⋇ thinner gates, depletion ⇛ improved radiation tolerance (in particular ionising radiation)
  - ⋇ faster read-out ⇛ improved time resolution
  - ⋇ possibility of stitching ⇛ multireticule sensors
- **Development plans :**
  - ⋇ also motivated by **ALICE-ITS/MFT, CMB-MVD, AIDA-**SALAT**, eRHIC-VD**, ...
  - ⋇ step 1 : MIMOSA-32 ▷ submission on 24.10.11
    - —o exploratory sensor (various sensing systems, amplifiers, discri., ...)
  - ⋇ step 2 : MIMOSA-22THR & SUZE-02 ▷ submission in Spring '12
    - —o M22-THR : 128 col. of 512 pixels, ended with discri.
    - —o SUZE-02: zero-suppression μcircuit
  - ⋇ step 3 : Full Scale Basic Block (FSBB) ▷ submission in Spring '13
    - —o 1x1 cm^2 sensitive area ($\sim$ 20 μm pitch)
    - —o combination of M22-THR & SUZE-02
    - —o scalable to various applications ($\geq$ 2014) ▷ ▷ ▷

FSBB



MIMOSA-32 : Prototyping a 0.18 μm Process

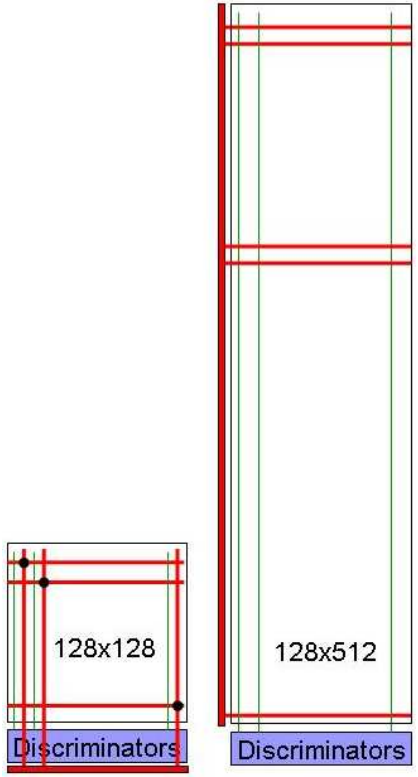
- **0.18 μm imaging technology options used :**
  - Epitaxial layer $\sim$ 14 μm thick with High-Resistivity (1-5 $k\Omega \cdot cm$)
  - Quadruple well : deep P-type layer embedding N-well hosting P-MOS transistors
  - "Low Leakage" transistors
  - MIM capacitors
  - start with 4 Metal Layers (6 ML run in 2012)
  - CIS (very low noise) sensing system



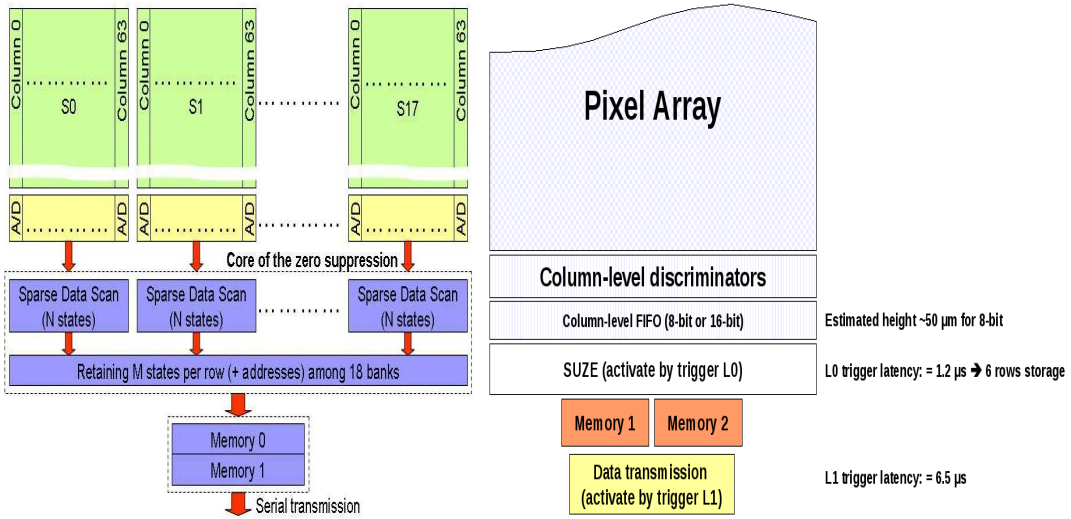
- **Prototype sub-divided in several blocks :** ▷ ▷
  - Sensing elements and in-pixel amplifiers :
    - pixel dimensions : 20$\times$20, 40, 80 μm^2
    - 3 different types of sensing elements : diodes of $\sim$ 10–150 μm^2
    - N-MOS and P-MOS transistor based amplifiers
  - Discriminators :
    - Col. // pixel array ended with 1 discriminator/col. (2 variants)
    - Pixel array with in-pixel discriminator (16$\times$80 μm^2 pixels)
  - Total surface $\sim$ 33 mm^2 ($\longmapsto$ 70 kE ?)
- **Submission :** *Octobre* 24th, 2011

MISTRAL : Architecture Prototyping

- **MIMOSA-22THR (Upstream part of MISTRAL) :**
  - ⁕ Col. // pixel array with in-pixel ampli + pedestral subtraction (cDS)
  - ⁕ Each of 128 columns ended with discriminator + 8 columns without discri.
  - ⁕ Pixel array sub-divided in sub-arrays featuring different pixel designs
  - ⁕ 2 options for row sequencer :
    - —∘ parallel to columns ⇛ dead zone inbetween neighbouring chips
    - —∘ together with signal processing circuitry ⇛ avoids the dead zone



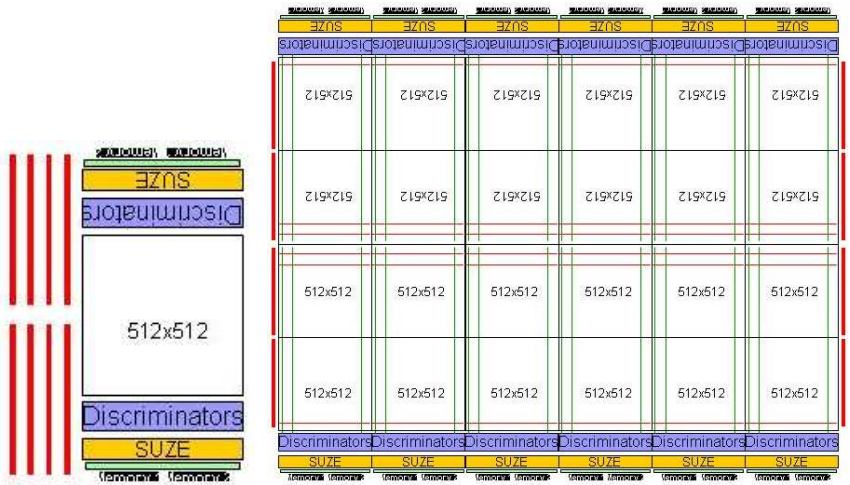
- **SUZE-02 (Downstream part of MISTRAL) :**
  - ⁕ $\emptyset$ μ-circuits & output buffers ($\equiv$ SUZE-01)
  - ⁕ add trigger L0 info after discriminators for data filtering ⇛ flow & power reduction ?
  - ⁕ add trigger L1 (?) downstream of output buffers for further filtering ?



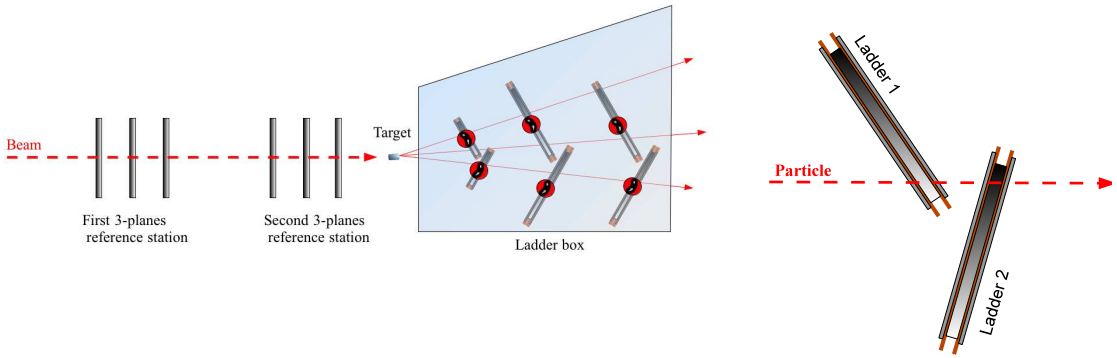
- **Submission** $\leq$ Spring 2012
  - ↪ determine sensor adequacy w.r.t. rad. tol. spec.

AIDA Project : Assessment of Stitching & 2-Sided Ladder

- **Single Arm Large Area Telescope (SALAT):**
  - ※ *2048×3072 pixels (∼ 20 μm pitch)*
    - ⇛ *4×6 cm^2 sensitive area, ∼ 3.5 μm spatial resolution*
  - ※ *requires combining several reticules (based on FSBB)*
    - ⇛ *stitching process ⇛ establish proof of principle*
  - ※ *2-sided read-out of 1024 rows in ∼ 200 μs*
    - ⇛ *3 planes of Large Area Telescope for AIDA project (EU-FP7)*
  - ※ *windowing of $\lesssim$ 1×6 cm^2 (collimated beam)*
    - ⇛ *∼ 50 μs r.o. time*
  - ※ *50-100 μm pitch variants under consideration (trackers)*



- **Alignment Investigation Device (AID) :**
  - ※ *box allowing to mount 3 pairs of ladders arranged in 3 consecutive layers ≡ VTX sector*
  - ※ *can be equipped with PLUME (2-sided) ladders*
  - ※ *ladders are mounted on movable micrometric support*
    - ⇛ *investigate alignment with particles traversing overlapping regions of neighbouring ladders*
  - ※ *allows developing clustering, tracking & vertexing algo. with particle beams*



SUMMARY

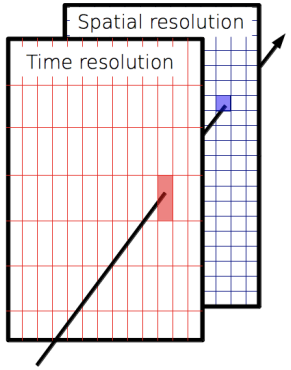
- **Sensor architecture developed in 0.35 μm technology validated :**
  - ▷ complies with specs of σ_{sp}, thickness, rad. tol. (T_{room}), r.o. speed & P_{diss} of VTX
  - ▷ sensors getting implemented in various devices: STAR-PXL, NA-63, CMB-MVD, ALICE-ITS & MFT ? , ...
  - ▷ final prototypes under way : MIMOSA-30(in) & MIMOSA-31(out)
  - ▷ validation of complete concept in 2012

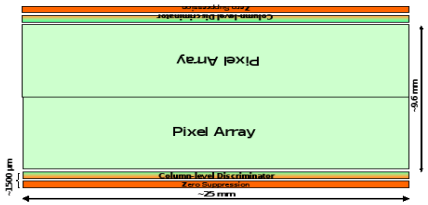
- **Translation 0.35 $\mu m \rightarrowtail$ 0.18 μm CMOS under way :**
  - ▷ exploratory chip (MIMOSA-32) to be submitted for fabrication on 24.10.2011
  - ▷ mid-scale prototypes validating architecture (MIMOSA-22THR, SUZE-02) in Summer 2012 ▷ DBD
  - ▷ Full Scale Basic Block (FSBB) expected to be validated in 2013
  - ▷ design flexible enough to be adaptable to various designs

- **Long range R&D : In-pixel discri., 3D sensors for SiD, ILC-1000, CLIC**

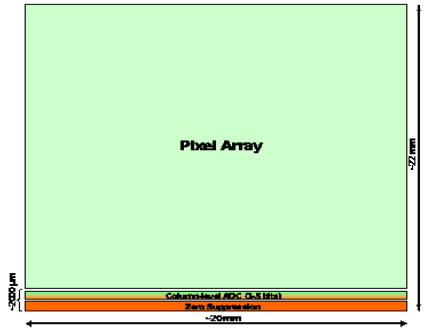
Mid-Size Prototypes of Inner & Outer Layer CPS

- **Inner layers ⇛ 2-sided read-out prototype MIMOSA-30**
  - 2-sided read-out : square pixels on one side, elongated pixels on other side
  - 128 columns of 256 pixels (16×16 μm^2) :
    - r.o. time ∼45 μs
    - expected σ_{sp} ∼ 2.7-2.8 μm (binary charge encoding)
  - 128 columns of 64 pixels (16×64 μm^2) :
    - r.o. time ∼10 μs
    - expected σ_{sp} ∼ 5 μm (binary charge encoding)
  - 8 columns with analog output on each side





- **Outer layers ⇛ large pitch prototype MIMOSA-31**
  - single side read-out with 2-4 bit progressive charge encoding
  - 48 columns of 64 pixels (35×35 μm^2) :
    - corresponding $t_{r.o.}$(2 cm long columns) ∼100 μs
    - expected σ_{sp} ∼ 4 μm (≤4-bit charge encoding)
  - 8 analog outputs (no ADC)



- **Both sensors were sent for fabrication early Septembre '11**
  - expected back in Decembre '11 ⇛ lab tests in Q1+Q2 (2012)
  - beam tests in Summer 2012 ? ⇛ in time for DBD ?