DEPFET APS – from ILC to SuperKEKB to future linear colliders

- DEPFETs at Belle II
- Module Concept
- results with 50µm thin DEPFETs ..

Laci Andricek for the DEPFET collaboration

KEKB to SuperKEKB

Machine parameter	HER (KEKB)	LER (KEKB)	HER (SuperKEKB)	LER (SuperKEKB)
Vertical beam size	0.94μm	0.94μm	59nm	59nm
Beam current(mA)	1188	1637	2600	3600
luminosity($cm^{-2}s^{-1}$)	$2.1x10^{34}$		$8x10^{35}$	

-: e^-/e^+, 7 GeV & 4 GeV

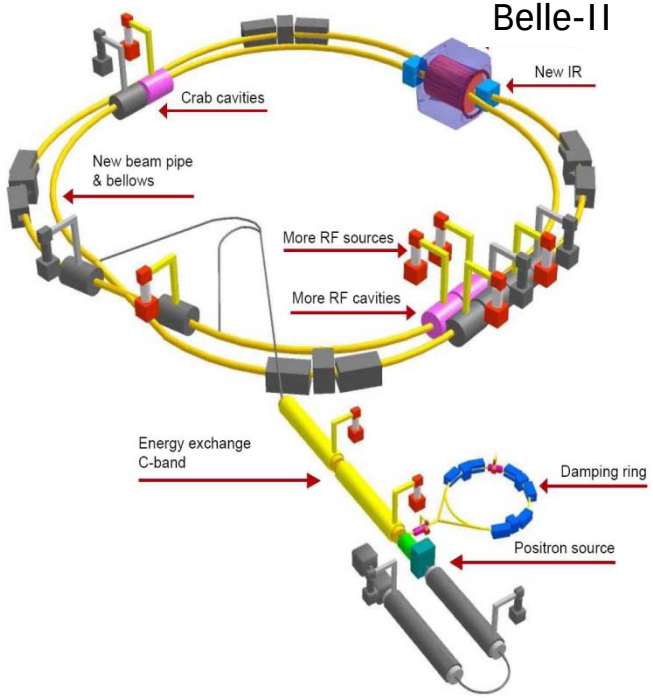
-: E_{cm} at Y(4s) Resonance, (10.58 GeV)

-: goal L = $8x10^{35}$ $cm^{-2}s^{-1}$

Schedule and Milestones:

10/2014 ..... first beam
10/2014 – 05/2015 ..... beam commissioning
05/2015 – 09/2015 ..... shut down, sub-det install.
09/2015 – 11/2015 ..... det. commissioning
12/2015 ..... physics run

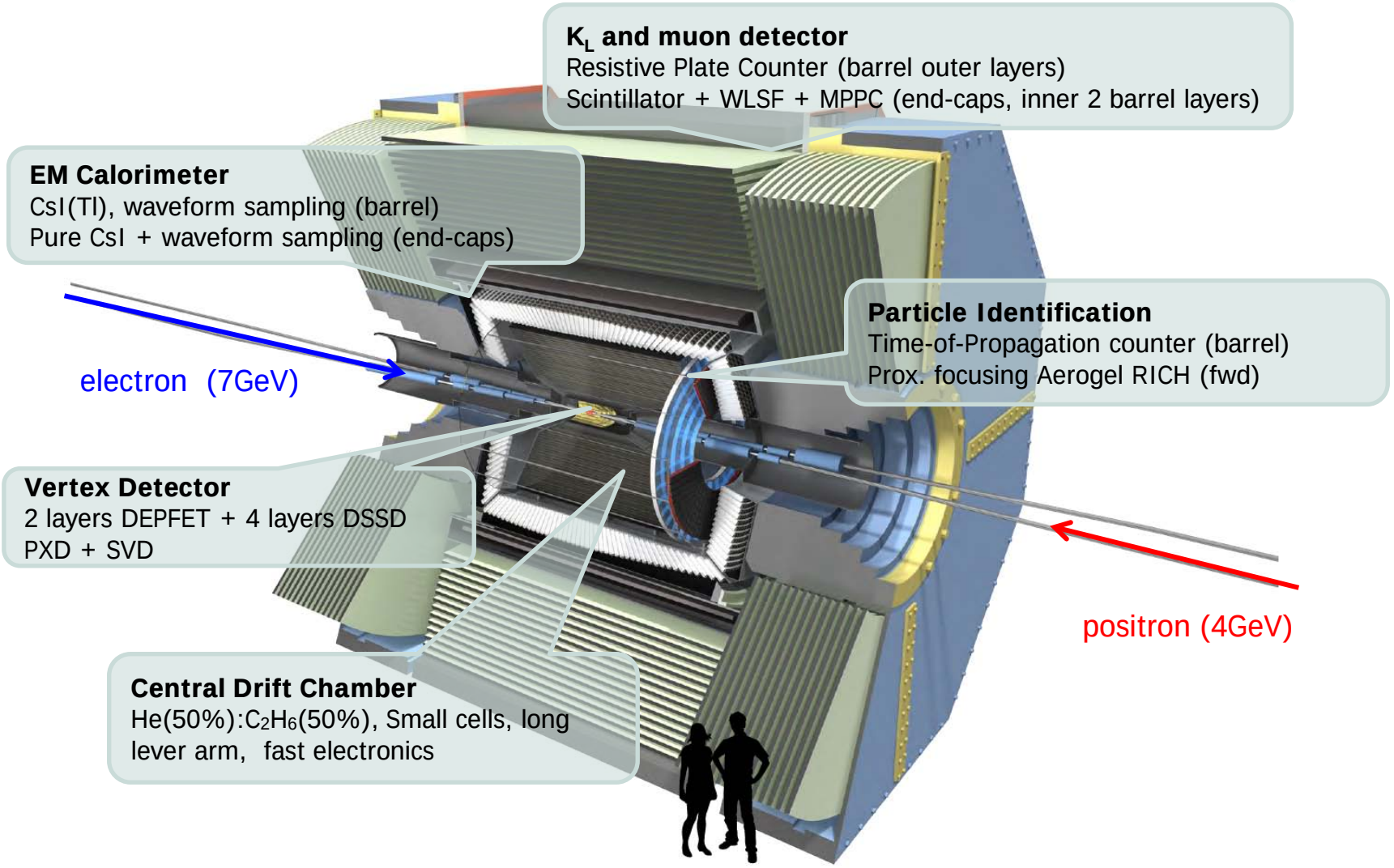
Belle-II



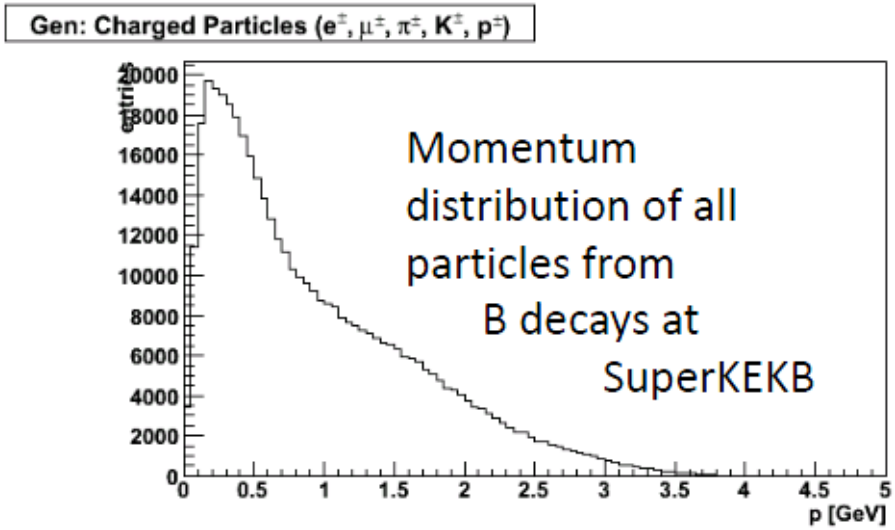
Smaller beam size & more current:
→ 40x higher luminosity

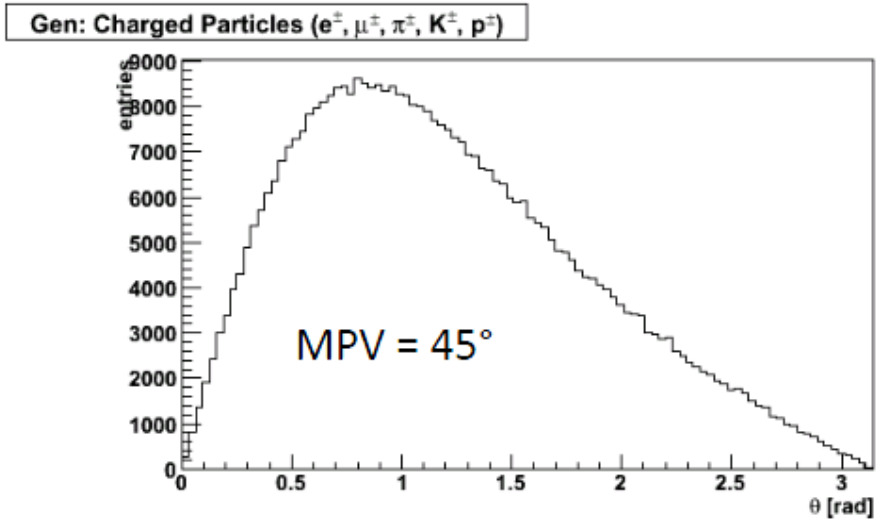
Higher Background: occupancy and rad. damage
-: QED background, intra-beam scatter., beam-gas, synchrotron

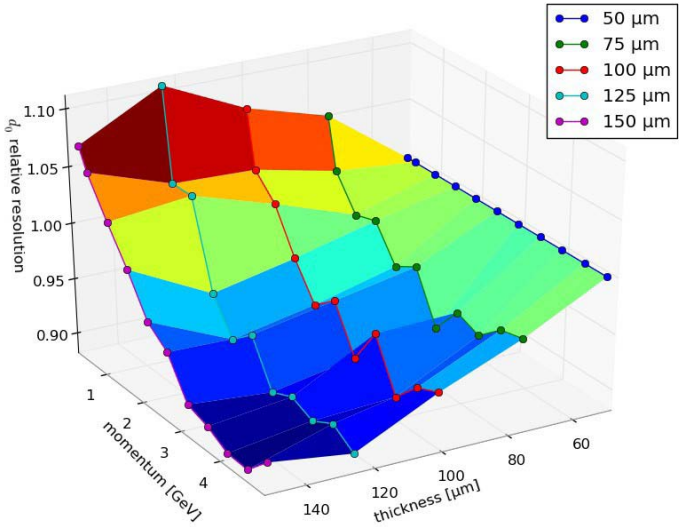
Belle II at SuperKEKB



Which physics to optimize for?



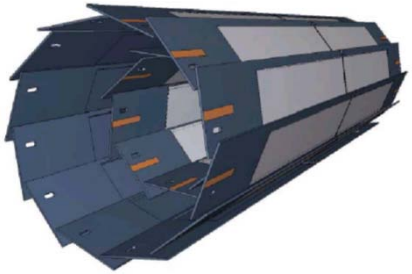




Find best technically feasible compromise:

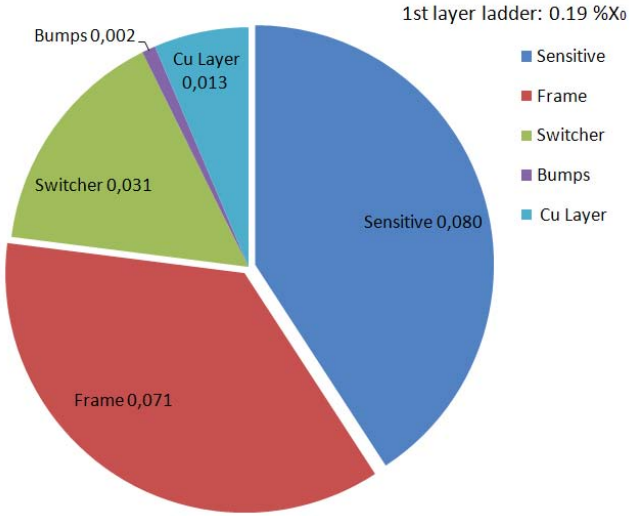
- for central und forward region
- signal/noise of the sensors
- # of r/o channels
- occupancy
- single point and impact parameter res.

The DEPFET Belle-II PXD

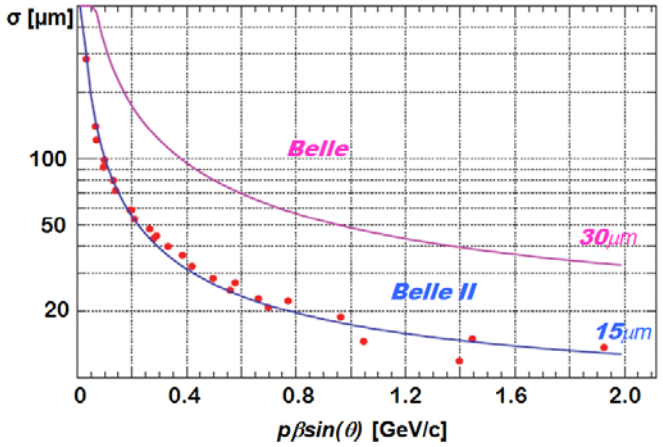


Angular coverage 17°<θ < 155°

	Inner layer	Outer layer
# ladders	8	12
Sens. length	90 mm	123 mm
Radius	1.4 cm	2.2 cm
Pixel size	50x50 μm^2	50x75 μm^2
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 μm	75 μm
Frame/row rate	50 kHz/10 MHz	50 kHz/10 MHz

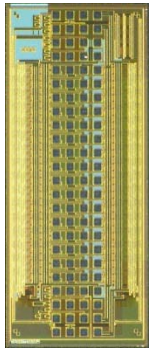


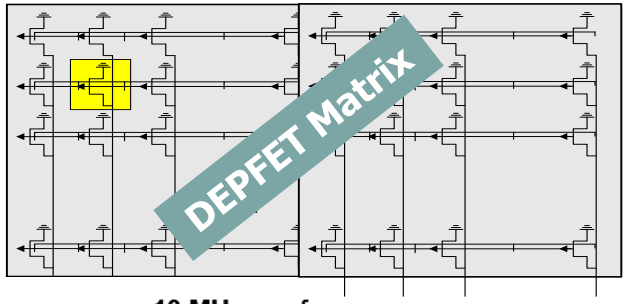
z vertex resolution significantly improved (PXD & SVD)



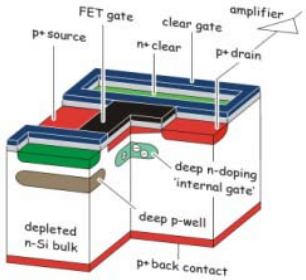
DEPFET and auxiliary ASICs

Switcher:
180nm HVCMOS AMS
Size 3.6 × 1.5 mm²
Gate and Clear signal
Fast HV up to 20V

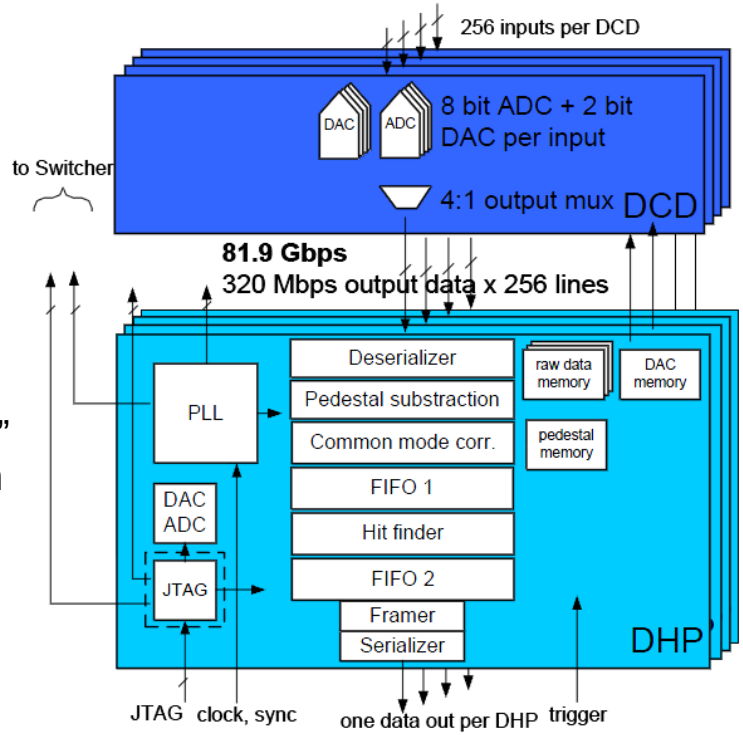




10 MHz row frequency
100 ns ADC conversion time



DCD:
"Drain Current Digitizer"
UMC 180nm
f/e and ADC



5 Gbps (1.25 Gbps link per DHP)

DHP:
"Data Handling Processor"
IBM 90nm → TSMC 65nm
Digital control chip

Power dissipation

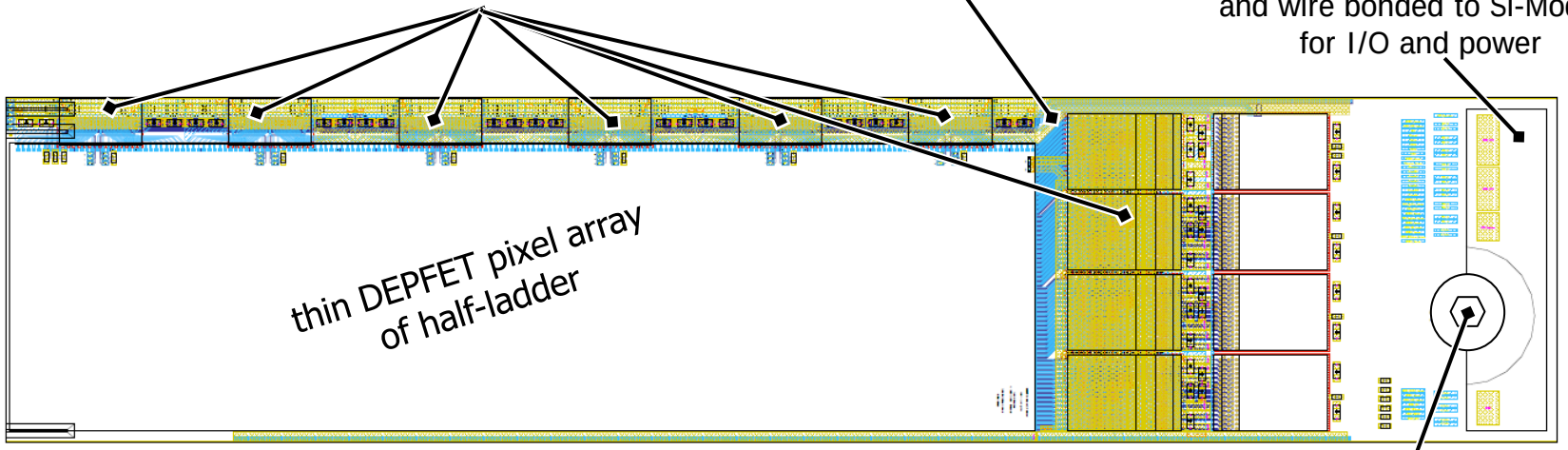
DEPFETs	~	1 W
Switcher	~	1 W
DCD/DHP	~	8 W on each ladder end

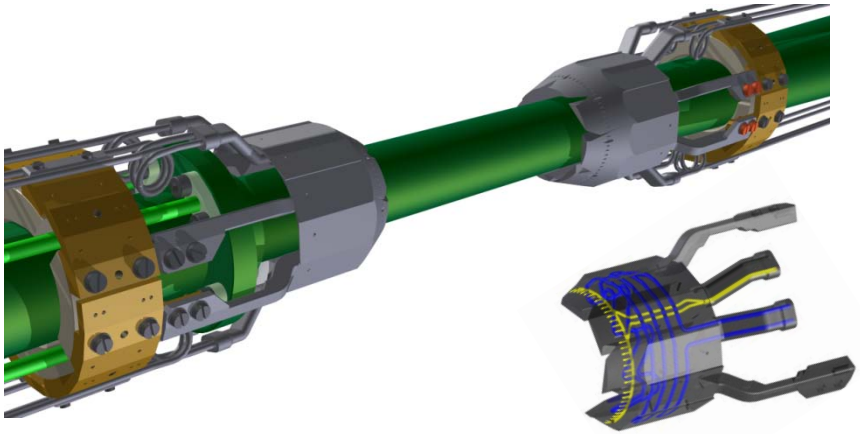
→ 160 W on each side of the detector
→ 40 W in sensitive volume

- CO_2 cooling at end flange
- gentle gas flow in sensitive region

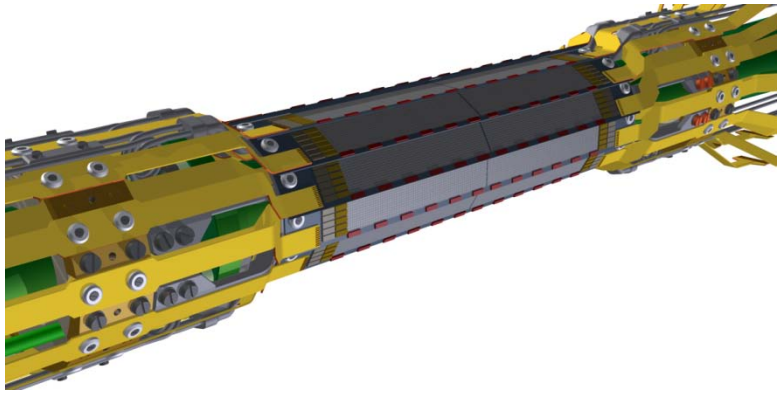
→ see Arantza's talk in R&D7, Thursday morning

self supporting all-silicon module

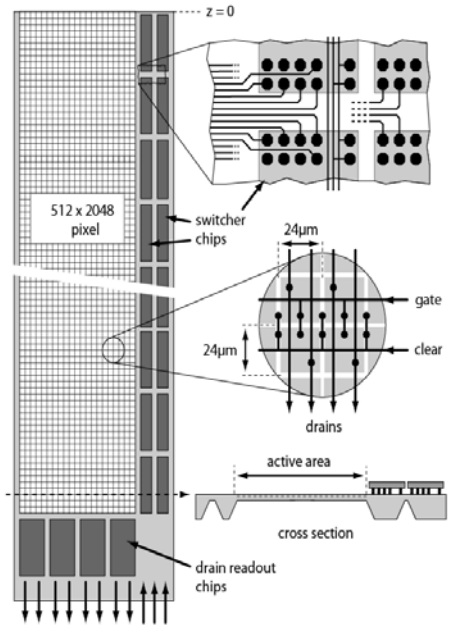


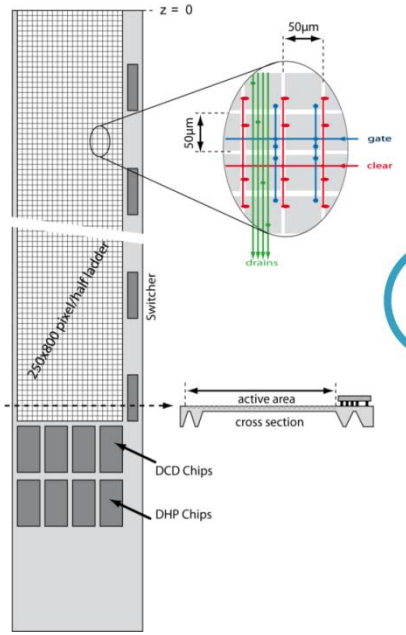


end-flange with CO2 channels and capillaries for air cooling (RPT sinter process)



ILC VXD vs. SuperKEKB PXD (from a DEPFET point of view)

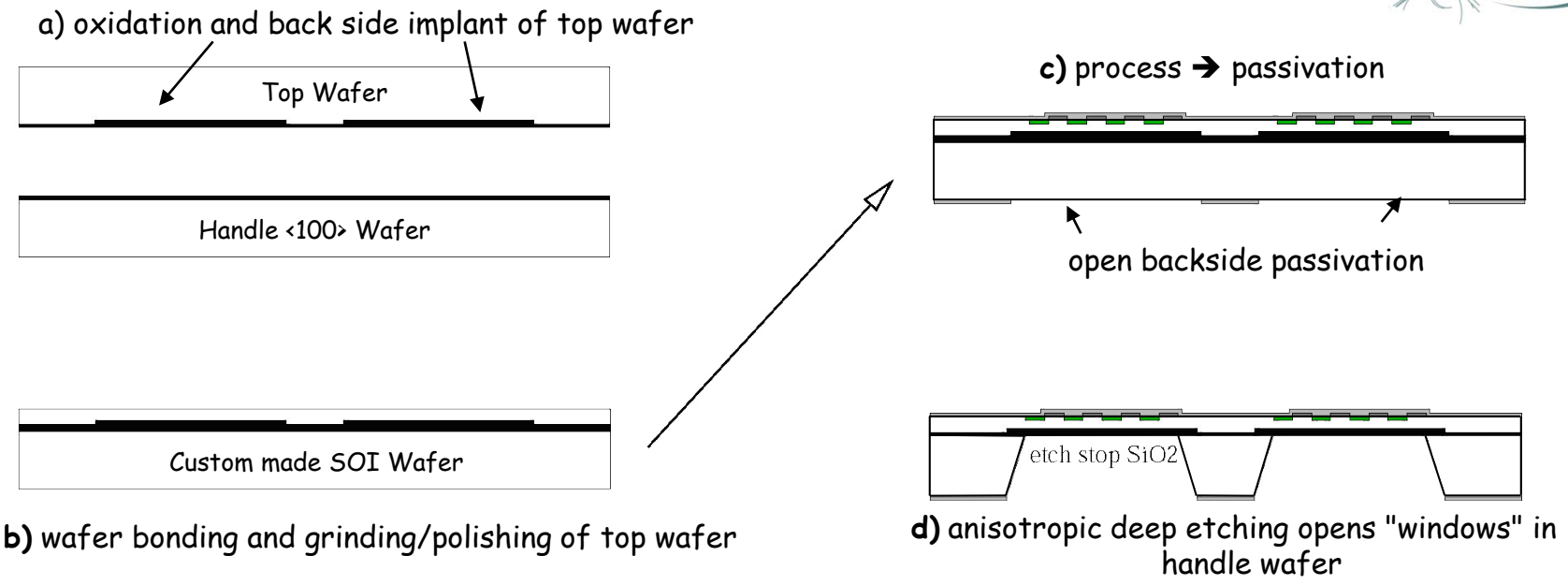




-: radii: 15, 26, 37, 48, 60 mm	.....	14, 22 mm
-: ladder length: 125mm(L0) and 250mm(L1-4)	.....	136 mm(L0) and 169mm(L1)
-: sensitive width: 11mm (L0), 15mm(L1), 22mm(L2-4)	.....	12.5mm (L0, L1)
-: number of ladders: 10/11/12/16/20 → 130 sensors	.....	8/12 → 40 sensors
-: pixel size: ≈20 µm	.....	50x50 µm^2 (L0) 50x75 µm^2 (L1)
-: Row rate: ≈20 MHz	.....	≈10 MHz
-: number of pixels: ≈800 Mpix	.....	≈8 Mpix

minimal material in both application!!! (for sensor and support)

Processing thin detectors - the SOI approach

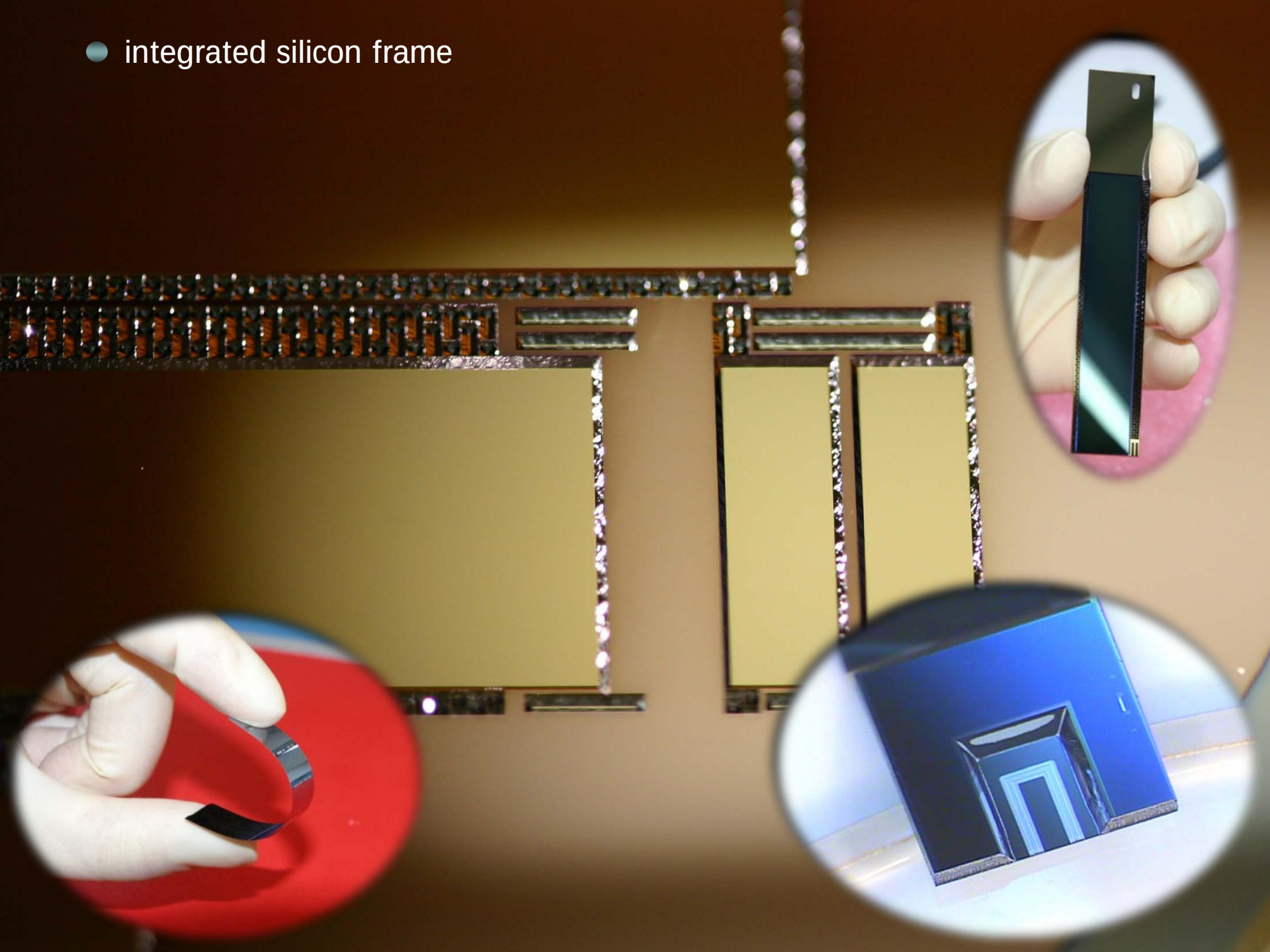


The DEPFET thickness becomes a free parameter, adjustable to the needs of the experiment!

Key Process Modules:

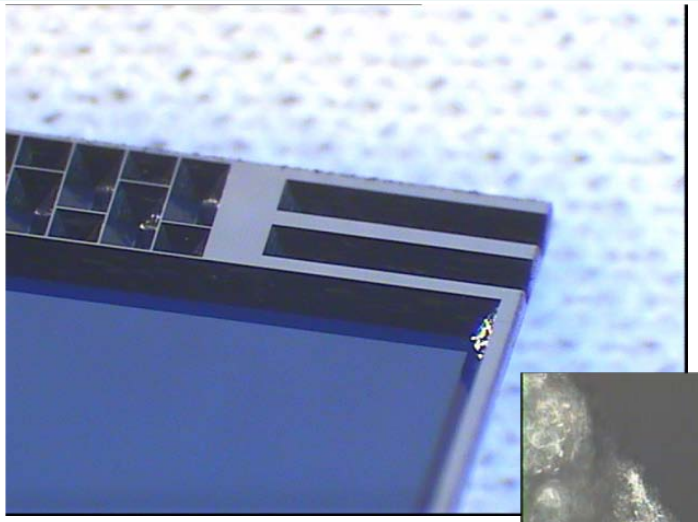
-: Wafer Bonding and thinning of top layer (external)
-: Sensor fabrication on SOI
-: Etching of the Handle Wafer
-: Litho on extreme topographies

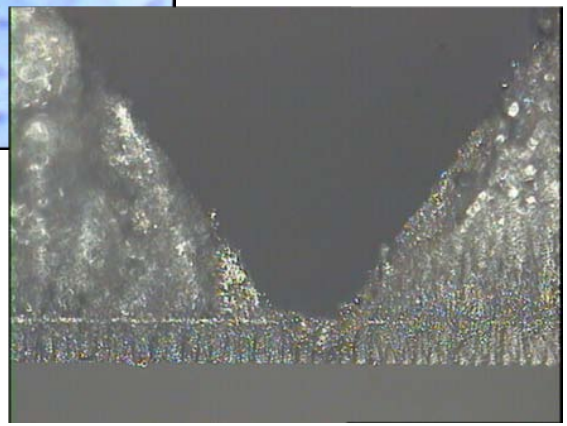
- integrated silicon frame



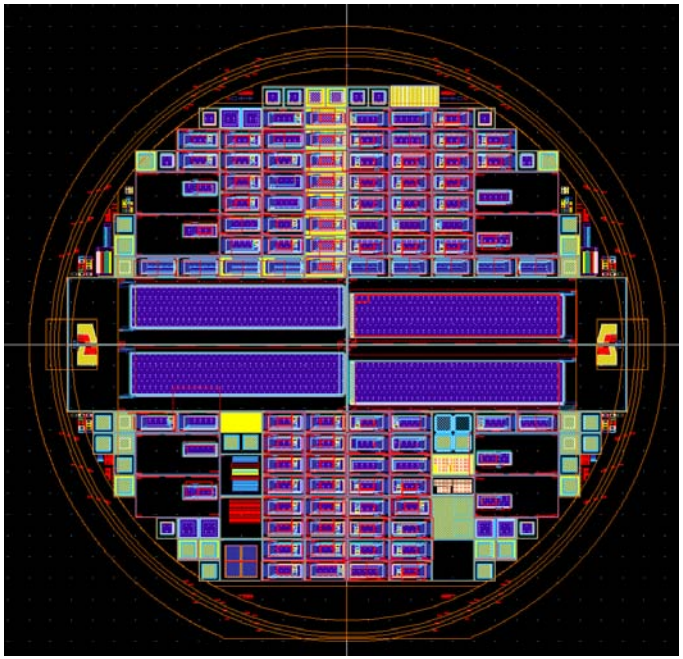
Micro joint between half-ladders

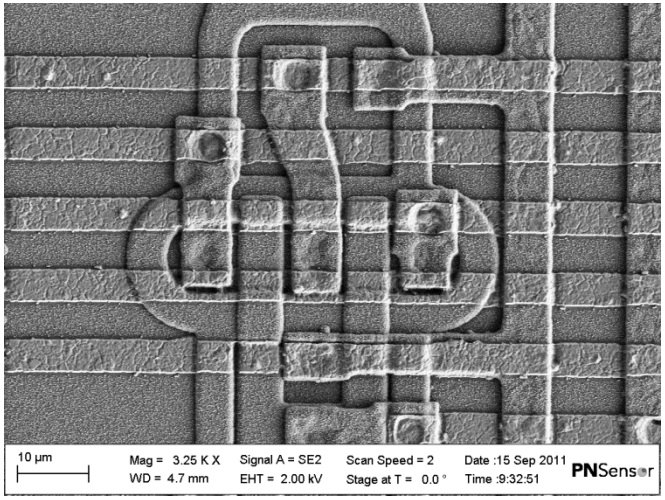
- butt-joint between two half-ladders
- reinforced with 3 ceramic inserts
- 2x300µm dead area per ladder
- mechanical tests → remarkably robust!!
- bowing: up to 1 mm sagitta (over 10 cm)
- tension: 40 to 60 N, then the Si broke



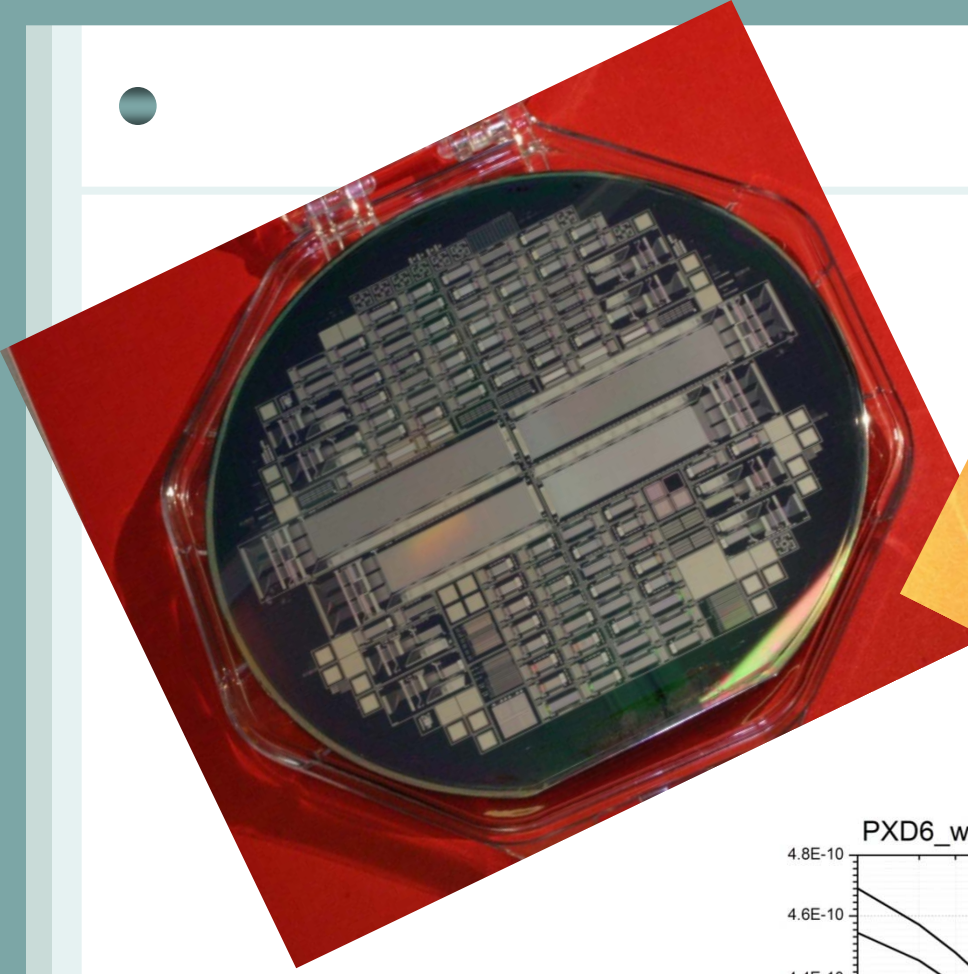


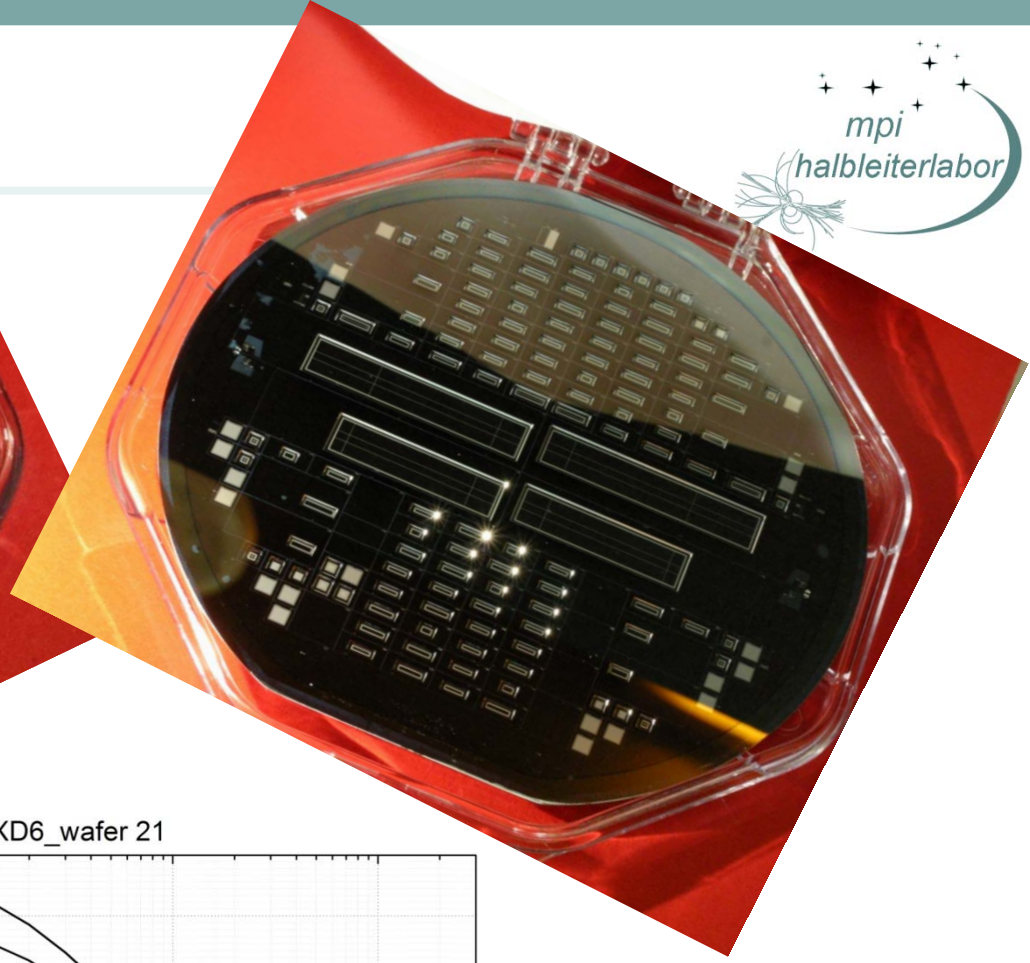
PXD6: prototyping for Belle II and ILC

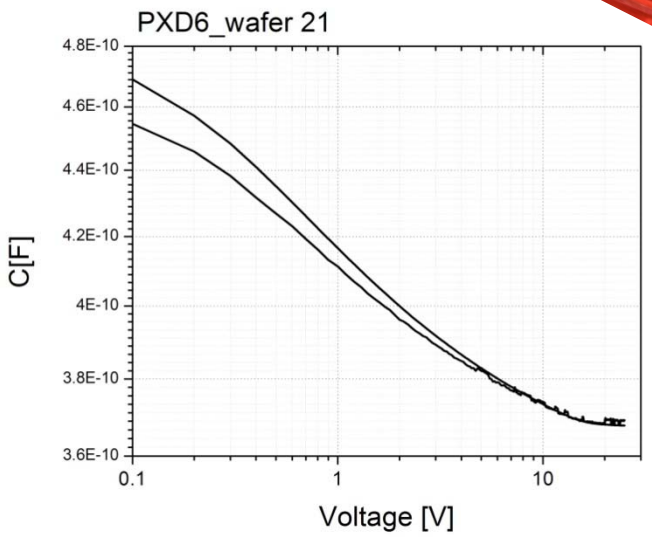




- 8 SOI wafers (50 top layer, 400 µm handle wafer)
  + 2 reference wafers on std. 450µm material
- Pixel design and material (“low res” FZ) adapted to 50 µm top layer thickness (Vfd≈15V), extensive device simulations to find the right geometry for the optimal electric field shape
- About 100 test matrices in different variations
  - pixel sizes from 20 µm to 200 µm
  - shorter gate length,
  - improved clear structures,
  - various field shapes..
- Technology variations on the wafer level (new dry etch techniques..)
- 4 half-ladders for Belle II with the most promising design options







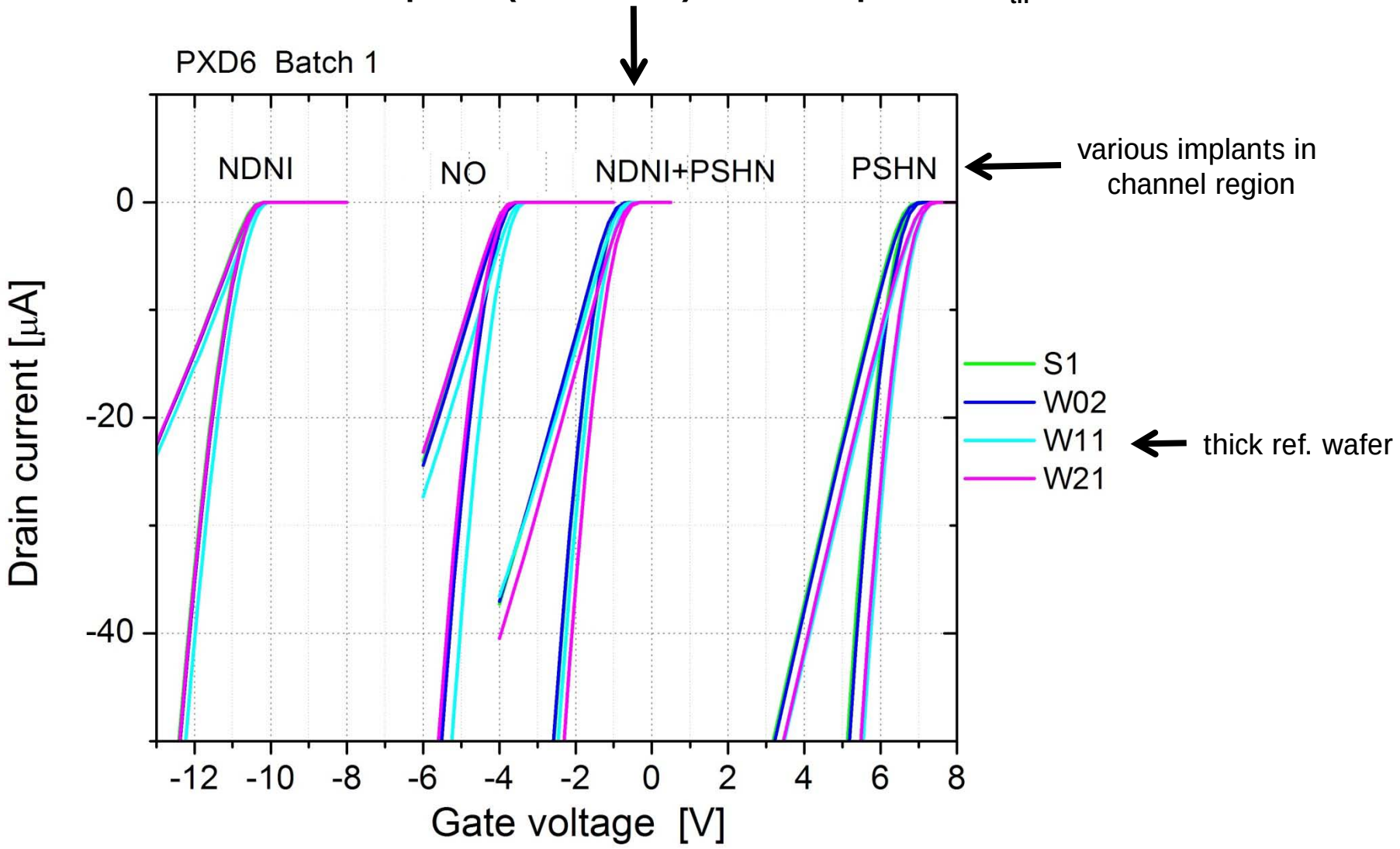
CV measurements:

- ✓ Full depletion as expected 10..15 V
- ✓ from C_{min}: thickness **is** 50 µm ☺

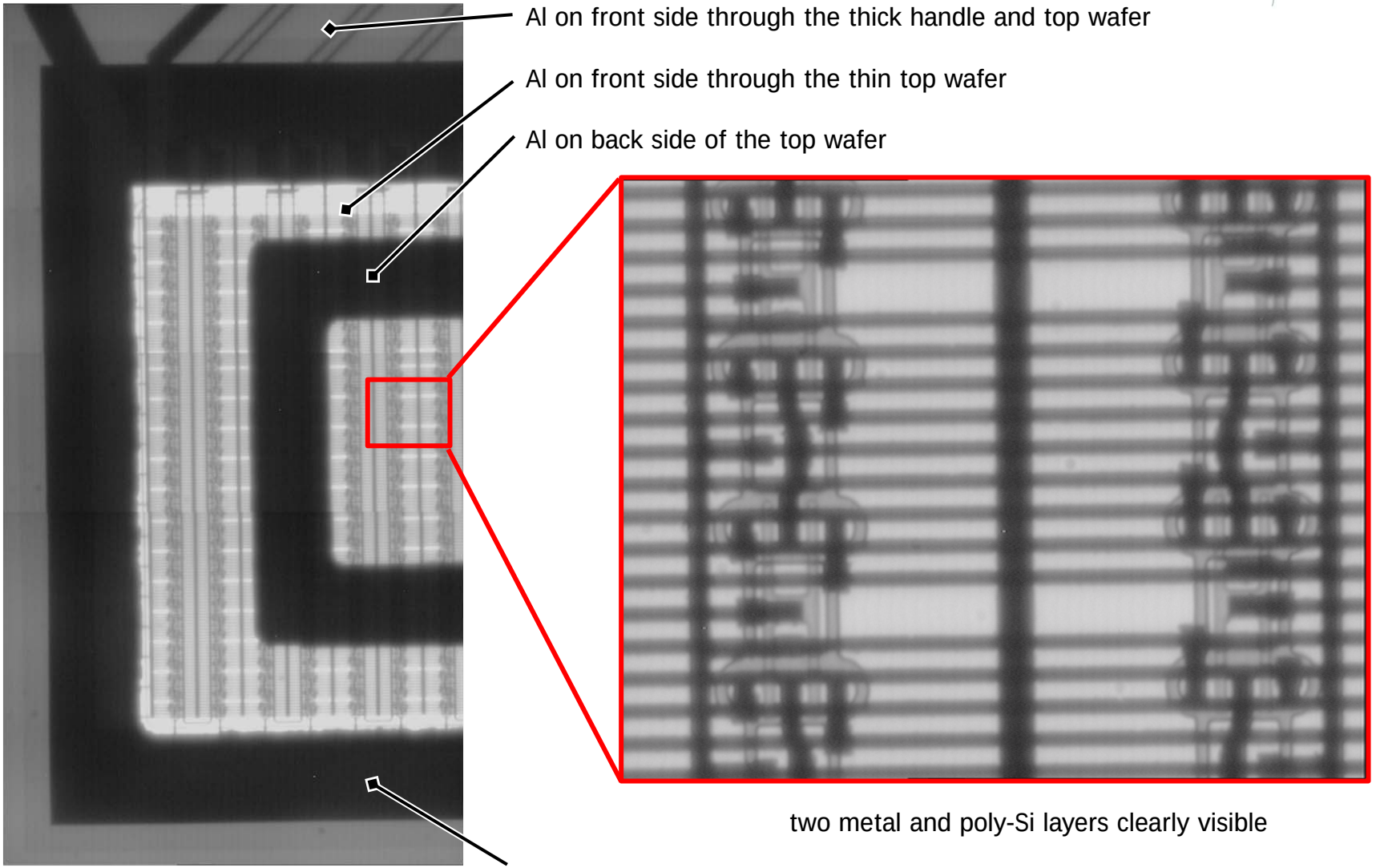
IV measurements: $I_{rev} \approx$ 200 pA/cm^2

- DEPFET (and MOSFET) input characteristics → V_{th}

MOSFET with all implants (→ DEPFETs) have as expected a V_{th} ~ 0V

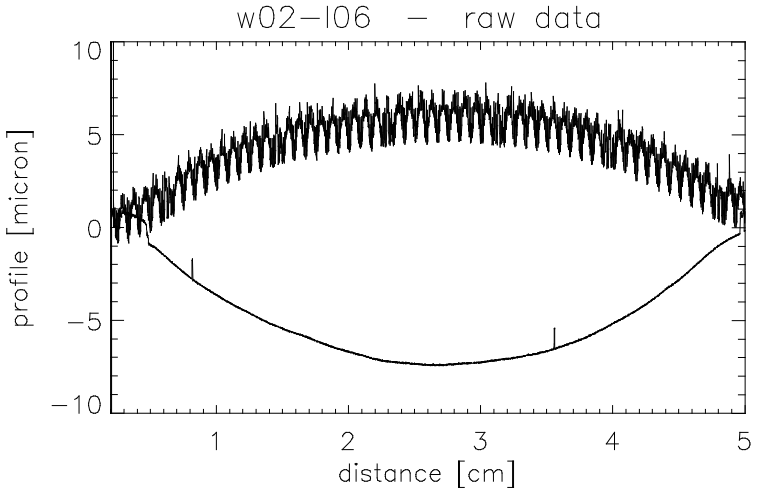


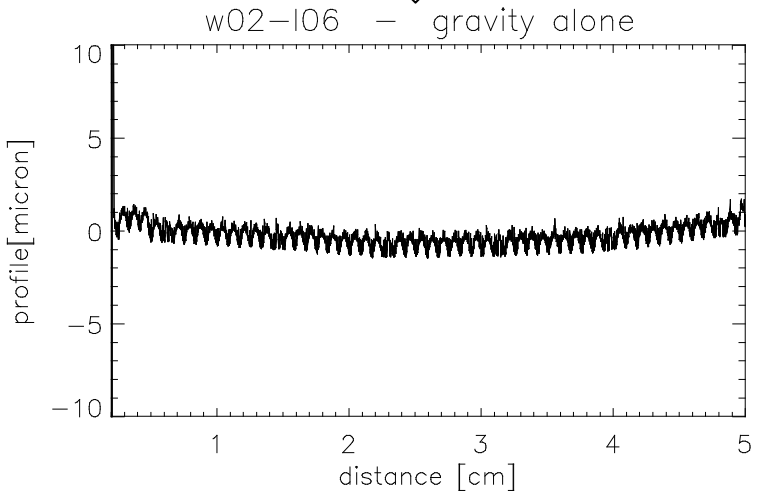
IR micrographs

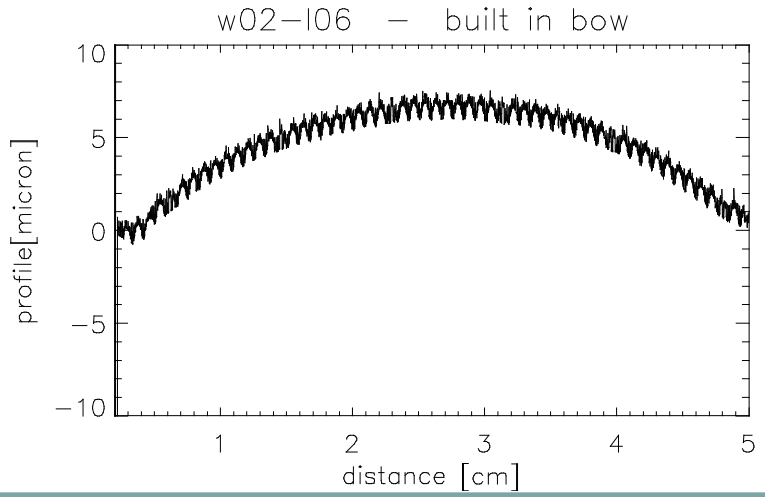


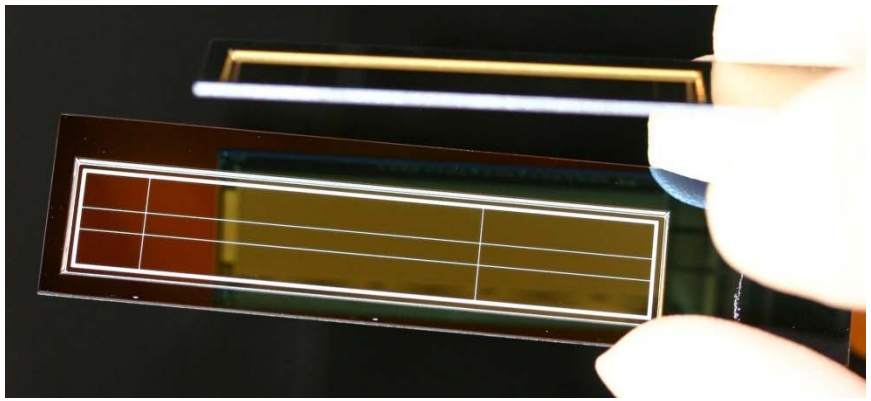
distortions – bow and warp

gravity effect = Δy/2





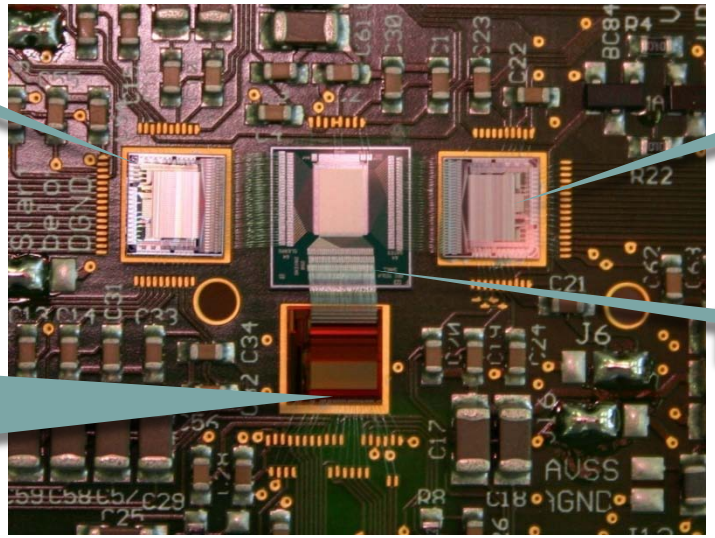




first tests with the well known ILC prototype system

Gate Switcher

Clear Switcher



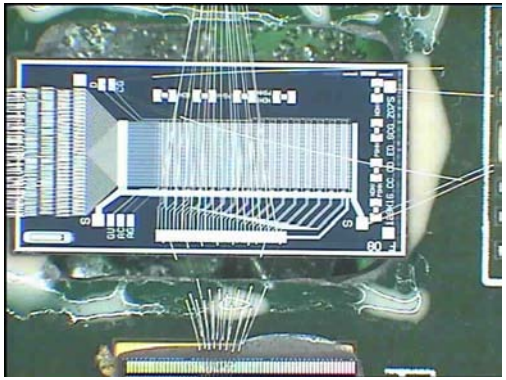
thick ILC DEPFET Matrix

r/o ASIC CURO

- current based readout chip
- 50 MHz band width in the f/e

- our well known work horse since years!
- but with known features resulting in a higher noise

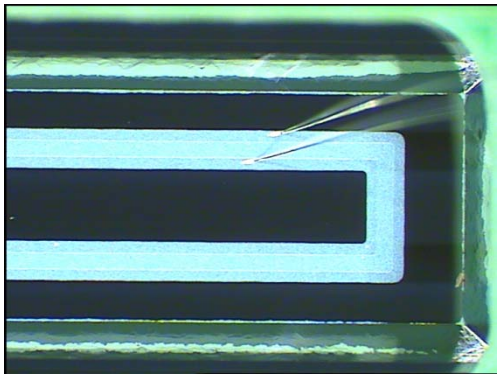
→ layout of the sensor has changed and so did the connections to the read-out system!!



creative bonding on the front

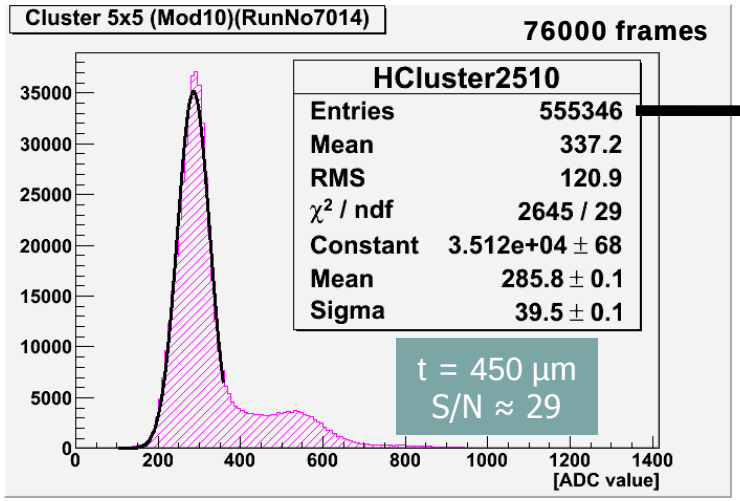
Many thanks to Danilo,
our wire bond expert!!!

wire bonds on 50 µm Si on the back

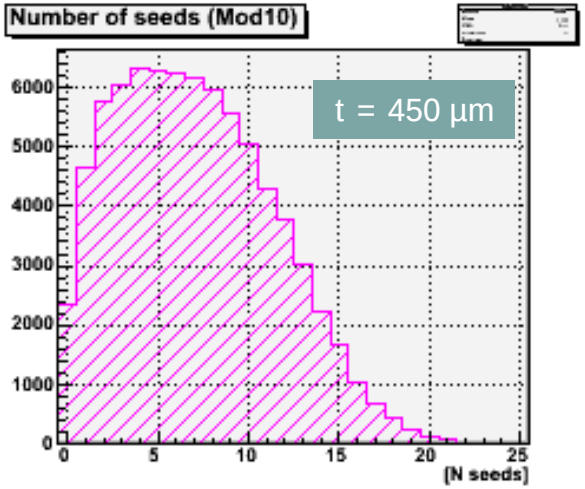


signal measurements I – Cd109

- 2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm², same design on front
  - I : 450 µm standard FZ material
  - II: 50 µm SOI

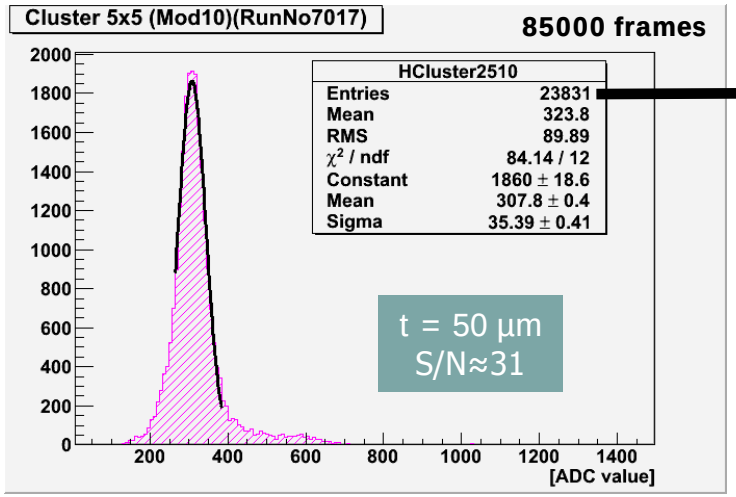


Thick: 7 clusters/frame

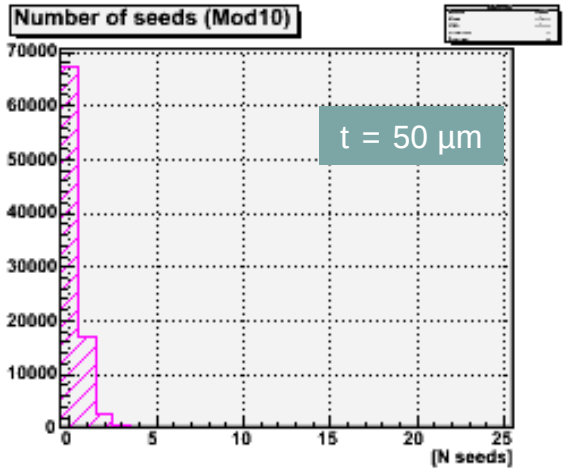


- 22keV photons
- ~6000 e/h pairs
- does not depend on t!

- but count rate is reduced
- photons just pass w/o conversion

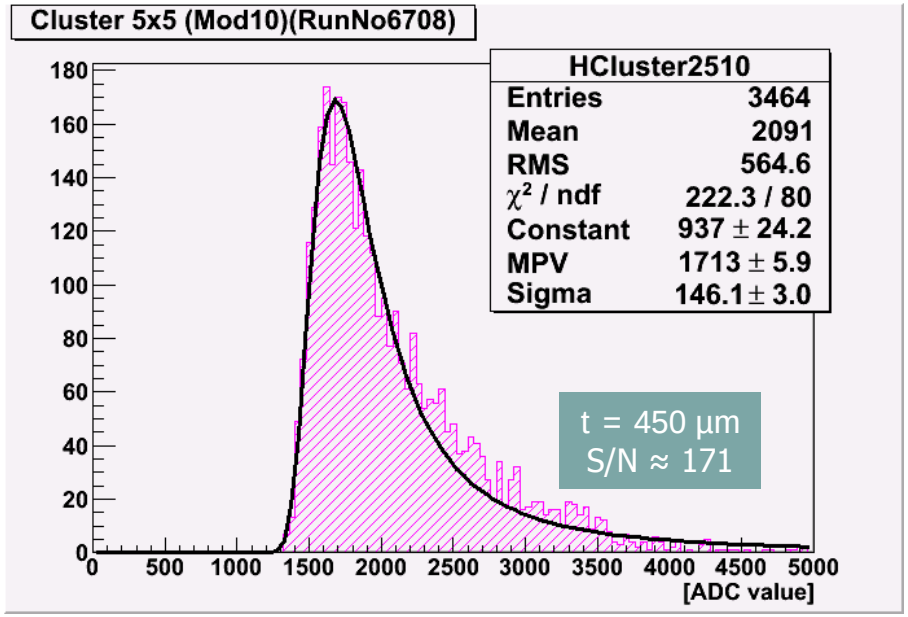


Thin: 0.28 clusters/frame

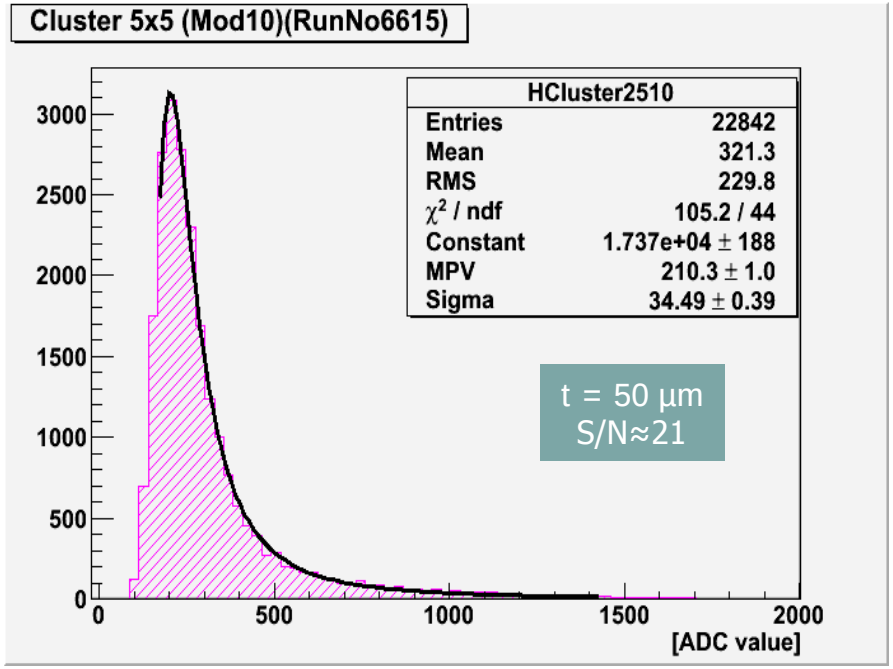


signal measurements II – Sr90

- 2 DUTs: 32x64 pixels Belle II PXD design, L=6 µm, pixel size 50x75 µm², same design on front
  - I : 450 µm standard FZ material
  - II: 50 µm SOI



- β source, ~2MeV end energy, close to mip
- photons and LE e⁻ blocked by 4.3 mm plastic
- external scintillator trigger below the sensor



- from Cd90 we know: 1 ADU → 19.8 e⁻
- Sr90 signal with 50µm: 210 ADU → 4164 e⁻
- expect ~80e-/µm for a mip: ~4000 e⁻ for 50µm
- signal(450µm) : signal(50µm): 8.2

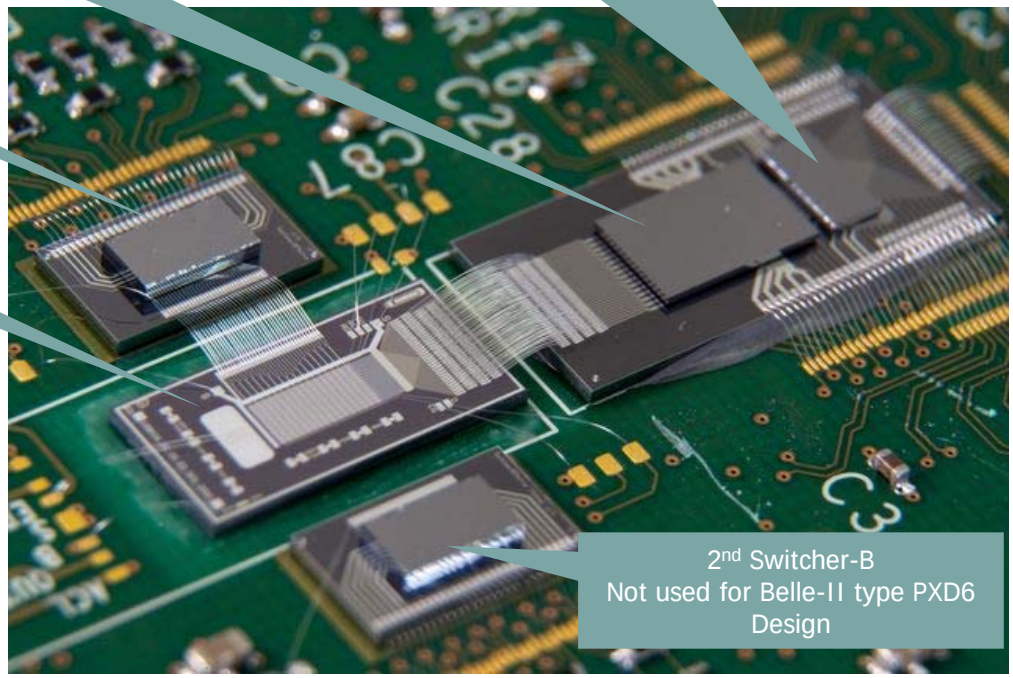
The new r/o system

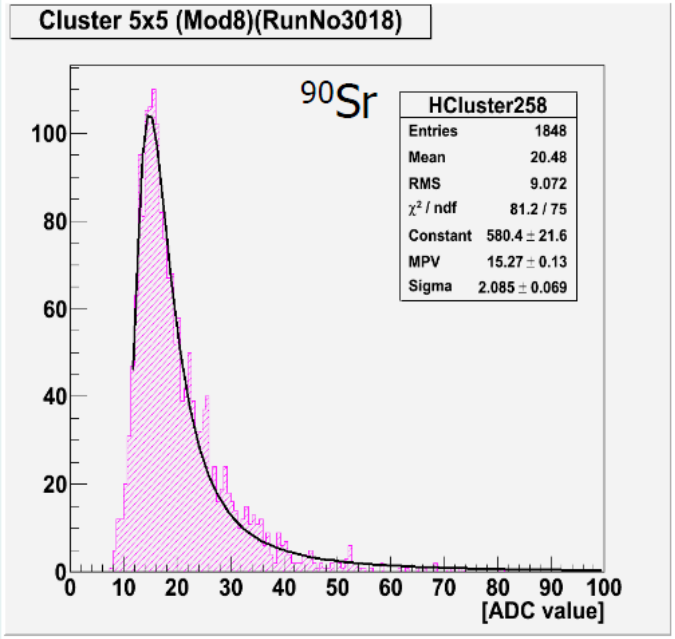
Switcher-B
for Clear and Gate Control

DCD-B
Read-out Chip

DCD-RO
Line Driver and Buffer to FPGA

PXD6 Belle-II DEPFET
Matrix 32x64 Pixels
L = 6 µm
Pixel Size 50 x 50 µm²

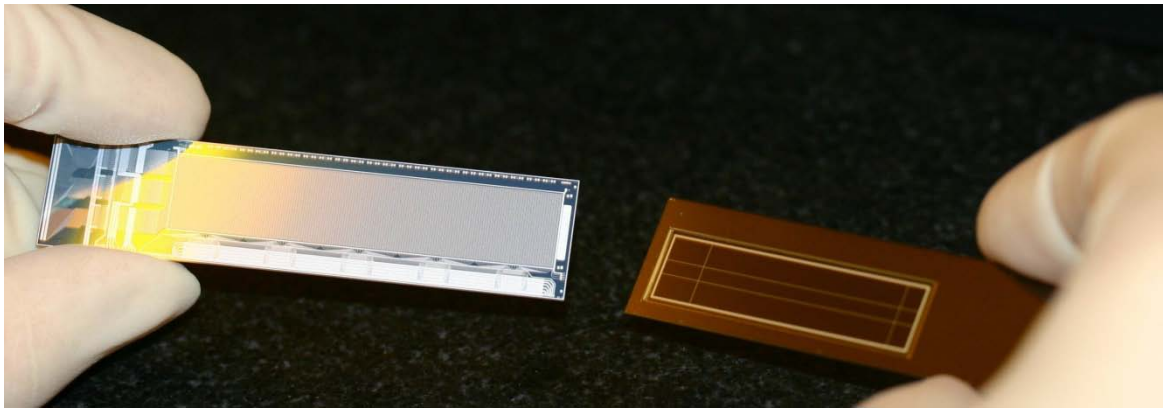


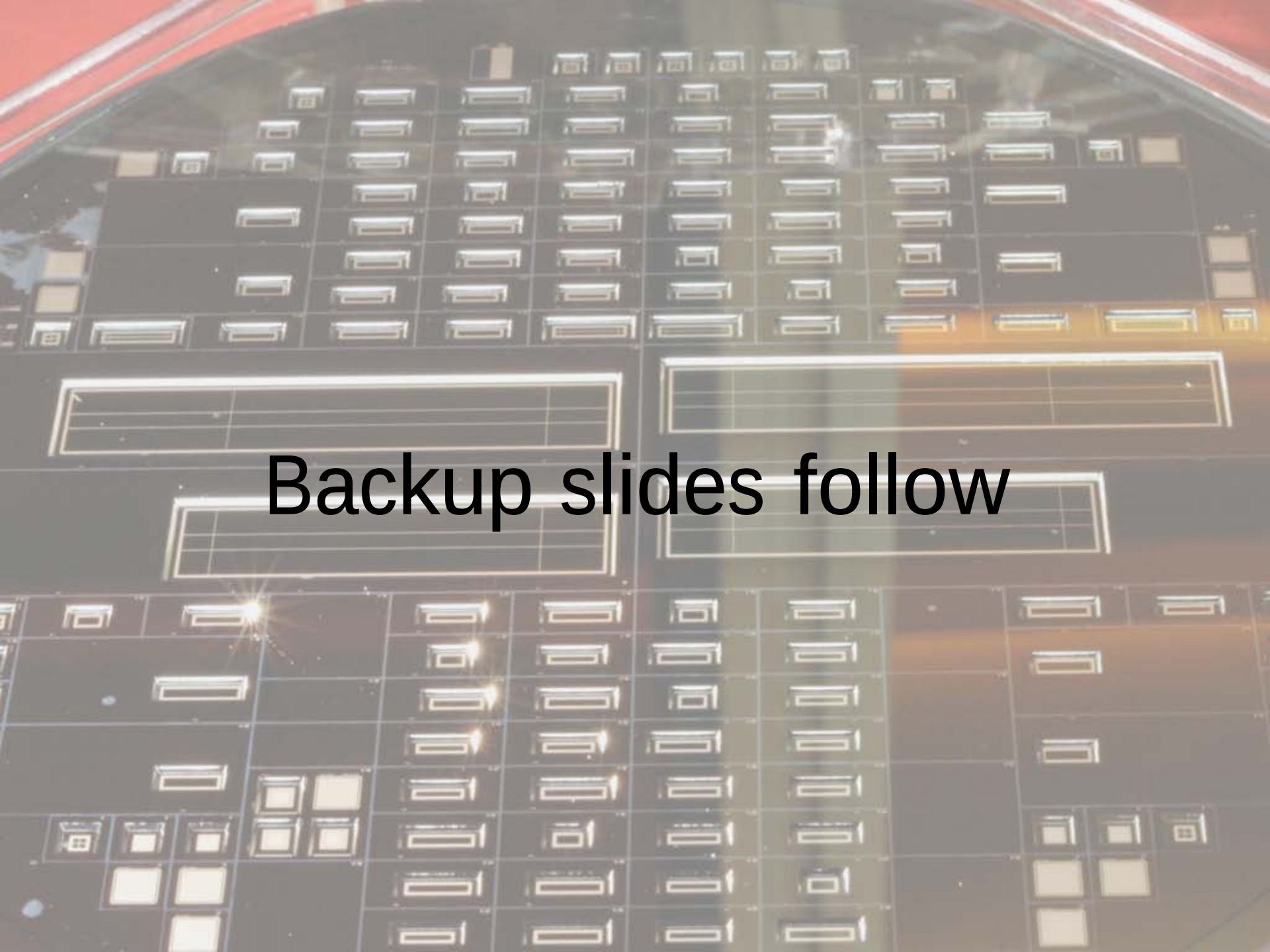


- 320 MHz DCD-B clock
- → **100 ns** signal processing time per row
- **S/N=17 for Sr90 "mip",** settings not yet optimal ..

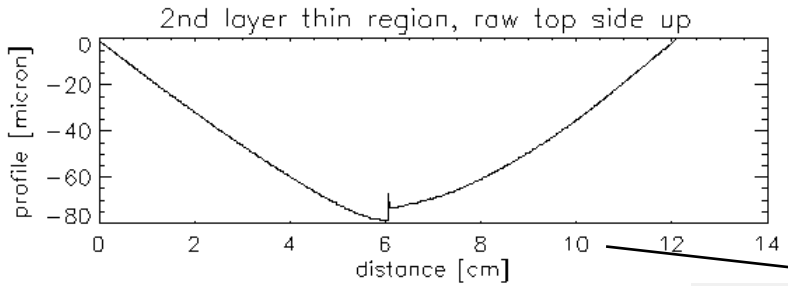
Summary

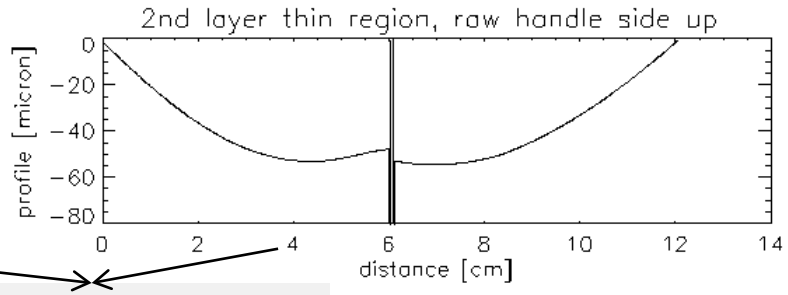
- The DEPFET technology, including thinning and the module concept, initially developed for application at the ILC found it's way into a high precision vertex detector at SuperKEKB.
- The mechanical concept and the thermal management is adapted to the Belle II geometry, but engineered designs, techniques, technologies can and will be transferred to the barrel geometry at future linear collider.
- A new read-out chip generation (DCD-B) has been designed and tested and shows the expected performance with the DEPFET. The read-out speed (line rate) is close to the requirements at a future linear collider.
- First test show that thin DEPFETs have the expected performance. More tests, in particular beam tests to measure the single point resolution of thin active pixel sensors will follow.



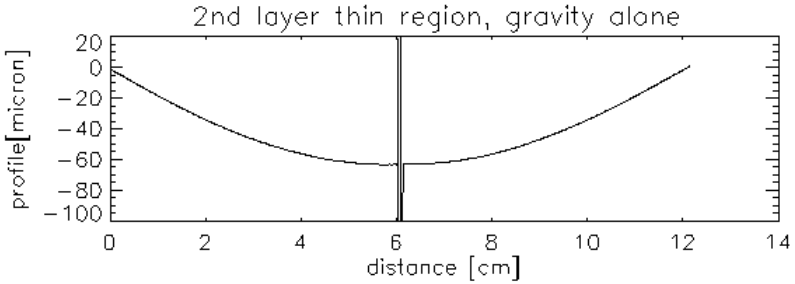

Backup slides follow

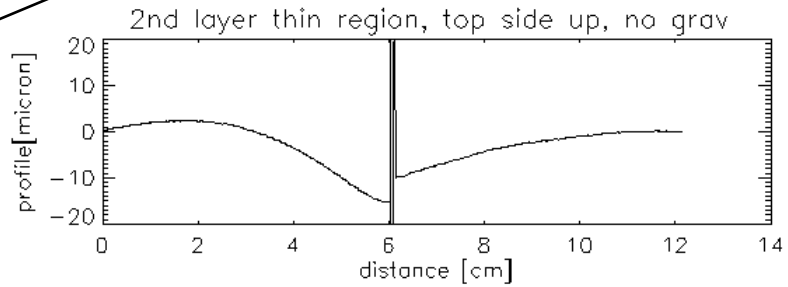
Micro joint between half-ladders

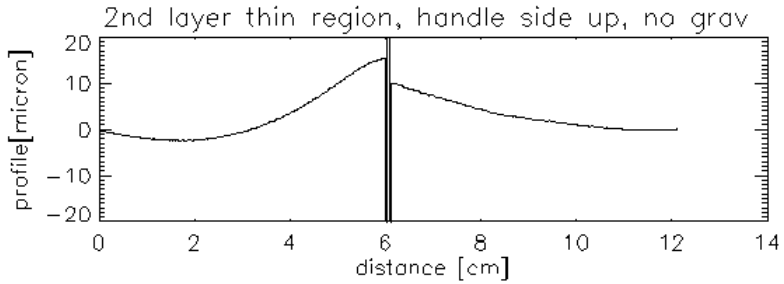




gravity effect = Δy/2

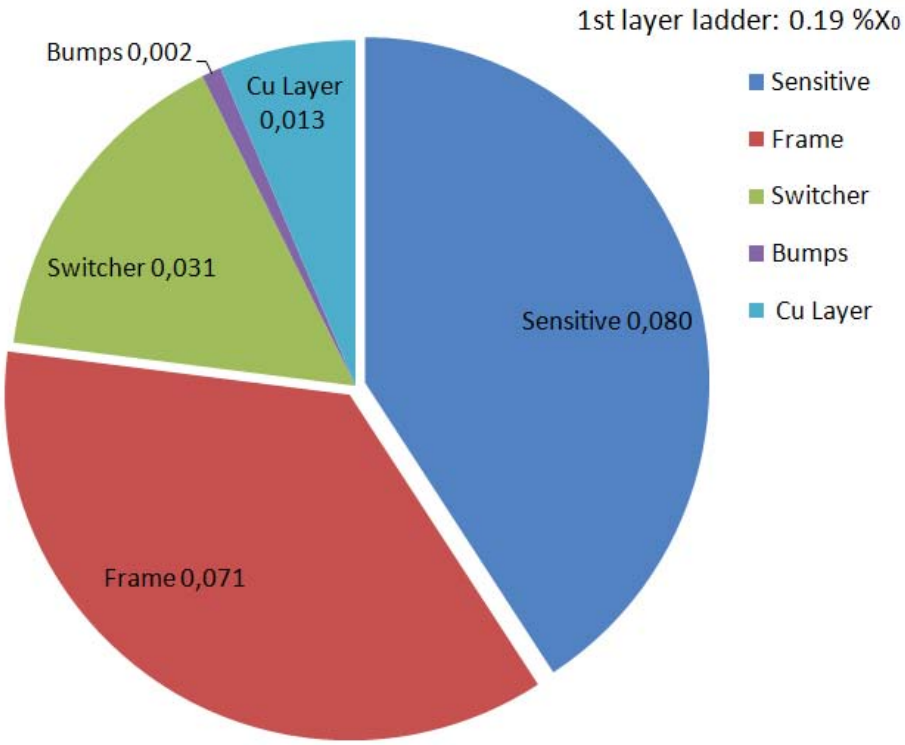






Total Material Budget within the Sensitive Volume (Belle II)

- sensitive area of the first layer ladder: 1.25x9.0 cm^2 (1.5x9.0 incl. frame), 75 µm thin
- support frame: 0.1+0.2 cm, 420 µm
- Switcher-Sensor Interconnect: Gold stud bumps, one bump/connection, Φ=48 µm
- Cu Layer t=3 µm, 50% coverage in acceptance
- Switcher dimensions: 0.15x0.36 cm^2
- Number of Switchers: 12 (32x2 channels per chip – gate and clear)
- Material reduction by frame perforation: 1/3



→ 0.19 %X_0 in total

Silicon contribution (0.15%) experimentally confirmed