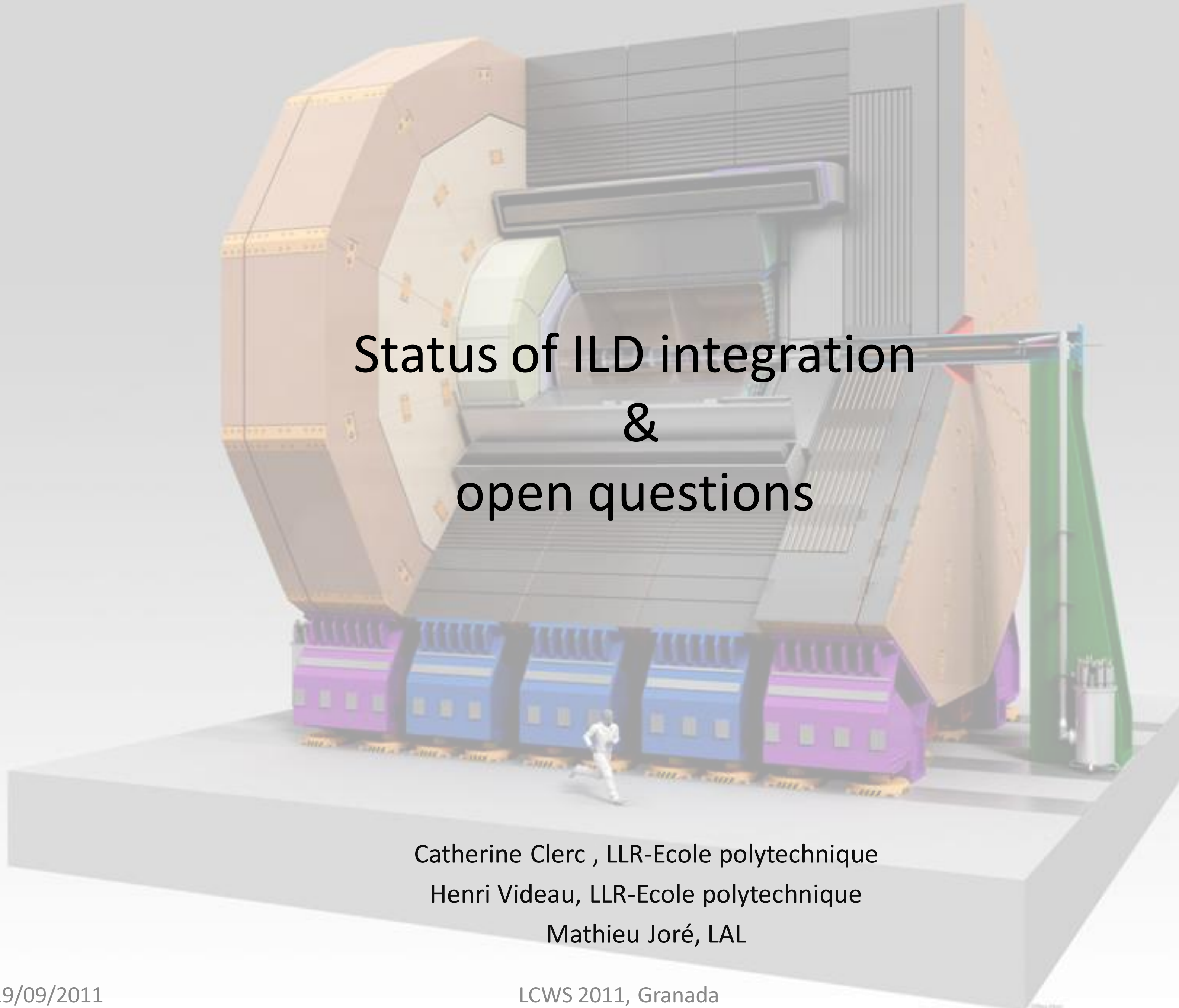

Status of ILD integration
&
open questions

Catherine Clerc , LLR-Ecole polytechnique

Henri Videau, LLR-Ecole polytechnique

Mathieu Joré, LAL

ILD and Power pulsing meeting in may 2011 *(G.Blanchot, R.Poeschl, M.Weber, A.Brogna)*

data collection

		weight	sensor m²	Ch	granularity	Main chip	chip cons.P.P	total P W Main chip	Duty Cycle	Power distribution	cooling	remark +	Cabling/services
Magnet	**Yoke**	13400 t											
	Coil	155t (cryostat)											
muons													
Hcal	**Ahcal**	1153 t	7300	8,1 MCh	3*3 cm²	SPIROC	25+15(DC SIPM Bias) µW/ch	320 W	1%		Liq. (Water?)		1Power/ 1 HDMI/1GL per layer (1536 full barrel) cooling?
	SDHcal	1188t	same ?	71 Mch		HARDROC	7,5µW/C	532 W	0,50%		Liq		voltage :HT f14+ 1 Data acq. F14 per module (40); Liq. 2 loops f14 + 2 loops f 4 per module (40) Gaz : 2 loops f14 + 2 loops f 4 per module (40)
Ecal	**Wsi**	130 t		100 MCh	0,5*0,5 cm²	SKIROC	25µW/C	2500 W	1%	Si sensorsHV=150V, 0.005 mA, continuously ROCsEach ROC needs: DVDD=3.3V, 11mA (ACQ) / 8mA (other op.)AVDD=3.3V, 77mA (ACQ) / 20mA (CONV) / 0.01mA (other op.) DIF:DVDD=3.3V, 300mA, continuously	Water, leakless		
	SciW			11 Mch	0,5*4,5 cm²	SPIROC	25+7 µW/ch	352 W					
TPC	**GEM**	4 t		4 Mch	1*4 mm²	S-ALTRO		1,3 KW to 2,4 KW per side	1,50%	70 KV qq mA central anode	CO2 ?		
	µmegas ?				55*55 µm²	Timepix3 ?	20 µW/pixel) @1.2 V					Expected ON → 350 mW/cm2; OFF → <5 mW/cm2	
	strip												
ETD	**strip**	186 kg	26 m²	1,3 Mch									
SET													
VTX	**CMOS**			10^8ch	16*16µm²			12 W non pulsed+ 688 W pulsed = 20-30 W	1 to 2 %	Cables 5A@1.8 V: up to 390 A	airflow	40 W in conductors	16 AGW 10 cables per side
	FCCPD			10^{10}Ch	6*50(?)µm²		10 mW/ch	inside cryo: 100 W; + outside (junction box) 200 W per side			•CO2 cooling		16 lines S= 8 mm² to J.B / 20 AGW14 from JB to outside
SIT													
FTD	**pixels**												
	strips			2,4 MCh	pitch 50µ		12A(1,25V)+ 6A(2,5V) in pulse	35 W per side	0,50%	Two operations voltage 2.5/1.25 V 650 A per side	airflow		96 AGW15 per FTD + 32 OF
LumiCal	**W/Si**	250 kg		200000			15mW/chan if No pulse	28W/8,5A with pulsing	1%	2.8kW/850A, Commercial voltage regulator (ADP3336)			
Bcal	**W/Si**	200 kg				Kpix							
	W/Diamond												
LHCal	**W/?**	2,6 t											
Ecal ring	**W/Si**	600 kg											

ILD and Power pulsing meeting in may 2011

data collection

Under construction

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ILD and Power pulsing meeting in may 2011

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Lumi															
Bcal															
LHCal	W/?	2,6 t													
Ecal ring	W/Si	600 kg													

Conclusions and requests of the PP group :

What is Power pulsing ?

How to deal with :

- DCDC convertors
- Storage capacitors (+ low drop out)
- +…

To be added in this table :

- Nber+length + cross section of input/output cables
- Regulation & power delivery system
- Peak consumption and idle consumption
- Radiation levels of the front end

Yoke and Magnet

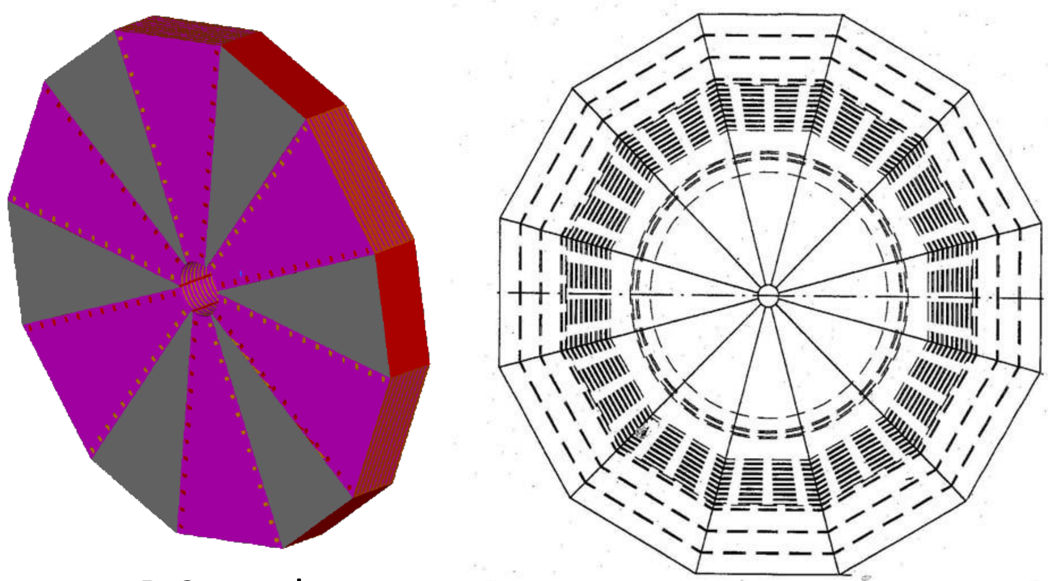
1. **<u>Yoke and stray field:</u>**

Decision made on no compensating coil :

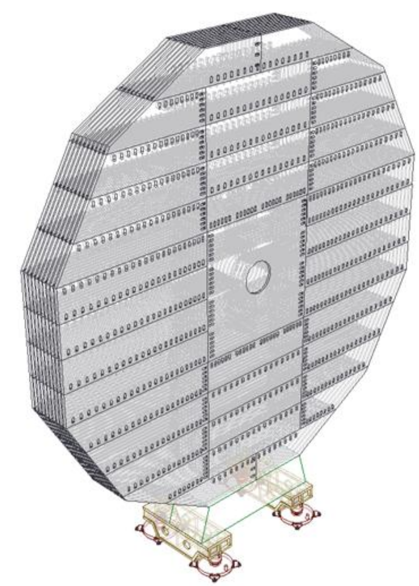
- reduction of the store energy (2.7GJ> ≈ ?GJ)
- Might change the stray field = possible reduction of the return yoke
  - ✓ reduction of the beam height, length of ILD (i.e. opening access)
  - ✓ Reduction of the cost
- Stress forces on the FSP and 1^{St} layers of the Hcal endcap (distortion)

Simulation (magnetic field and Mechanical)needed

2. **<u>Return yoke design</u>**

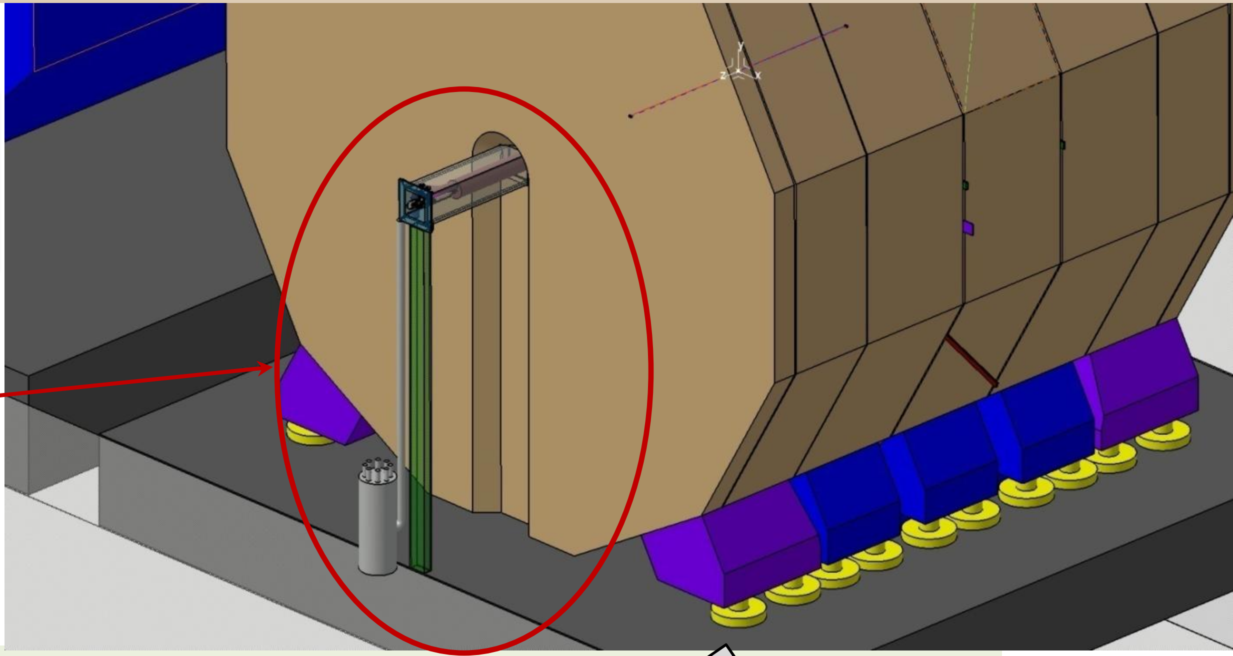


R.Stromhagen



Hubert GERWIG &Nicolas SIEGRIST

Split or no split
cf presentation M.Jore in Orsay,
June 2011



Possible by
Reducing the pillar +
trench in Return Yoke

Mathieu comments in June :

"Non split end cap seems feasible with 915mm for access on beam "

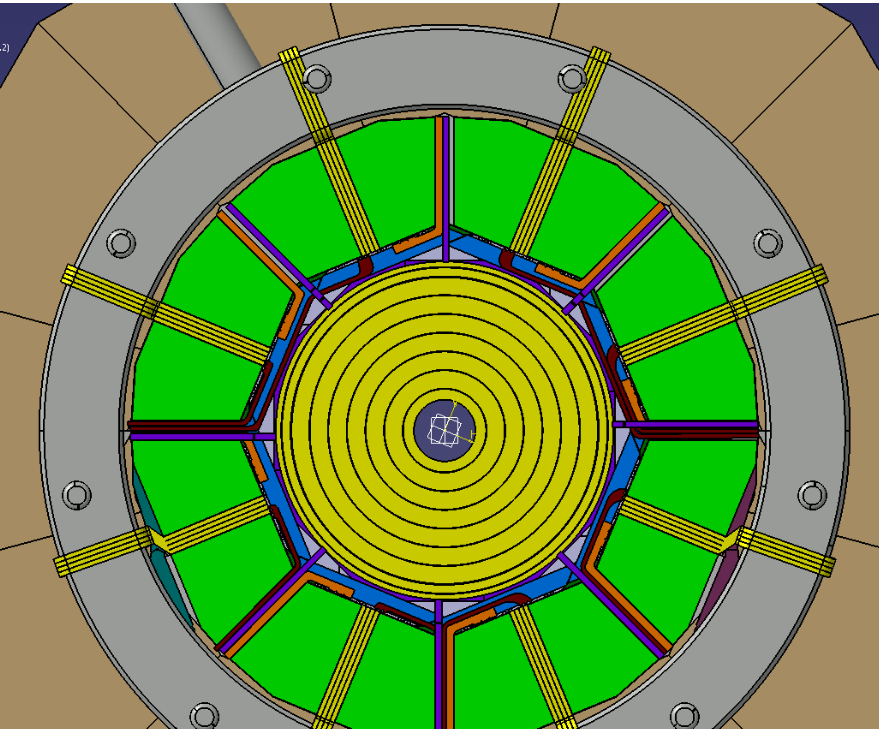
Acted..

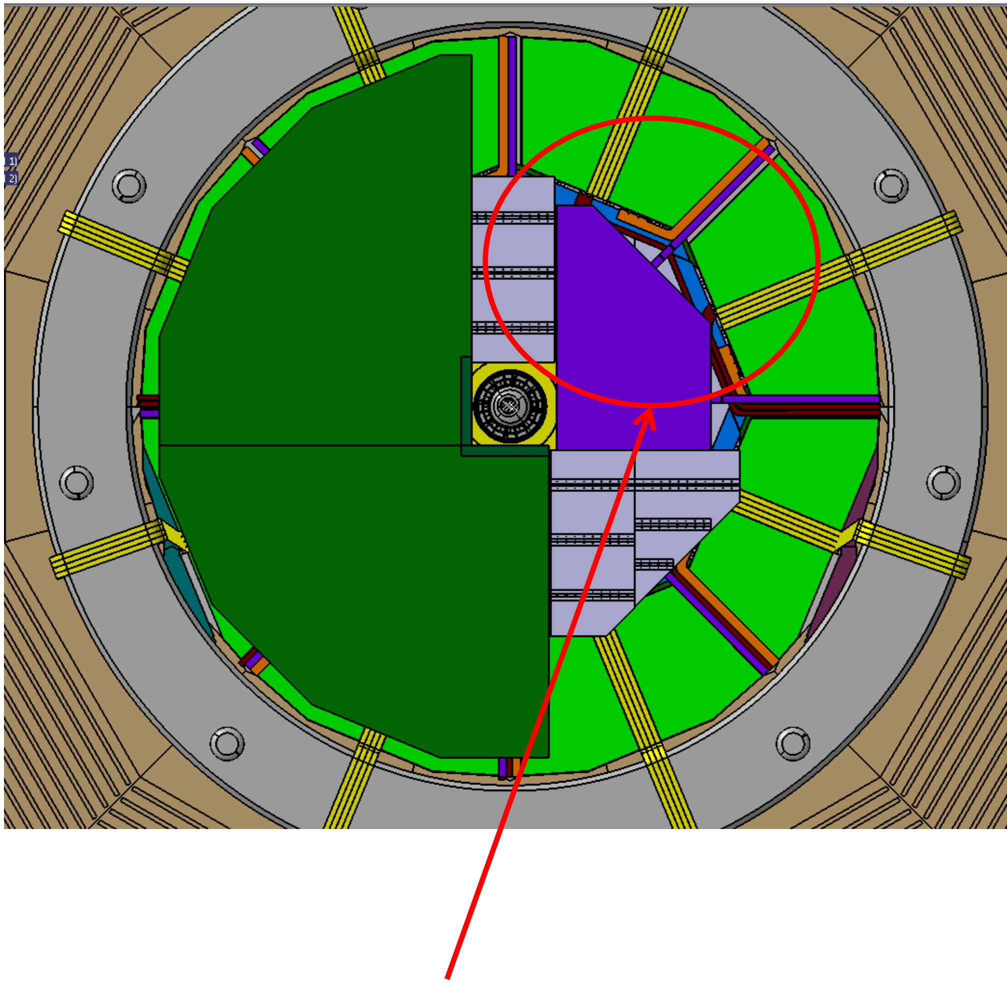
- To be studied :
  - **Detail design of the pillar and the trench**
  - **Detail opening scenario**
  - **Impact on the fringe fields**
  - **Pacman compatible with SiD and our pillar**
  - **Tooling**

- For discussion …. **Do we really need the last 560mm yoke ring?**

Still to be studied..

Tilt of the Ahcal (22.5 °)
(because of self load deformation)



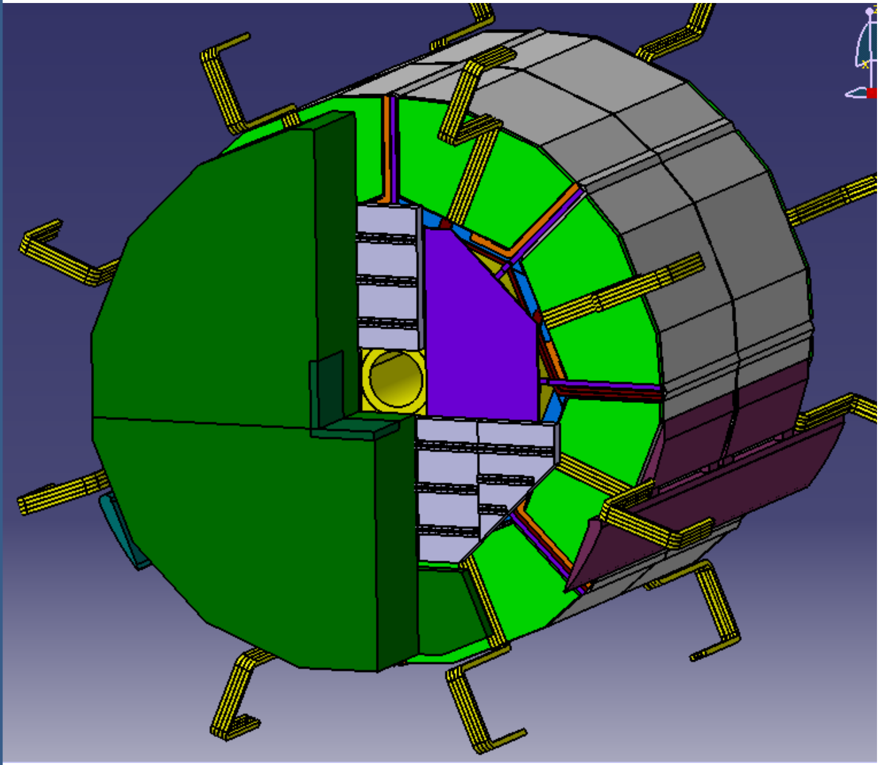


- Problem with actual shape and construction of Ecal endcaps (+ ETD?)
- No tilt in simulation.

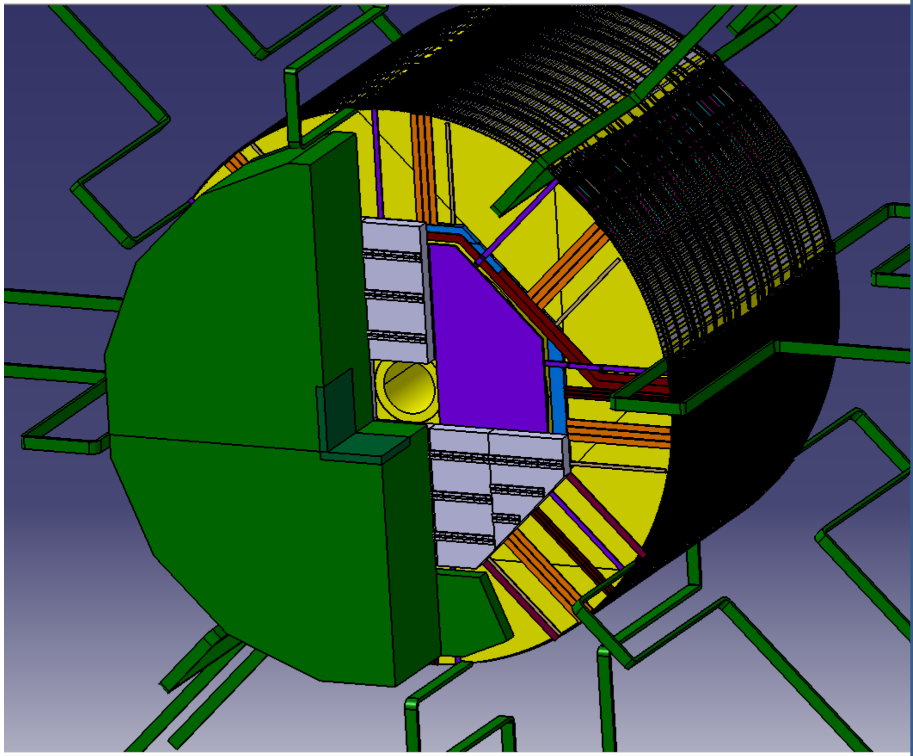
Updates of the services paths for both **Ahcal** (with tilt of barrel)

SDHcal :

- ✓Placeholders in the CAD model
- ✓Data of X0 calculated and to be implemented soon in simulation

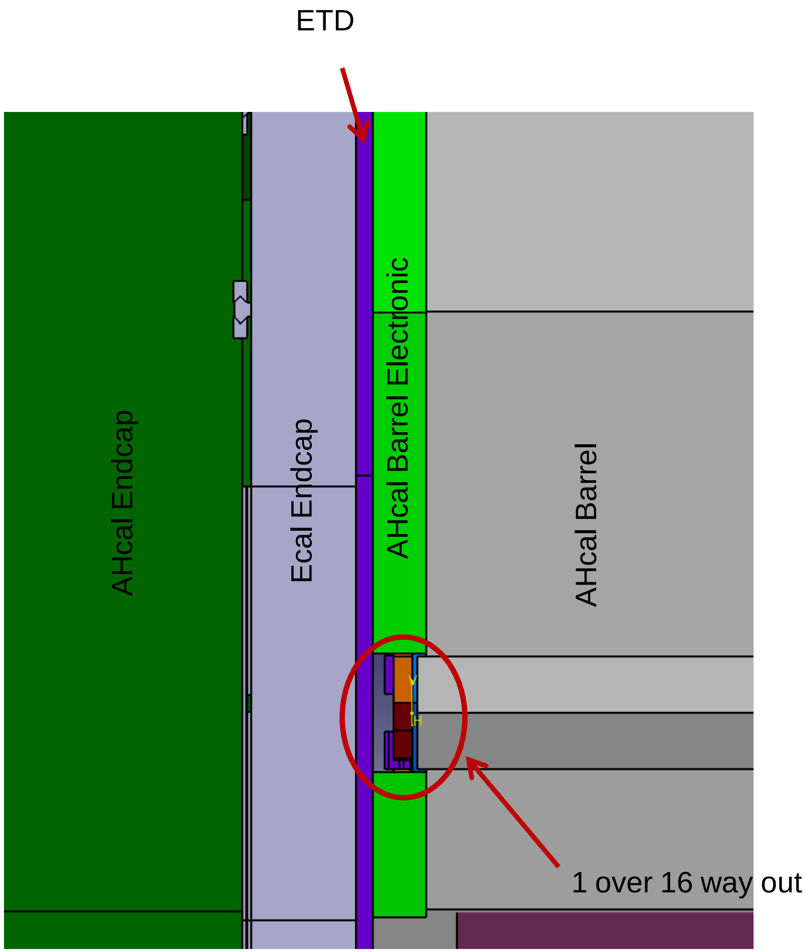


AHcal

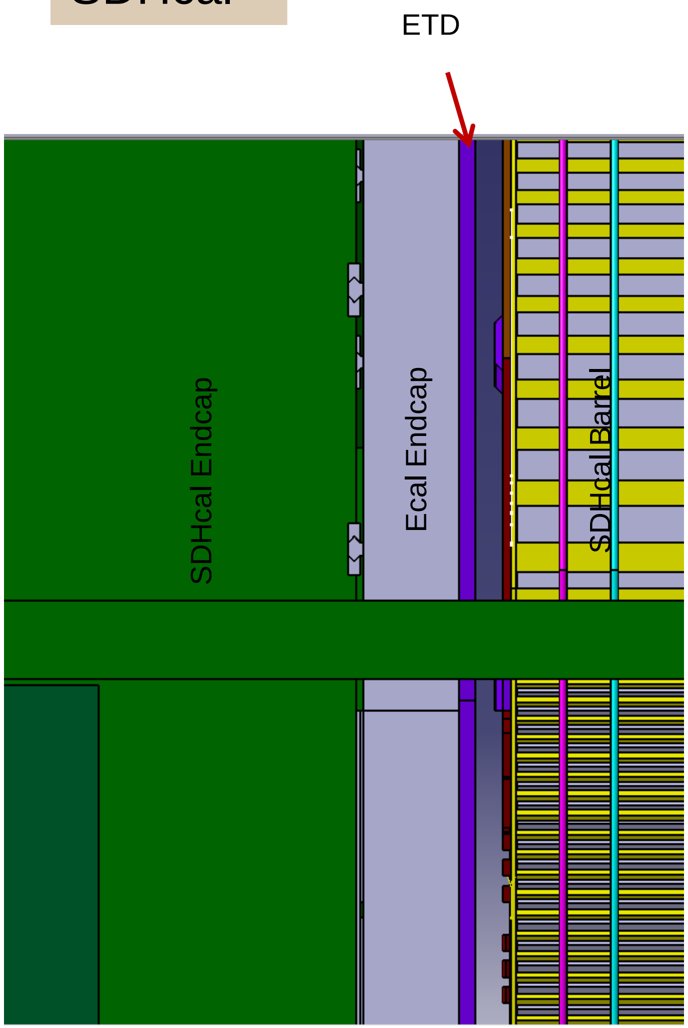


SDHcal

AHcal



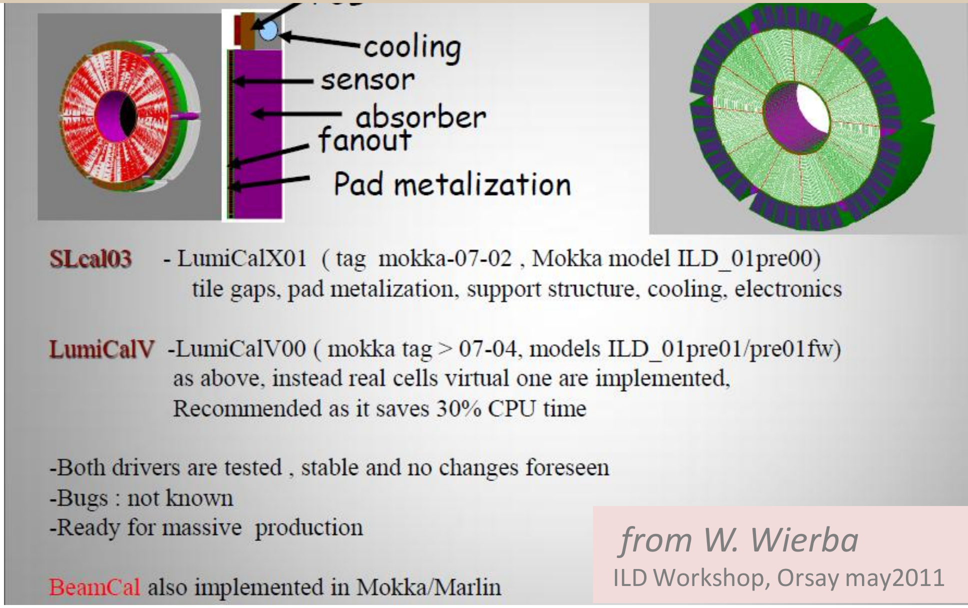
SDHcal



SDHcal : possible to reduce the gap by few tens of mm

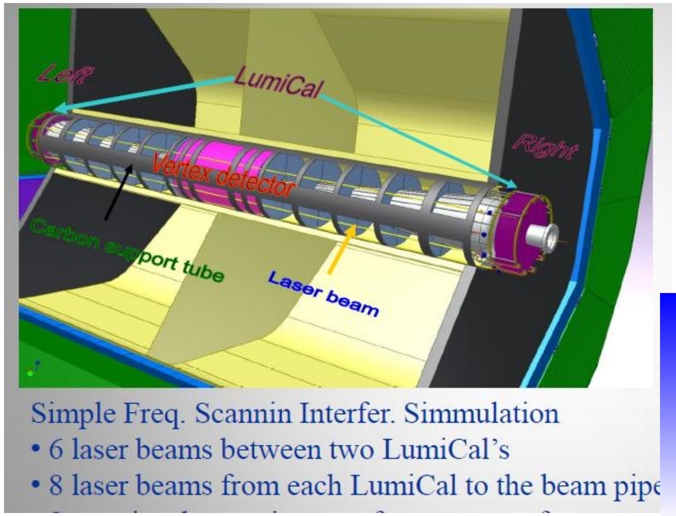
- Lumical & Beamcal in simulation model
- Mechanical design well advanced, certainly need to be updated in CAD model and dimensions checked
- Power pulsing & power needs are known

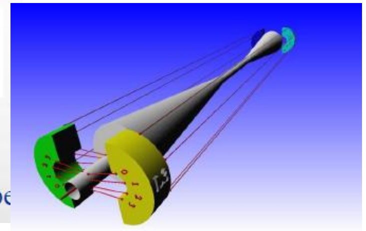
But :



from W. Wierba
ILD Workshop, Orsay may2011

Alignment system : <u>6 laser beams along the beam pipe </u>(through FTD)





Certainly not the only one : impact?

See Szymon Kulis presentation, LCWS11

SIT, ETD & SET

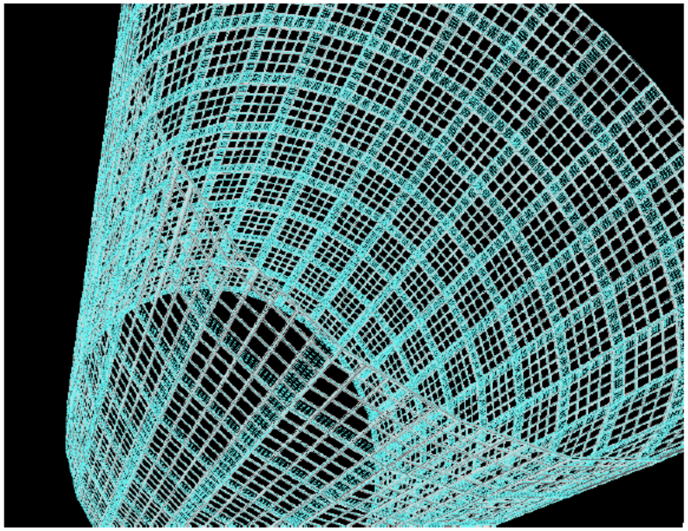
SIT,ETD,SET : a lot has been done for ***simulation model***:

Silicon tracking status.
SIT, SET, ETD

ILD DETECTOR OPTIMIZATION August 24th 2011

Alexandre Charpy - professional@charpy.net
Aurore Savoy-Navarro - aurore@apc.univ-paris7.fr
Konstantin Androsov - konstantin.androsov@gmail.com

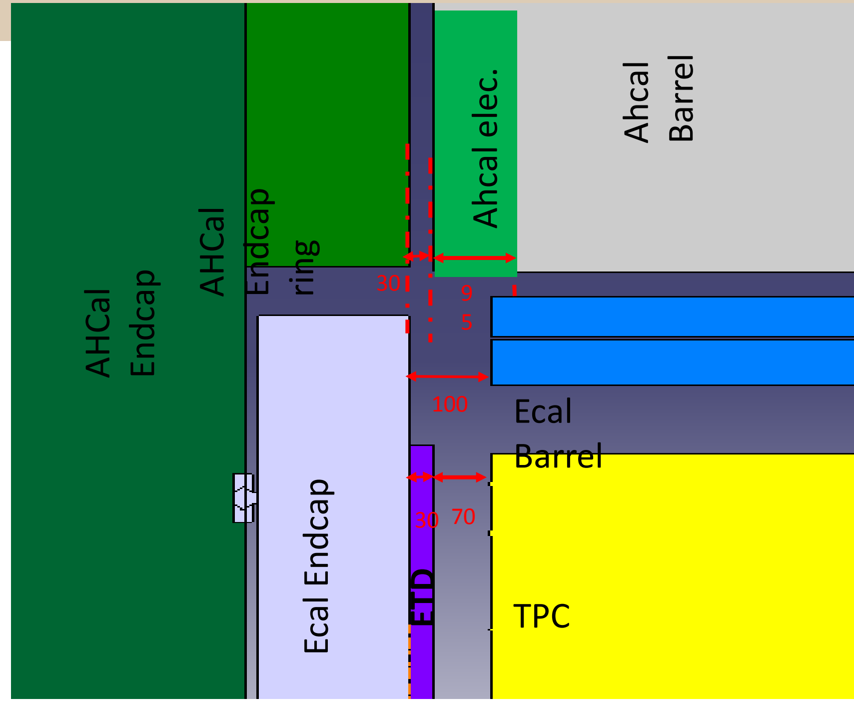
SIT, SET & ETD support simulation status:

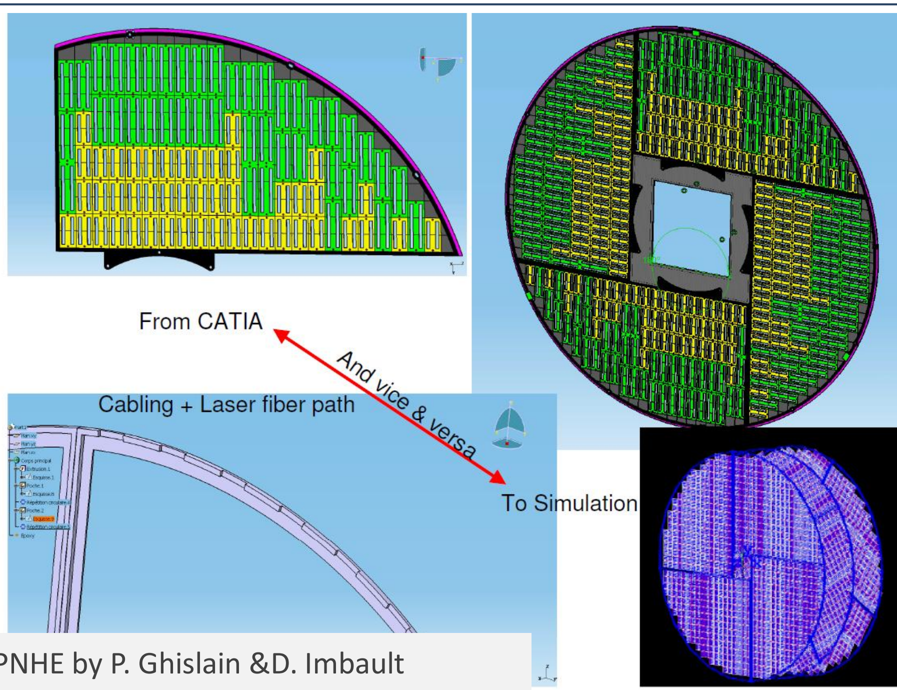


- *SIT & SET simplified support design* based on two components: silicon and support with variable thickness (%X0): ***almost done***.
- *SIT & SET detailed support design*: ***will be ready for September***
- *ETD detailed support design* ***is available***

BUT about ***integration*** ???
Latest news :
ILD SOFTWARE and INTEGRATION WORKSHOP, July 6-8, 2010, DESY-Hamburg

- **Its mounting system (very preliminary on Rout) and services, might limited its thickness , because: in the paths of the services.**
- **Segmentation of mechanical submodules to be studied**





LPNHE by P. Ghislain &D. Imbault
in collaboration with
LPSC (D. Grondin), LAL (M. Jore),
LLR (P. Anduze). ***July 6-8, 2010,***

<u>Nbre of layers :</u>

- **Thickness: actually still 30 mm in CAD model (i.e.) 2 layers**
- **but in simulation 3 layers XUV**
- **Latest news of mechanical studies (July 2010) : still considering 3 layers i.e. 45 mm total thickness,**

Are 2 layers XY enough?

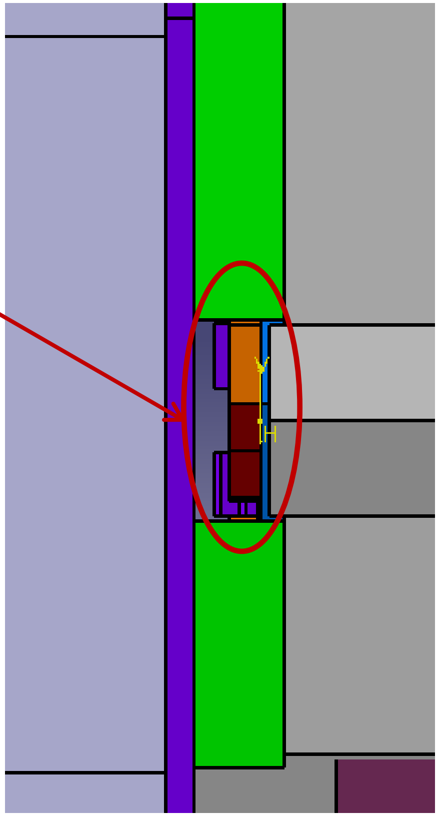
Definition of the SET :

Still not in the *CAD model* .

+ its services have to share the same ways-out than ETD/Ecal/Ecal endcaps/TPC/ TPC support…. At least in case of AHCAL

Critical space between TPC and Calo actually 35 mm available, is it enough ?

In *simulation* 2 layers with total thickness 30mm



SET

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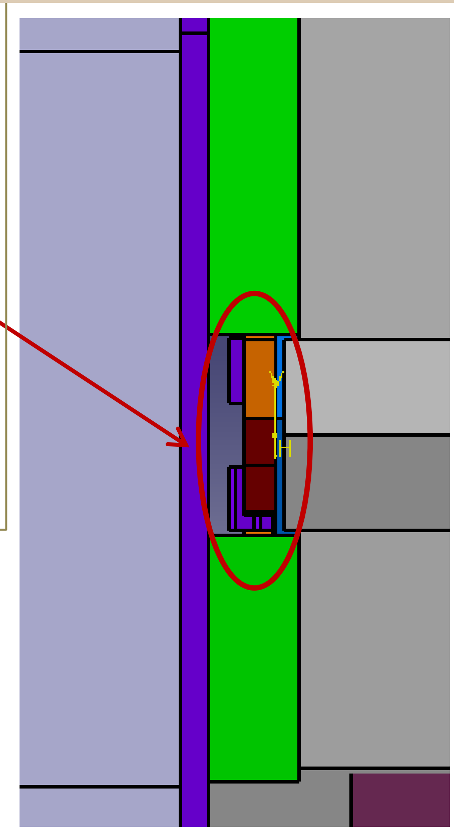
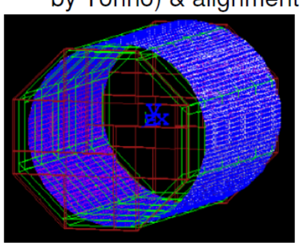
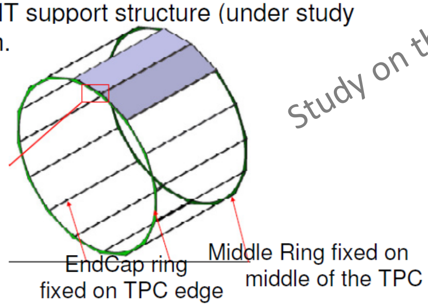


Questions concerning the SET

- Space needed between TPC and em calorimeter: to be studied in details. Presently needed: ~ 2.5 cm.
- Alignment vs SIT & TPC (pixel+laser based system)
- Fixation of SET:
  - Need a fixation point in the middle of the TPC and
  - Fixation at theTPC end plate edge ? or
  - Bicycle wheel on both sides of the TPC, independent of the TPC, that could also serve for the SIT support structure (under study by Torino) & alignment system.



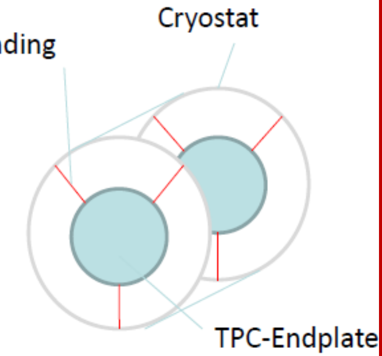


Study on the SET performed by Paolo MEREU
July 6-8, 2010,

TPC support

ILD support structure preferred design

- Binding structure, 120 degree each using a cobweb“ design
- Fixing points on the Cryostat and preferrably on the Endplate
- Adjustable bracket at the cryostat
- Material: CFK, GFK, small parts made out of metal or non magnetical material



Sketch of the cobweb

Required items

- Min free space required is about 10 x 100 mm
- Gap to neighbouring Detectors and other Components about 10 mm (this may be very optimistic)
- Straight line between Endplate and cryostat is necessary

V. Prahl

Is it necessary to go up to cryostat ?

with SDHcal : fixation on Hcal endplate (20 mm thick)

with AHCAL

tension rods sharing the spaces with services in 2/3 ways out

Fixed on structural skin of the “ way out “ 2 cm thick SS?

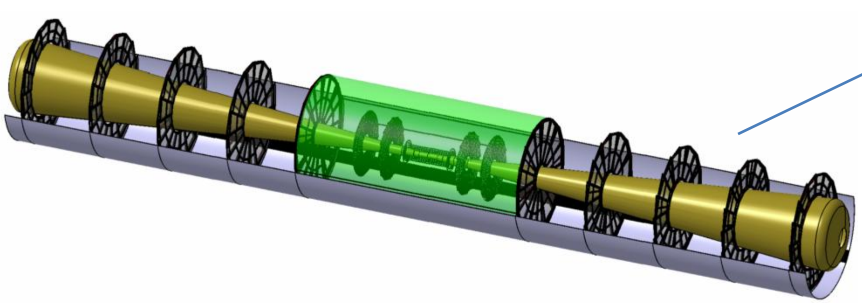
- Neither in CAD model, nor in Simulation
- No decision made on the hanging system only conceptual
- FEA calculations?
- Placeholder ?

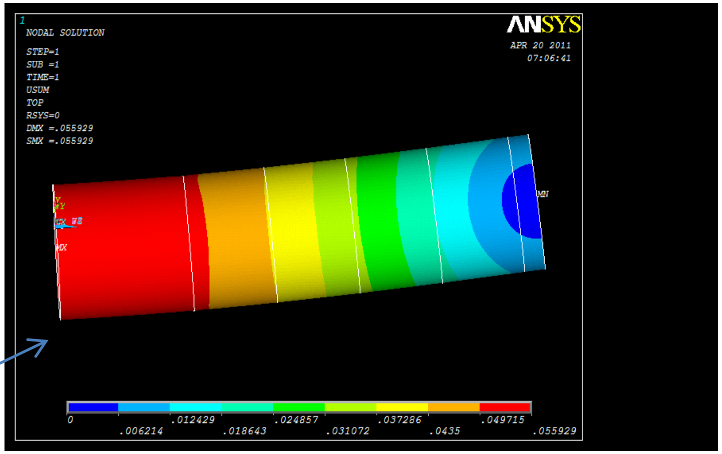
•**<u>Support structure</u>** ; 1 mm of carbon ?

- ✓ still no conclusion
- ✓ not in simulation

But possible structure studied by D.Moya

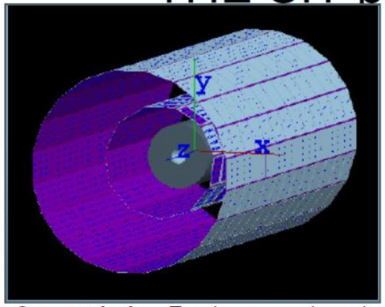
- Material used for the composite: best results M55J
- Cylinder eight Layers 1,04 mm thickness
- Rings four Layers 0,52 mm thickness
- All the layout symmetric with respect to the central line
- A mechanical simulation of the inner most part support cylinder has been done with different layout. 0º/90º/45º/-45º seems to be the best for the cylinder.





- **SIT :** present design for simulation well advanced but structure/support/services ?

THE SIT present design



From simulation (A. Charpy+K. Androsov)

Minimum Radius (mm)	Maximum Radius (mm)	Z Length (mm)
172.3	179.6	708.4
319.5	323.5	1315.6

Number of modules along Z	Number of modules along φ
7	11
13	20

Current design: Two layers, each made of 2 SSD and stereo (6 degrees)
SSD strips sensors (10.12x10.12cm²), 200µm thick, 50 µm R.O.pitch, active edge.
SiTR based FE readout on chip
Support structure following the SET model, thinner and space frame

Questions:

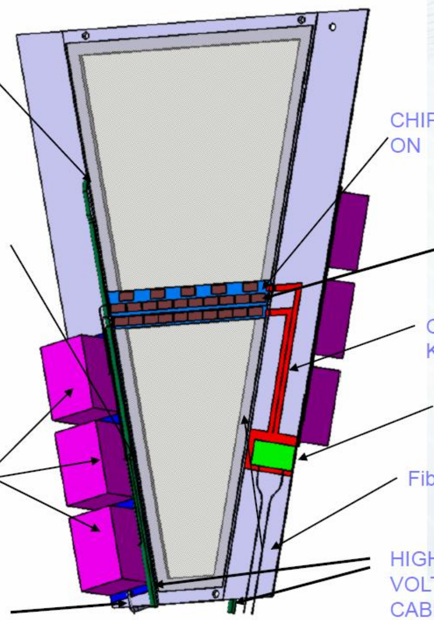
- Nb of layers: More than 2 layers (cf study by Korean team with 3 or 4 layers)
- time stamping (currently Si tracker -> bunch crossing stamping if more needed => additional layer (SIT?); dedicated FEE designed for CLIC
- including SIT into the vertex detector cryostat if any (see Snowmass 05 !)

- **FTD1/FTD2** : same questions + do they have to be in the cryostat or at least a field cage

- **Path of the cables** :

  first assumption, along the forward detectors, seems no more valid due to the congestion around the Ecal ring and the needed space for connections box => inner services in the gap barrel-endcap with first patch-panel close to /on the TPC endcap.

4.1Powering schemes: DC-DC based Power System



- Detailed study is on progress.
  - Location
  - Material
  - Transients

21 de 22

Linear Collider Power Distribution and Pulsing workshop
Paris, 9th May 2011

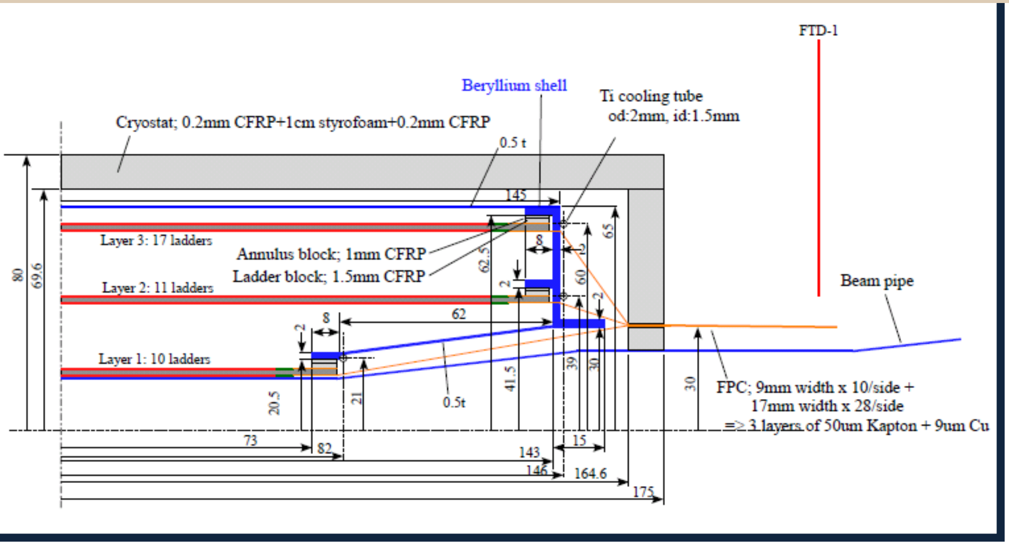
ita

- To each petal will arrive:
  - 2 *12 Volts cables AWG 15 (chips alimentation) to the DC-DC electronic plate
  - 4 AWG 15 high voltage cable (sensors polarization)
  - 2 fibers of 300 um diameter (control of the chips and signal of the sensors)

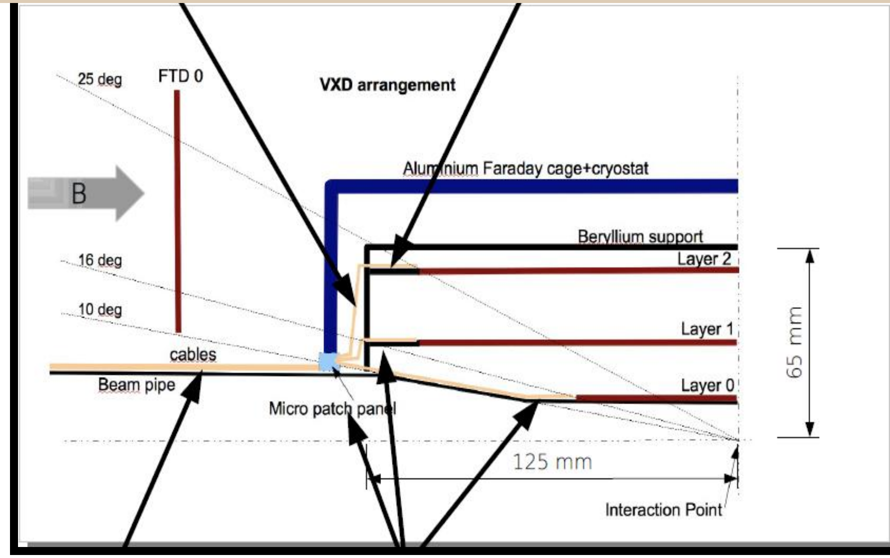
16 petals per FTD
6 AWG 15 per petals + 2 OF

<u>So per FTD :</u>

- ✓ *96 AWG 15* *(s=1.65mm² Cu)*
- ✓ *+ 32 Optical fibres*
- ✓ *158 mm² of Cu*
- ✓ *Placeholders 39x0.9 cm²*



FCPPD (from Y.Sugimoto)

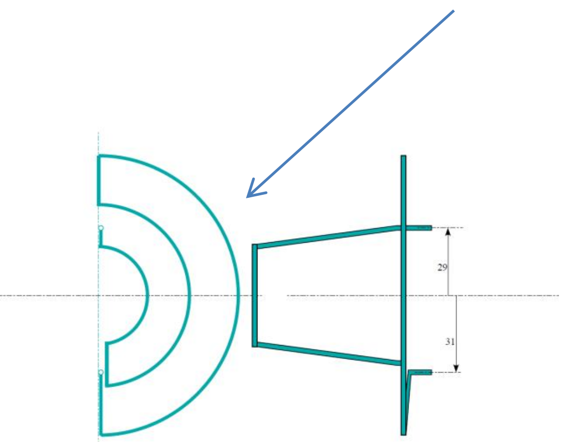


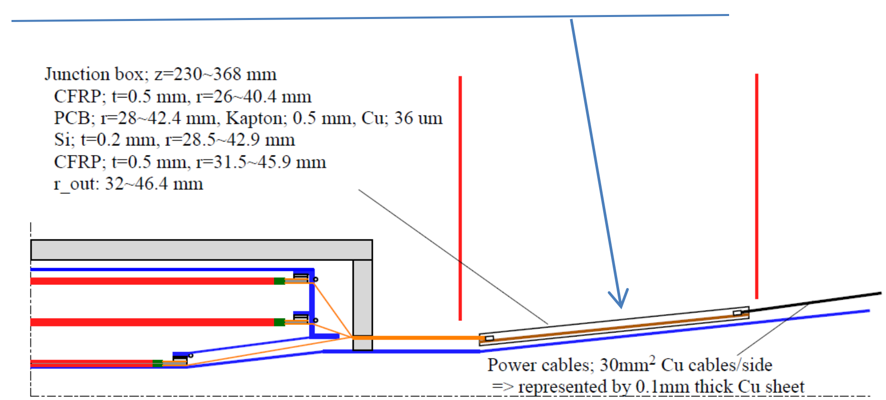
CMOS(from J.Baudot)

The 2 designs are considered to be compatible for simulation in the inner part of the cryostat,
But as <u>**FPCCD**</u> not pulse :

CO2 cooling foreseen , Titanium tube 2mm o.d. and 1.5mm i.d

+ **junction box** between the 2 first FTD





Inner detectors (5) : vertex CMOS cables *(from J.Baudot)*

CMOS Cable type (outside the cryostat)

Nominal voltage power transport

✗ At 1.8 V : current to transport in activity is ~400 A (otherwise ≤ 10 A)
✗ Requiring a voltage drop < 0.1 V → section of conductor ~ **0.8 cm2** (copper)
✗ Power dissipated in conductors 40 W (with duty cycle 1/100 to 1/50)
➔ Small compared to 700 W

Subdivided in 15 cables SCu=5.3 mm² (AWG10?)

Technical solutions still to investigate:
- power supplies
-cables with high rise time if no DC-DC converters

Control signals

✗ ~**15 lines** with ~15 Amps total per side
✗ To limit voltage drop to 100 mV with copper cables
➔ Cable copper section ~ 5mm2 in total ?
➔ equivalent to a weight load ~0.5 g/cm per side ??????

Cu 5 mm² : AWG10 type
Or 15 AWG21

Data

✗ optic fiber featuring 5 Gbits/s:
➔ OPTION with instantaneous (during 1 ms) readout: data rate ~ 150 Gbits/s → 15 fbers per side
➔ OPTION with delayed readout (during 200 ms): data rate ~ 750 Mbits/s → 1 fber per side

Eq to **85 mm²** of Cu
Eq to **1.9 kg** on each side of the beam pipe.

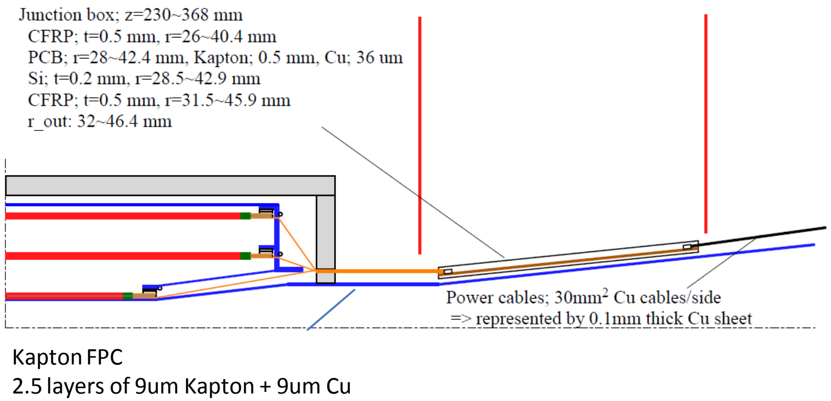
Placeholder size ≈ 16x1.2 cm²

FPCCD Cable type (outside the cryostat)

Electronics (3)

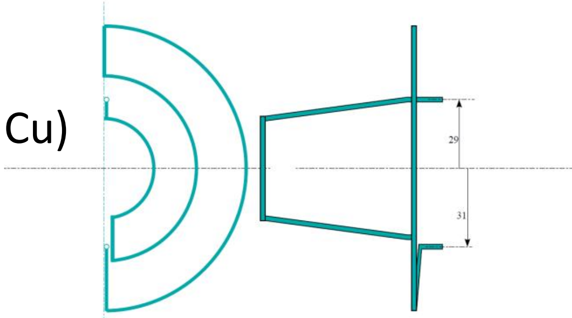
- cryo to JB :
  16 lines/side (4 kinds of voltage x2 (return ground) x2 (two half shells)) of 8mm2 cables are enough *i.e. 128 mm² of Cu between cryostat and Junction box (?)*
- Material budget of optical fibers is not estimated yet

•From JB to outside : 20 AWG14 (diameter=1.628mm, 2 mm²) cables/side equally distributed along the beam pipe. i.e. 40 mm² of cu , Dout(2wires)= 9 mm



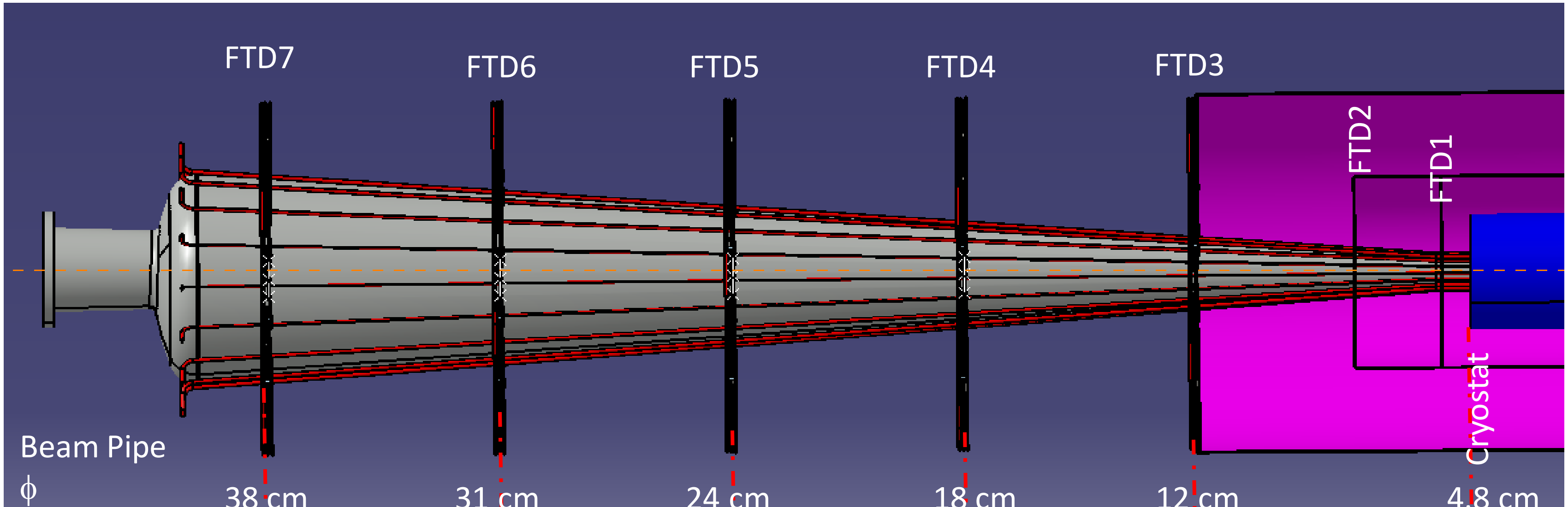
Cooling :
FPCCD VTX is cooled by 2-phase CO2 cooling system : 4 outlet cooling pipes
– **Outlet line (J.B. – outside IST): 4mm/3mm (or 2mm/1.5mm**)

(5,5 x4 mm² of Cu)



Total from Junction box to outside inner part : 62 mm² Cu
Placeholder (after JB : 9x1 cm²)

Inner detectors (6) : X0 along the beam pipe



BP circumf 119 cm 97 cm 75 cm 56 cm 38 cm 15 cm

5 FTD + VXD	4 FTD + VXD	3 FTD + VXD	2FTD + VXD	1FTD + VXD	VTX :
875 mm²	717 mm²	559 mm²	401 mm²	243 mm²	CMOS 85 mm² or FPCCD : 65mm²
Cu eq to 0,73mm	Cu eq to 0,74 mm	Cu eq to 0,74 mm	Cu eq to 0,71mm	Cu eq to 0,64mm Cu	CMOS:4% X0
5.1% X0	5.2% X0	5.2% X0	5.% X0	4,5% X0	FPCCD:2.9% X0

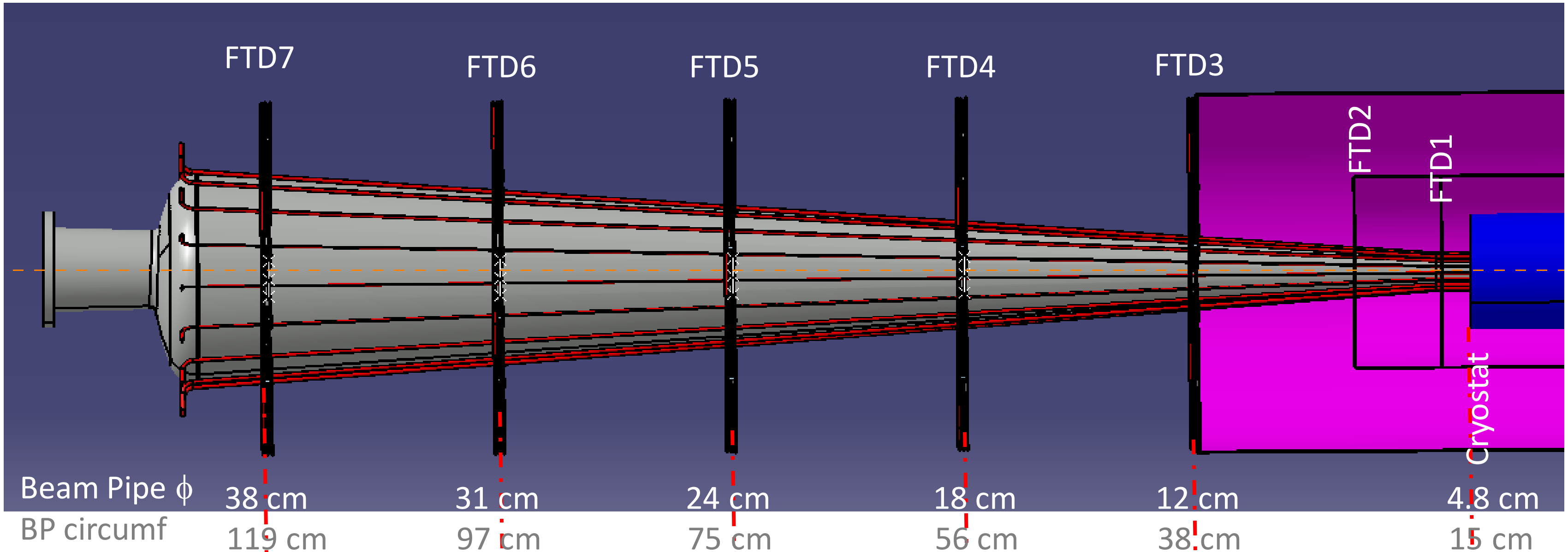
So, with actual data : about 5% of X0 all along the beam pipe.

That means also

- *about 9 kg of material on each side*
- *a minimum gap between FTD supports and beam pipe of 2 cm for path of all the cables….*

And SIT/ FTD1&2 services not included…

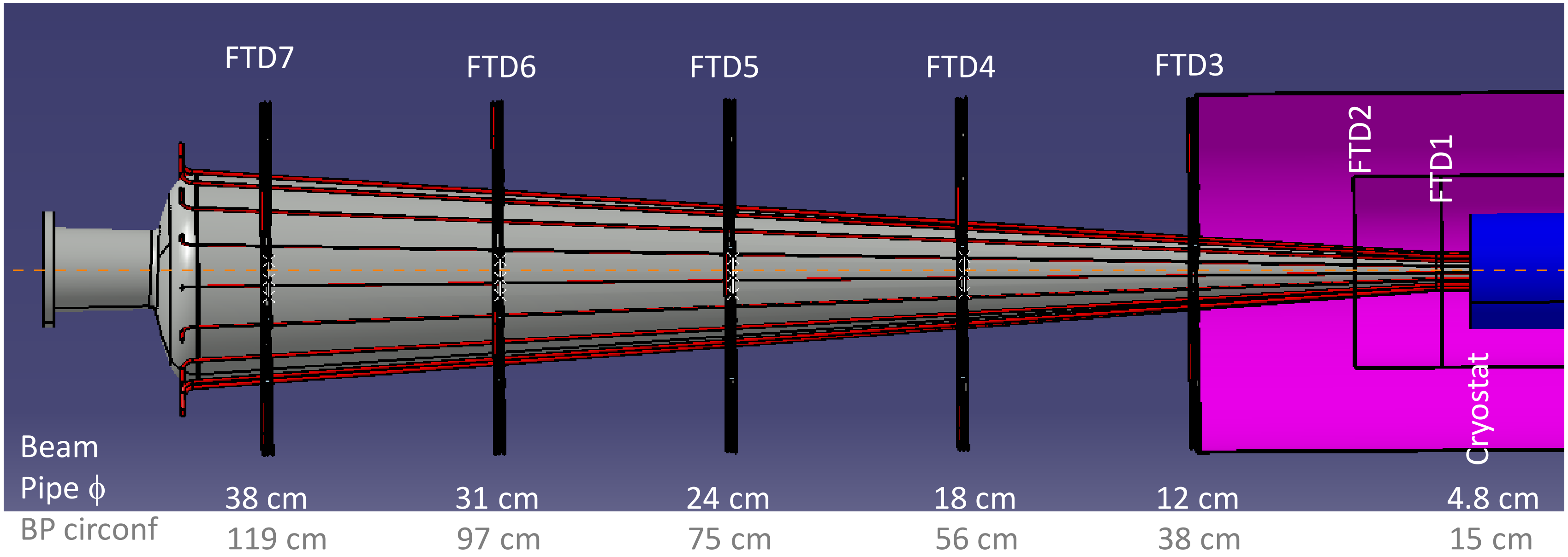
Inner detectors (6) : X0 along the beam pipe



5 FTD + VXD	4 FTD + VXD	3 FTD + VXD	2FTD + VXD	1FTD + VXD	VTX : CMOS 85 mm² or FPCCD : 65mm²
875 mm² Cu eq to 0,73mm 5.1% X0	717 mm² Cu eq to 0,74 mm 5.2% X0	559 mm² Cu eq to 0,74 mm 5.2% X0	401 mm² Cu eq to 0,71mm 5.% X0	243 mm² Cu eq to 0,64mm Cu 4,5% X0	CMOS:4% X0 FPCCD:2.9% X0

***BUT :** in discussion with FTD group (Santander) , in order to optimise the volume of cables : possible gain of factor 2 (serialisation & optimisation of section)*

Inner detectors (6) : X0 along the beam pipe



BUT (again):
SIT = 6,9 m² versus FTD (µstrips)= 4,8 m²
FTD 1&2 =0,67 m² per side versus VTX = 0,17 m² per side

We need to gain more than factor 2 !

Conductor (Cu >>> Al ?)
+
Optimisation of the power distribution
Study of the heating of the beam pipe

Summary :

A lot of information= a lot has been done , but still a lot to be done

Inner part : obviously where integration data are crucial and needed for DBD

Huge number of cables = size and position of patch panels

Begin to think " globally " in some case?

- **Alignment systems**
- **Cooling**
- **Patch panel**
- **Power distribution**
- **…**