Status of the AHCAL engineering prototype

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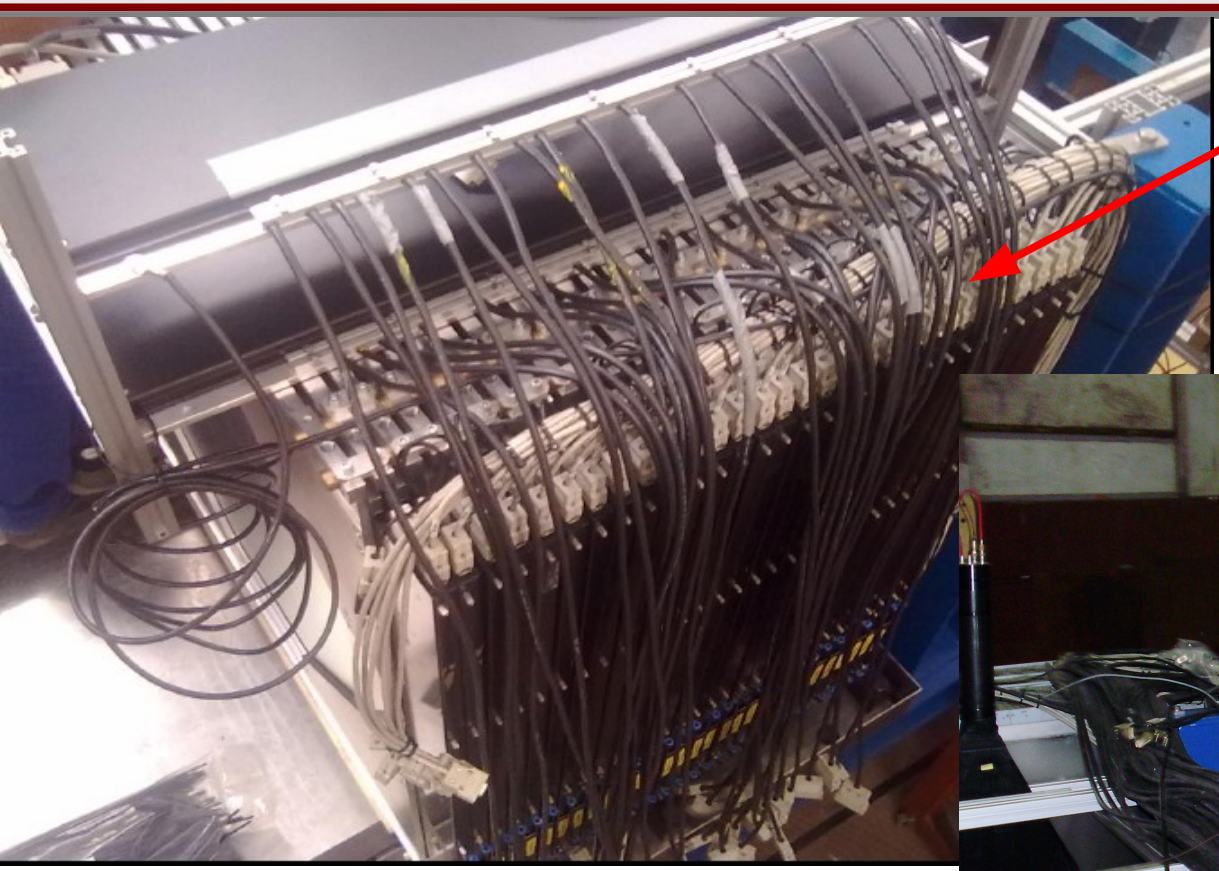
LCWS11

Granada, September 28th, 2011

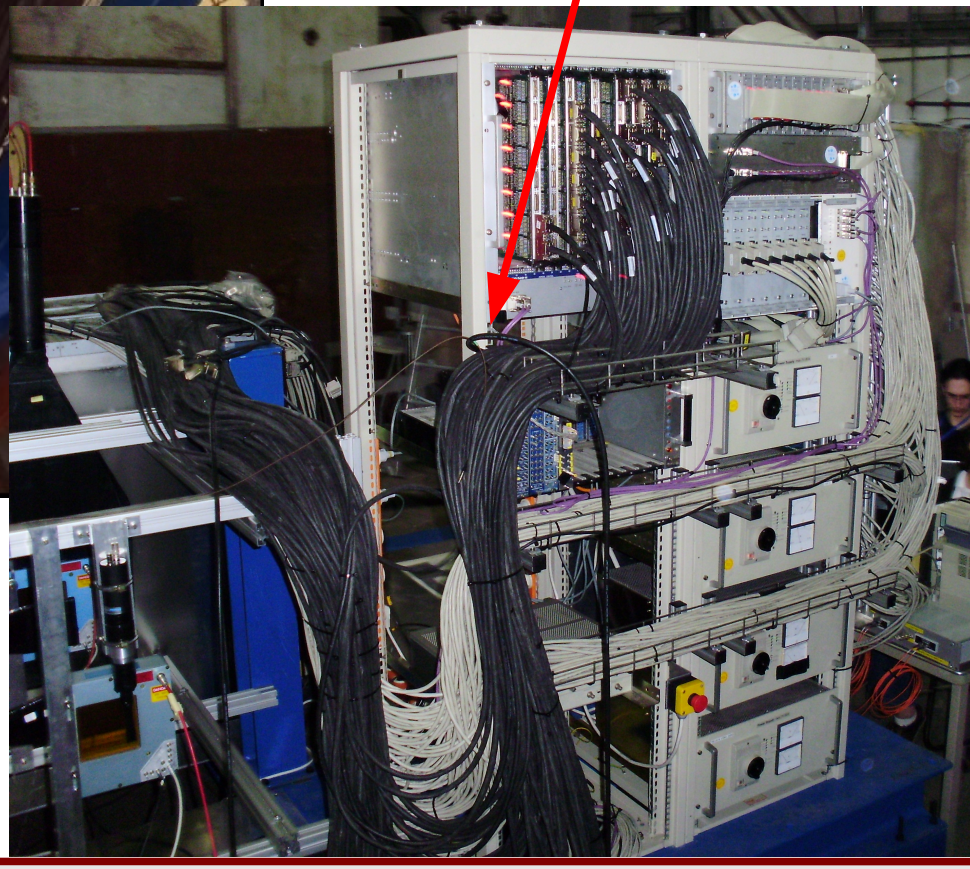
- Tiles
- First SPIROC2b tests
- New front-end board
- DAQ

The AHCAL physics prototype



Cables for calibration boards

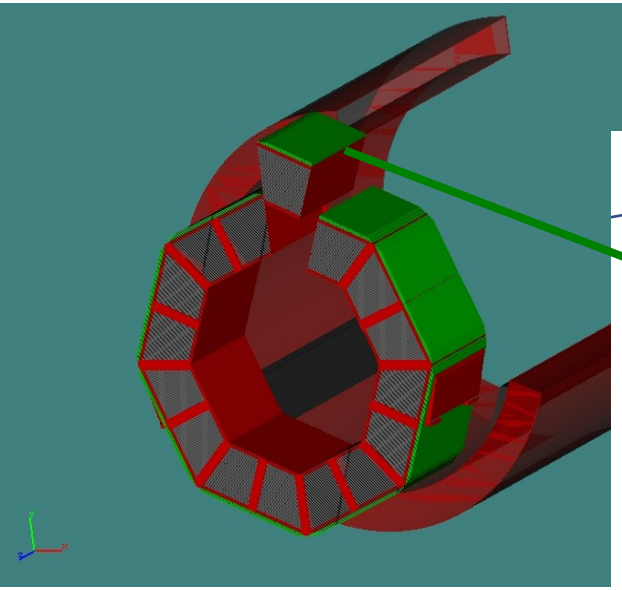
Cables from analog to digital part of electronics

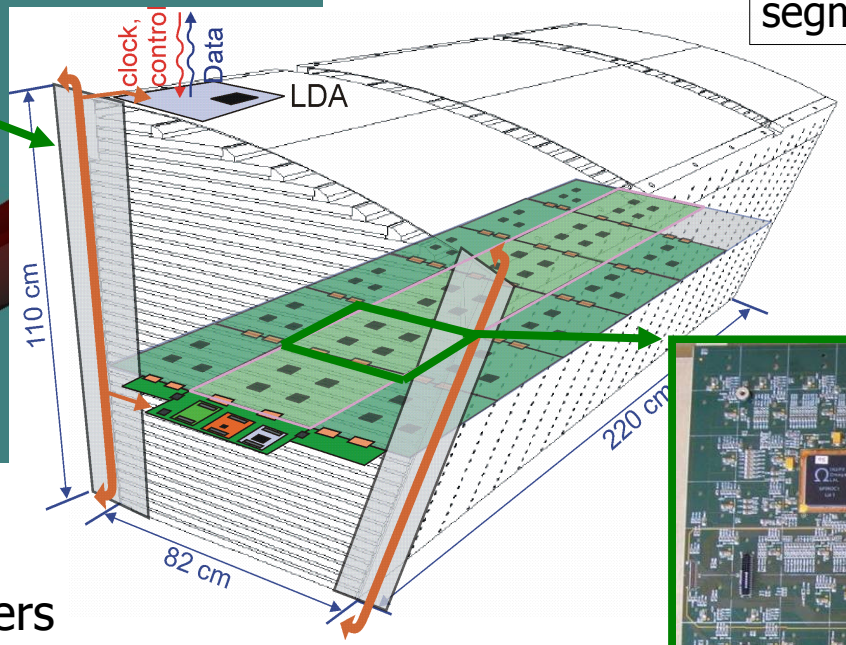


→ Need to build realistic engineering prototype!

The engineering AHCAL prototype

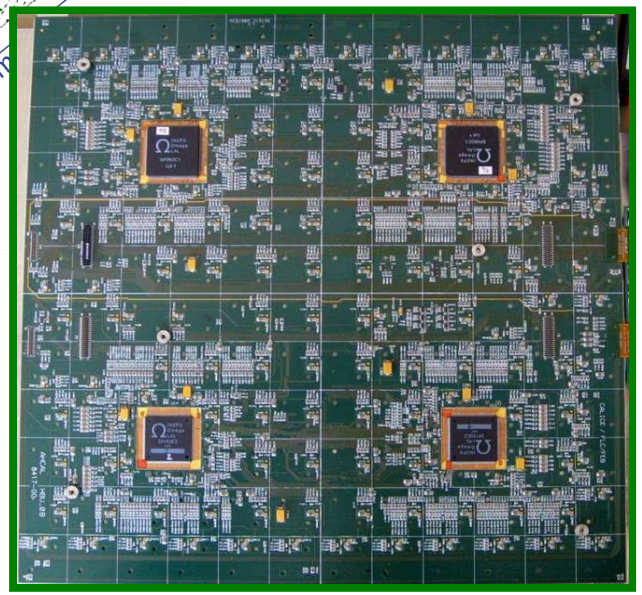
Development of scalable LC detector based on successful experience with physics prototype





Octagonal shape, 16 equivalent wedges, segmented in two along z

PCB with 4 ASICs, 144 scintillator tiles, SiPM readout



Challenges:

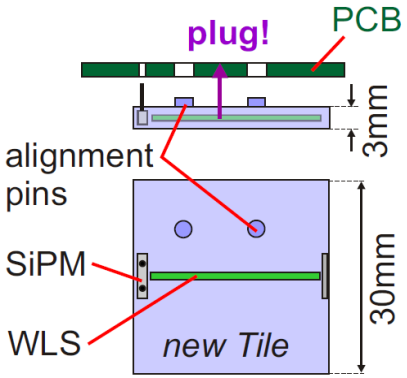
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

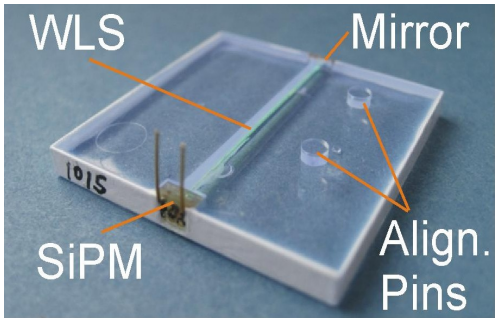
→ Integrated readout electronics

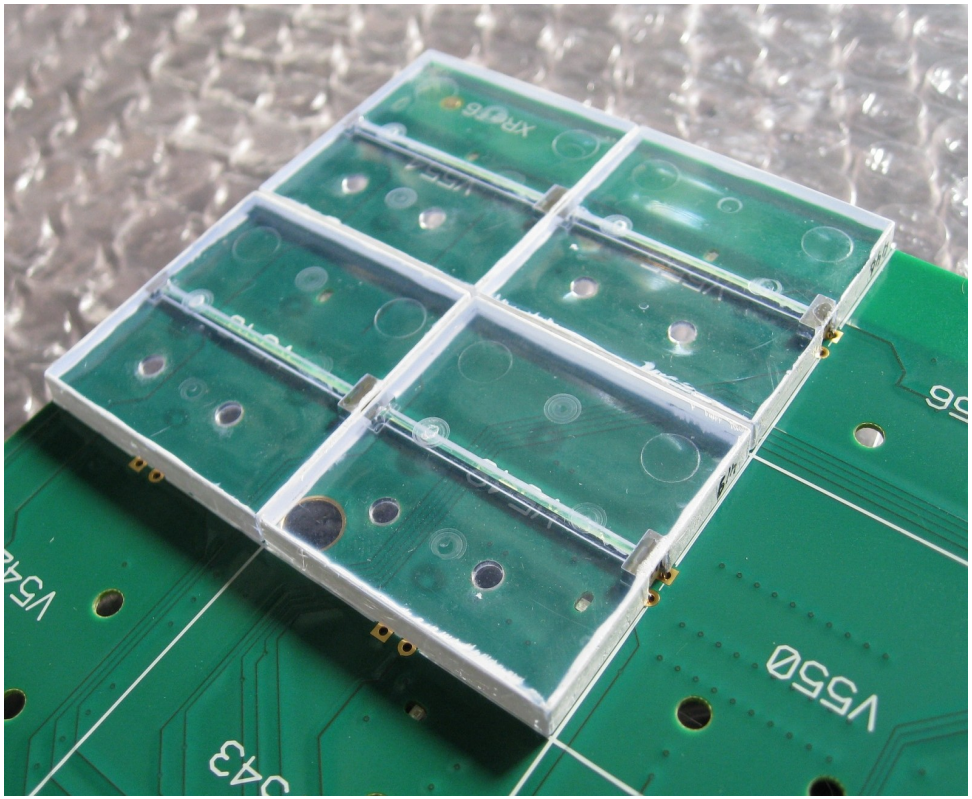
Scintillating tiles

- Signal sampled by scintillating tiles
  → 3x3x0.3cm^3, 2592 tiles per layer
- First version of PCB/tiles:
  - Gain/Noise ~ 4
  - MIP/Noise ~ 30 (in high gain mode, 2 GeV electrons)
- No large sample of tiles available at DESY yet
  → ~800 available at ITEP
  → Tests and selection ongoing
  → ~600 new tiles to be sent to DESY soon

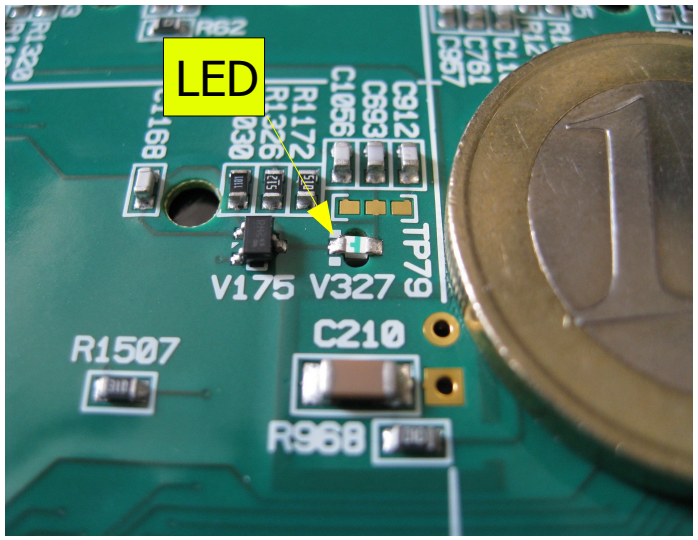
→ Equip 4 new PCBs

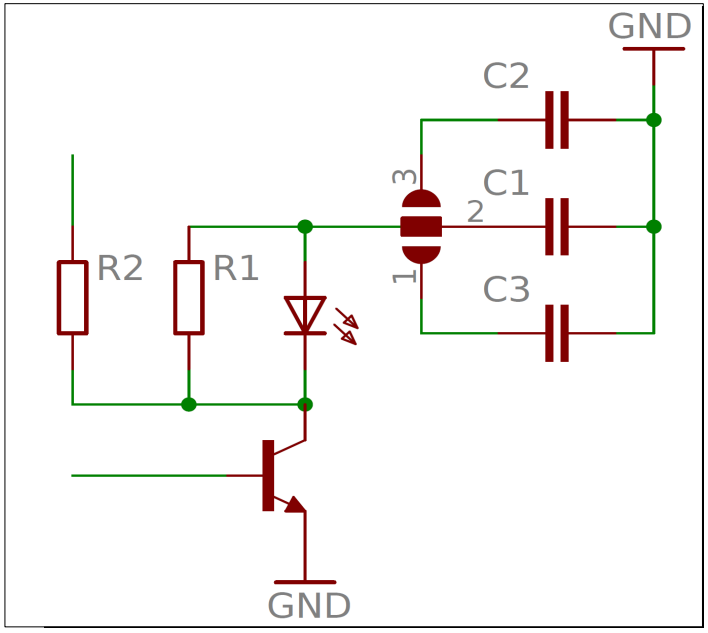






LED calibration system





System task:

- SiPM gain calibration (single pixel spectra)
- SiPM saturation (limited number of pixels)

Wuppertal solution:

- Light directly coupled into tile by 1 integrated LED per channel
- Light output equalization via C1 - C3
- New design implemented in new HBU2 and will be tested extensively

Prague solution:

- Light coupled into tile by notched fiber
- Mechanical integration difficult

  → First full layer tests soon at DESY

The readout chip - SPIROC

Specific chip for SiPM readout:

- Input DAC for channel-wise bias adjustment (36 channels)

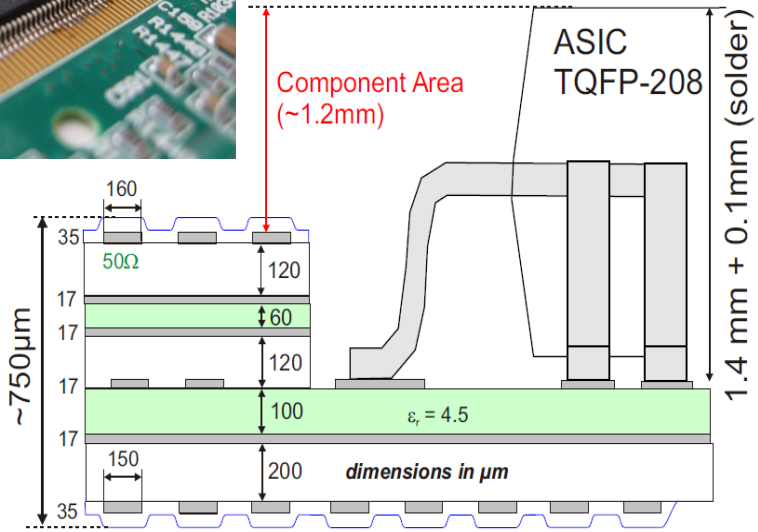
Designed for ILC operation:

- Power pulsing → 25µW/ch
- Dual-gain setup per channel

  → high gain/low gain ~ 10

  → 25fF – 1575fF per channel
- Auto-trigger and auto-gain mode
- Time stamp (12-bit TDC)

Designed by OMEGA/IN2P3



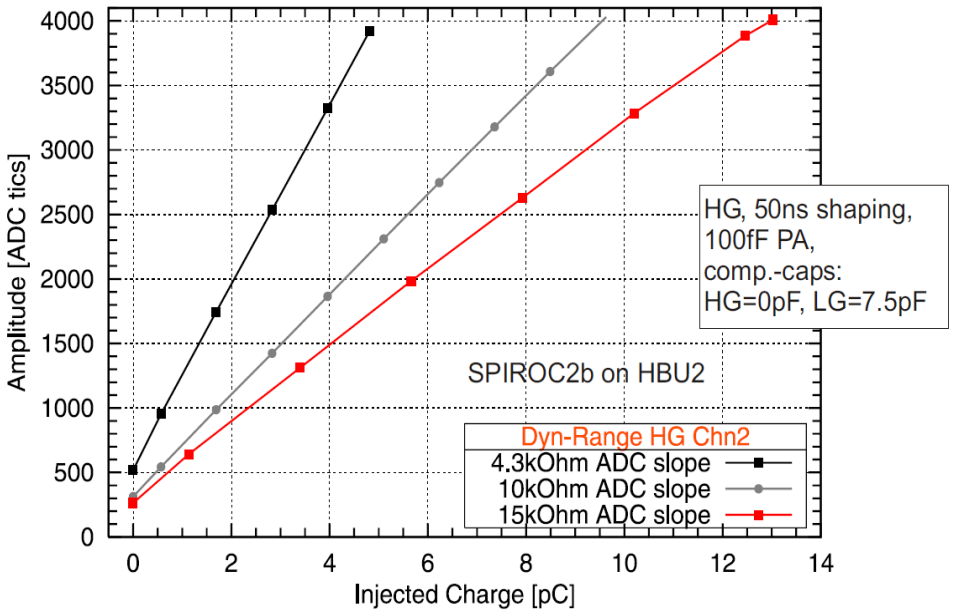
Placement of components in PCB cutouts

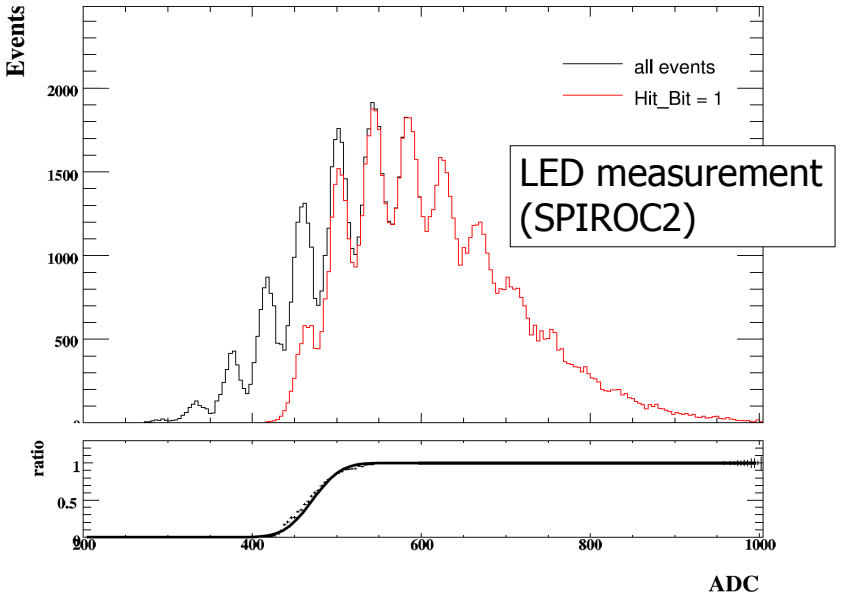
→ 500µm/layer

→ 50mm in total!

Although SPIROC3 is in the pipeline we will use SPIROC2b for first tests with large setups and testbeam!

The readout chip - SPIROC





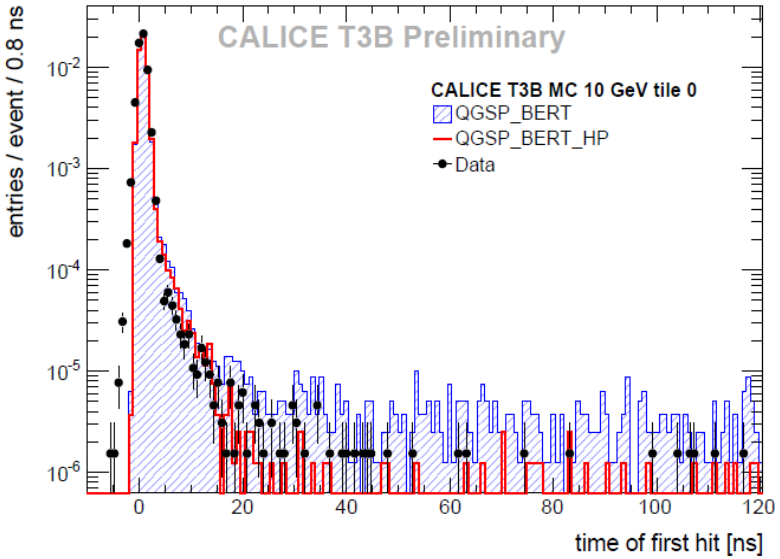
- SPIROC2b integrated in old HBU for first tests

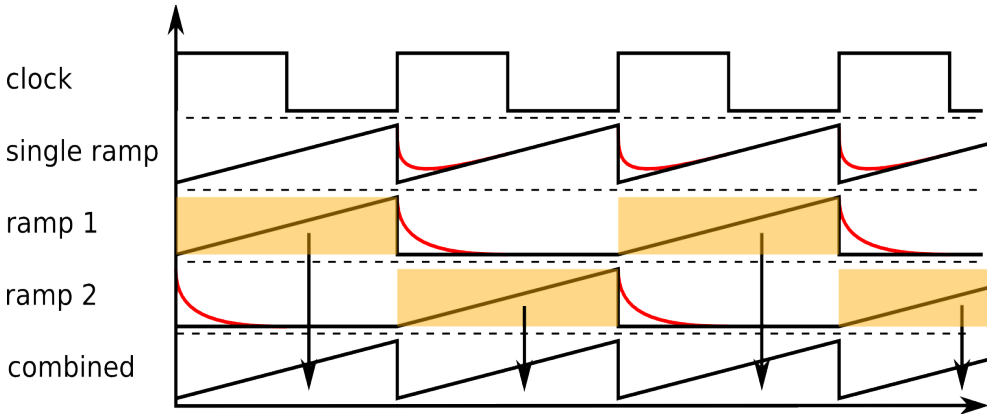
  → linearity, preamplifier gains and TDC
- We see first signals for new HBU!

  → Improved dynamic range visible!

→ Slow control programming, data taking with external trigger and readout works

SPIROC2b – Time measurements





- T3B measured radial development of shower in time in one row of last layer

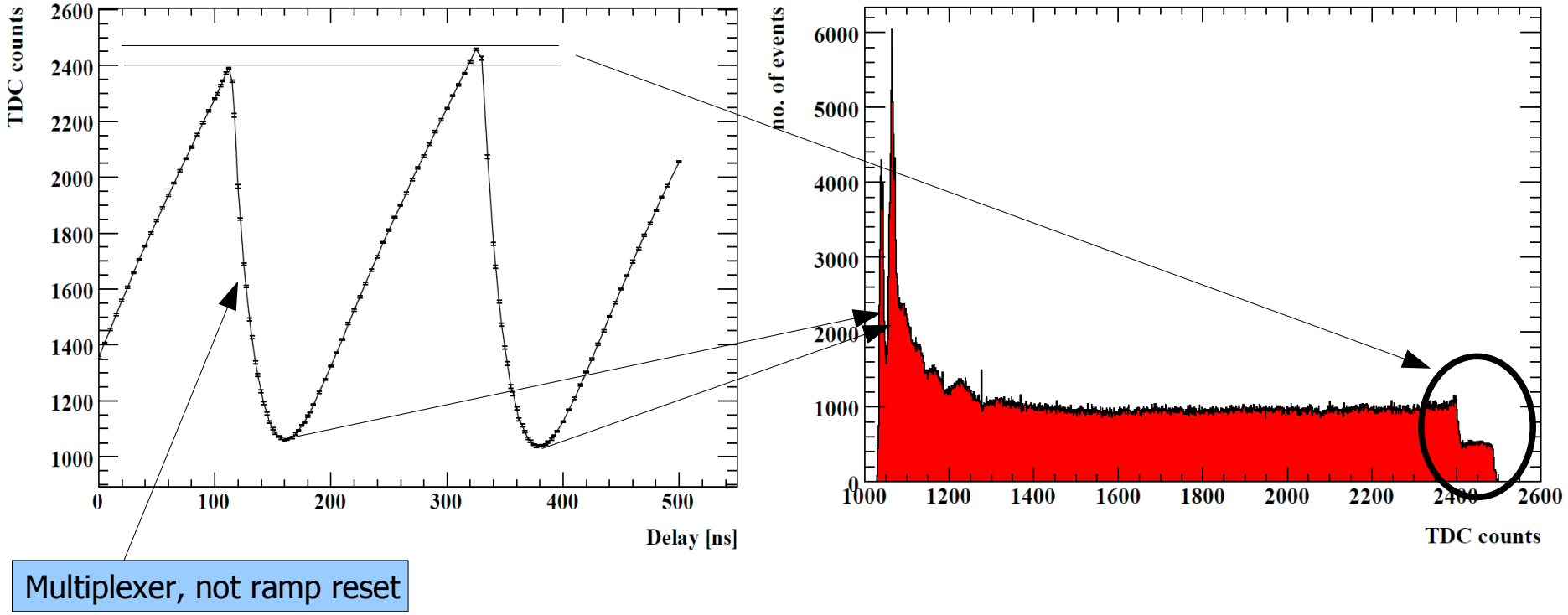
  → Repeat measurement with full layer or even multiple layers
- SPIROC2b measures time in auto-trigger mode relative to bunch clock

  → 2 ramps to reduce deadtime due to ramp reset

  → ILC mode = 200ns ramp, testbeam mode = 5µs ramp (less dead time)

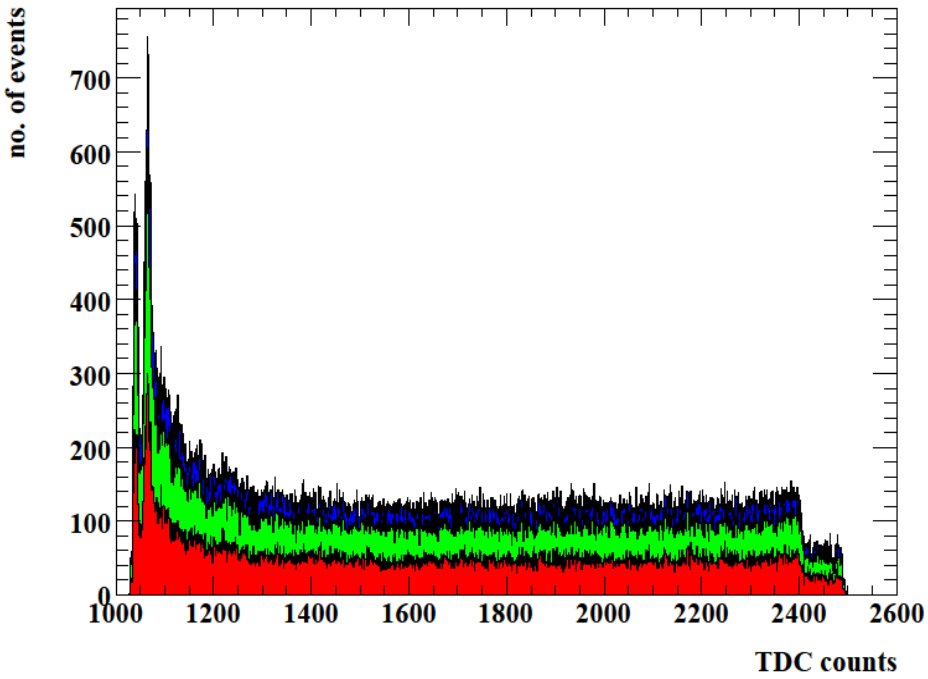
  → Investigate time resolution to optimize ramp slopes (and lengths)

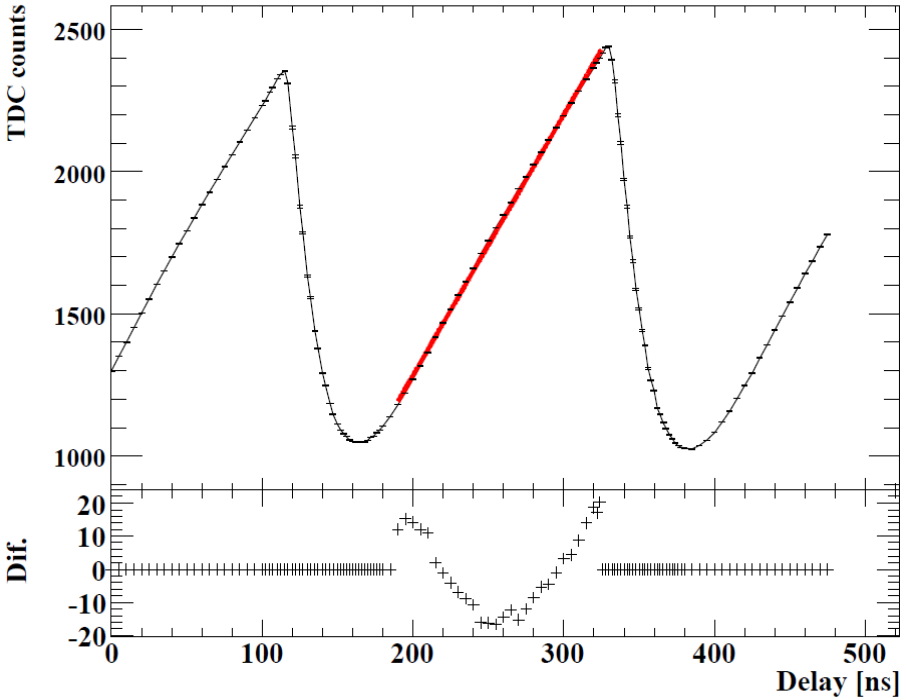
SPIROC2b – TDC (ILC mode)



- First tests of TDC ramps in SPIROC2b show promising results
- Resolution in ILC mode: ~250-350ps (dominated by linearity)
- The 2 ramps have different slopes/heights in ILC mode
- A few aspects will change in SPIROC3, but we have to use SPIROC2b!

SPIROC2b – TDC (ILC mode)





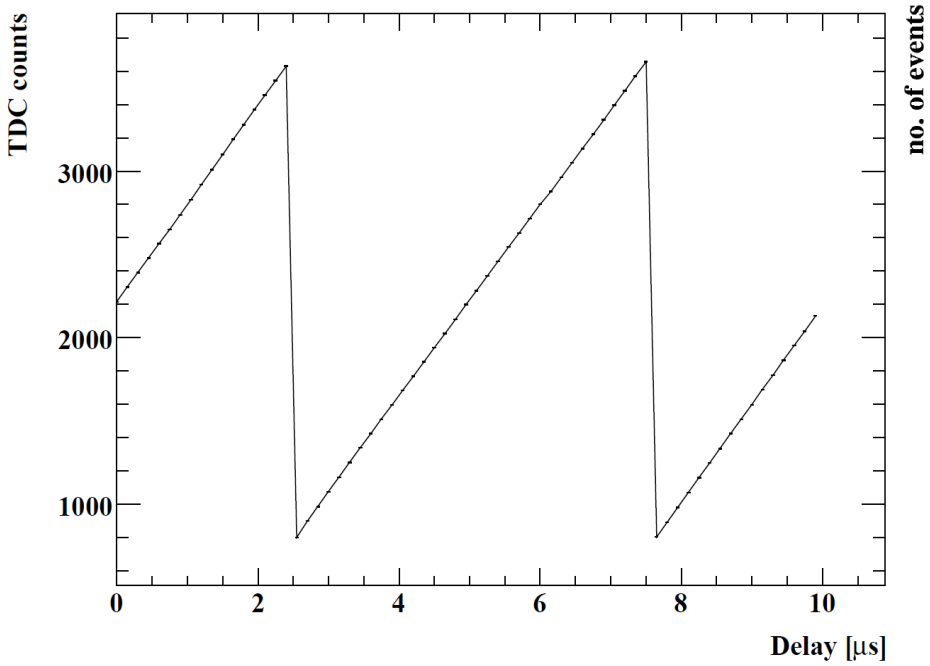
- No correlations visible between ADC and TDC measurements
- Resolution in ILC mode limited by linearity (~1ns)

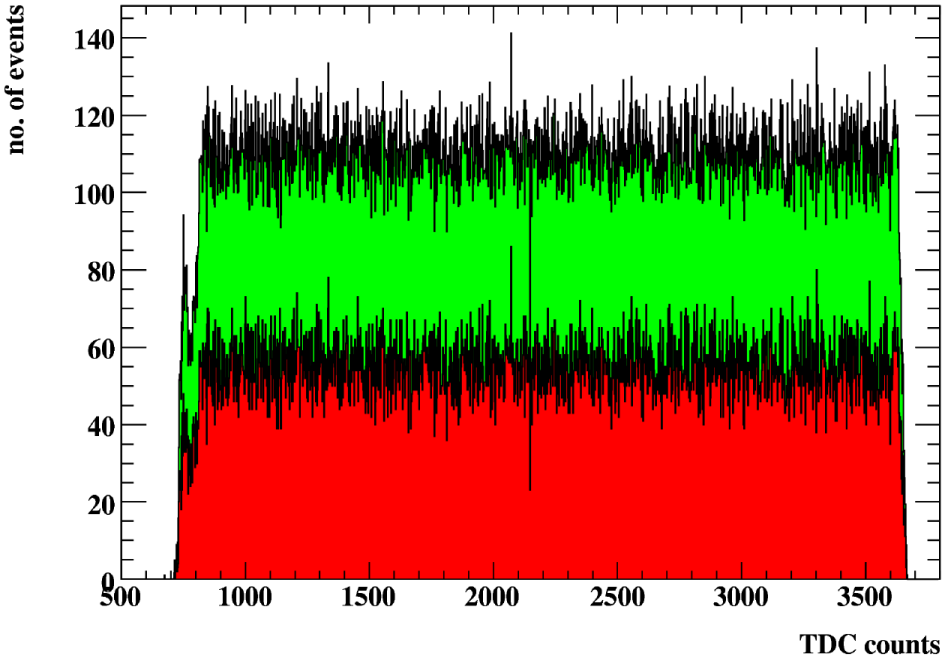
  → Linear fit reveals clear structure

  → Fit of 2 linear functions improves resolution (~300ps)

  → What is the most reasonable measurement/fit strategy?

SPIROC2b – TDC (testbeam mode)





- Multiplexer deadtime very small in testbeam mode (longer ramp)
- Resolution in testbeam mode: ~3ns
- Very small differences for the two ramps in testbeam mode
- Resolution of ~1ns possible by optimizing ramp slopes (and dynamic range)

  → Tests with 1.25µs ramp promising

New HCAL Base Unit (HBU2)

- 4 new HBUs in DESY lab

  → 144 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs

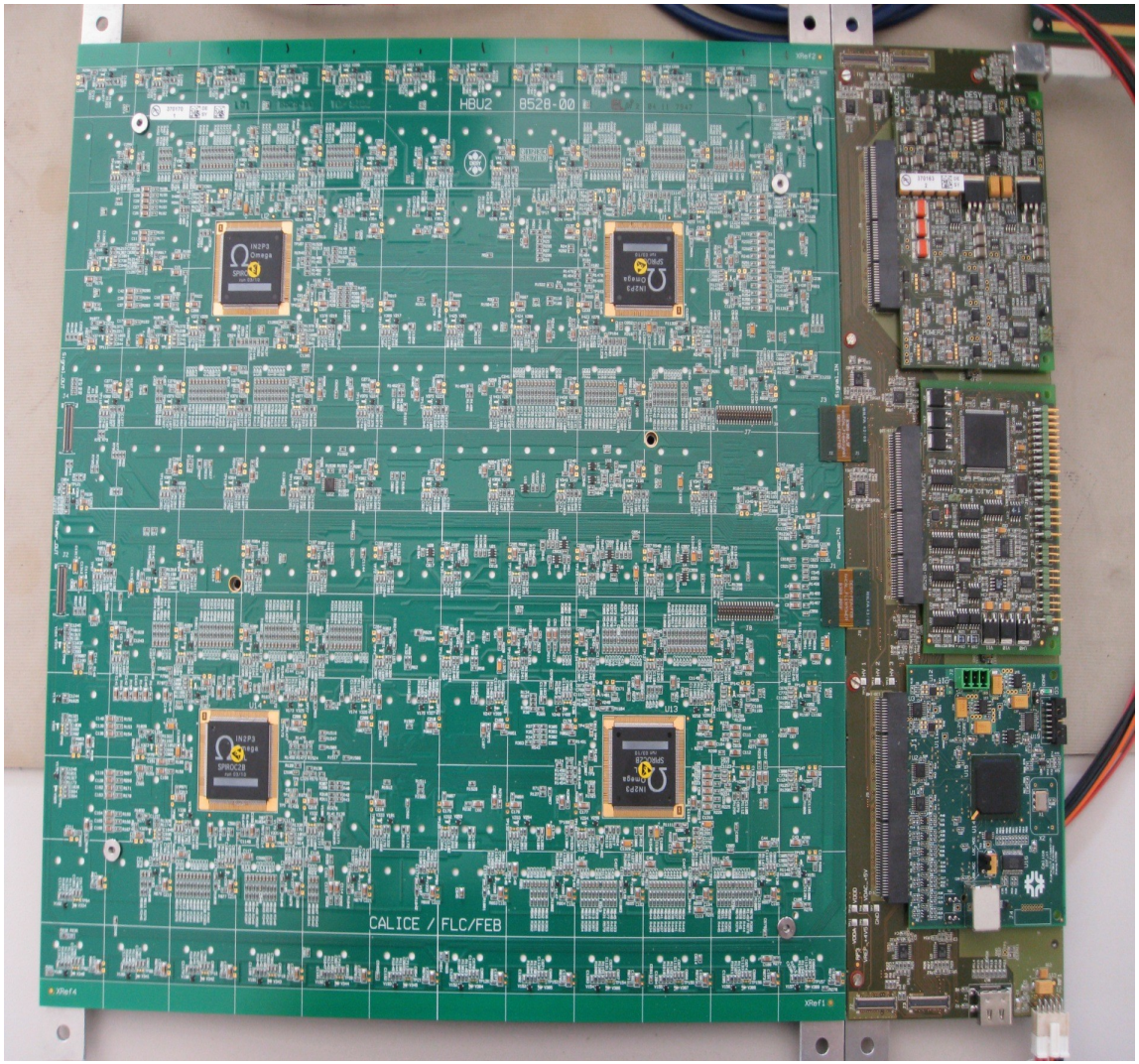
  → No cooling, power pulsing

  → 1 layer = 6x3 HBUs

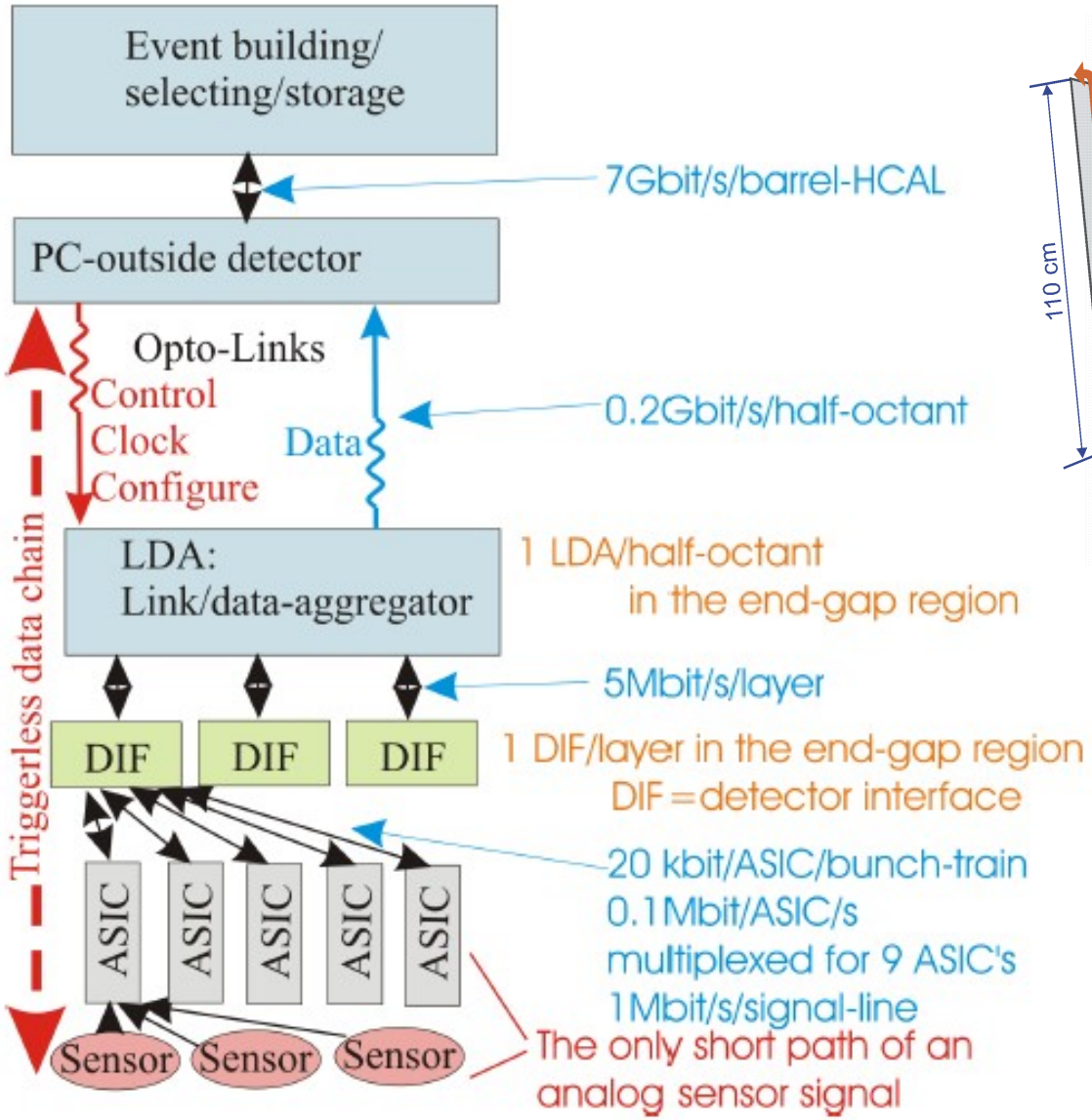
  → ~30.000 in HCAL barrel
- 1 HBU2 connected to DAQ modules for first tests

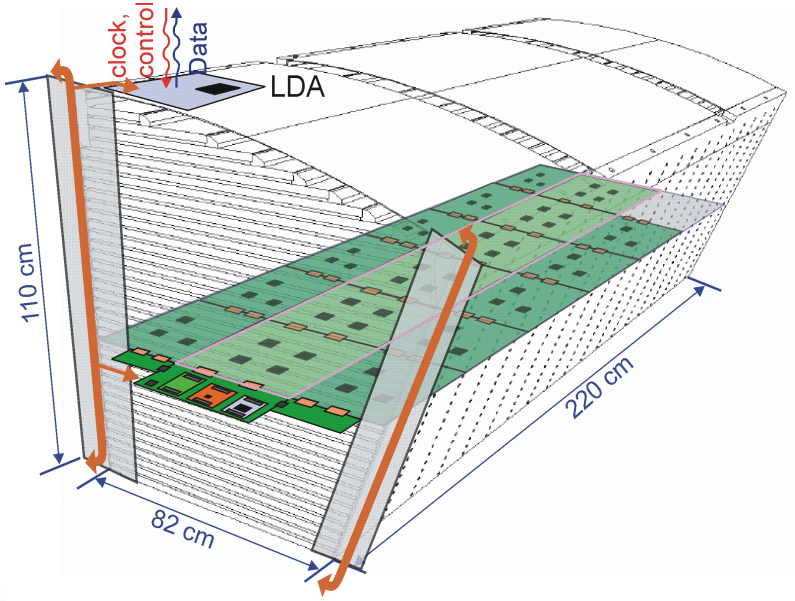
  → so far fully functioning!
- 6-8 HBU2s till end of year

  → New SiPM production at ITEP to be started
- Go to DESY testbeam soon



Data acquisition





- Moderate data rates using channel-wise self-triggering

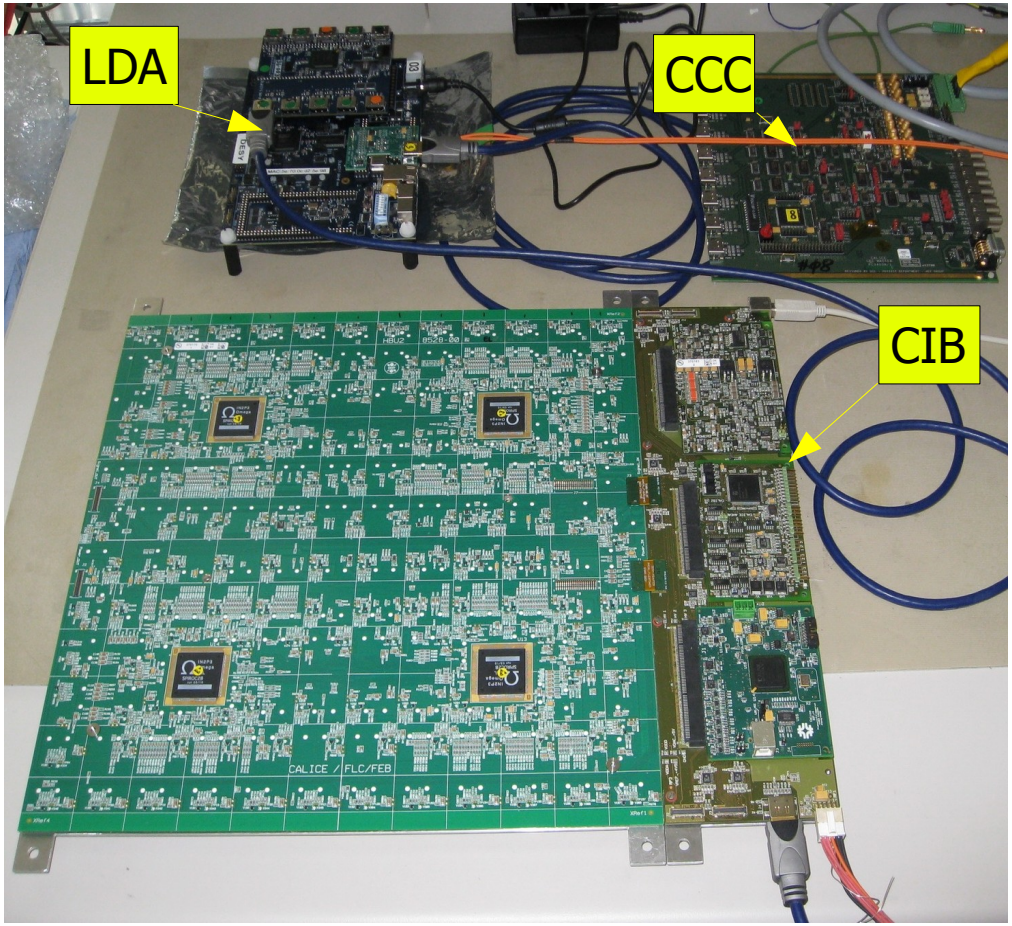
  → No need for further front-end event selection

Data acquisition

- All components working at DESY
- 2 options:
  - Labview based DAQ for SPIROC2b tests and single HBU2 testbeam (finished)
  - XDAQ for full detector operation

    → to be started
- Currently 3 DIFs from NIU

  → Duplicate setups for more students, for Wuppertal, testbeam etc.



Summary and outlook

- HBU2 under test at DESY, so far fully functioning!
- First SPIROC2b tests in (old and new) HBU environment
  - Channel-wise preamplifier gain setup works
  - TDC measurements show promising results, both in ILC and testbeam mode
  - First successful data taking in HBU2 environment
- Tiles to be sent to DESY soon

To do

- System tests of calibration system
- Plenty of SPIROC2b tests in HBU2 environment
- Assembly of multi-HBU2 setup (~6 HBU2s at end of the year)
- DAQ development
- etc. etc.

Selection of new tiles

- ITEP proposed selection criteria for new tiles

  - HV such that we have 13 pixels for Sr90 signals

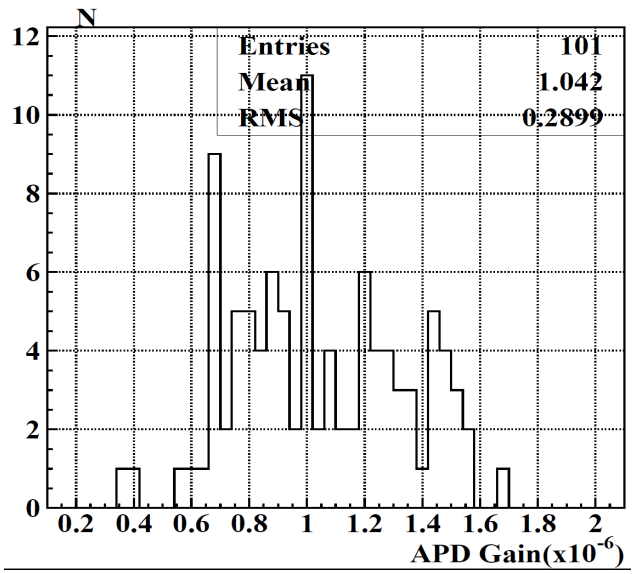
  - Gain larger than 450000 for 140ns gate, >400000 for 100ns gate (~50ns shaping)

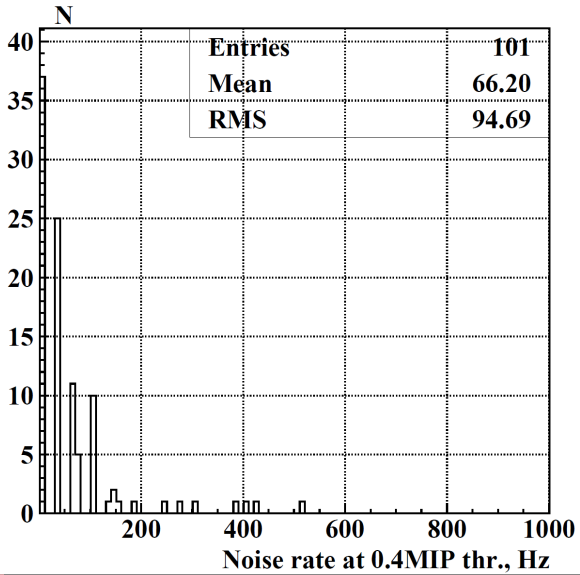
  - Noise at 0.4 MIP smaller than 500Hz → <100Hz at 0.5 MIP

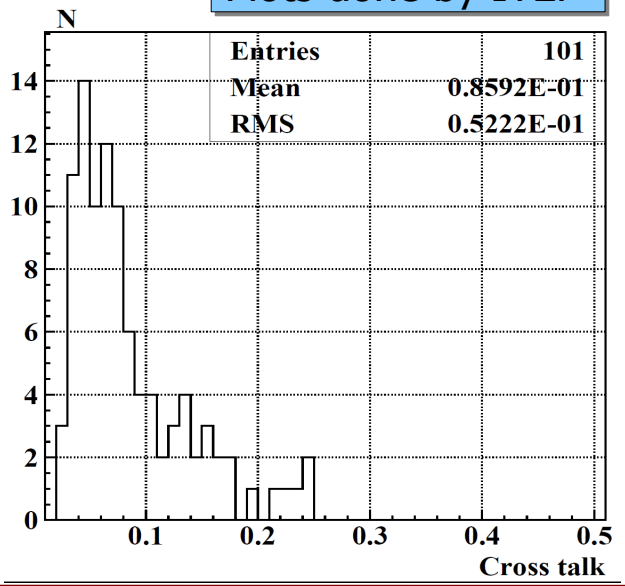
  - Cross talk less than 20%

  - Number of pixels at maximum light >700

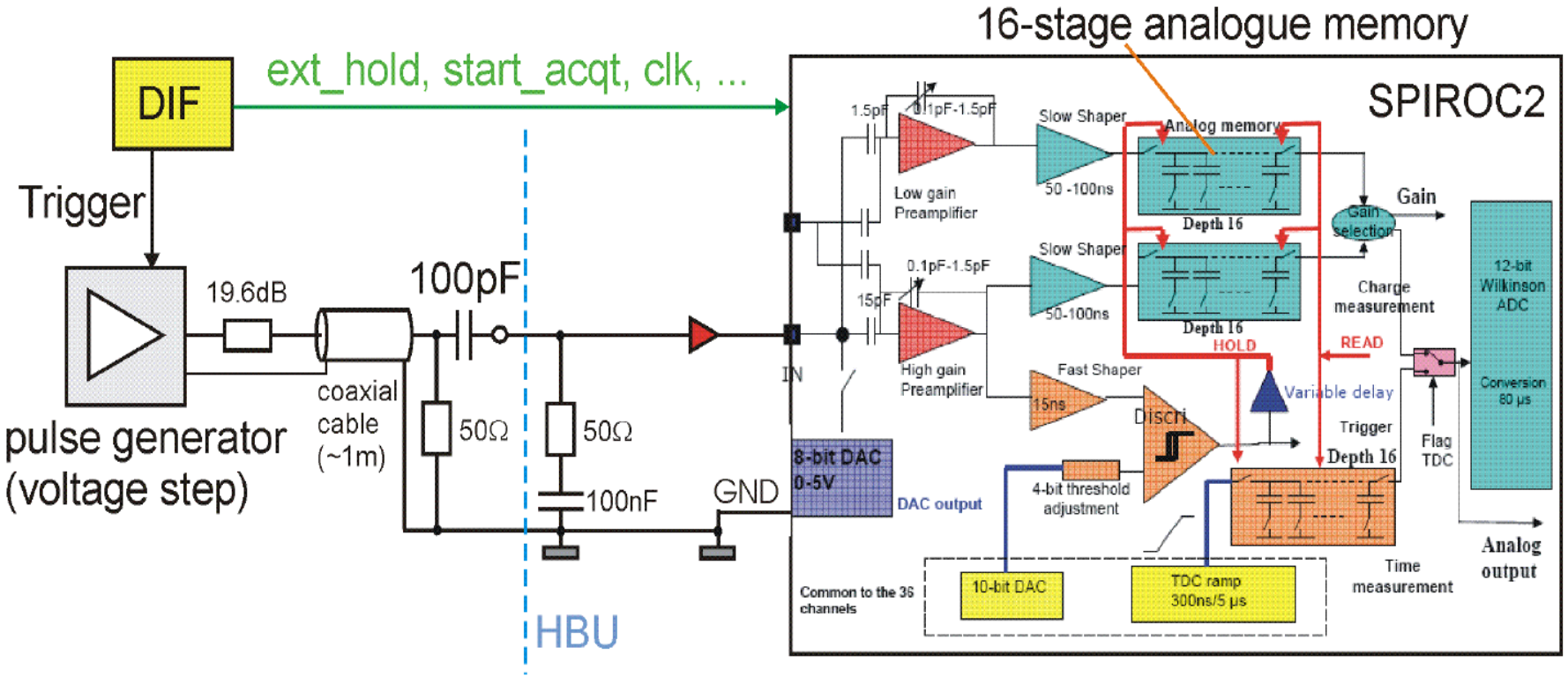
Plots done by ITEP



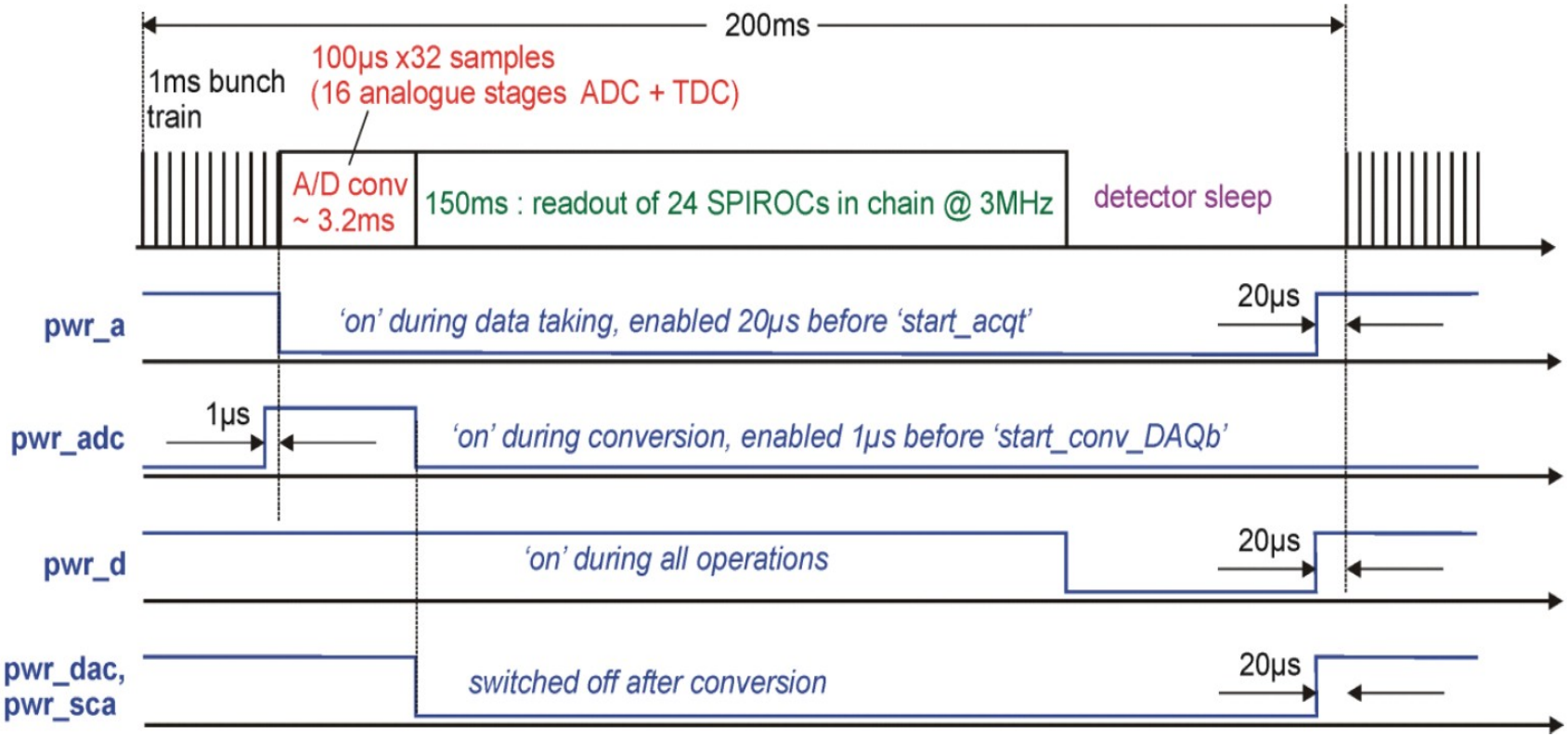




SPIROC2b

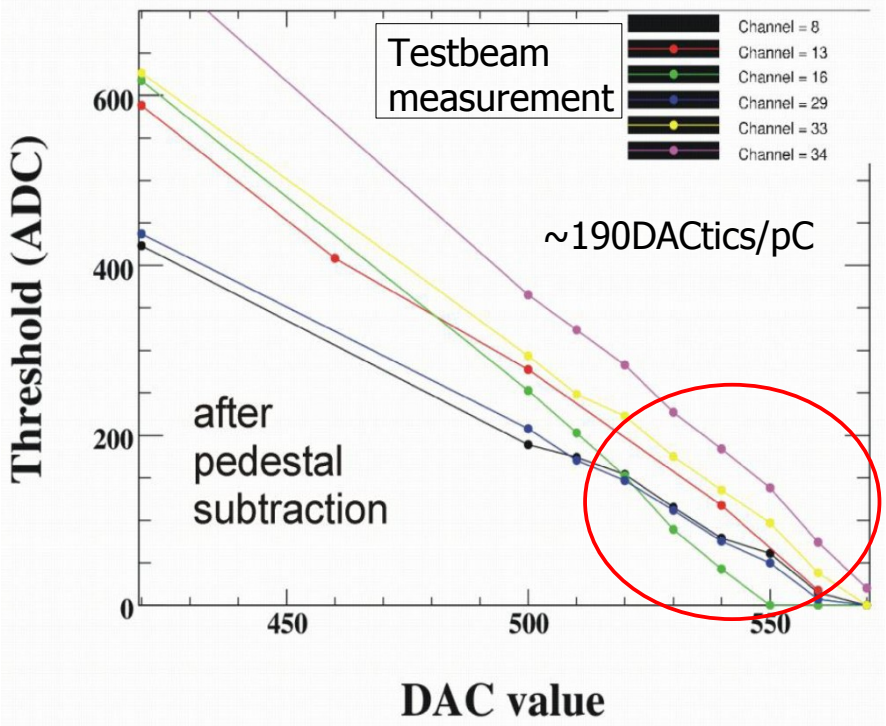

16-stage analogue memory
DIF
ext_hold, start_acqt, clk, ...
Trigger
19.6dB
100pF
coaxial cable (~1m)
pulse generator (voltage step)
50Ω
50Ω
100nF
GND
HBU
IN
SPIROC2
1.5pF
0.1pF-1.5pF
Low gain Preamplifier
Slow Shaper
50 -100ns
Analog memory
Depth 16
Gain selection
Gain
0.1pF-1.5pF
15pF
High gain Preamplifier
Slow Shaper
50-100ns
Depth 16
Charge measurement
HOLD
READ
Fast Shaper
15ns
Discri
Variable delay
Trigger
Depth 16
Flag TDC
12-bit Wilkinson ADC
Conversion 60 µs
8-bit DAC 0-5V
DAC output
4-bit threshold adjustment
Common to the 36 channels
10-bit DAC
TDC ramp 300ns/5 µs
Time measurement
Analog output

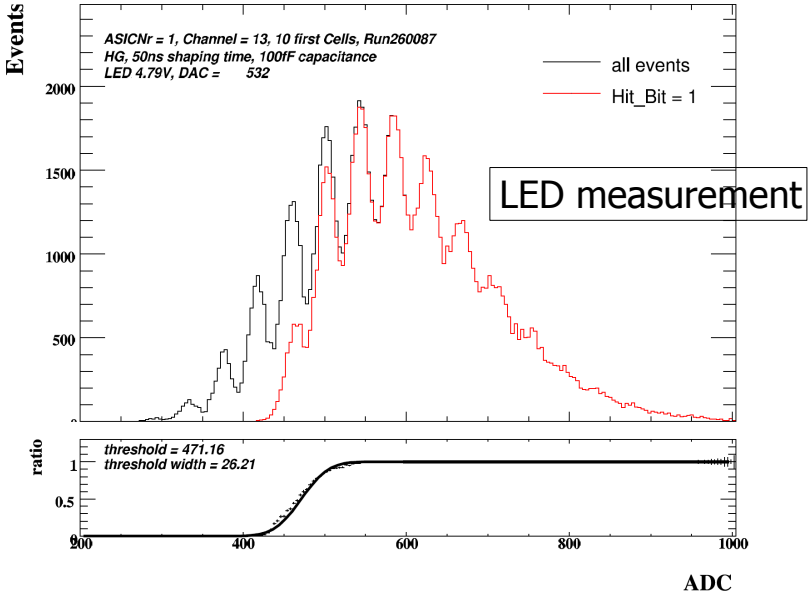
Power pulsing

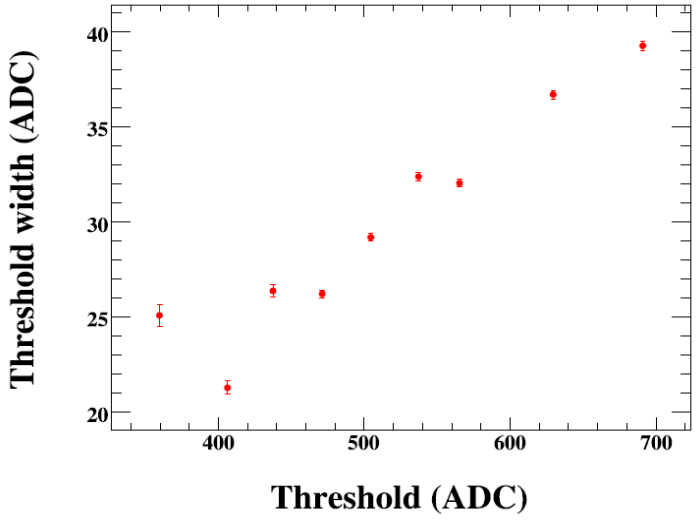


Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency

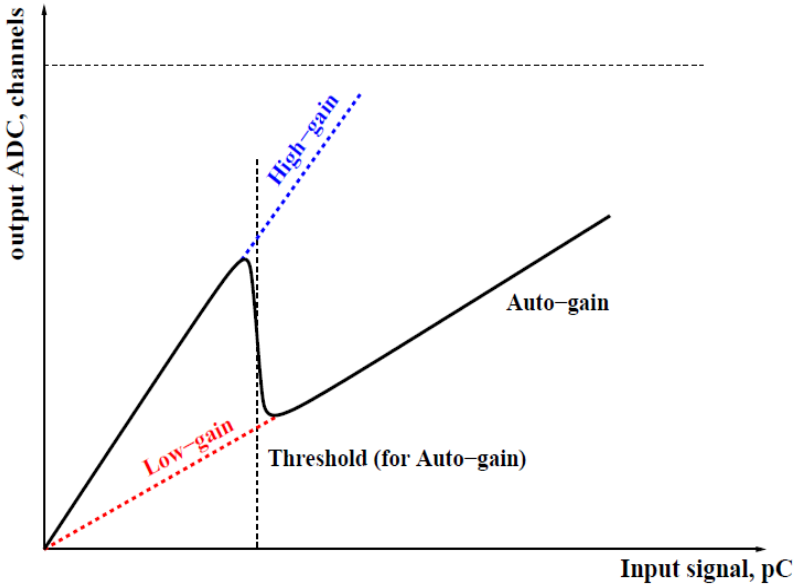


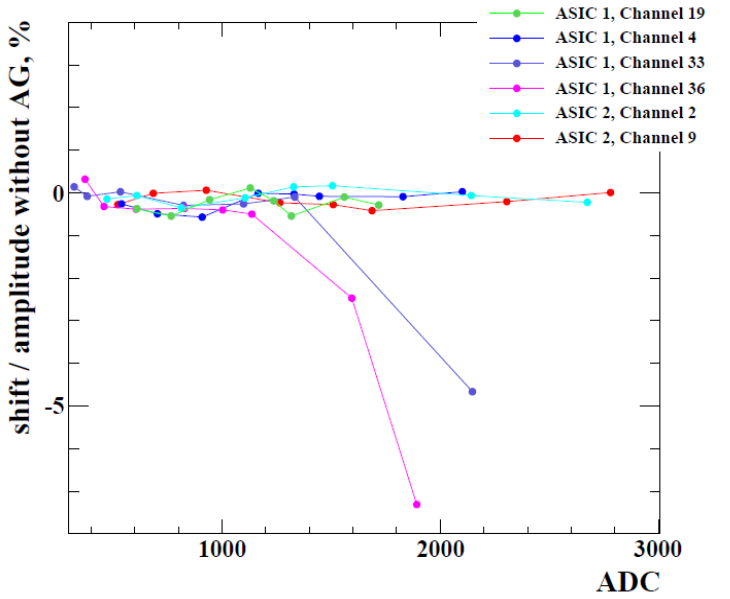


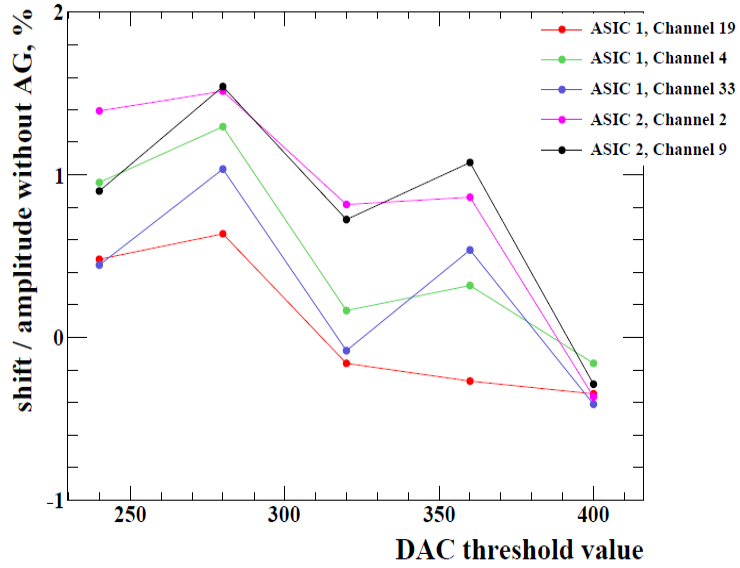


Autogain performance - Linearity

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, but still slightly depends on:
  - Amplitude
  - Distance to threshold

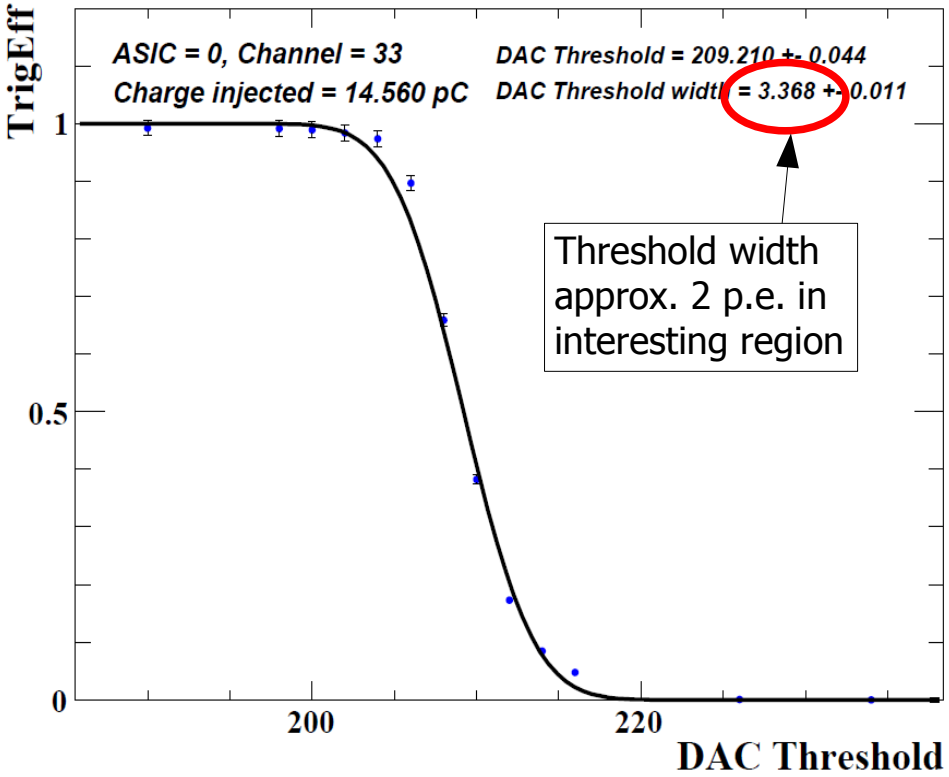


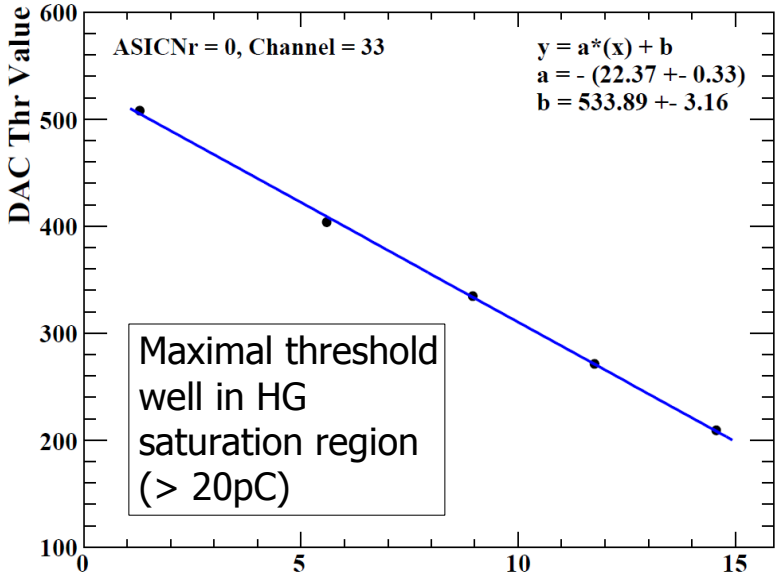


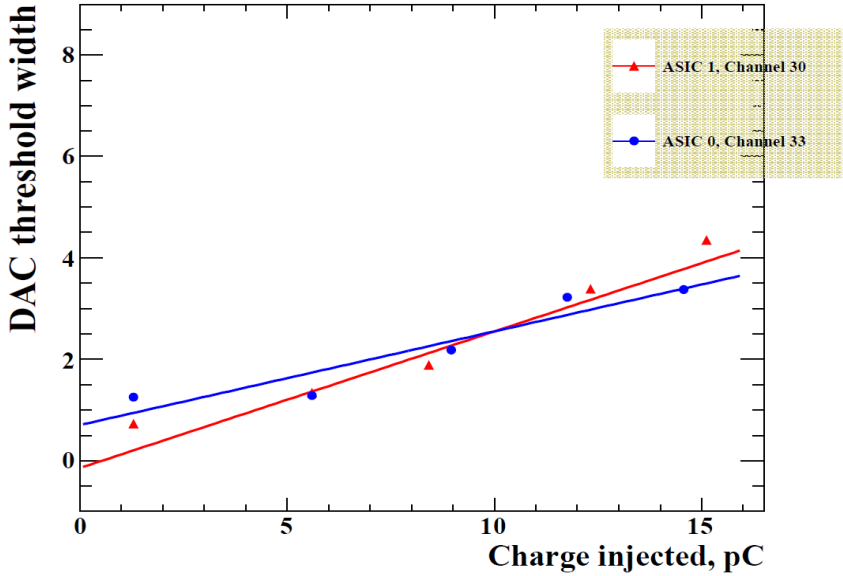


Autogain performance - Thresholds

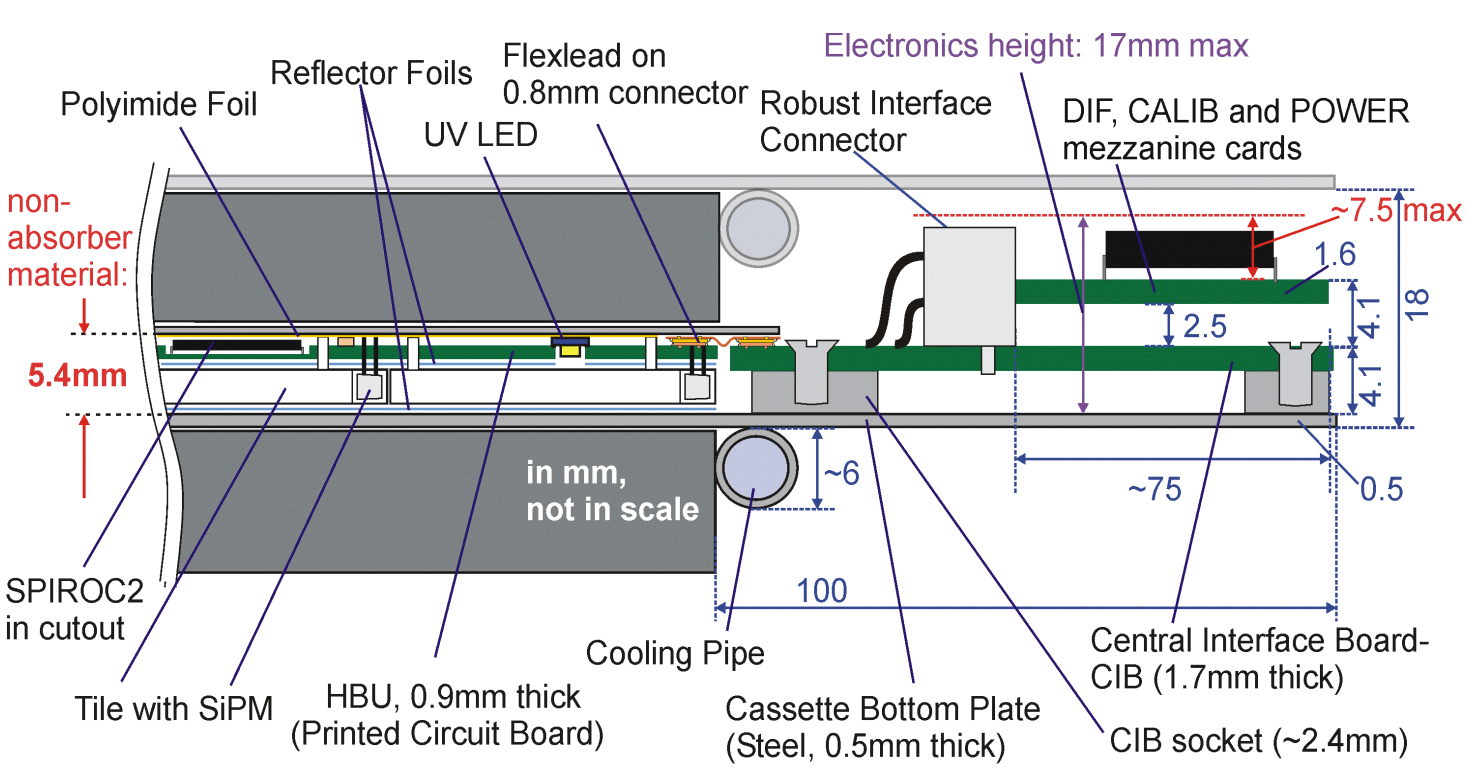
- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Similar performance as for autotrigger

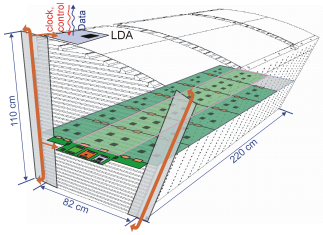






AHCAL layer – cross section





Abbr.	Name
DIF	Detector Interface Board
CALIB	Steering for LED calibration
CIB	Central Interface Board
HBU	Front-end board

- Compliant with steel and tungsten options
- Redesign and production of components almost finished