AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Development of readout electronic and test-beam results of FCAL detector prototype

Szymon Kulis for AGH-UST
on behalf of **FCAL Collaboration**

Labs involved : Argonne, Vinca Inst Belgrade, Bukharest IFIN, CERN, Univ. of Colorado, Cracow AGH-UST,Cracow INP, JINR Dubna, Royal Holloway, NCPHEP Minsk, Santa Cruz, Stanford University, SLAC, Tuhoku Univ., Tel Aviv Univ., DESY (Z.)

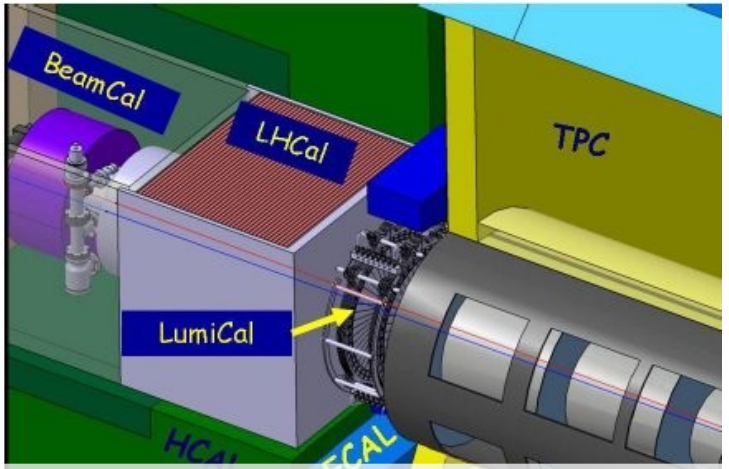
Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

International Workshop on Future Linear Colliders 2011
Universidad de Granada (Palacio de Congresos, Granada, Spain)

Agenda

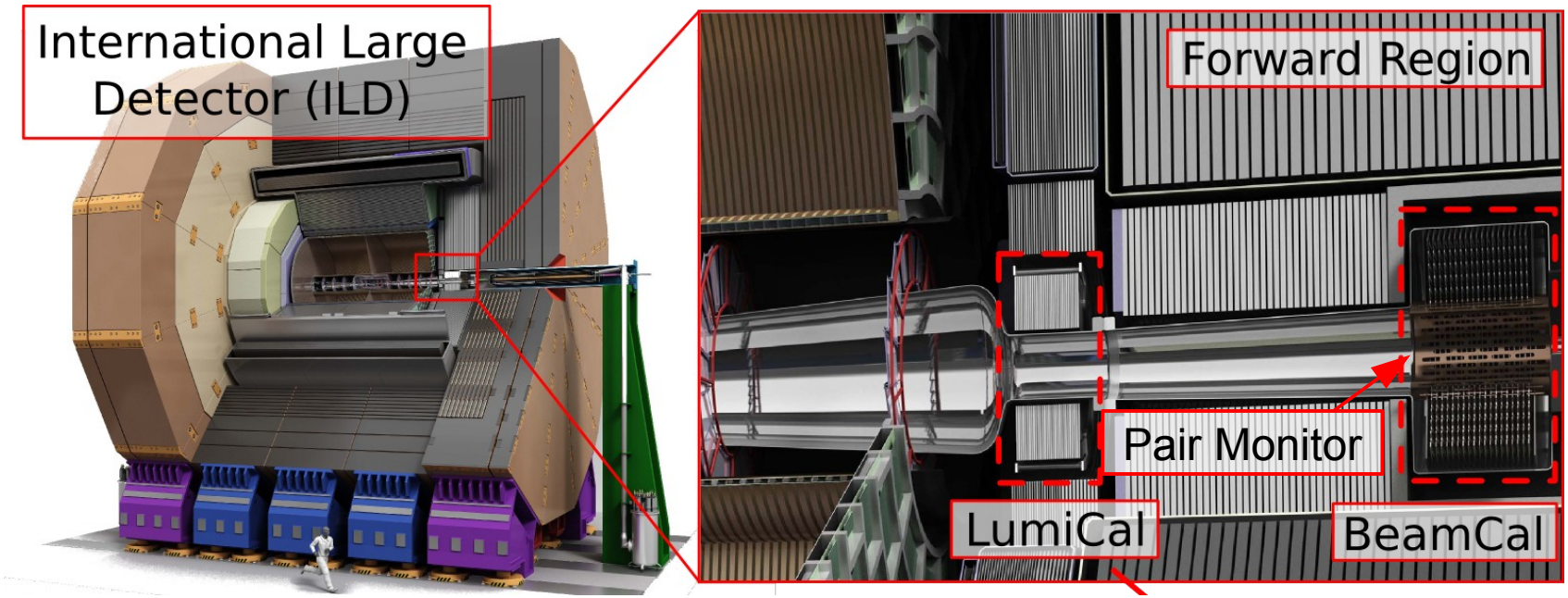
- FCAL@ILD detector
- Readout architectures
- Test beams
- Detector positioning
- General purpose

  Mechanical frame
- Summary and future plans



ILD @ ILC
Very Forward Instrumentation

Forward Region in ILD



- **BeamCal**: Beam diagnostics and low angle electron detection
- **LumiCal:** Precise measurement of integrated luminosity
- **Pair Monitor**: precise beam profile measurement

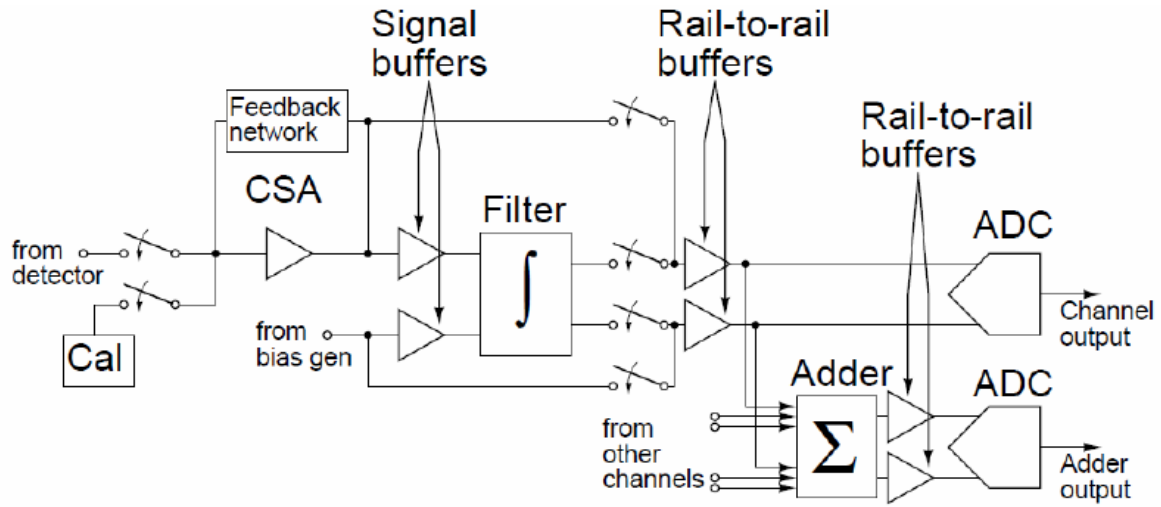
Construction: sampling calorimeter

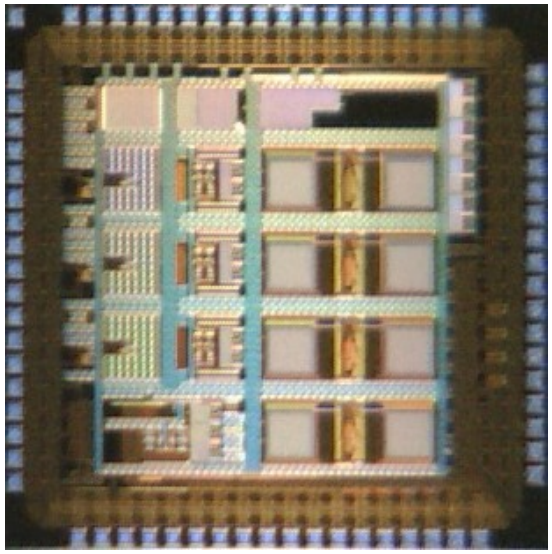
30 (ILC) / 40 (CLIC) layers sensor/tungsten

Challenges:
radiation hardness (BeamCal), high precision (LumiCal) and fast readout (both)

See more : H. Abramowicz et al. "Forward Instrumentation for ILC Detectors" JINST 5:P12002,2010

BeamCal readout architecture

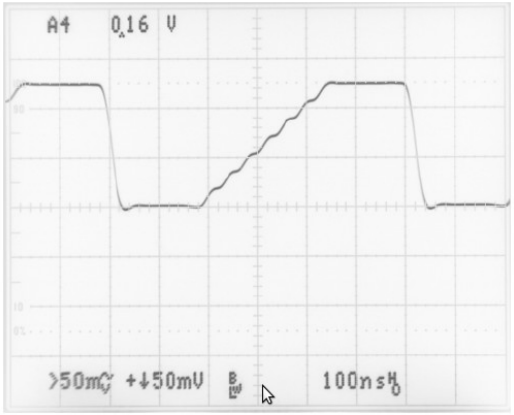




•**KPIX ASICs -** Designed especially for BeamCal (fast feedback function).

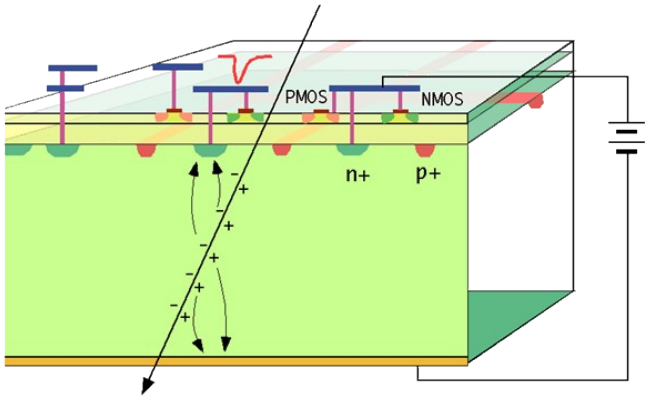
First prototype done in TSMC 0.18um, 1.8V. It comprises:

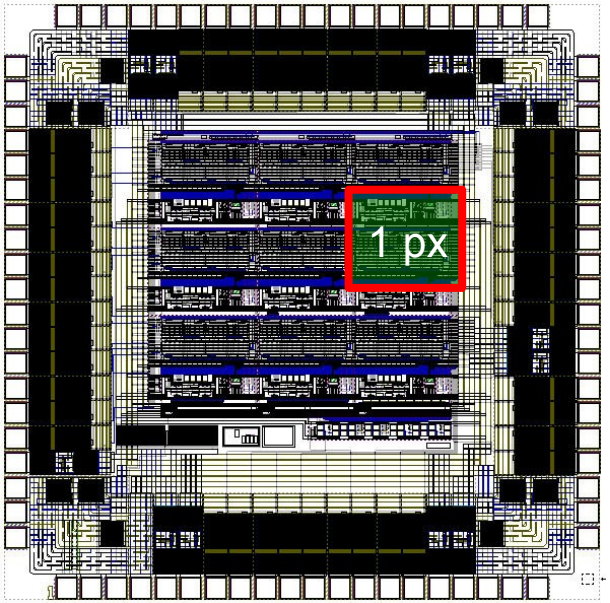
- 3 charge amplifiers
- 4 x 10-bit SAR ADCs,
- 1 Switched Capacitor adder,
- 3 Switched Capacitor filters



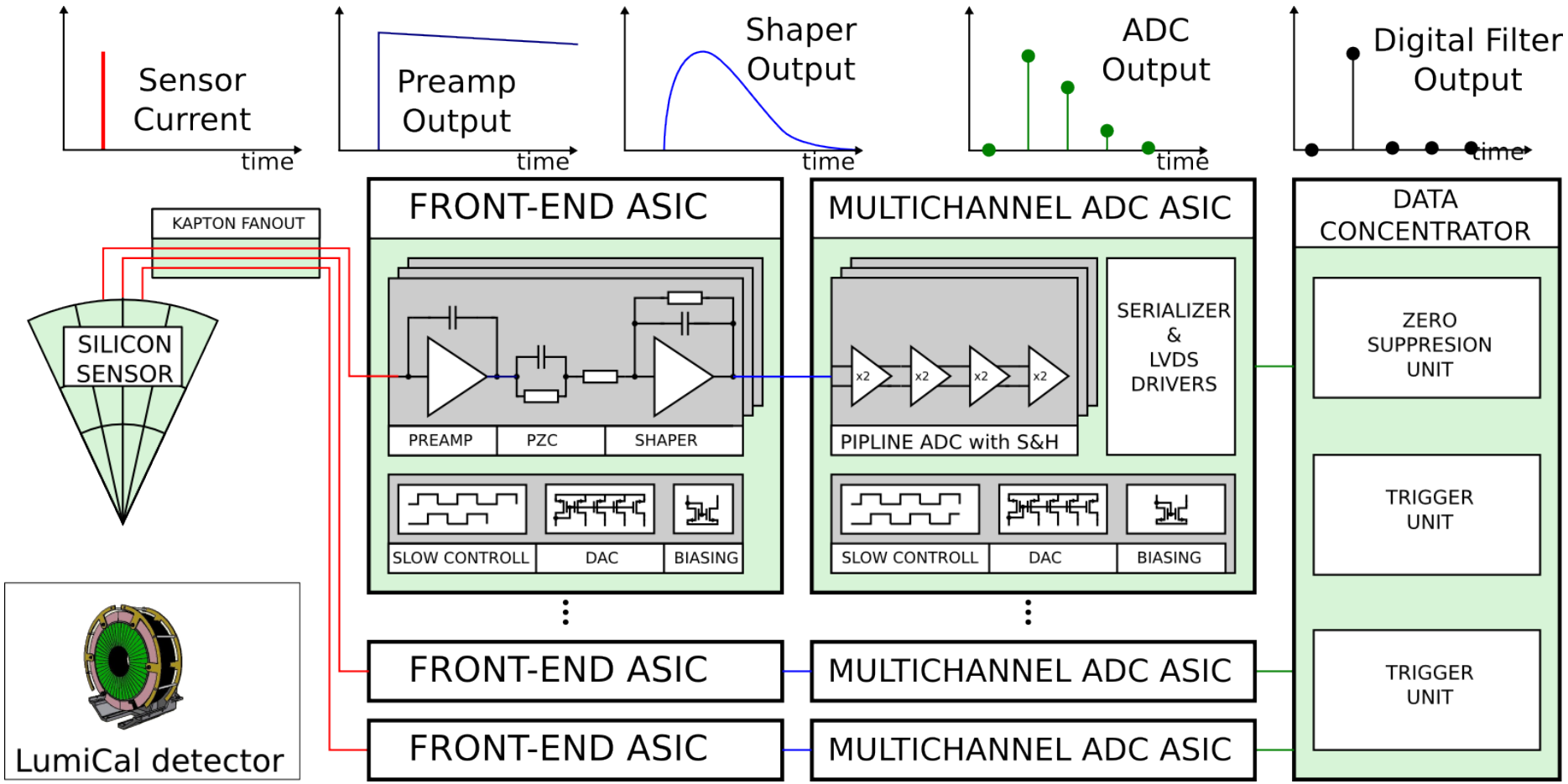
Pair Monitor

- Pair Monitor Detector :
  - Pixel size: 400 x 400 μm2
  - Active Radius: 10 cm
  - Total number of pixels: ~200,000
  - CMOS 0.2 μm, SOI technology (Monolithic construction allows the elimination of the bump-bonding process)
- First readout prototype
  - 3x3 pixels
  - digital readout (preamp, discriminator, counter)
  - performance measurements done and published

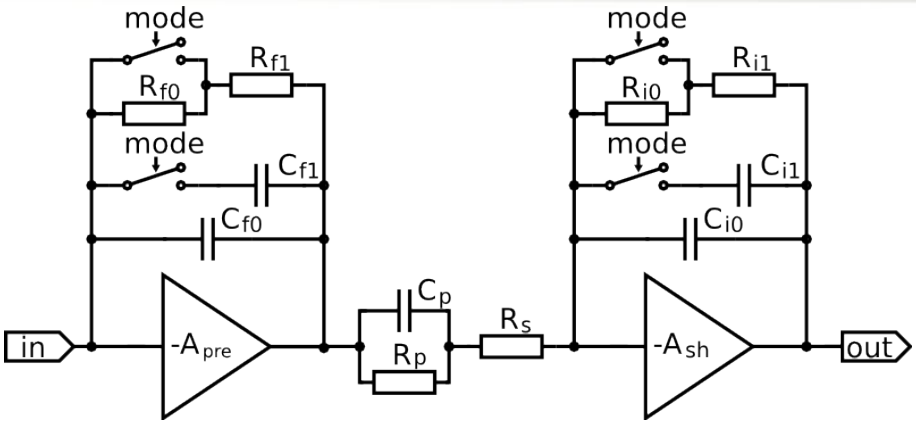


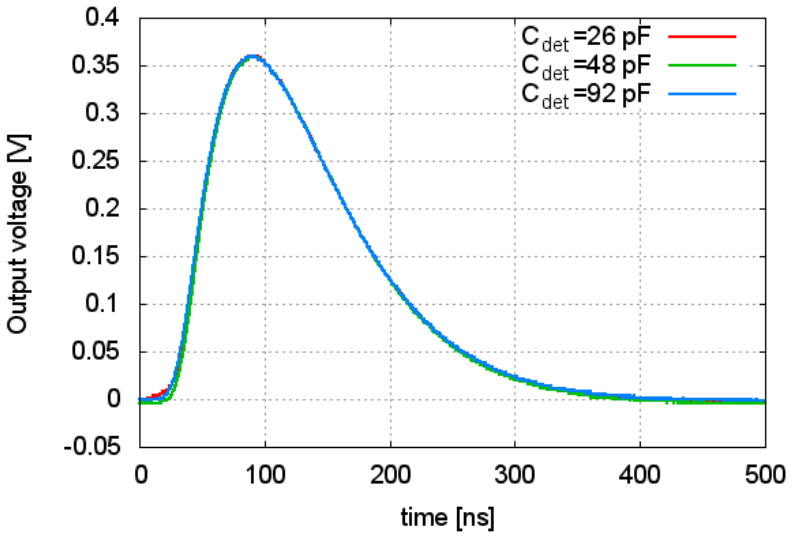


LumiCal readout architecture



Front-end Electronics

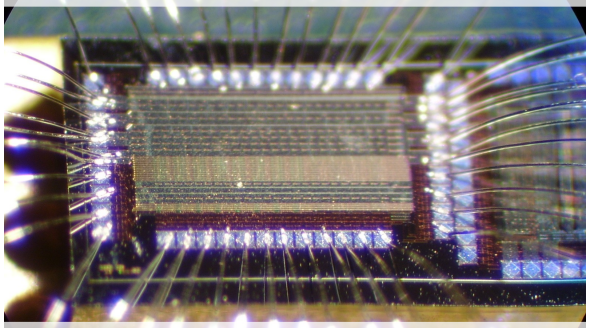




- Cdet ≈ 0 ÷ 100pF
- 1st order shaper (Tpeak ≈ 60 ns)
- variable gain:
  - calibration mode - MIP sensitivity (~4fC)
  - physics mode - input charge up to 10 pC

- prototypes fabricated and tested → **fully functional**
  - power consumption 8.9 mW/channel
  - event rate up to 3 MHz
  - Crosstalk < 1%

ASIC contains 8 channels



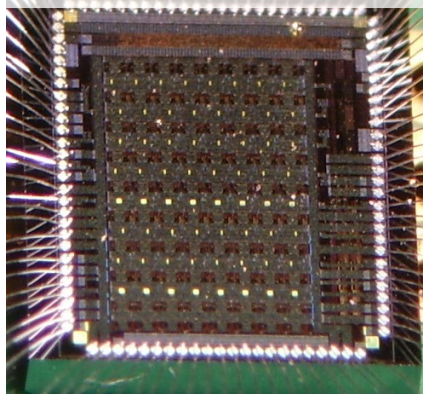
AMS 0.35 µm

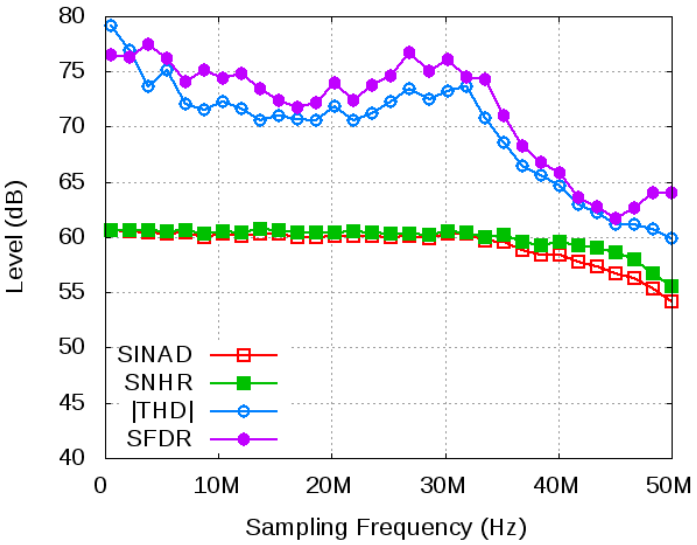
See more : M. Idzik, Sz. Kulis, D. Przyborowski "Development of front-end electronics for the luminoisty detector at ILC" Nucl. Instr. and Meth. A 608 (2009) pp.169-174

Multichannel Digitizer

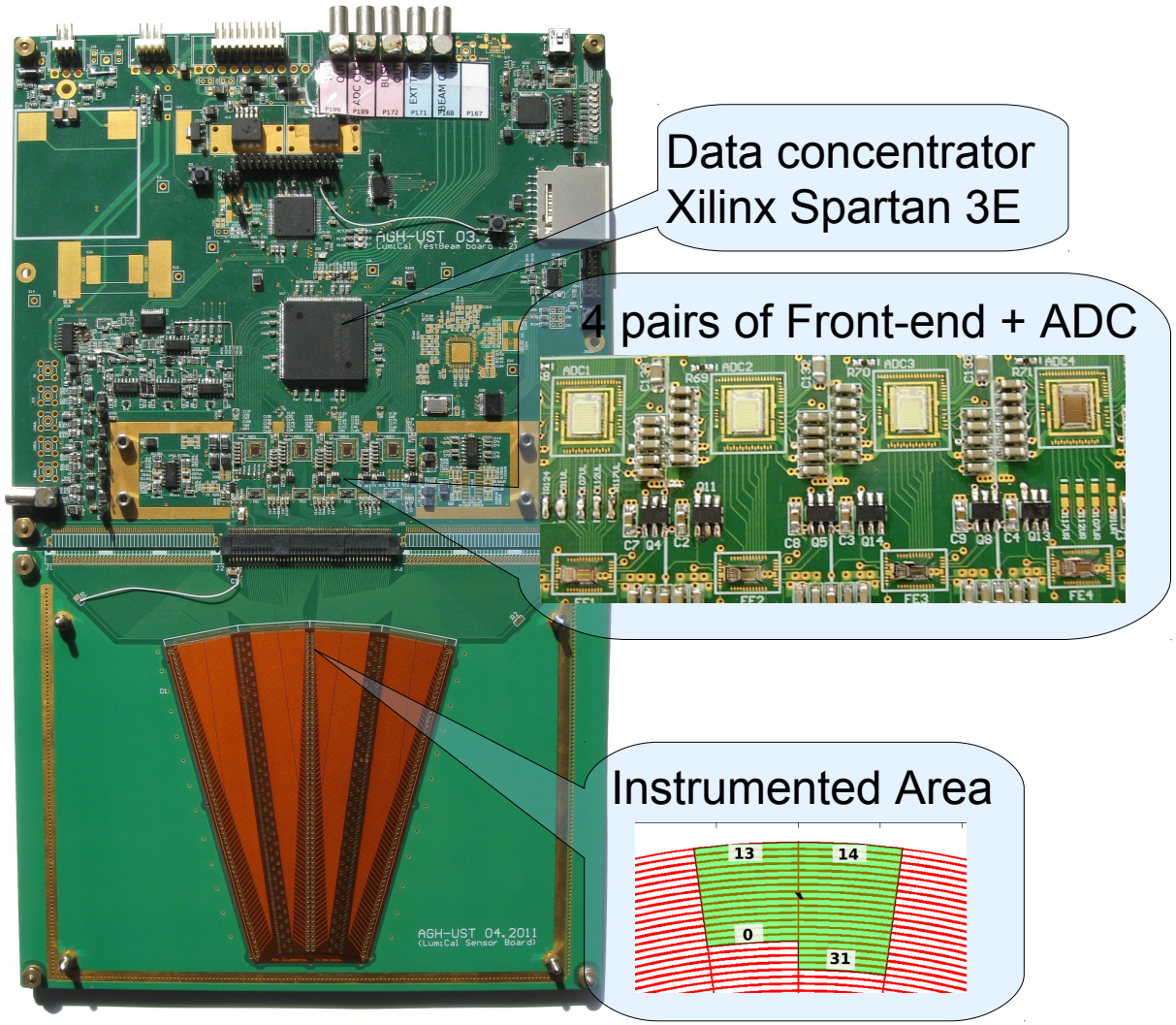
- Design
  - **8 channels** of pipeline ADC
  - **Multimode Digital multiplexer/serializer**
  - **High speed LVDS** drivers (~1GHz)
  - Low power **DAC control references**
  - Precise **BandGap** reference source
  - **Temperature sensor**
- Performance
  - **9.7 ENOB** up to 25 Ms/s (8 channels)
  - Power scales linearly with sampling rate **~1.2mW/channel/MHz**
  - ADC core works up to **50 Ms/s** (1 channel)
  - Gain spread < 0.1 %
  - **Crosstalk < -80dB**
  - **Power pulsing embedded**

ADC ASIC prototype





LumiCal detector module



- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam) ILC mode

Deconvolution for CR-RC shaping

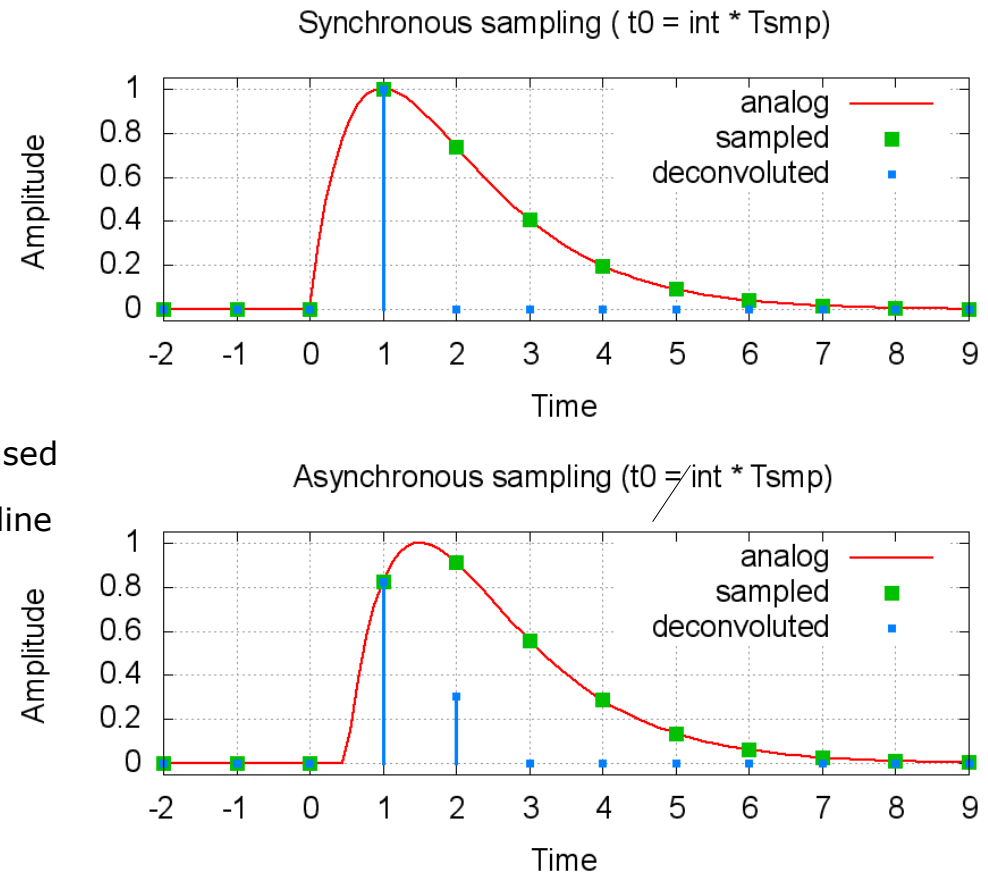
$$d_i = V_i - 2e^{-T/\tau} V_{i-1} + e^{-2T/\tau} V_{i-2}$$

- Only two multiplications and additions (very fast and light !)
- Deconvolution produces non-zero data only when one or two first samples are on baseline, and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples
- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor

} Look Up Tables used; Can be done off-line

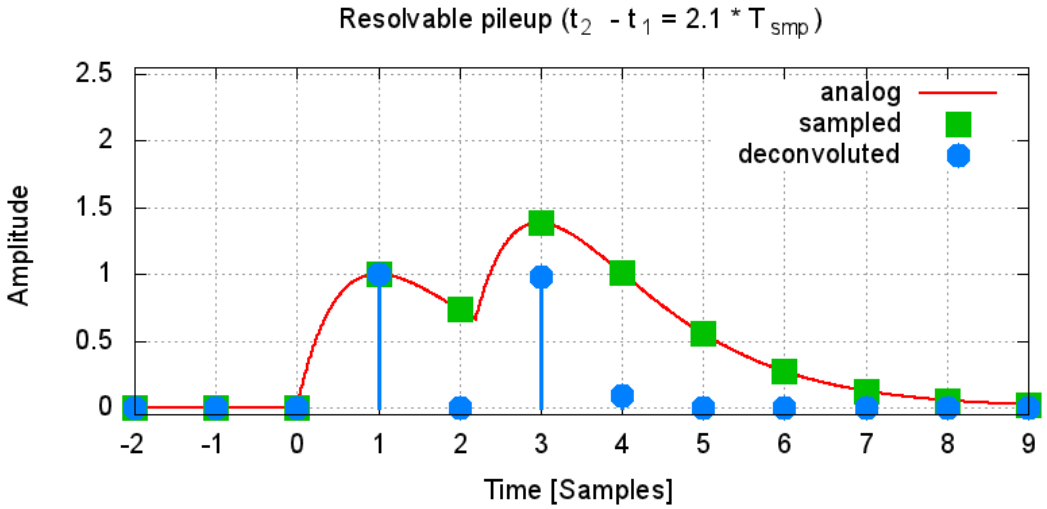
- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non zero samples !

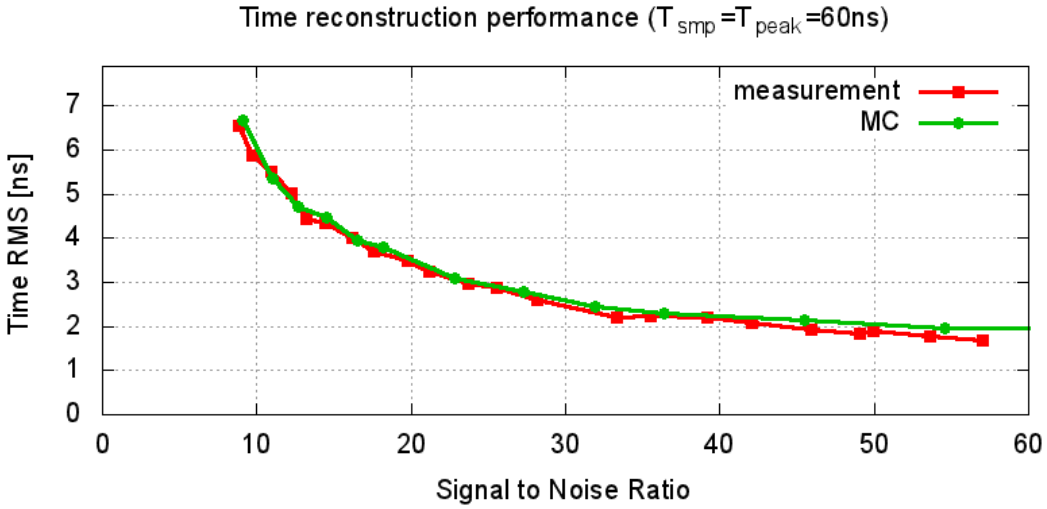
Example : CR-RC, $T_{smp}=T_{peak}=1$, amp =1



CR-RC Deconvolution properties

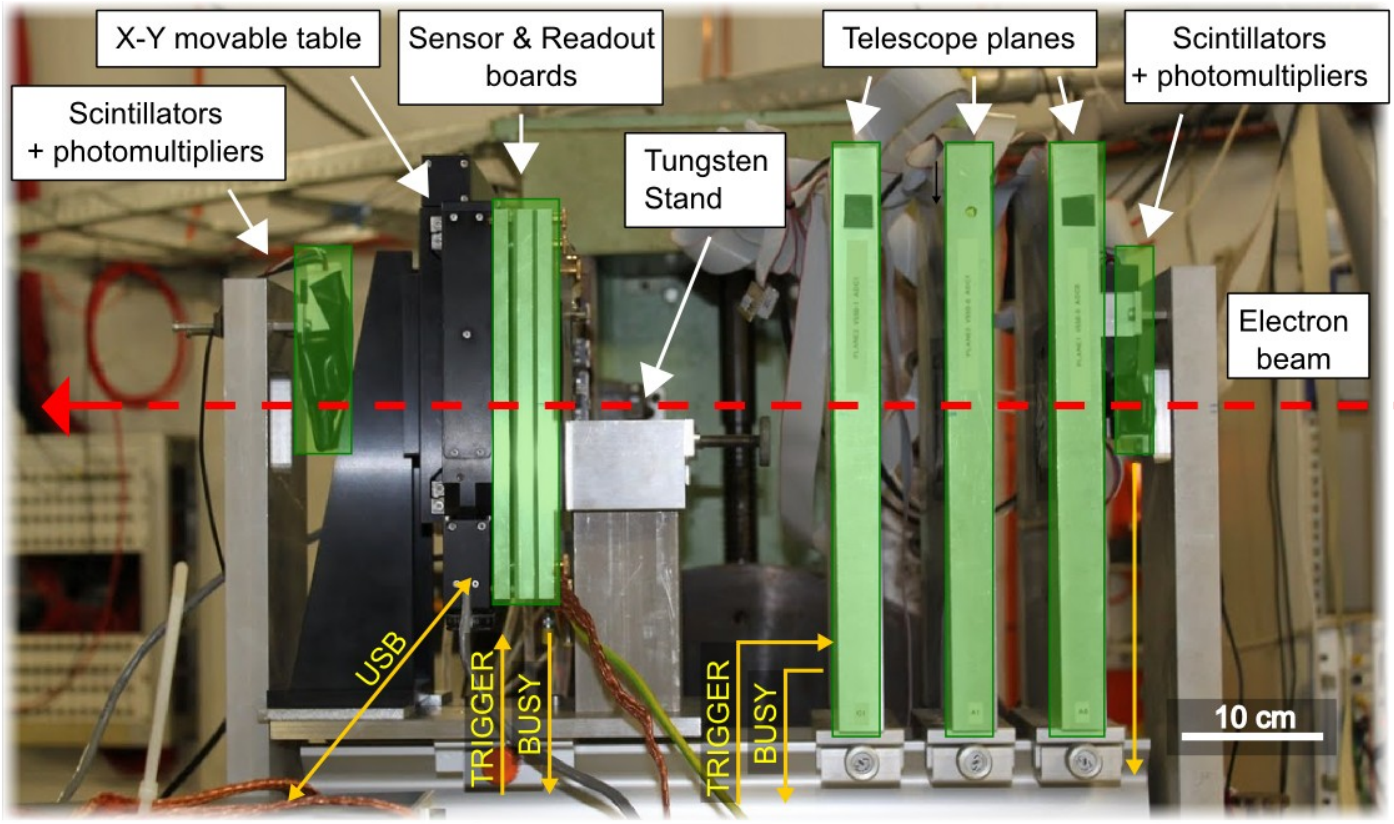
- Two events can be separated and precisely measured if they are distant 2-3 T_{smp}
- For $T_{peak} = T_{smp}$ = 60ns time resolution in range **2-7 ns** is obtained
- Increasing sampling frequency to 25 Msps (T_{smp} = 40ns) time resolution may be reduced down to 2 ns for SNR ~20
- SNR is only slightly deteriorated
- Monte Carlo simulations fits well to measurements

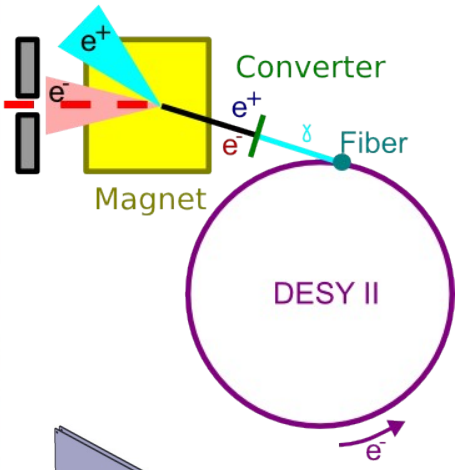


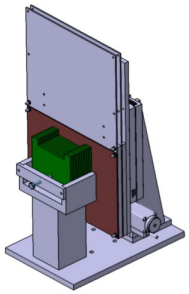


See more : Sz. Kulis, M. Idzik "Study of readout architectures for triggerless high event rate detectors at CLIC" LCD-Note-2011-015

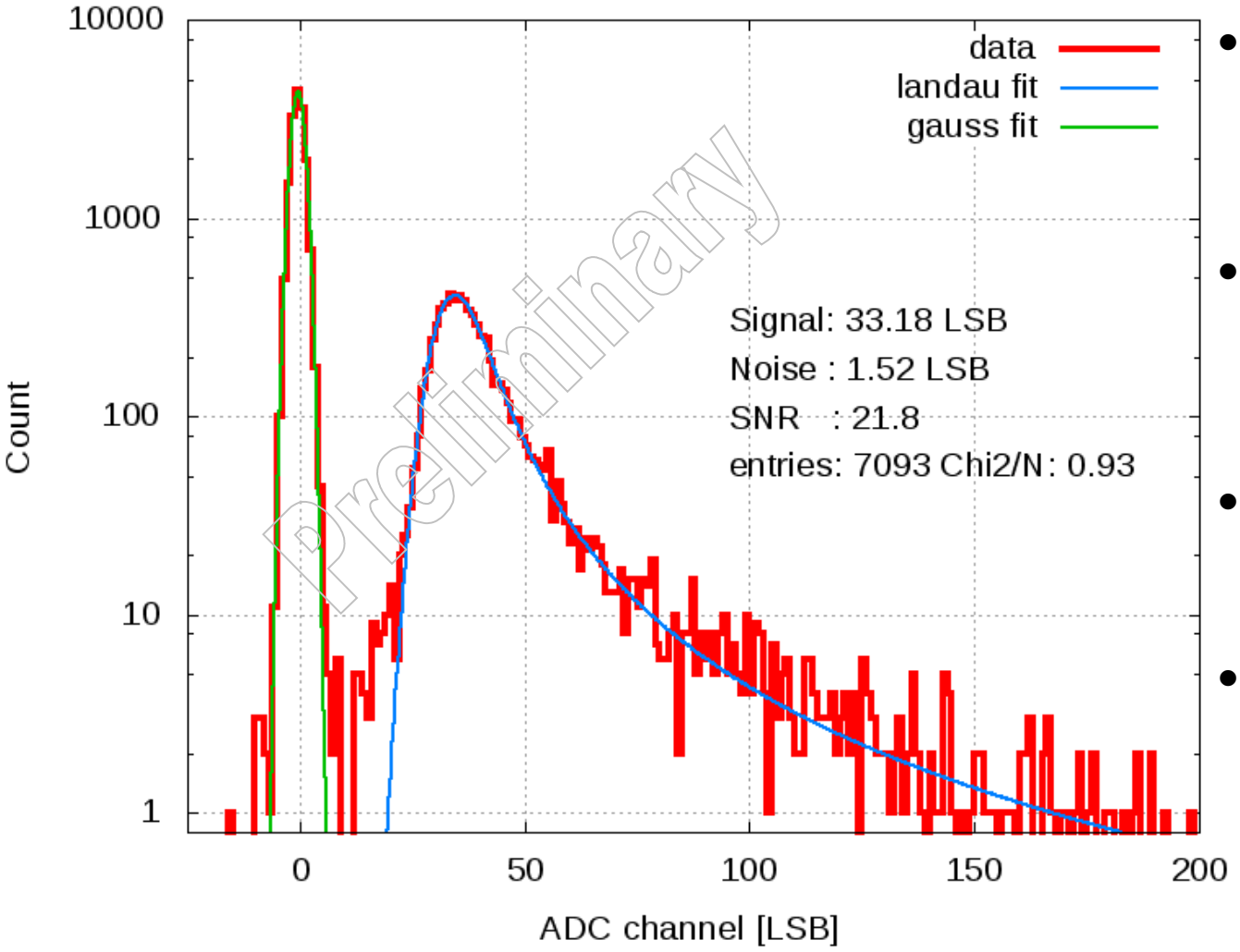
Testbeam Experimental setup





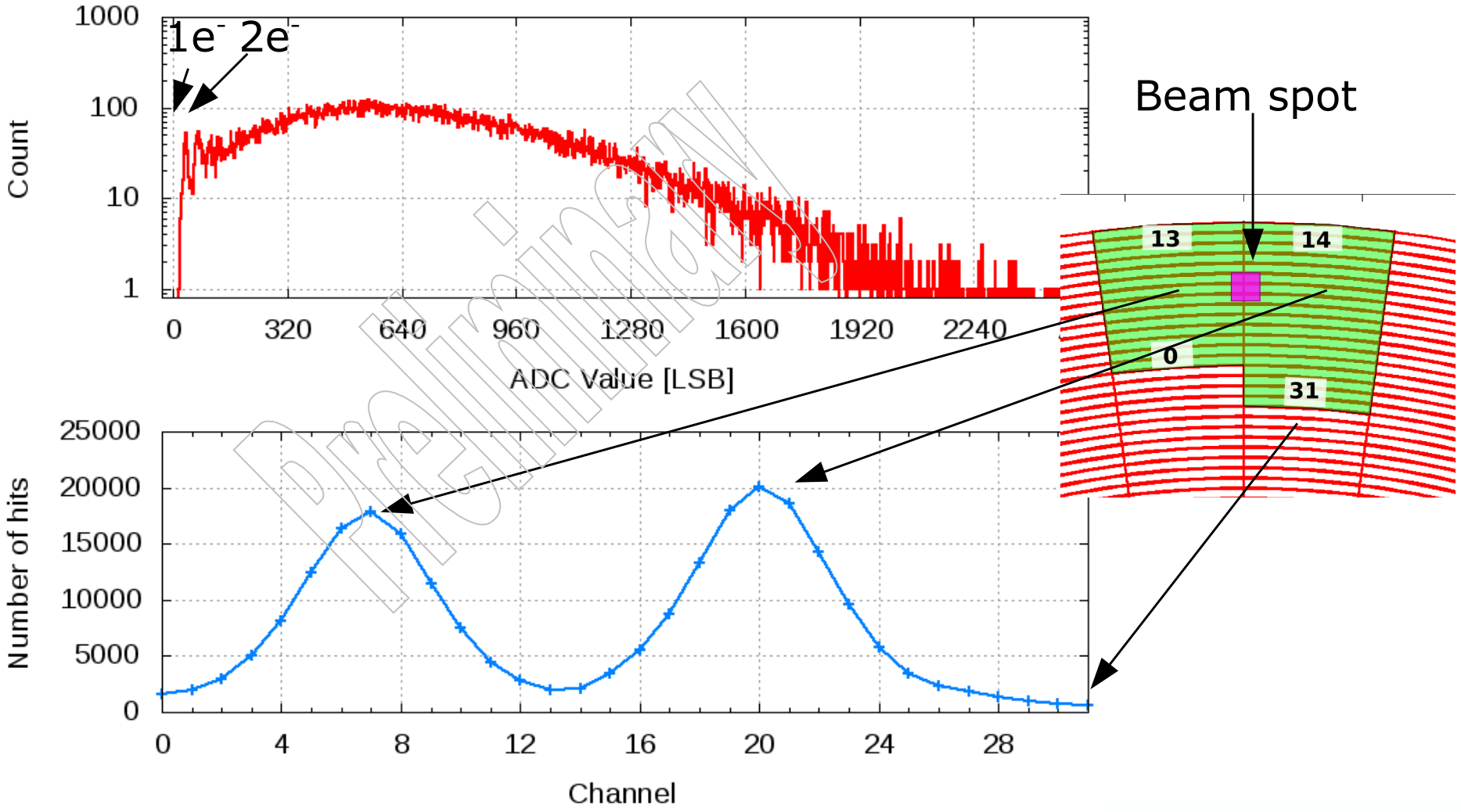


Example spectrum (without tungsten)

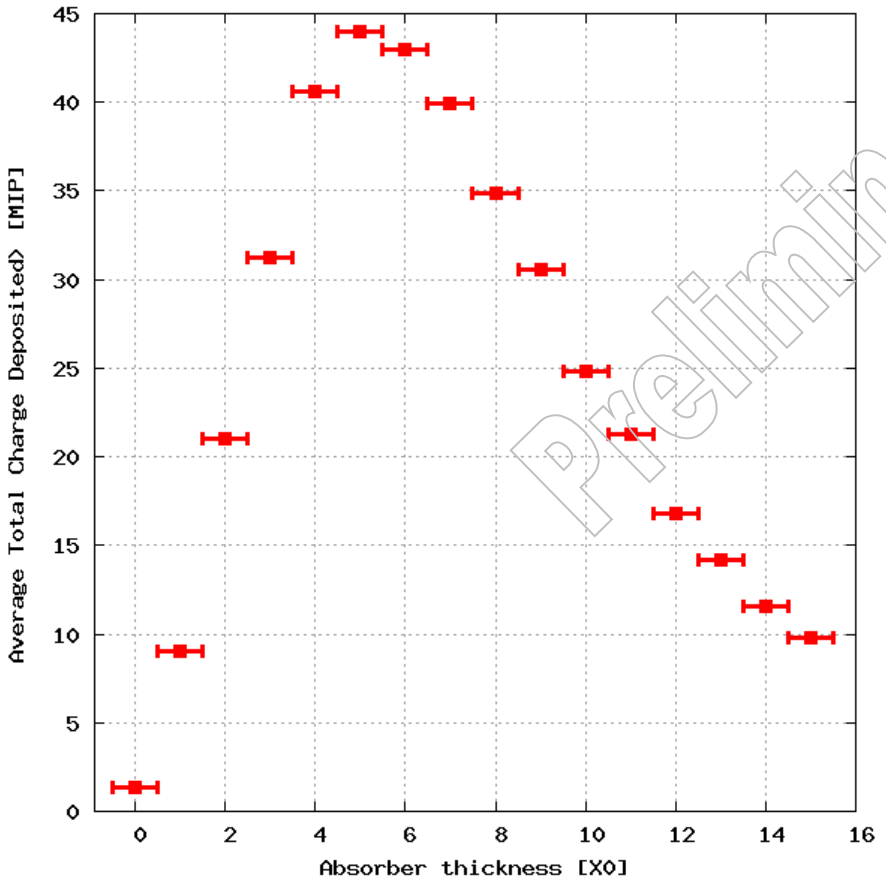


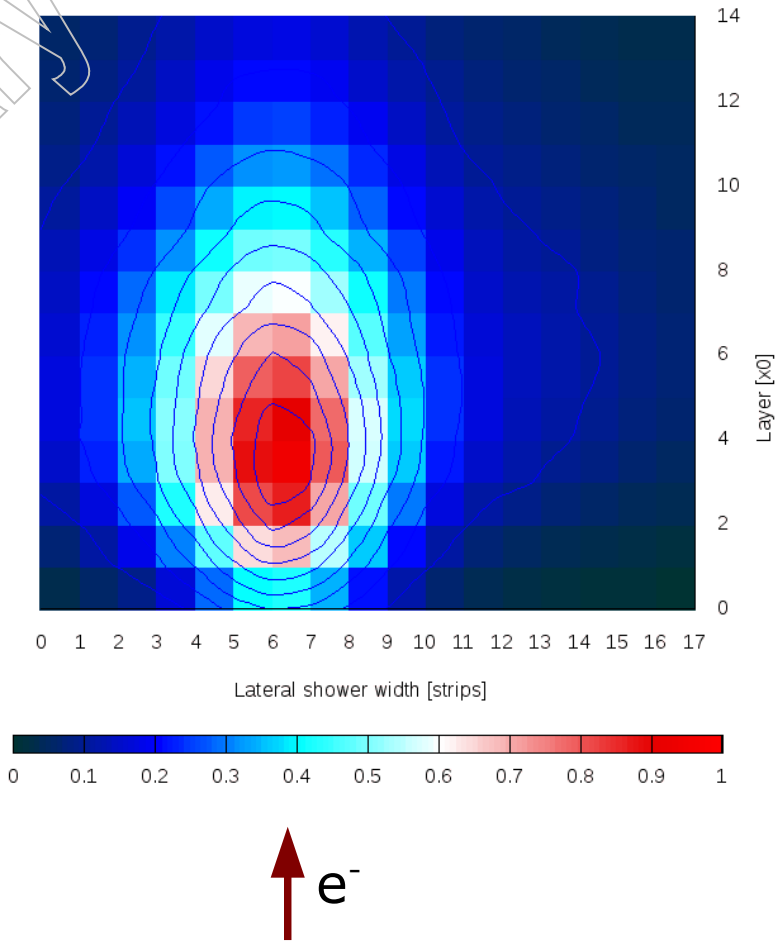
- Events processed using deconvolution algorithm
- Data fit to Landau-Gauss distribution very well
- SNR is above 20 for each channel
- Ratio of events in pedestal and signal peaks is geometry dependent

Shower development (one tungsten plane)

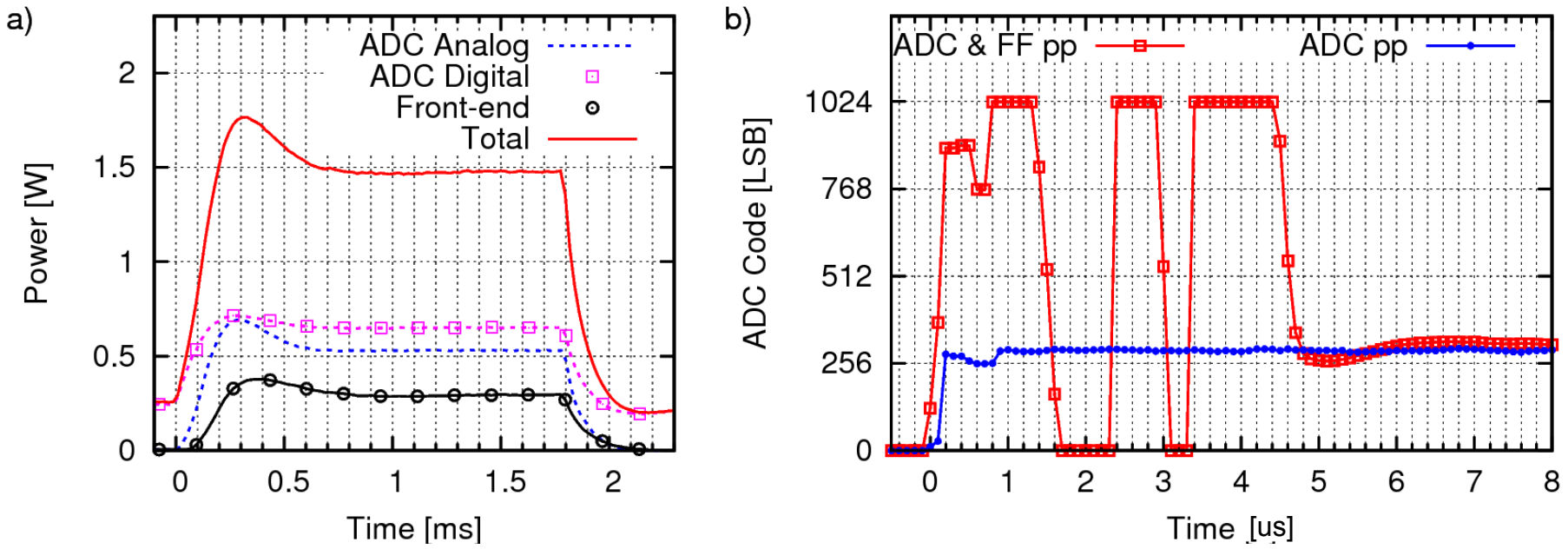


Shower profile





Power pulsing (not during testbeam)



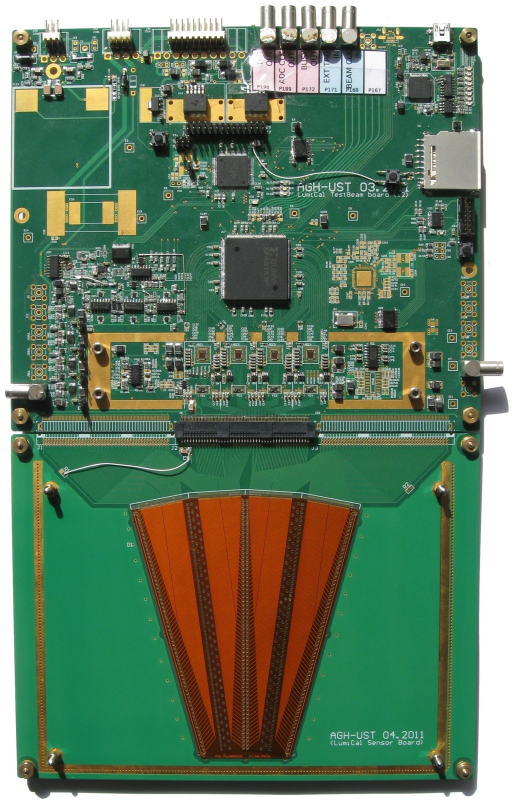
- Monitoring of on board power consumption, separate for front-end and ADC, implemented
- ADC needs < 10 samples to restart correct conversion independent on sampling frequency
- Front-end needs < 7 us to stabilize baseline

Detector Module Summary

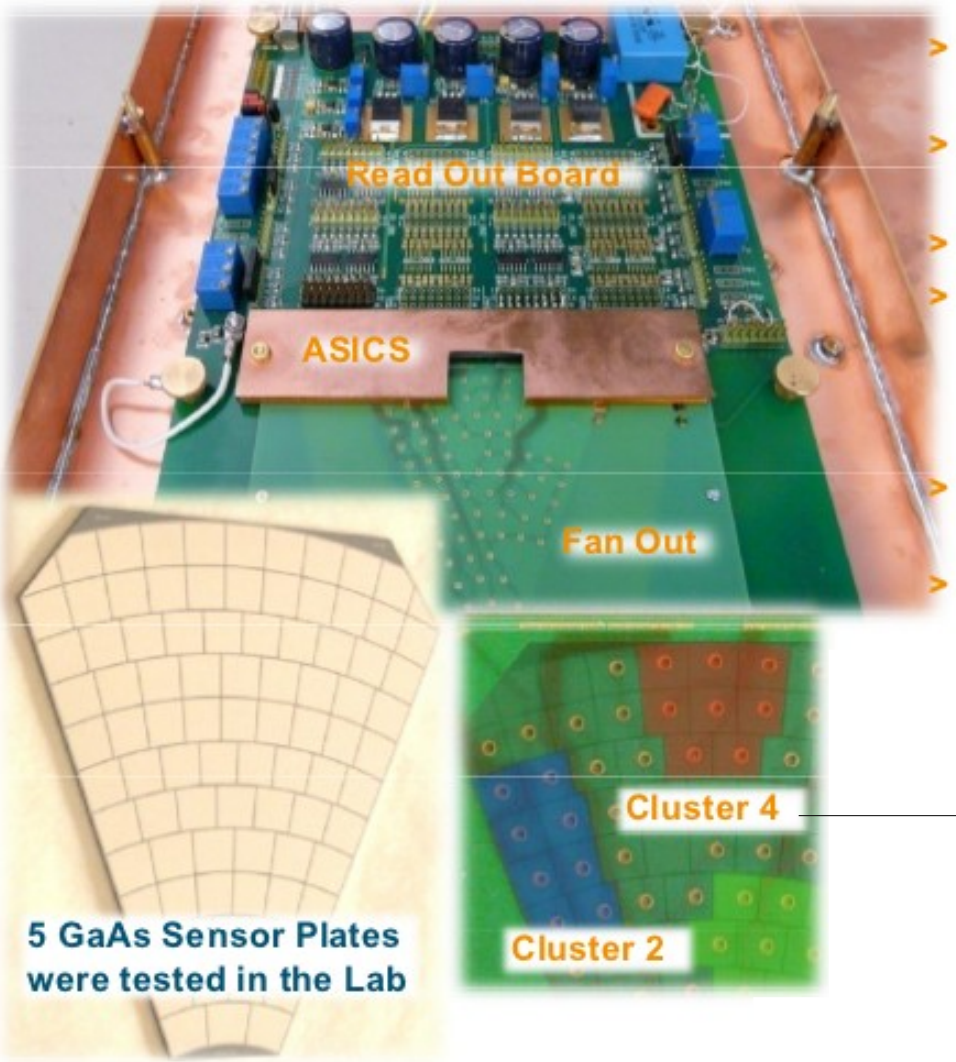
- The testbeam has proven **proper operation of complete multichannel detector module**, comprising front-end, multichannel ADC and FPGA based data concentrator

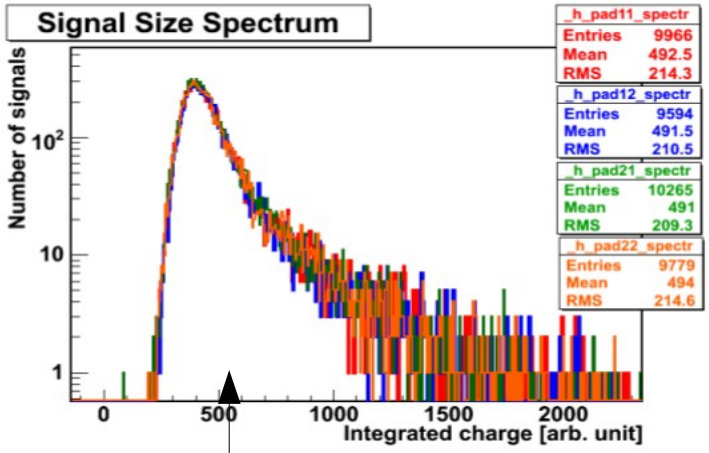
- Precise timing information, good amplitude reconstruction and pileup rejection was obtained using **deconvolution algorithm on CR-RC shaper** (T_{peak}=60ns) digitized at 16 Msps (T_{smp}=60ns)

- **Power pulsing** feature was **verified**, Less than 10 us needed to restart ASICs operation

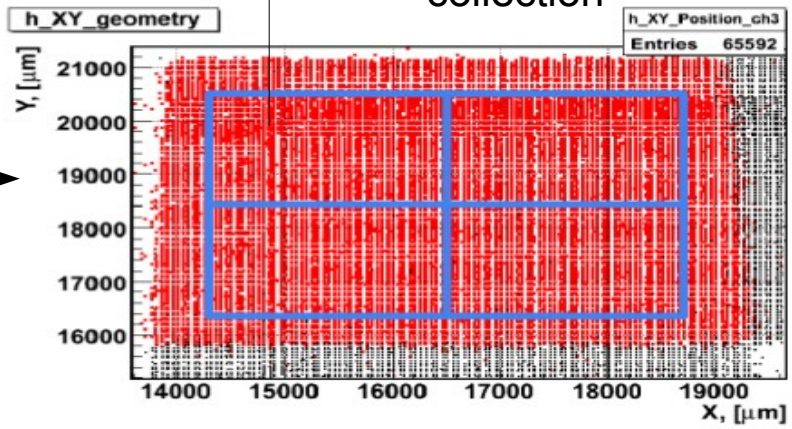


BeamCal TestBeam





4 independent pad areas show identical charge collection



Future plans

- The **developed multichannel readout system** will be extensively used in test beams and laboratory studies for ILC/CLIC. It should be integrated to **Flexible Mechanical Infrastructure** being developed. The readout should be integrated to Common DAQ.
- Continue studies of **asynchronous readout for CLIC**
- For **LumiCal readout** no further ASIC development in AMS 0.35um CMOS foreseen. The main reason is that for final ILC/CLIC detecting system the power consumption and radiation hardness may be not satisfactory with present technology.
- The good choice for future technology seems IBM 130nm CMOS, new FE and ADC need to be designed
  - ADC : 10 bits Successive Approximation architecture, sampling up to 50Ms/s , power consumption <2mW, is underway. We hope to submit it still in 2011.
  - Front-End: there are more questions, design has been started but goes more slowly, submission expected 2011-2012.