DEPFET Prototypes

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DEPFET collaboration

www.depfet.org

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- **Ramon Llull University**
- Bonn University
- Heidelberg University
- Goettingen University
- Karlsruhe University
- IFJ PAN, Krakow
- MPI Munich
- Charles University, Prague
- **IGFAE, Santiago de Compostela University**
- **IFIC, CSIC-UVEG, Valencia**
- University of Giessen

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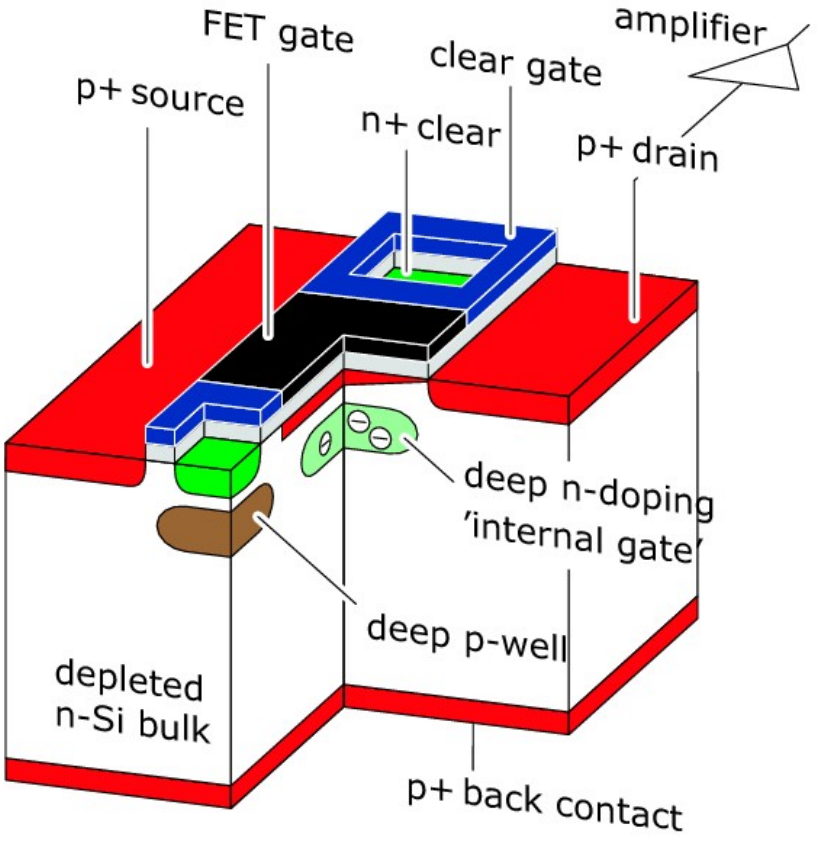
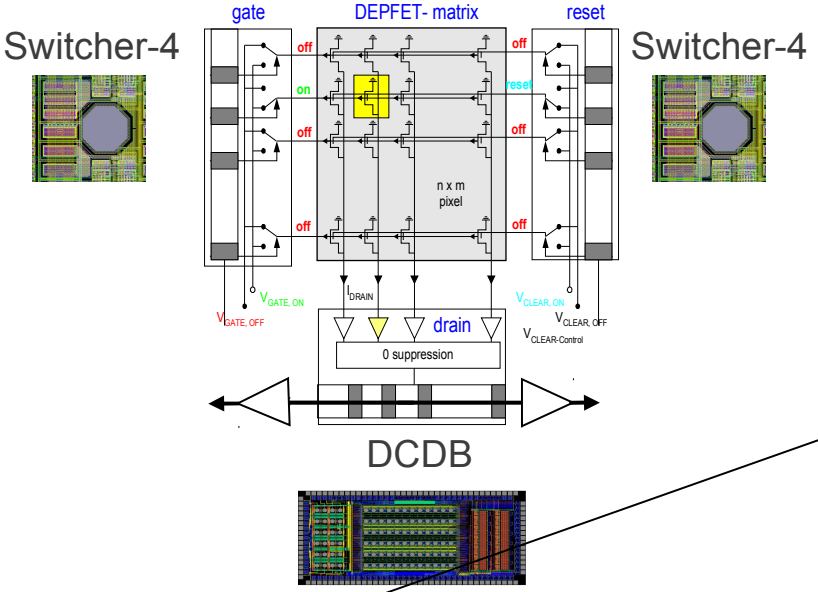
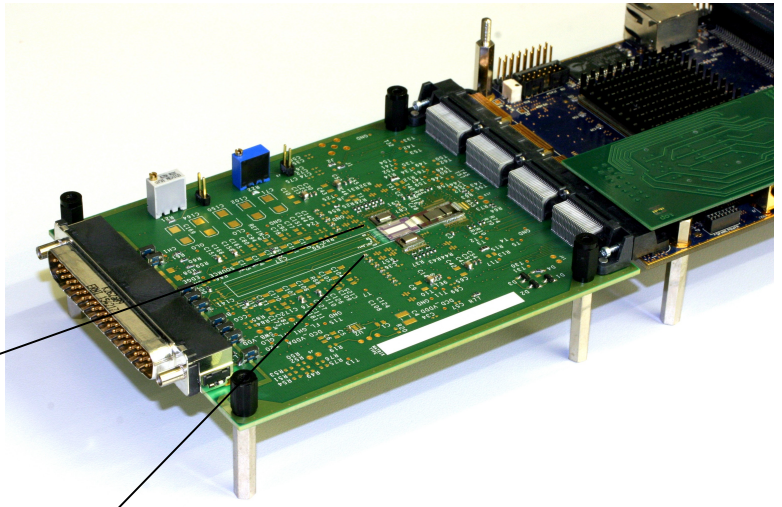
Introduction: Operation principles & features

- DEPFET is an active pixel detector:
  - Each pixel is a p-channel FET on a completely depleted bulk.
  - A deep n-implant creates a potential minimum for electrons under the gate (internal gate).
  - Signal electrons accumulate in the internal gate and modulate the transistor current (~300-600pA/e^-).
  - Accumulated charge can be removed by a clear pulse.
- Features:
  - Internal amplification.
  - Large SNR.
  - Thin detector ~ 50µm.
  - Good spatial resolution.
  - Low power consumption, only read out one row at time. Rolling shutter readout scheme.
  - Readout channels integrated over the detector. Chips laying on lateral balcony.

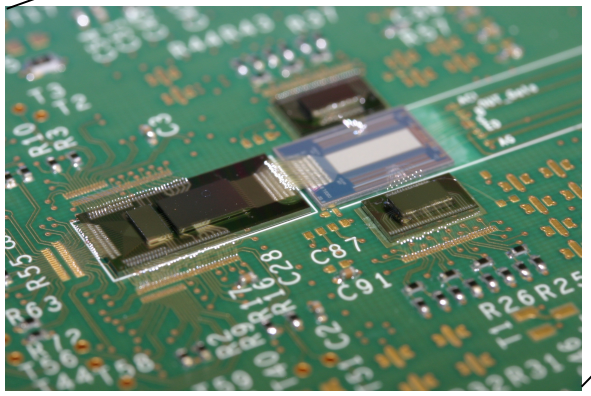


Introduction: Matrix & Prototype





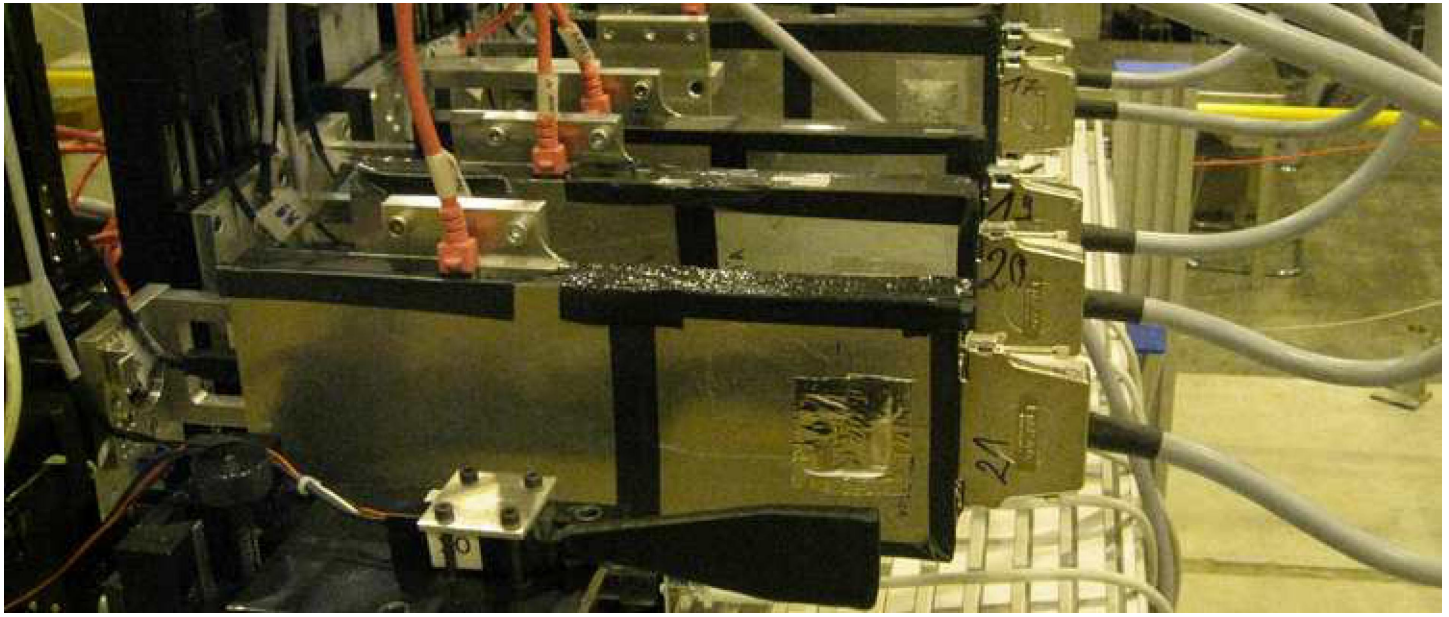
See Laci Andricek talk in this sesion



PXD5+DCDB prototype

- A 2D array of DEPFET forms a pixel detector with exellent position sensitivity.
- A readout module is created by mounting a sensor and several auxiliary chips on a board.

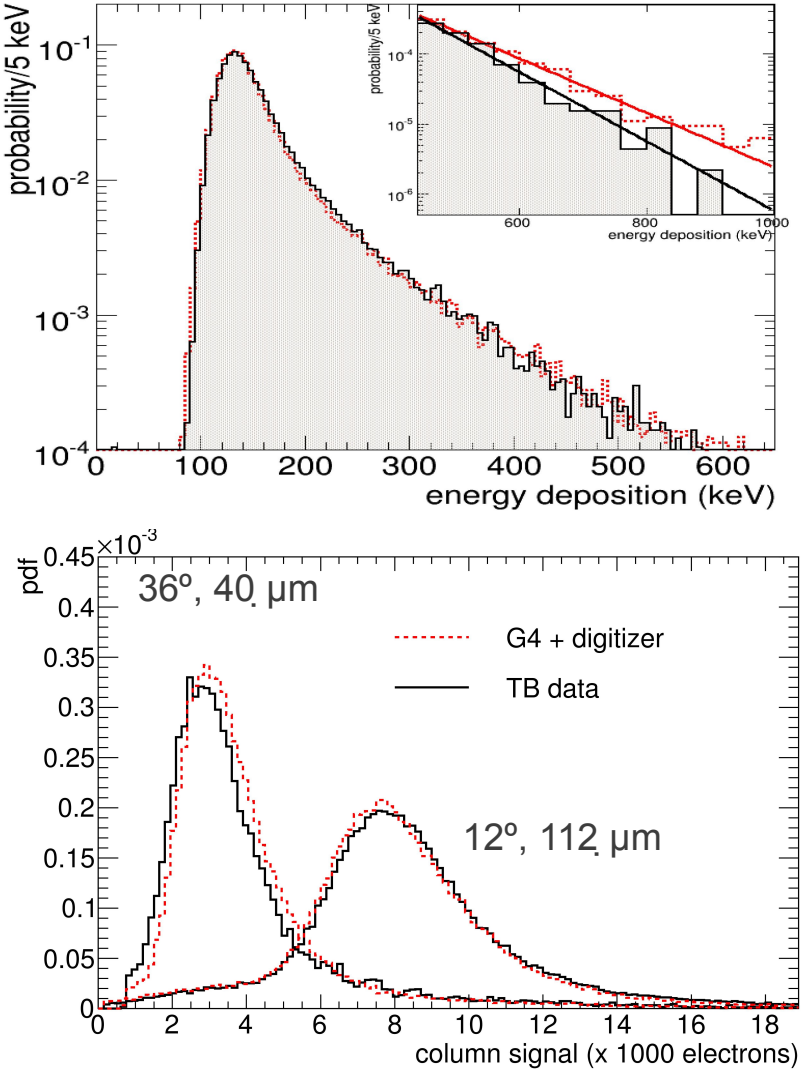
Beam Test



- Beam Tests with ILC geometry detector have confirmed the DEPFET characteristics.

Beam Test results

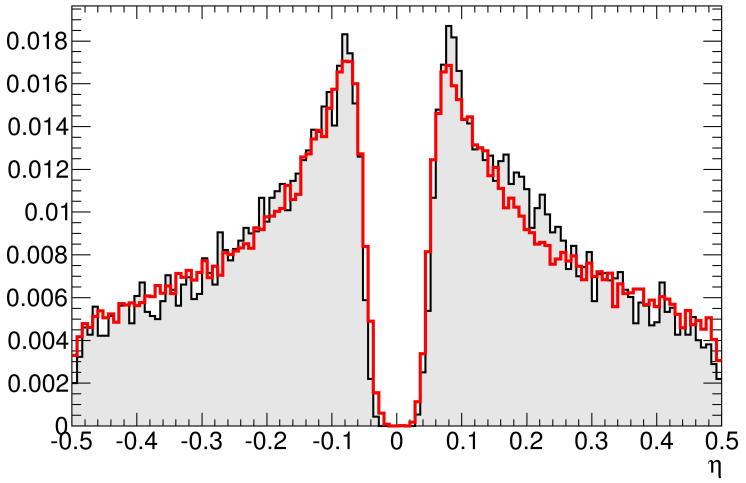
- Tests of DEPFET prototypes devices
- Validation of fast DEPFET simulation
- Response to minimum ionizing particle, performed at CERN SPS:
  - Use most probable signal to extract $g_q=\Delta I_D/Q$
  - 6 μm gate length→~300pA/e^-
  - 5 μm gate length→~650pA/e^-
  - Resolution ~1μm for 20x20 μm^2 pitch and 450 μm thick.
- Using information of one column we can predict the charge distribution for thin sensor.
- New prototypes thinned down to 50μm thickness tested (Beam Test next week in CERN SPS).



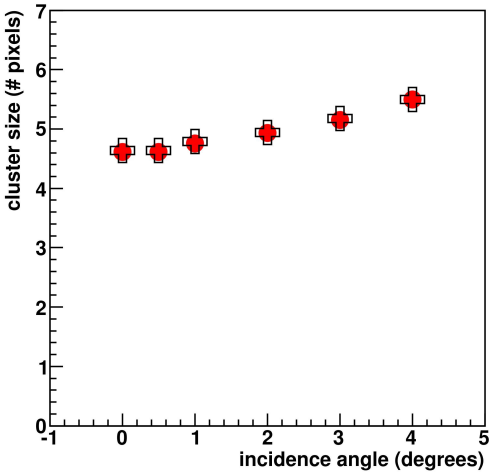
The column signal distribution from TB data (black continuous line) and MC (red dashed line) for incidence angles of 12º and 36º with respect to the perpendicular correspond to a sensor thickness of 112 μm and 40 μm, respectively

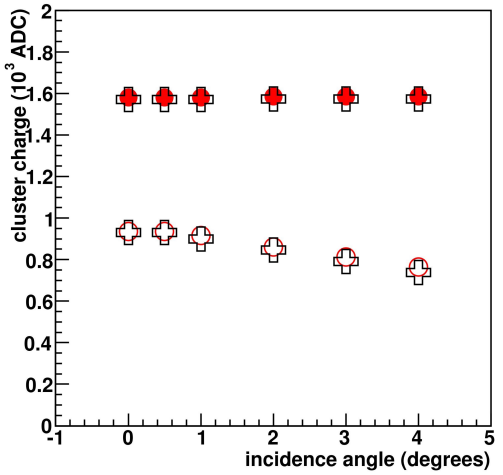
TDR Belle-II

Beam Test Results



Comparison of measured beam test data (black) to the prediction of the digitizer (red). The η distribution.



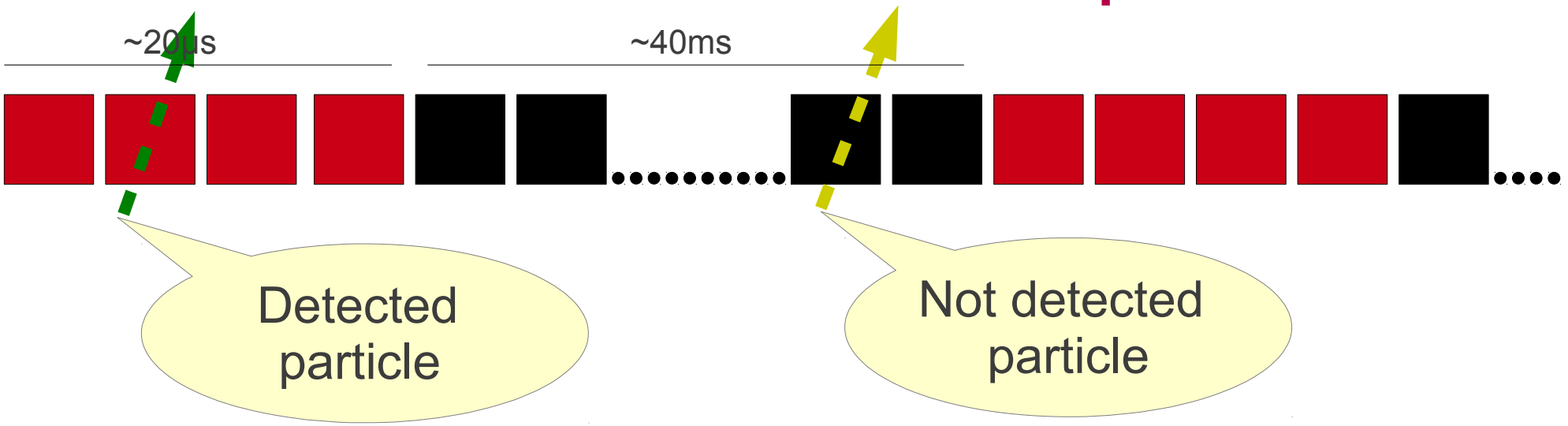


Left: cluster size vs. incidence angle. Right: seed (open circles) and cluster signal (filled circles) vs. incidence angle. The cross markers correspond to the result of a MC model.

TDR Belle-II

- Charge sharing between DEPFET pixels is understood.

Trailing Frames: modificated readout sequence



- Trailing Frames are a modificated readout sequence in which the information from four consecutive readout frames of the matrix can be saved (implemented in the DAQ by Sergey Furletov and his team in the test beam of 2010).
- This readout mode allows to measure the efficiency with which signal is removed under different circumstances.
- The matrix is doing its reading sequence continuously.
- Red squares represent the four consecutive frames where we see the matrix information.
- Black squares represent the frames that we don't see.

Trailing Frames: Source data analysis

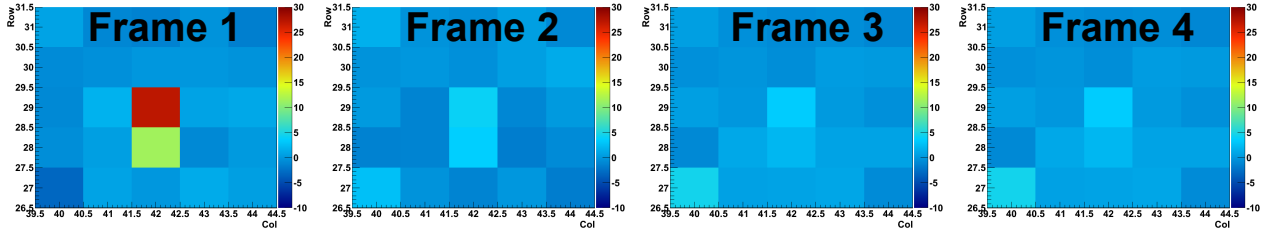
- Measures taken with ^{109}Cd source at MPI by Christian Koffmane.
- We define $V_{CL}^{eff} = V_{CL}^{Hi} - V_{CL}^{Lo}$, such quantity is a crucial voltage for the clear performance.
- Clear voltage scan: all voltages are referred to source.

Date	Run	CCG(V)	ClearHi(V)	ClearLo(V)	GateLo(V)
15/2/2011	2072	-1.5	18	2.5	-3.65
28/4/2011	3007	-1.5	17	2.5	-3.65
28/4/2011	3008	-1.5	15	2.5	-3.65
28/4/2011	3009	-1.5	13	2.5	-3.65
28/4/2011	3011	-1.5	22.5	2.5	-3.65
28/4/2011	3012	-1.5	20.5	2.5	-3.65
28/4/2011	3013	-1.5	24.5	2.5	-3.65

Trailing Frames: examples

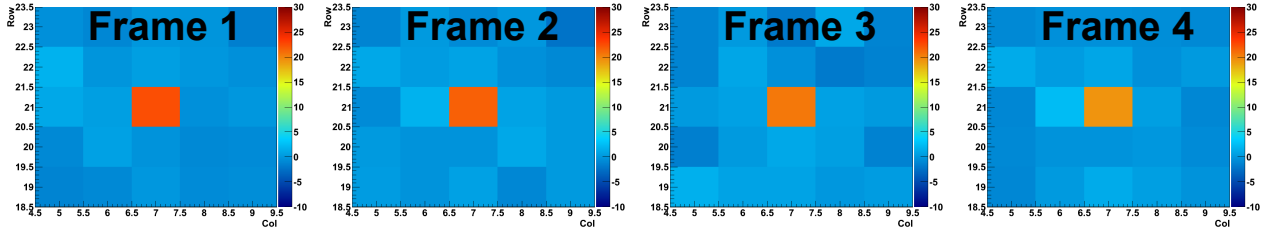
ADC counts after common mode and pedestal correction for four consecutive frames.

Run 2072 $V_{CL}^{eff} = 15.5\,V$



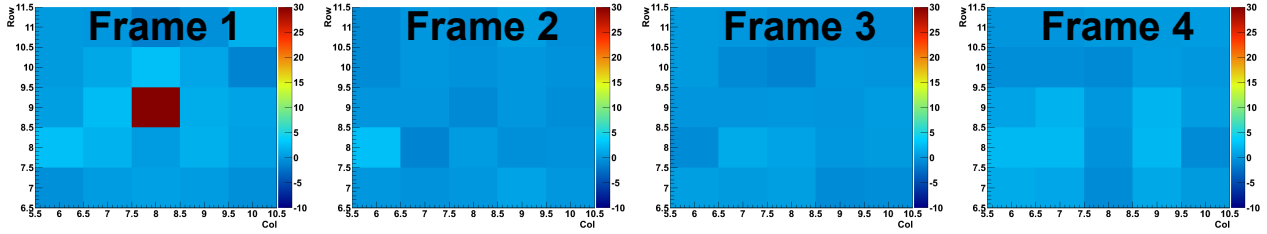
- A faint ”shadow” of the signal is visible after clear pulse.

Run 3009 $V_{CL}^{eff} = 10.5\,V$



- For low clear voltage, the signal remains large in multiple frames.
- # Clusters increases strongly when V_{CL}^{eff} diminishes. As the clear is inefficient we see the same cluster more than once.

Run 3013 $V_{CL}^{eff} = 22\,V$



- Raising the clear voltage, a complete clear is achieved.

Clear Performance: Clear Efficiency

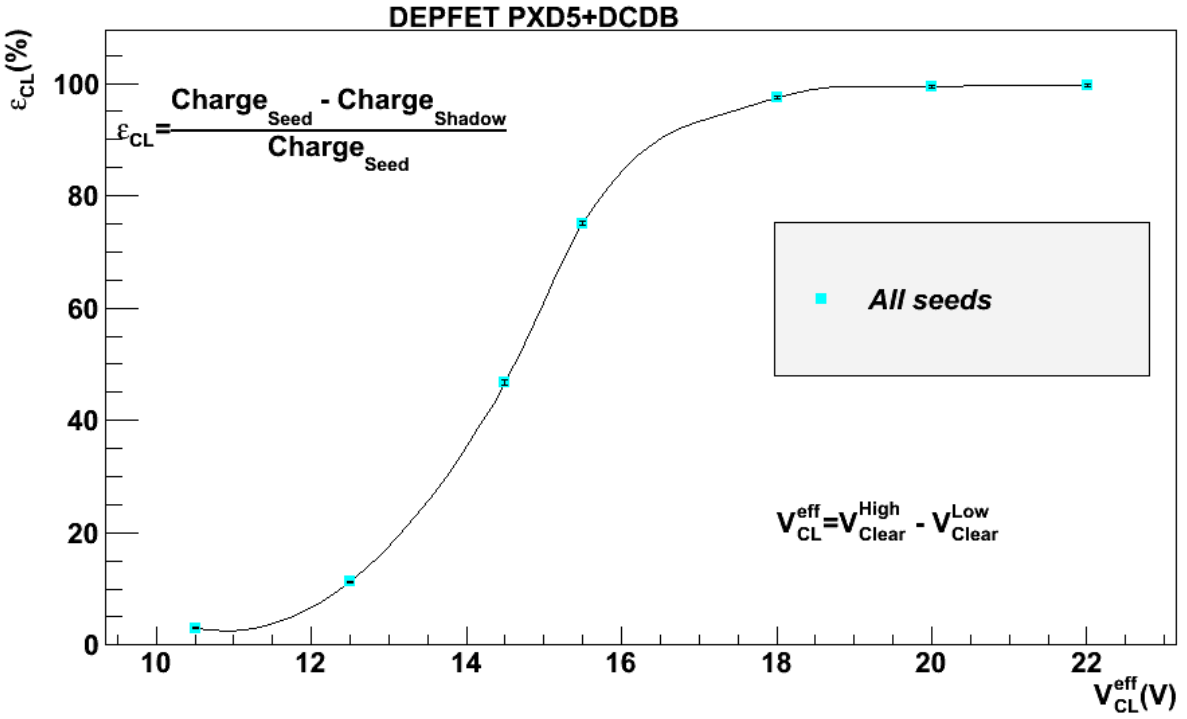
- We measure the clear efficiency by comparing the charge on the seed pixel of the cluster, Q_0^{seed}, and the charge in the same pixel after applying the clear pulse, Q_f^{seed}.
- To quantify the clear performance in a single figure of merit the clear efficiency, ε_{CL}, has been defined as:

$$\varepsilon_{CL}(\%) = \frac{Q_0^{seed} - Q_f^{seed}}{Q_0^{seed}} \cdot 100$$

- Measurements of this quantity under different circumstances and their corresponding analysis are presented below.

Clear Performance: results

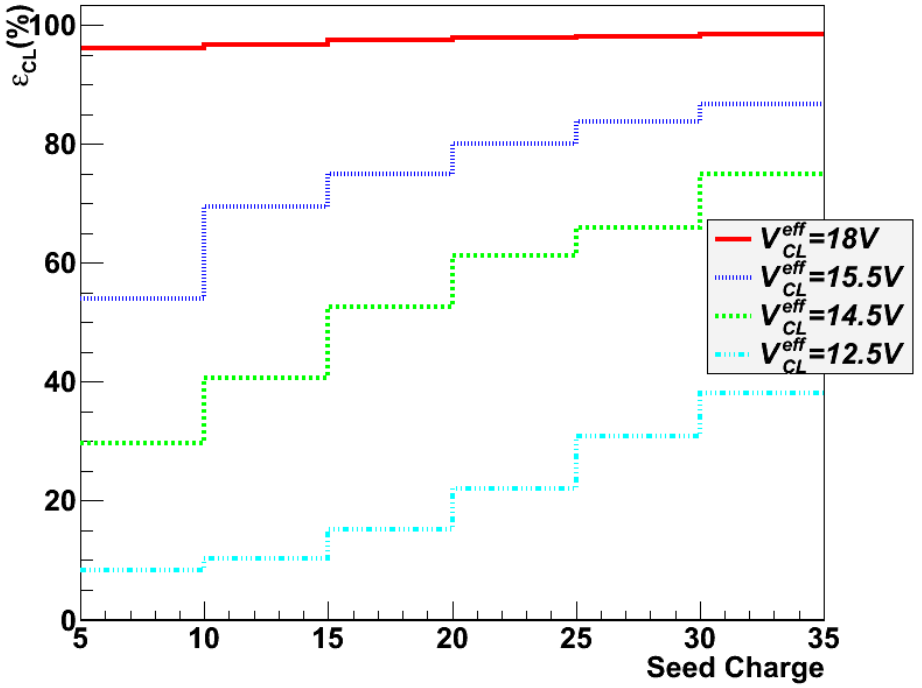
- The average clear efficiency as function of effective clear voltage increases strongly between 12 and 18 Volts. A *plateau* of 100% is reached at approximately 20V.



Clear efficiency as function of the effective clear voltage

Clear Performance: results

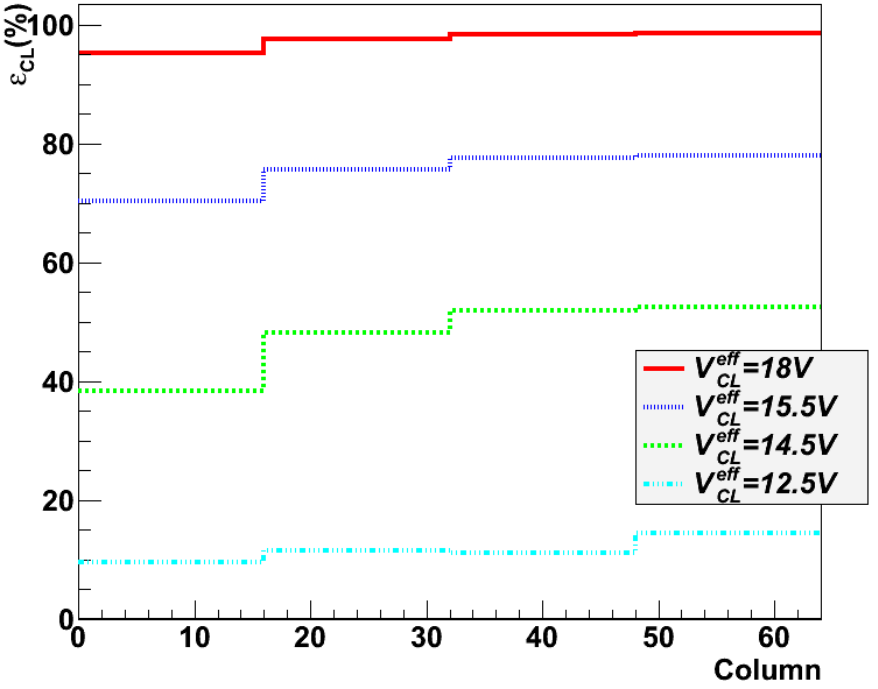
- Clear efficiency depends on the amount of charge accumulated in the internal gate. For intermediate voltages this dependence is more pronunciated. Qualitatively this can be understood as due to the repulsion of charge carriers.



Clear efficiency as function of the accumulated charge in the internal gate for different voltages.

Clear Performance: results

- There is a small, but significant dependence of the clear efficiency with the column number. The clear pulse is most effective for columns close to the switcher generating the clear pulse. As the clear pulse propagates over the line which carries from one side of the matrix to the other the pulse height is degraded (that explanation has to be confirmed by detailed simulations).



Clear efficiency as function of the distance to the switcher generating the clear pulse for different voltages.

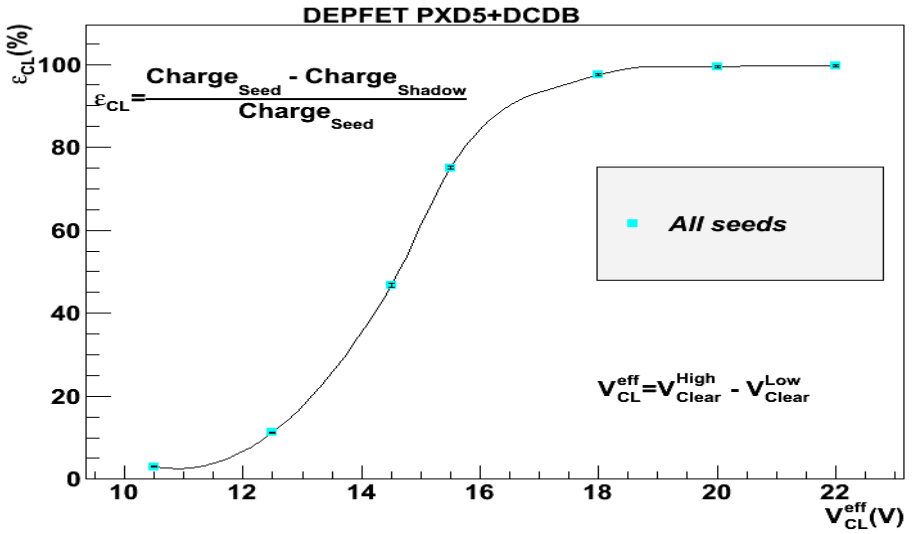
Conclusions

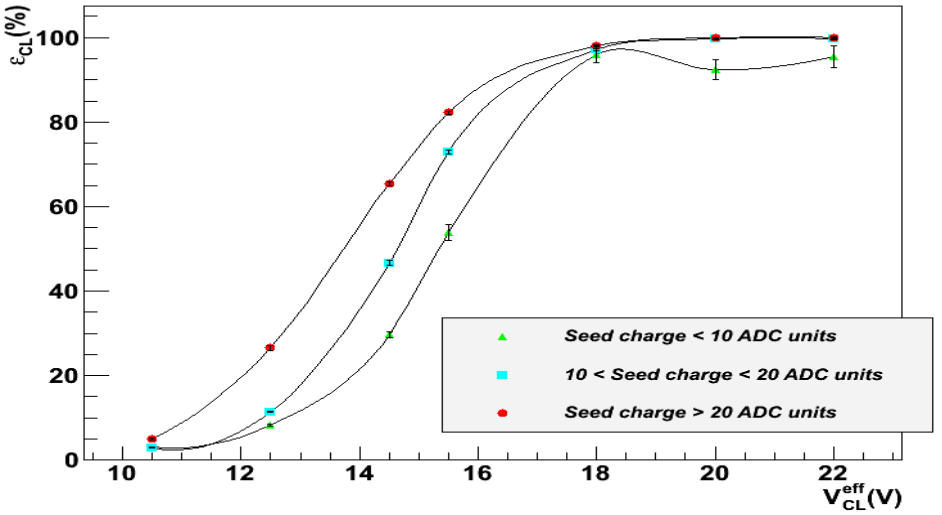
- DEPFET technology allows to build very thin detectors with high spatial resolution.
- DEPFET (ILC design) performance has been measured in Beam Tests. Program to continue in October 2011 with thin sensor devices.
- We have developed a new method to study the clear efficiency of DEPFET readout prototypes.
- We have measured a dependence on the effective clear voltage, the amount of charge accumulated in the internal gate and the distance to the clear switcher for the clear performance.

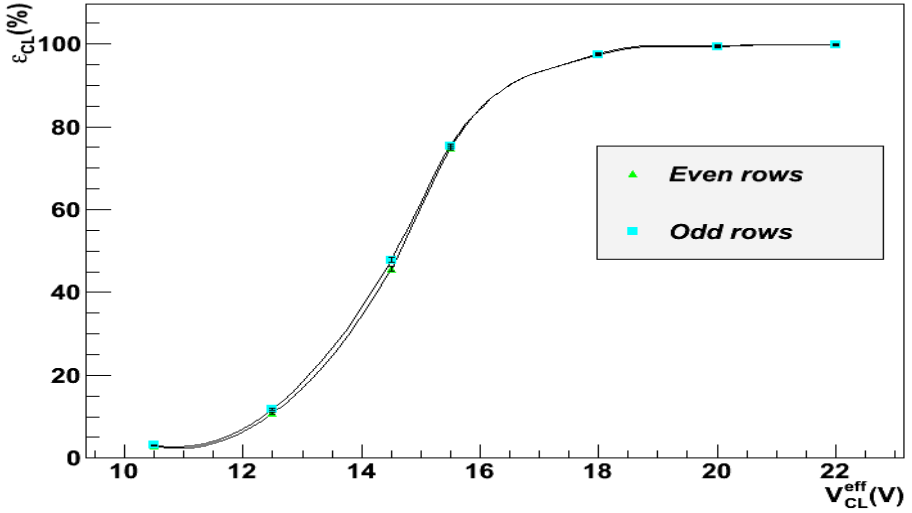
Thank you!

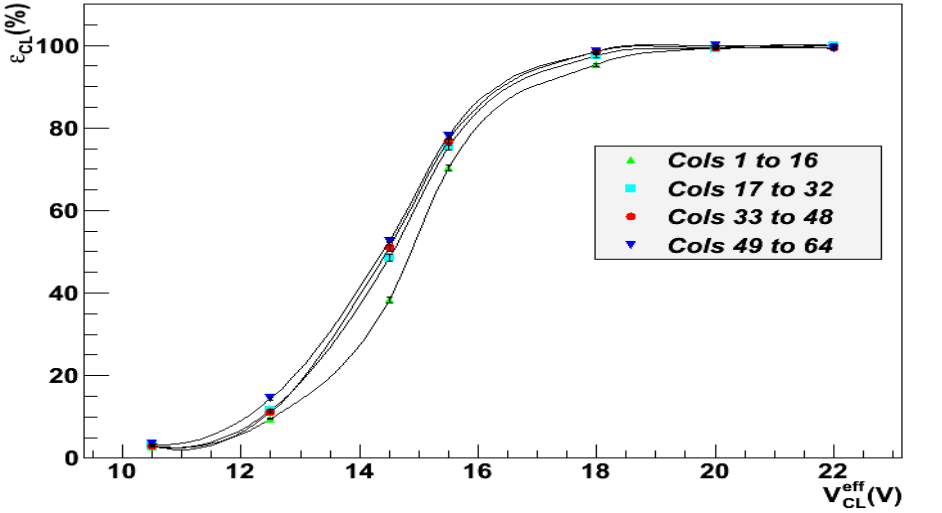
Back Up Slides

Clear Efficiency







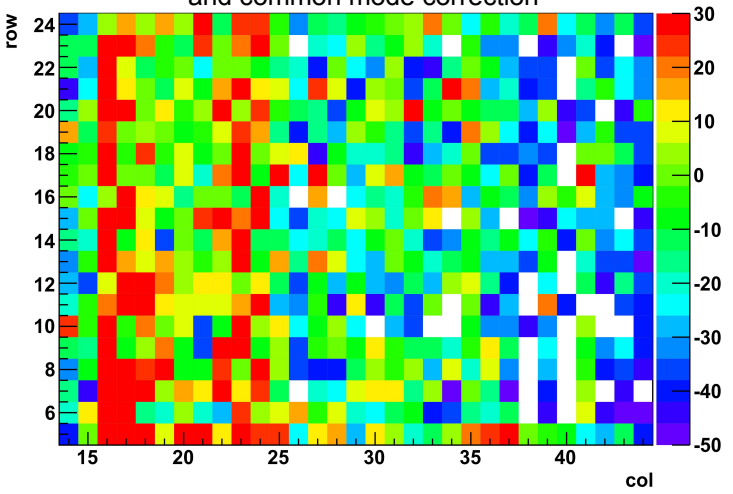


DEPFET: Extracting data from DEPFET

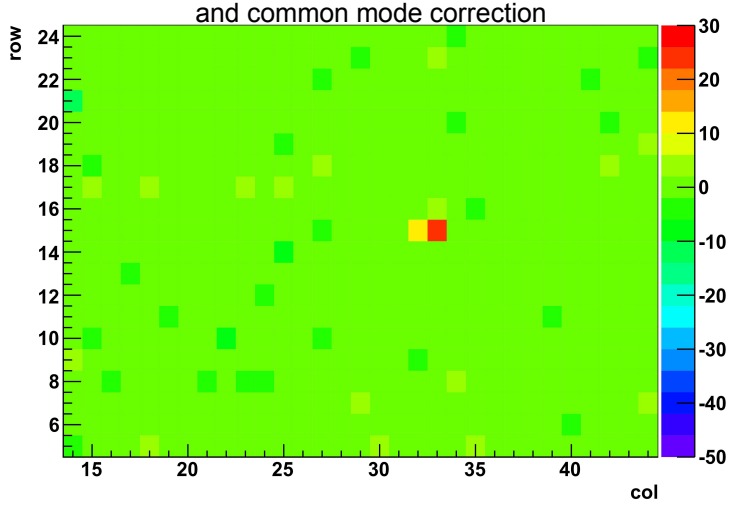
- Drain current when no charge is accumulated in the internal gate: pedestal, i_{ped}.
- Standard deviation of i_{ped}: noise, σ.
- A correction is applied that subtracts noise common for each row, i_{com}.
- The signal, i_{sig}, measured is then: $i_{sig} = i_{drain} - i_{ped} - i_{com}$
- If $i_{sig} > 10 \cdot \sigma$ we have a physical sign (only required for cluster seed).
- A neighbouring pixel is added to the cluster if $i_{sig} > 2.6 \cdot \sigma$
- The SNR of the total cluster has to be > 12.

ADC counts ploted in a 2D Histogram

Fragment of the matrix before pedestal and common mode correction

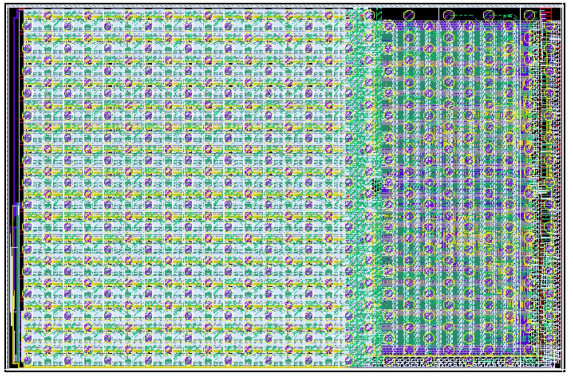


Fragment of the matrix after pedestal and common mode correction

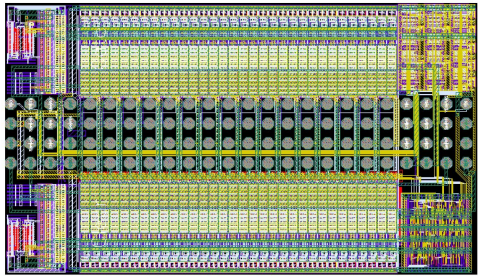


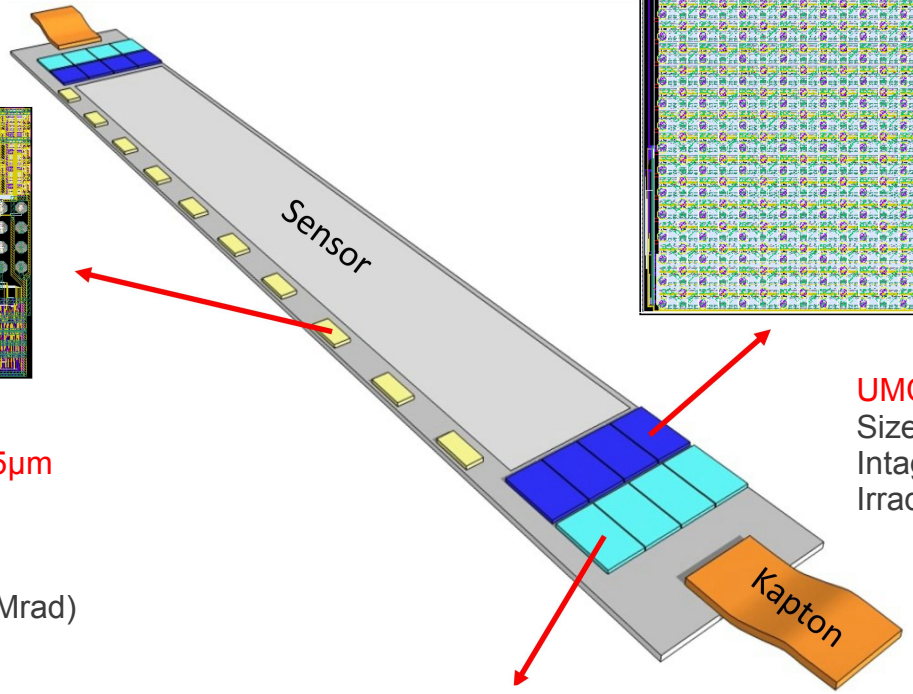
VXD ladder & Auxiliary Chips

DCDB (Drain Current Digitizer for BelleII)
Analog frontend and ADC



SwitcherB
Row control

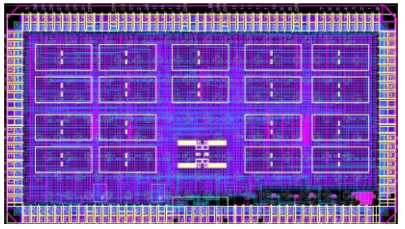




UMC 180 nm
Size 3.3x5.0mm^2
Intagrated ADC
Irradiation up to 7Mrad

AMS high voltage 0.35µm
Size 3.6x2.1 mm2
Clear and Gate signal
Fast HV up to 30V
Rad. Hard proven (36Mrad)

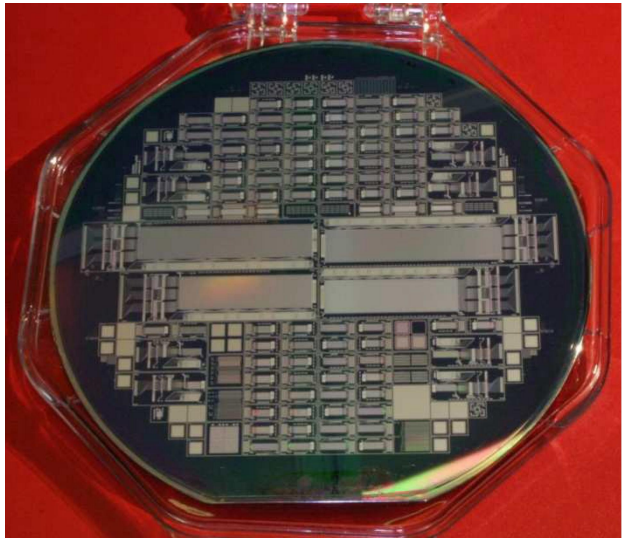
DHP (Data Handling Processor)
Data reduction and Processing

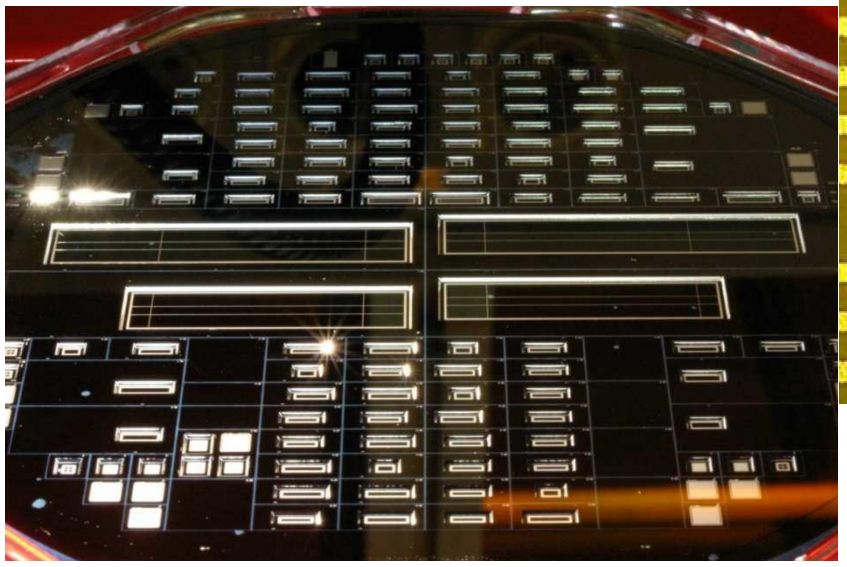


IBM CMOS → TSMC (65nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppresion)
Timing signal generation

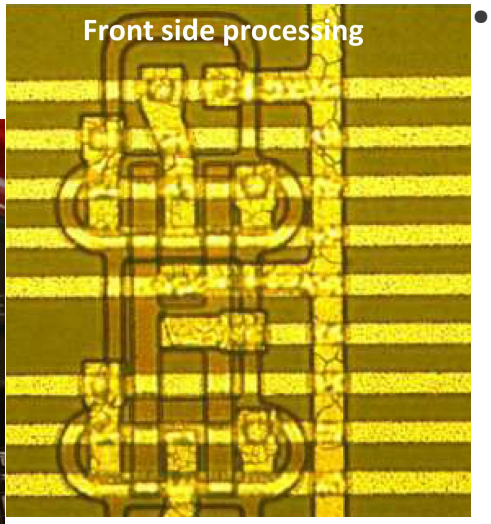
Switcher, DCD: Heidelberg U.
DHP: Bonn U., Barcelona U.

PXD6 prototypes: Thin wafers





- 8 wafers with thin sensors (50μm):
  - Small matrices to test different pixel size (50 to 200μm)
  - Design variations: short gate lengths, clear structures
  - Half ladders for prototyping (final size)
  - Technology variations on the wafer level



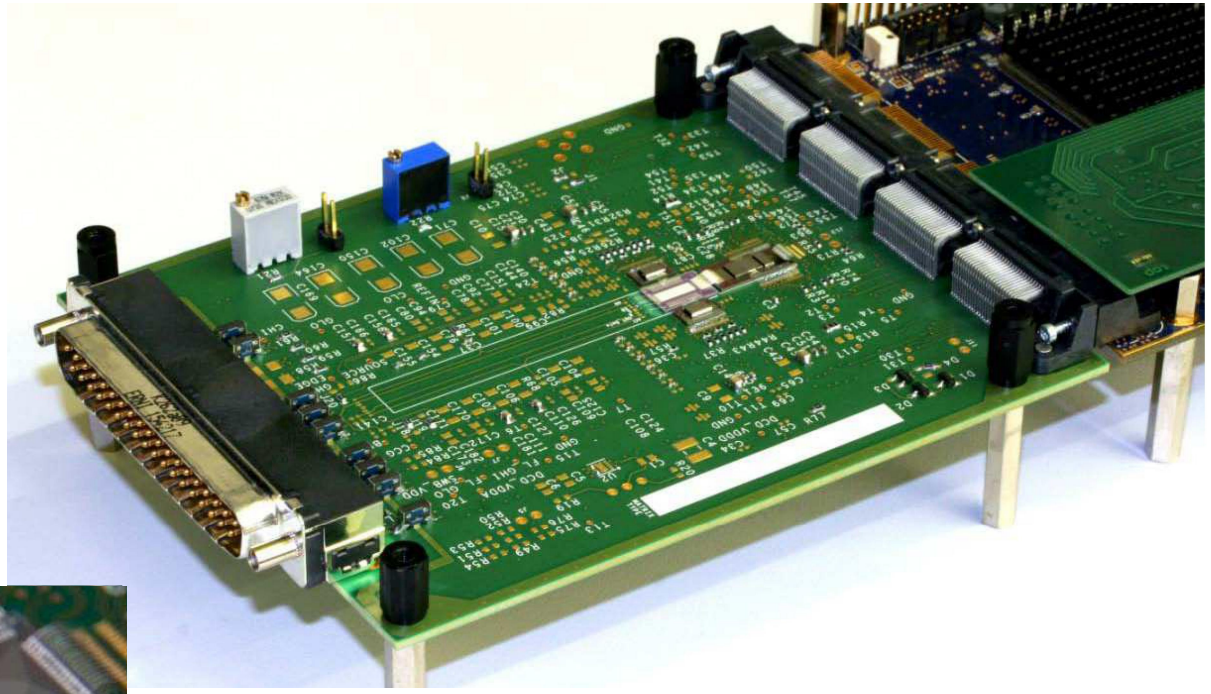
- 90 steps fabrication process
  - 9 Implantations
  - 19 Lithographies
  - 2 Poly-layers
  - 2 Alu-layers
  - Back side processing

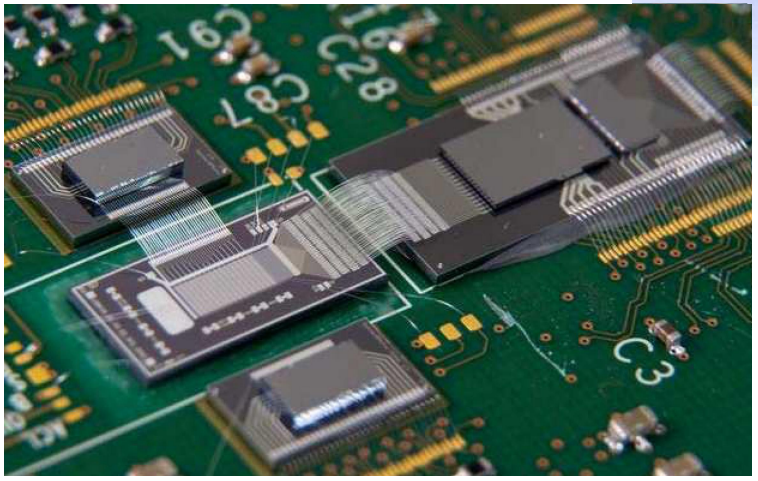
19 months processing time (16 after SOI pre-processing)

PXD6 prototypes: Test platform

Belle-II design

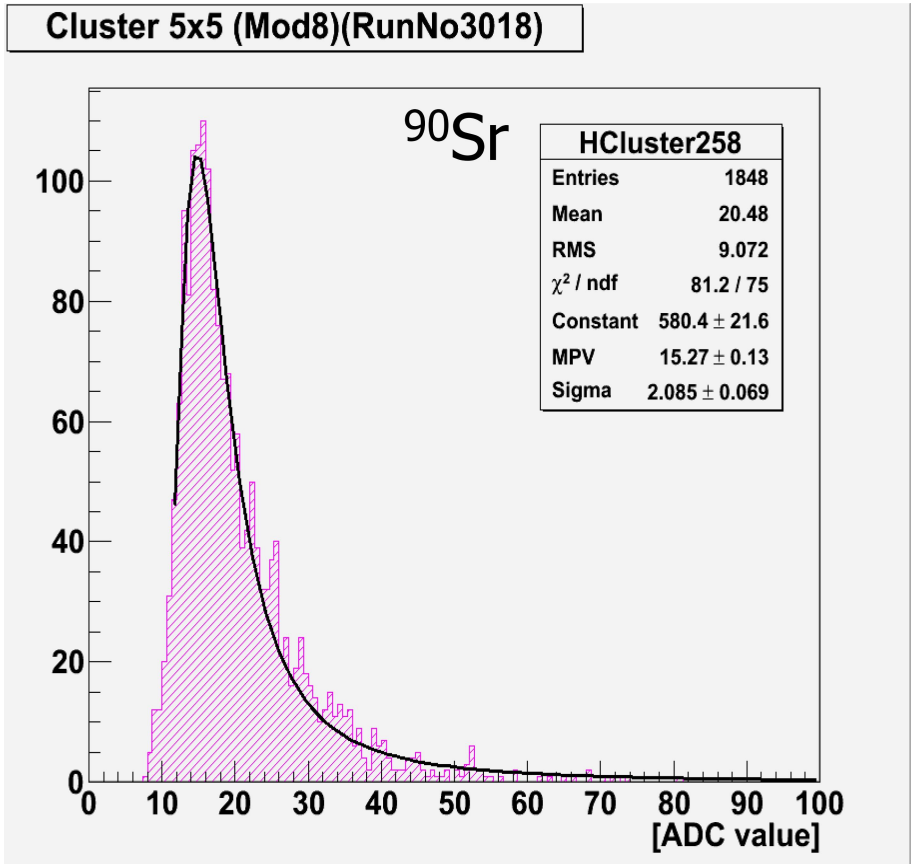
- Sensor 32x64 pixels
- 50x75x50 μm^3
- SwitcherB and DCDB at full speed

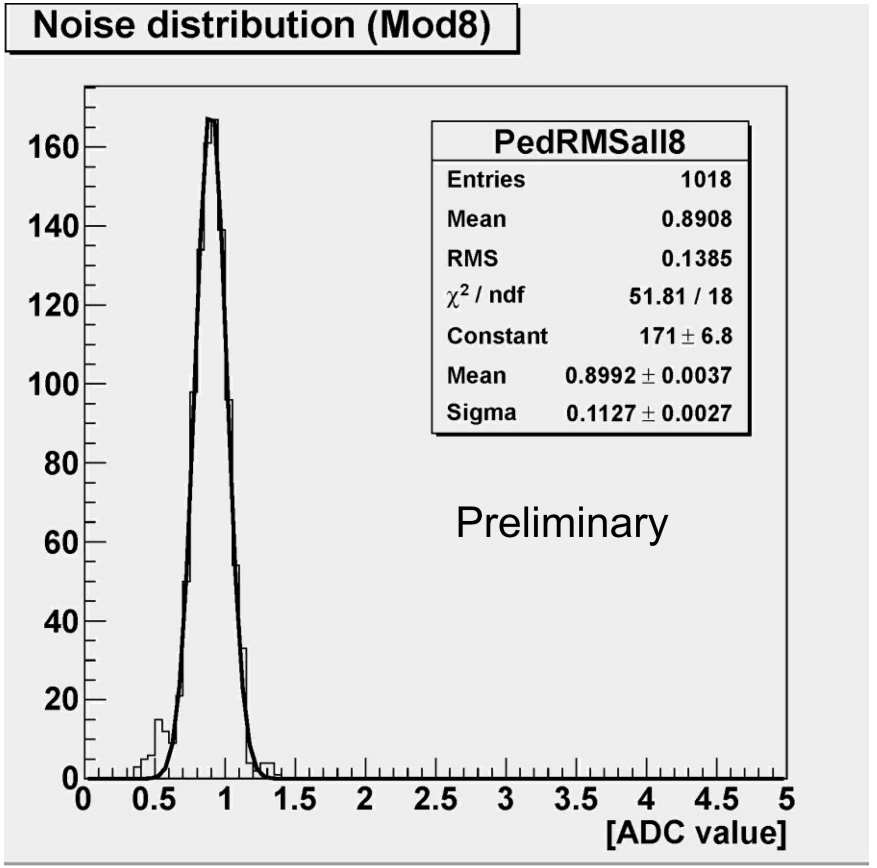




Prototypes with thin DEPFET sensors produced!

PXD6 prototypes: Fast readout





320MHz DCDB frequency→**100ns read-out time, S/N=17** (not optimal voltages)

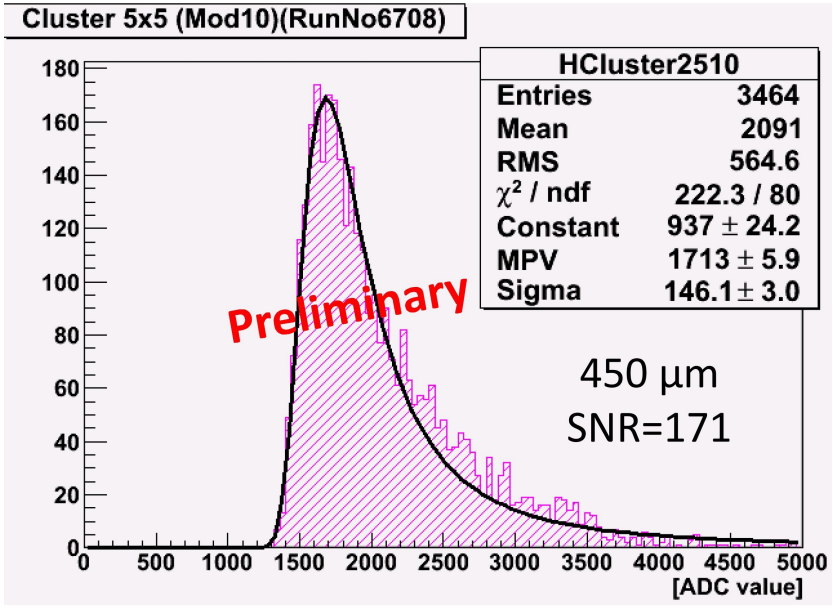
PXD6 prototypes: Thin sensors

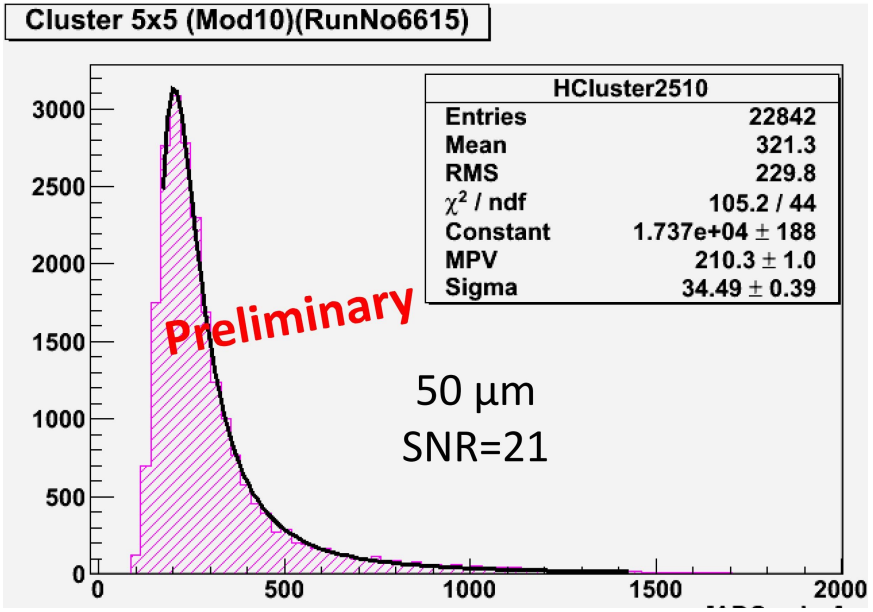
Thick and Thin sensors:

Belle-II design

Gate length = 6 μm

CURO readout





Signal(450μm):Signal(50μm)=8.2

As expected!