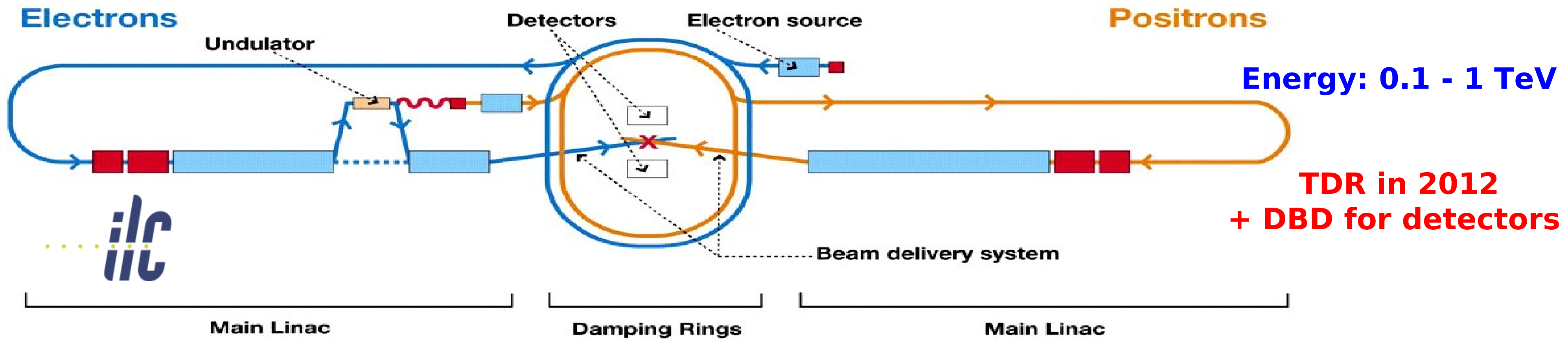
Status and plans for a highly granular SiW Ecal

EUDET Module extension

Roman Pöschl
LAL Orsay

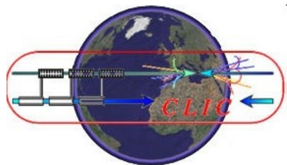
French Korean Electronics workshop at SKKU May 2011

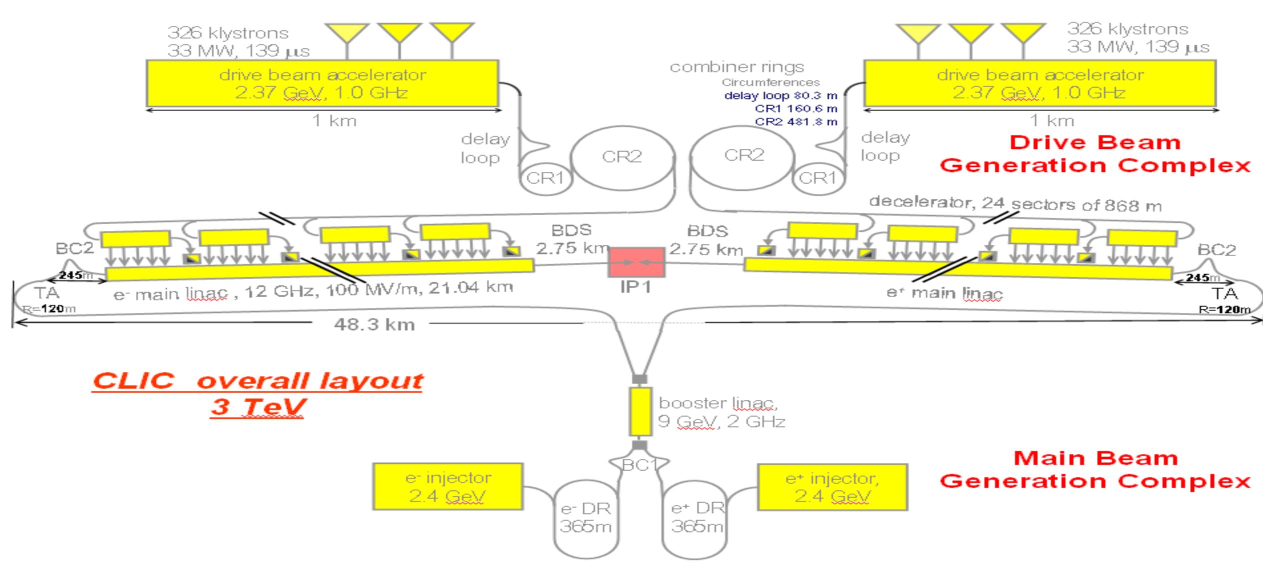
(Future) Linear electron-positron accelerators



Energy: 0.1 - 1 TeV

TDR in 2012
+ DBD for detectors





Energy: 0.5 - 3 TeV

CDR in 2011

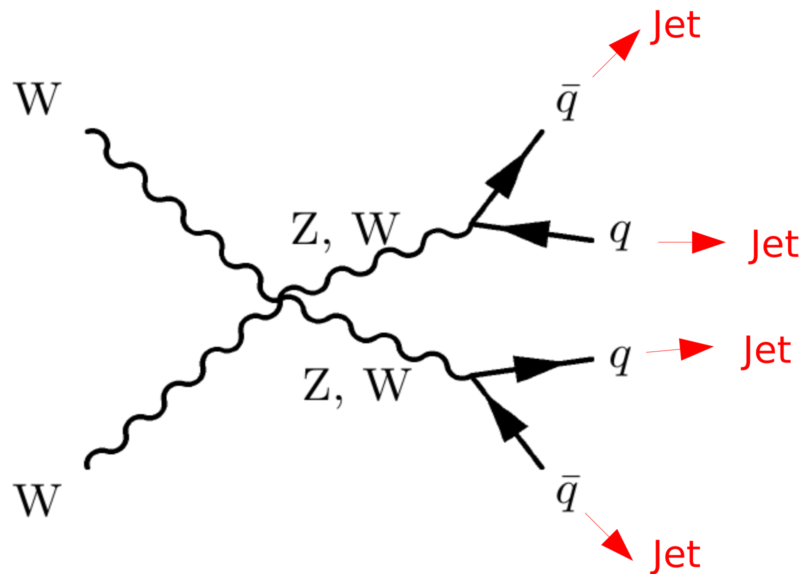
Linear collider is integral part of European Strategy beyond 2012

Hadronic Decays of W and Z Bosons

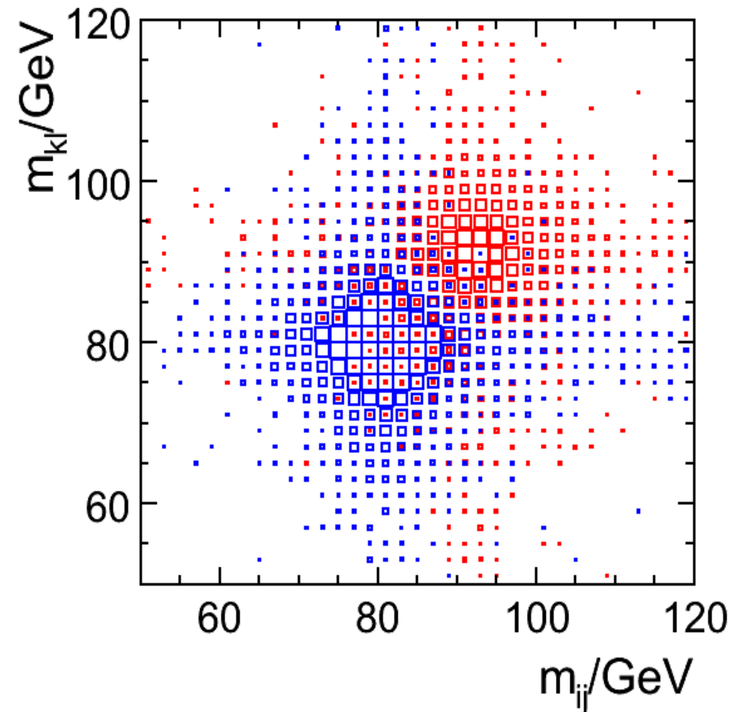
Boson Boson Scattering

What if no Higgs?

Manifestation of new physics
Strong Electroweak Symmetry Breaking



W, Z separation in the ILD Concept

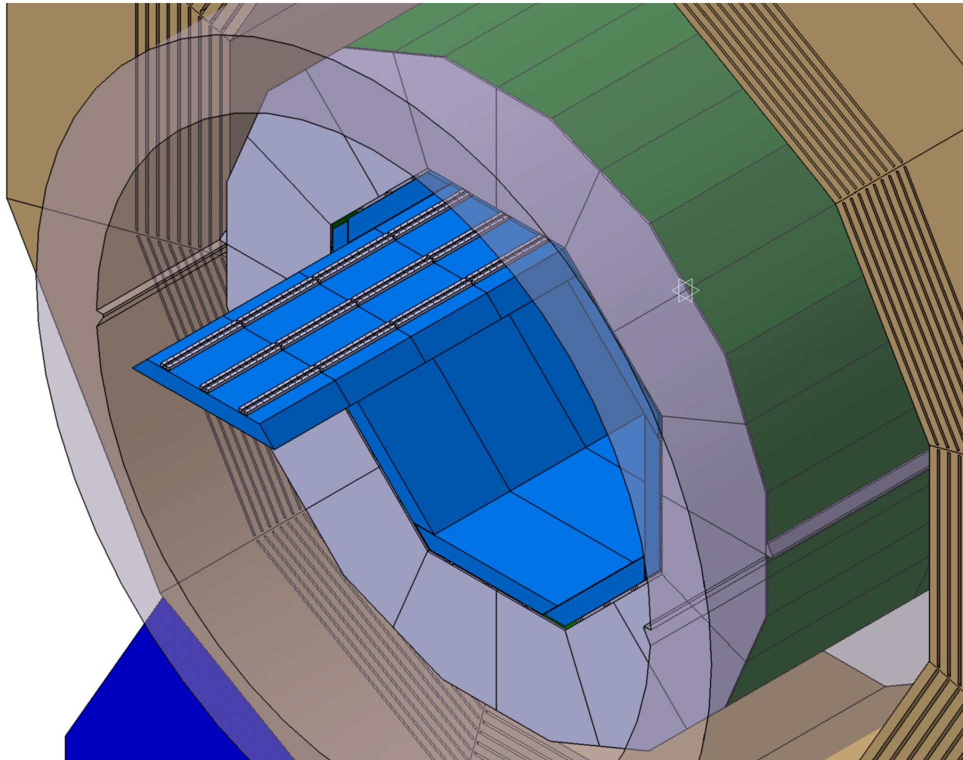


Remember: M_Z-$m_W \approx$ 10 GeV

- Need excellent jet energy resolution to separate W and Z bosons in their hadronic decays
  $3\%/E_{jet}$-$4\%/E_{jet}$
- Basic mean: Highly granular Calorimeters

SiW Ecal - Basics

The SiW Ecal in the ILD Detector



Basic Requirements

- Extreme high granularity
- Compact and hermetic

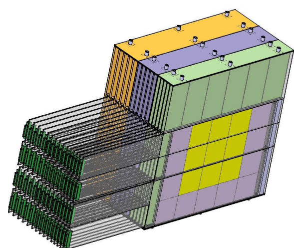
Basic Choices

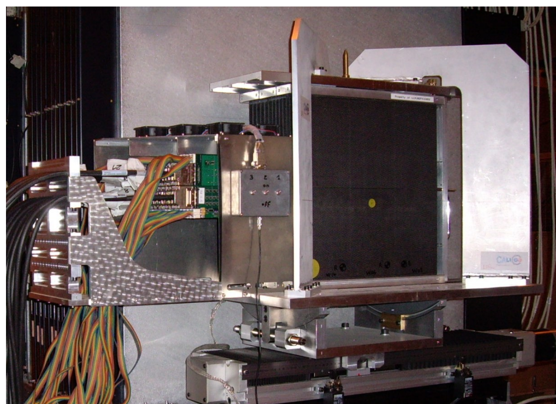
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design
- Silicon as active material
  - Support compact design
  - Allows for pixelisation
  - Large signal/noise ratio

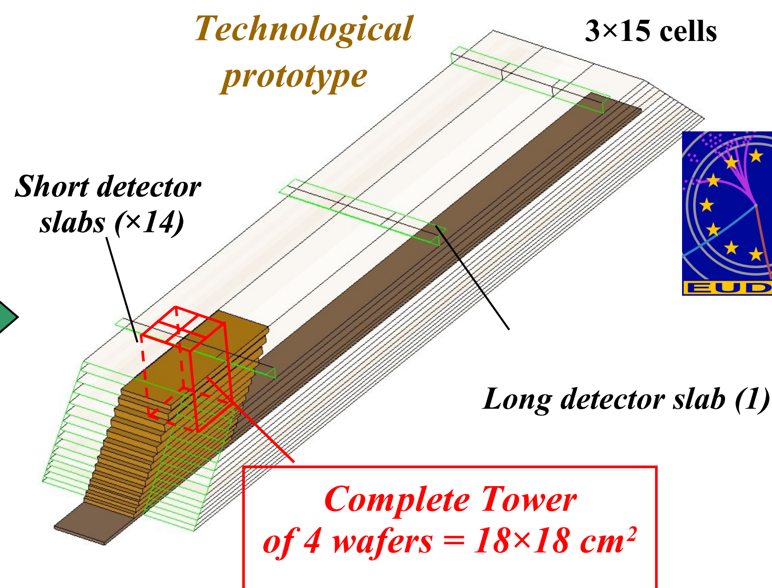
SiW Ecal designed as Particle Flow Calorimeter

Technological Prototype

Technical solutions for the/a final detector







- Realistic dimensions

- Integrated Front End Electronics

- Small power consumption

  Power pulsed electronics

- Construction 2010 – 2012, Test beams ~2012

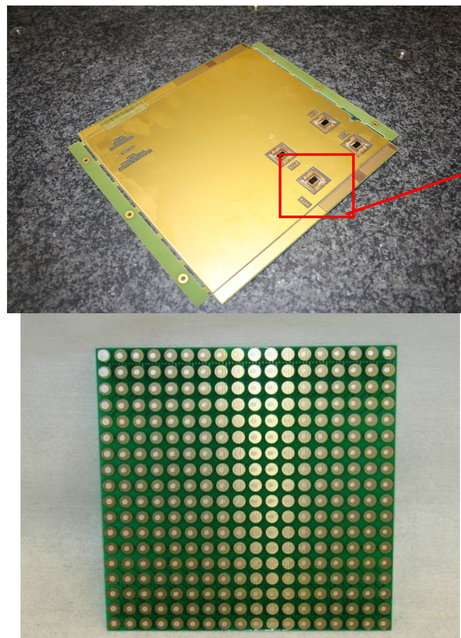
Ecal detector layer - principle

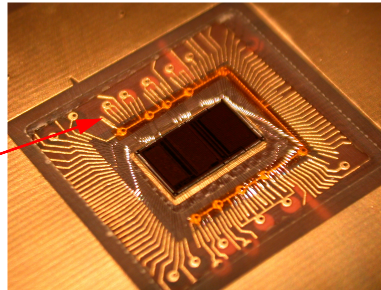
A layer is composed of several short ASUs:

- A.S.U. : Active Sensors Units

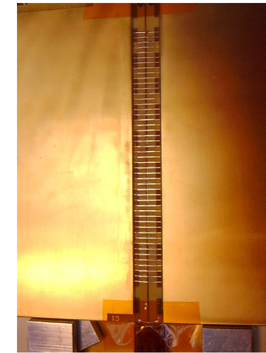
Chip+PCB+SiWafer =ASU

PCB is glued onto SiWafers

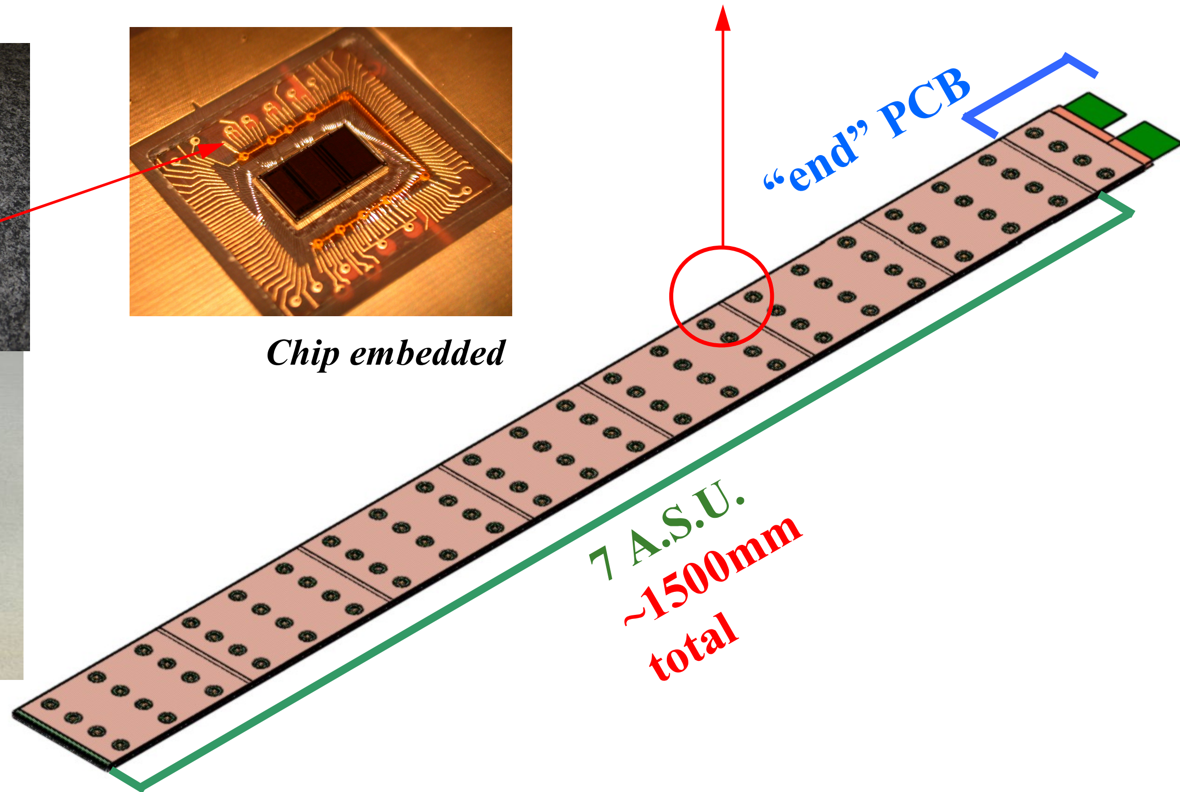




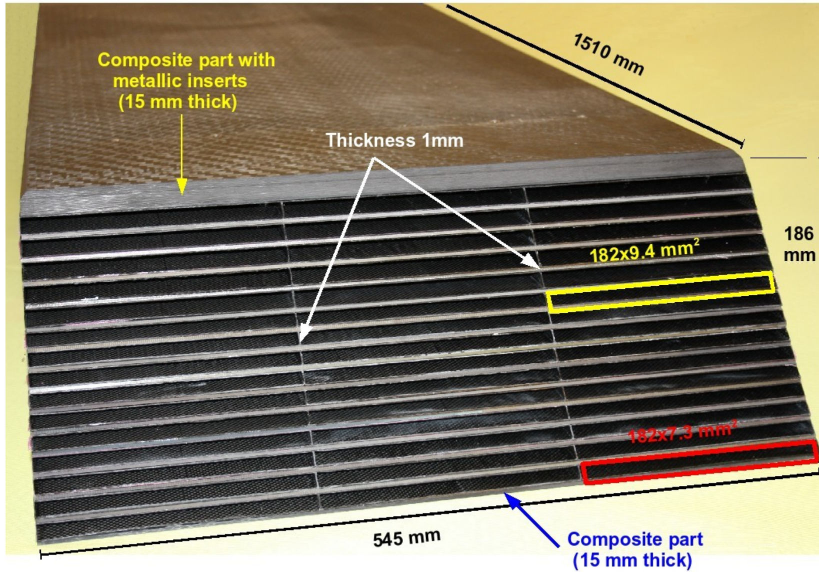
Chip embedded



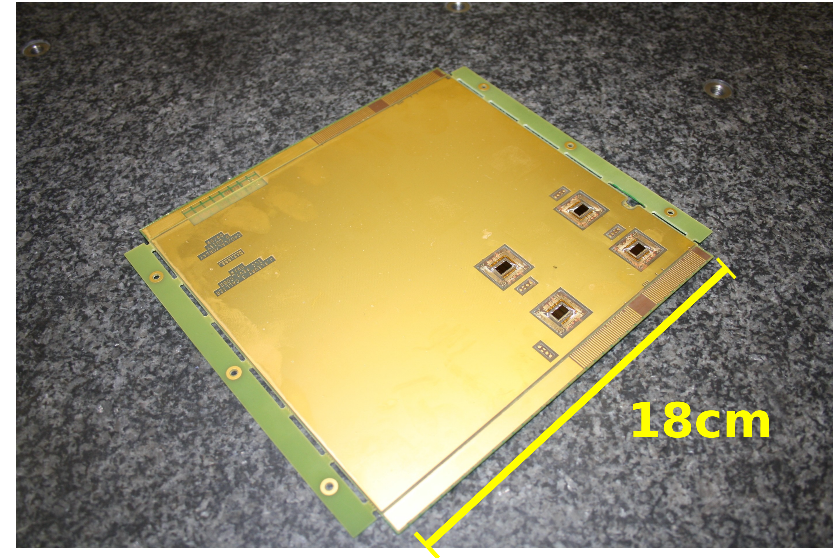
Interconnection by ACF ("Anisotropic Conductive Film")

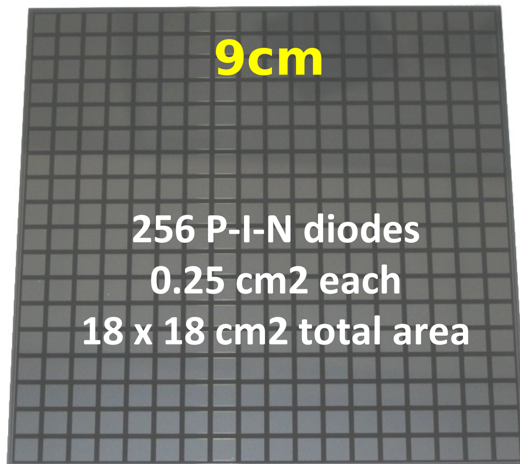


EUDET “legacy”

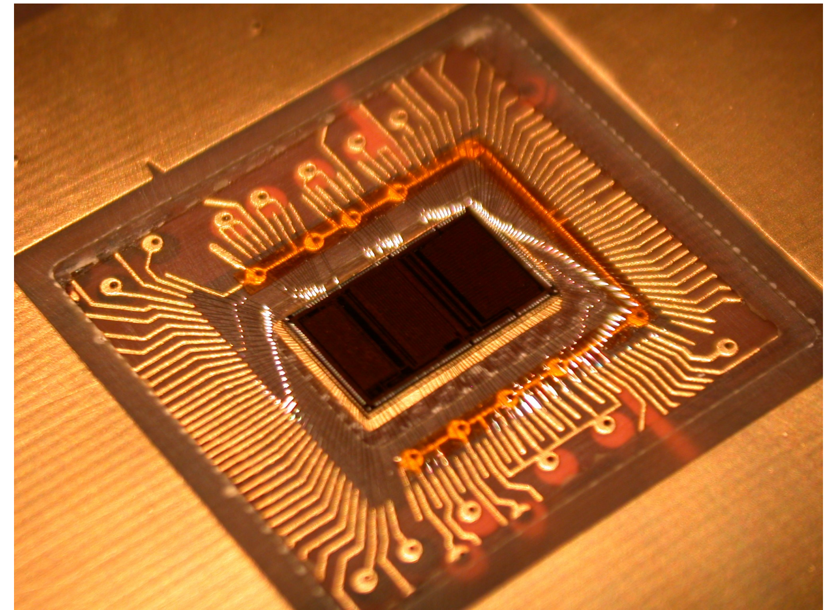


Alveolar strucuture
to house layers (self supporting)





Silicon sensors



Front end electronics

EUDET simulation

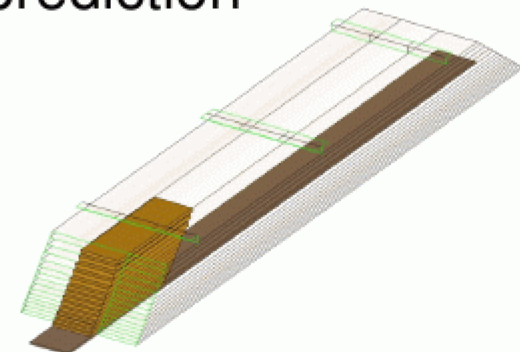
Calorimeter for ILC

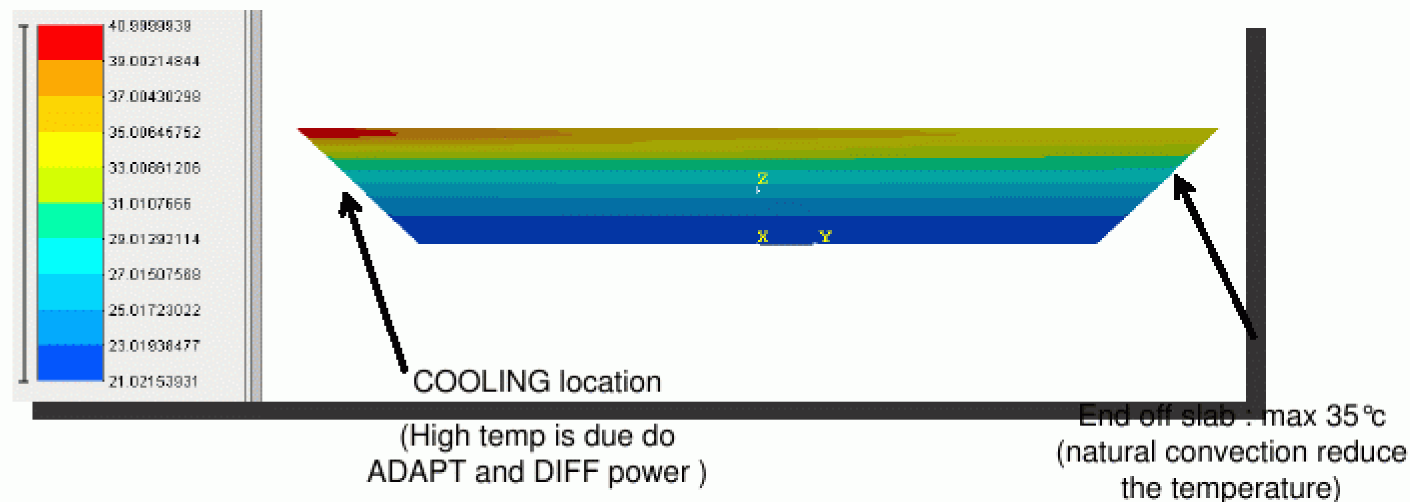
Thermal simulation with extreme power prediction

Extreme power pulsing on **ASU** => X 20 I

Initial total power for EUDET120 W => 143 W

Power on the longest SLAB : 8.2 W





EUDET temperature estimation with natural convection

(test beam configuration)

EUDET module provided(s) infrastructure for development of cooling systems

LPSC Grenoble

EUDET Cooling system

CALICE Calorimeter for ILC

Status of the portable cooling station for EUDET life:

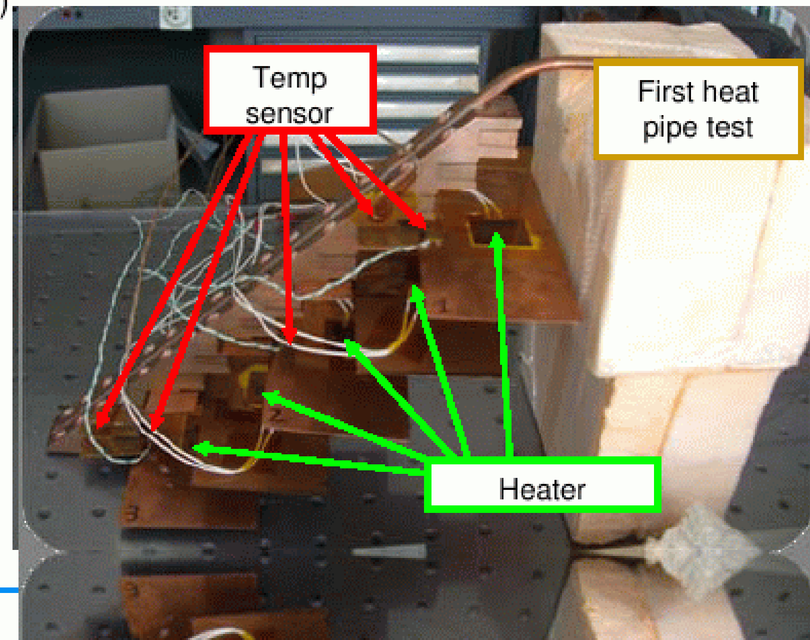
- Chiller and flow meter => ORDERED

- Important step : machining of heat pipe cooling system and water cooling system will begin after the final assembling of the alveolar structure (we need final dimension of the alveolar structure) => November 2010.

- Spring 2010 First test of heat pipe test (15 W design)
- November 2010 construction of both systems:

  Heat pipe

  Water cooling system for EUDET (143 W)



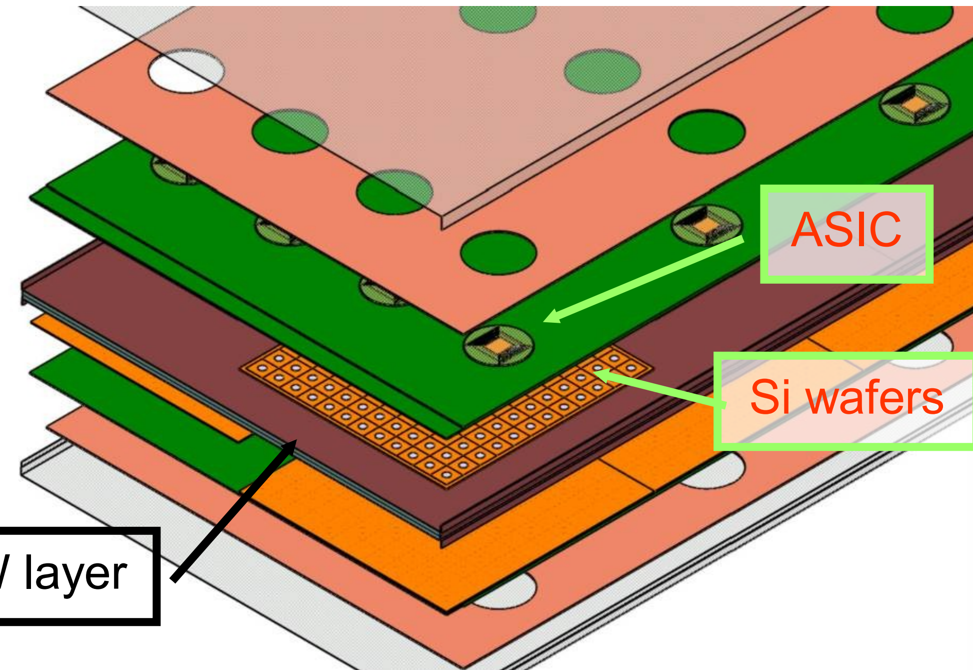
COOLING system for EUDET : march 2011

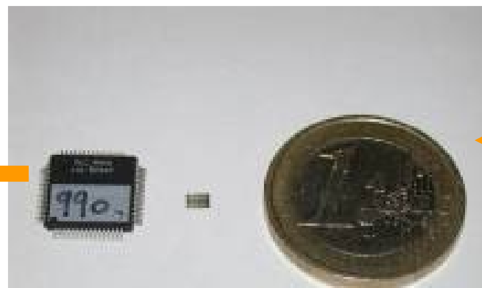
1st version

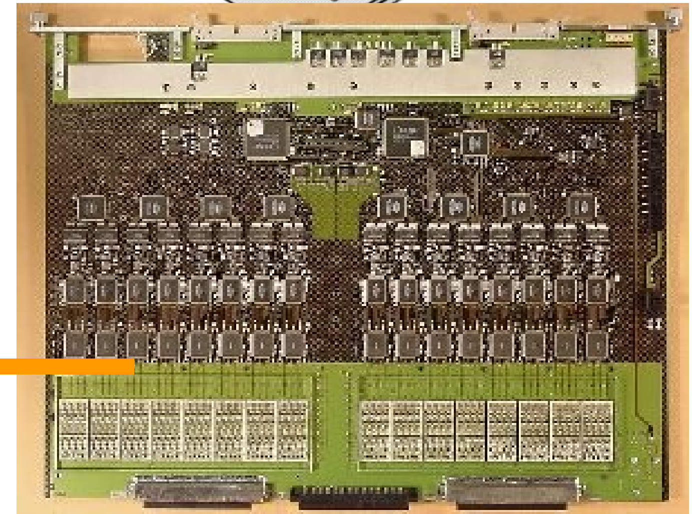
Front End Electronics

- Requirements to Electronics
  - Large dynamic range (~2500 MIPS)
  - 64 Channels
  - Front End Electronics embedded
  - Autotrigger at ½ MIP
  - On chip zero suppression

- **Ultra Low Power(«25µW/ch)**
  - 10^8 Channels
  - Compactness





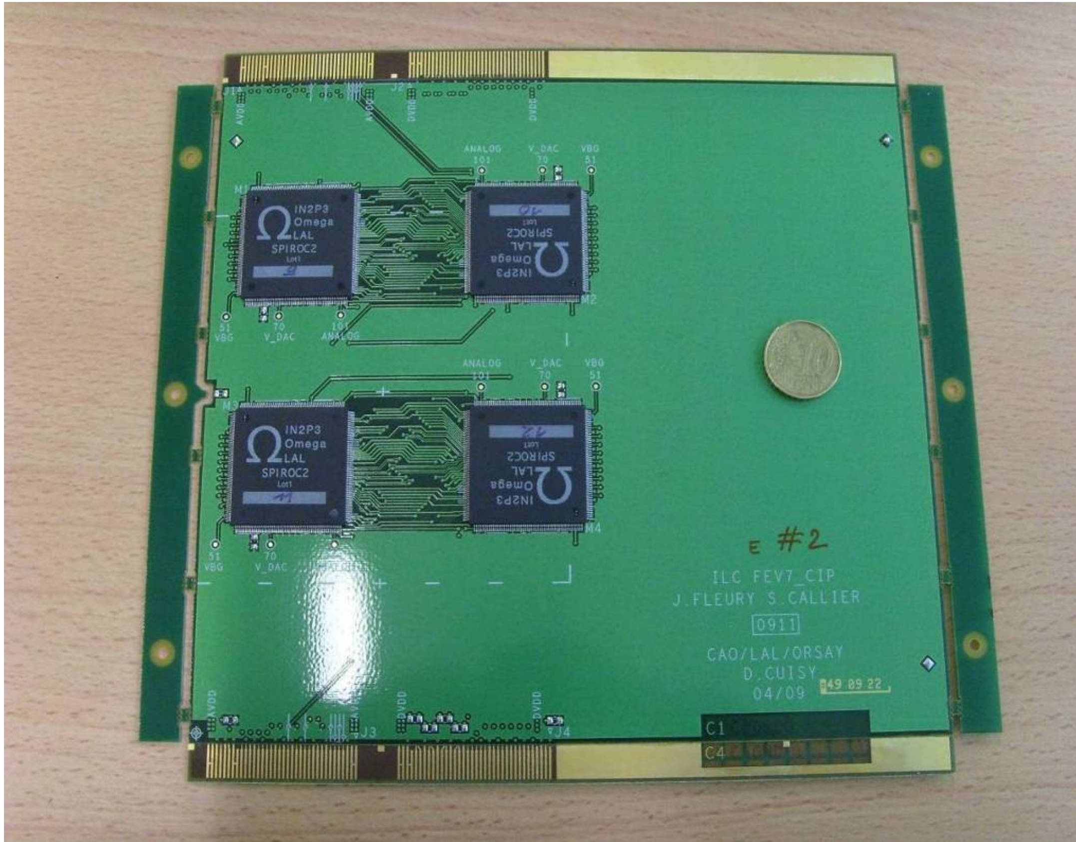


ILC : **25µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

SPIROC2 and FEV7



- FEE established designed and prototyped within EUDET

- Used SPIROC chip (AHCAL) for first version of Ecal ASU
  SPIROC: 30 channels
  500 MIPS dynamic range
  Chip for Ecal is SKROC
  SKIROC: 64 Channels
  2500 MIPS dynamic range
  At hand since autumn 2010

- Chip in package to validate principle of FEE design

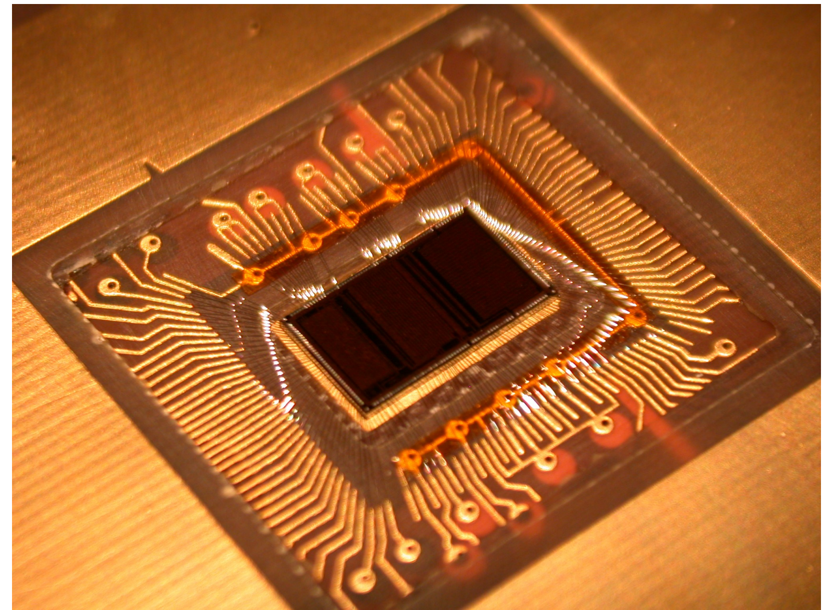
FEV7-COB: with SPIROC2 COB

- Front End Board using Chip-On-Board (spiroc2=208 pads)

- Nearly Identical to Chip-In-Package FEV7
  - Schematics identical
  - Same number of channels
  - Same pinout on Adapter Board/Slab Connector

- Except :
  - Pads connections to chip pins
  - Position of Wafer on the bottom side
  - Thickness: thinner to comply with H alveolar structure

Next step towards FEE for Ecal established



Goal: Ecal board FEV8 with SKIROC chip

FEV N Issues

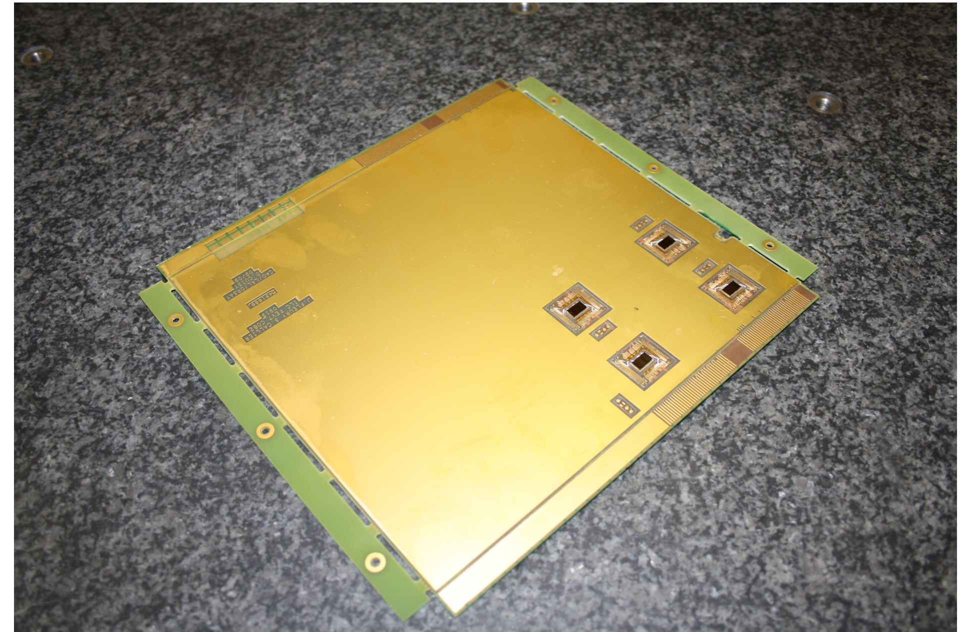
- FEV7 feature untolerable bending ~3mm

- Industrial standard is 1% of diagonal (30cm for FEV7)

- Would lead to mechanical stress during assembly

- Alternative assembly may reduce bending by 50% (still intolerable)

- Dedicated effort to reduce initial bending by ~50%



Remedies?: Contact with industry
Korean French collaboration within FKPPL
Contacts within AIDA?

Issue needs to be solved before before moving towards FEV8

FEV8 is actual board for SiW Ecal

PIN Diodes Silicon Sensors

Designed for ILC : **Low cost, 3000 m2** Minimized number of manufacturing steps

Target is 3 Euro/cm2

Now : 10 Euro/cm2

Somewhat reduced for mass order

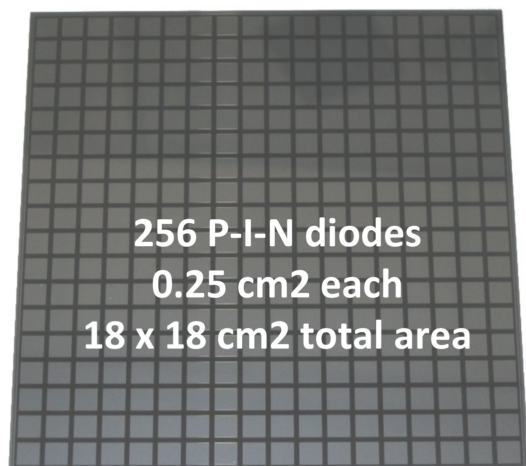
Known issues

Dead space optimization

Guard-rings do not collect charges

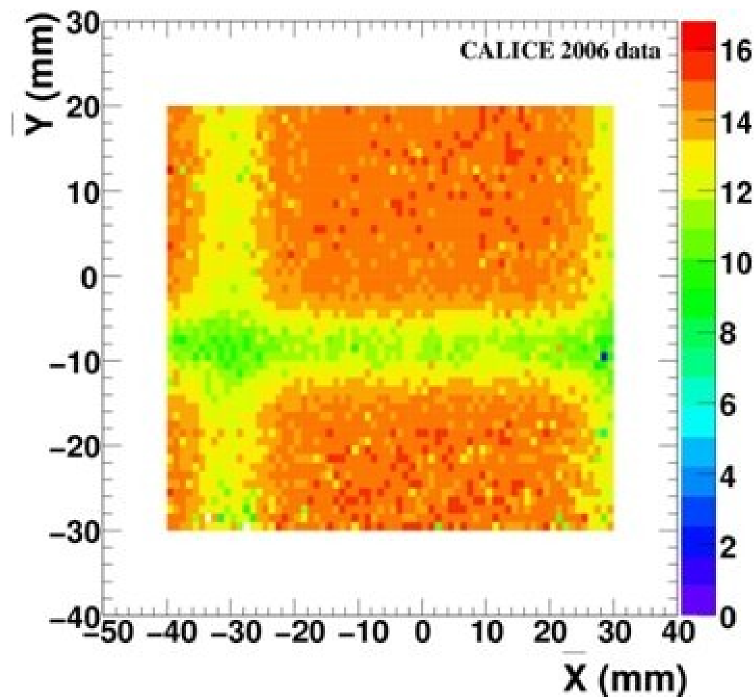
Dead space to be reduced

Use of **floating guard-rings**



EUDET layout

Prototype from Hamamatsu



Hit map from physics prototype

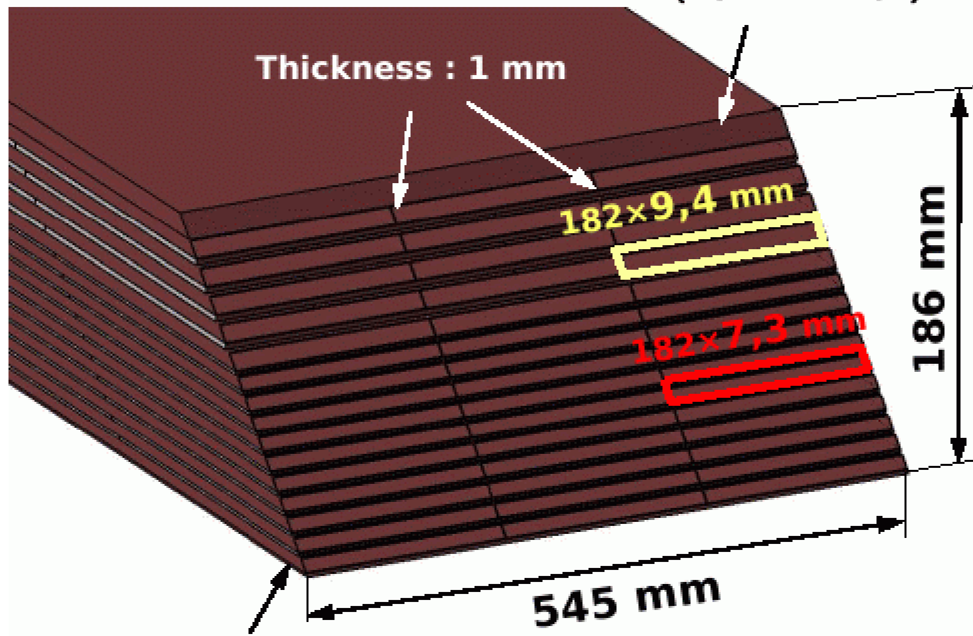
Industrialization

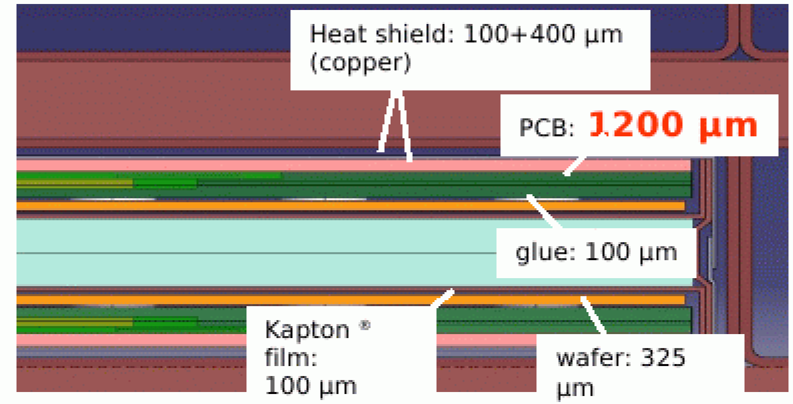
- Discussions with CEA/LETI (november 09)
  - 8 inches wafers, 4 matrices, 700 um thick (yield)
  - ST microelectronics
- Visit to HPK : confirm and complement what learned from LETI
  - Will use 6 then 8 inches wafers
  - 4 matrices processed at the same time (yield improvement)
  - R&D on laser sawing
  - Optimized thickness (yield vs width of dead space)
  - Optimized call of offer
  - ILD = 400% of production capability of a year (solid state devices division)
- Firsts contacts with VTT, SINTEF, MICRON semicond.
- In touch with PERKIN ELMER US & EU : both integration and manufacturing
- Not forgetting our historical collaborators : FZU (ONSemi), MSU, BARC, ...
- More discussions needed but a strategy is being build on "real" inputs from manufaturers

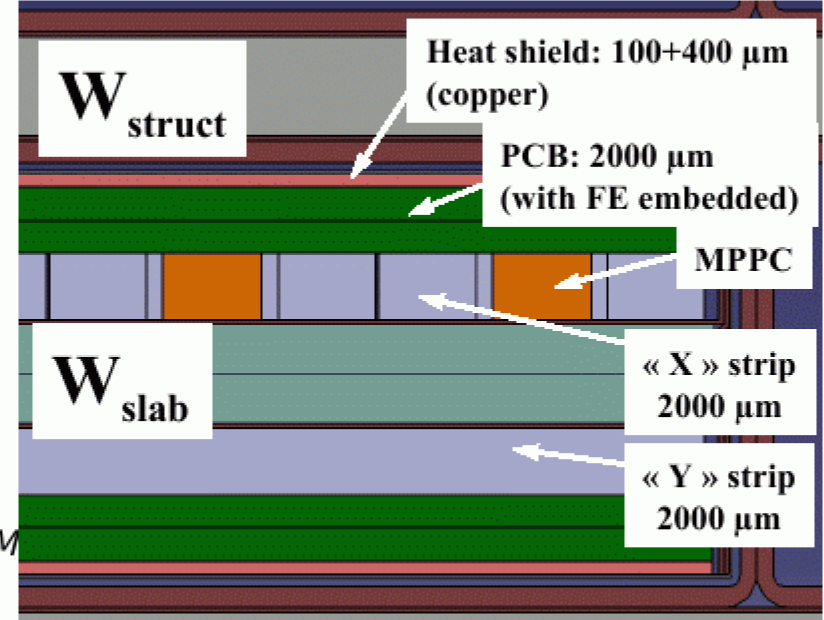
R. Cornat: LLR

→ Support by AIDA to purchase (several variants) of wafers

Study of alternative Ecal technologies







Alveolar structure applicable for
alternative Ecal proposals
"TNA"

EUDET Annual M

French Korean Electronics Workshop 2011

Coarse planning for SiW Ecal

- 2011: Completion of absorber structure and 1st version of cooling system

- 2011 - 2012: Test beams ("electrical", cosmics, beams at DESY) with small units

- 2011-2012: Continuous R&D on FEE
  FEV7/SPIROC → FEV8/SKIROC
  Risks: Hidden design bugs, mechnical issues of FEV

- 2011-2012: Continuous R&D for low cost R&D Si wafers
  Progressive purchase of wafers

- 2013: Test beam with ASUs in absorber structure (CERN preferred)
  Risks: Shutdown of test beam site(s)

Backup

Evolution of Task – JRA3 Ecal EUDET Module

2006

Conceptual Phase – Definition of Project Targets
Detection of problems with Si-Wafer Guardrings and start of investigations for remedies

2007

Decision to go for 0.5x0.5 cm^2 Si-Wafers instead of 1x1 cm^2 Wafers
Contacting and negociations with manufacturers
⇒ Wafers with dimensions of 9x9cm^2
Continuation of studies for building large alveolar Structures
Dimensions depend on wafer dimensions and constraints of challenging Very Front End Electronics

2008

Decision to go for a demonstrator to allow for validation of mechanical concept
Milestone: Design of Moulds and Alveolar Structures finished (EUDET-Memo-2008-07)
Milestone: TDR of SiW Ecal EUDET Module – Details of design fixed (EUDET-Memo-2008-11)
Delivery and Examination of 30 Si-Wafers (Hamamatsu)

2009

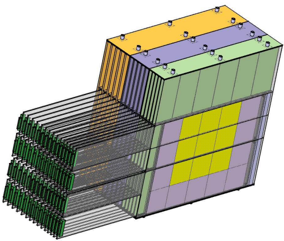
Demonstrator built and start of thermal studies
Demonstrator is to be taken as EUDET Deliverable!!!!
Ordering of pieces for 'real' EUDET module in autumn 2009
Next steps depend on progress of VFE
Advancing the VFE has top priority

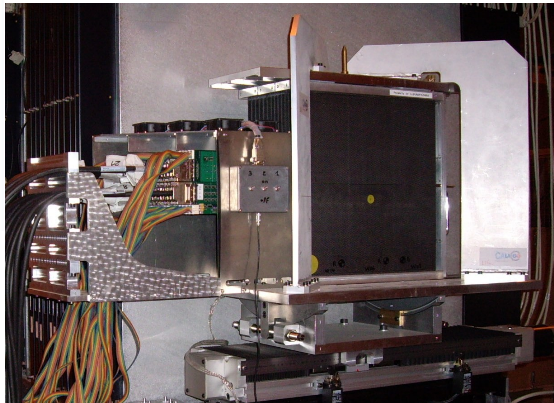
2010-2011

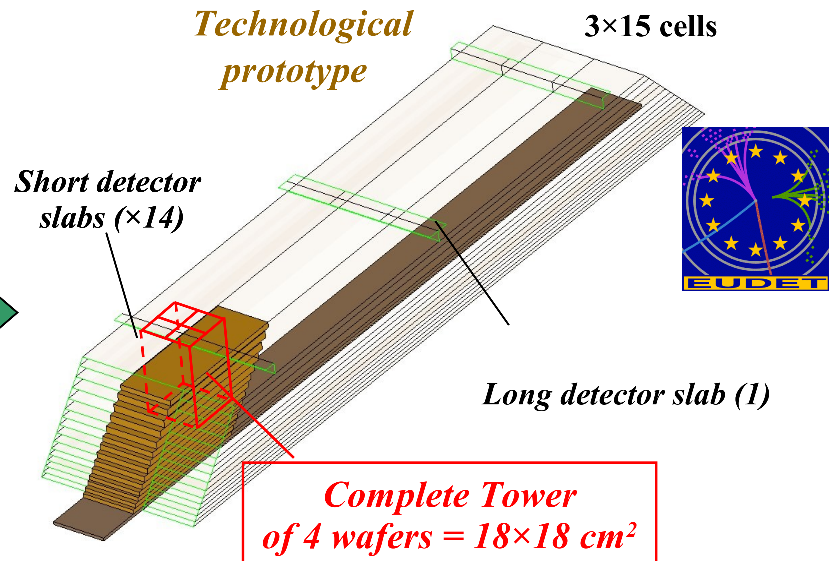
Towards the EUDET Module ?

EUDET Prototype

- Logical continuation to the physical prototype study which validated the main concepts : alveolar structure , slabs, gluing of wafers, integration
- Techno. Proto : study and validation of most of technological solutions wich could be used for the final detector (moulding process, cooling system, wide size structures,…)
- Taking into account industrialization aspect of process
- First cost estimation of one module



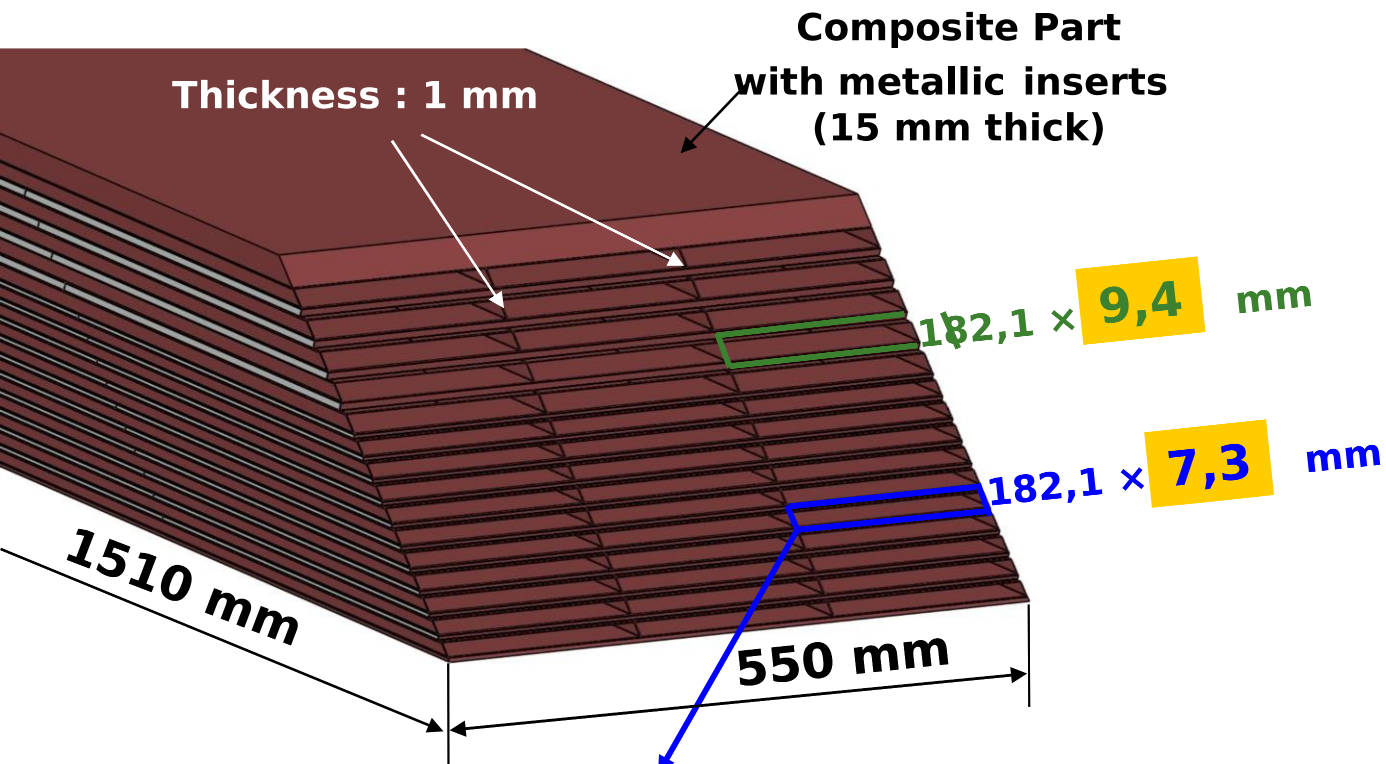


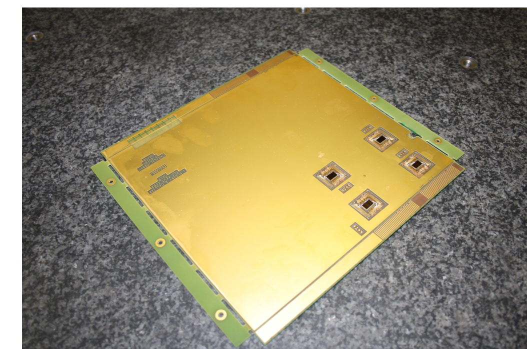


- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

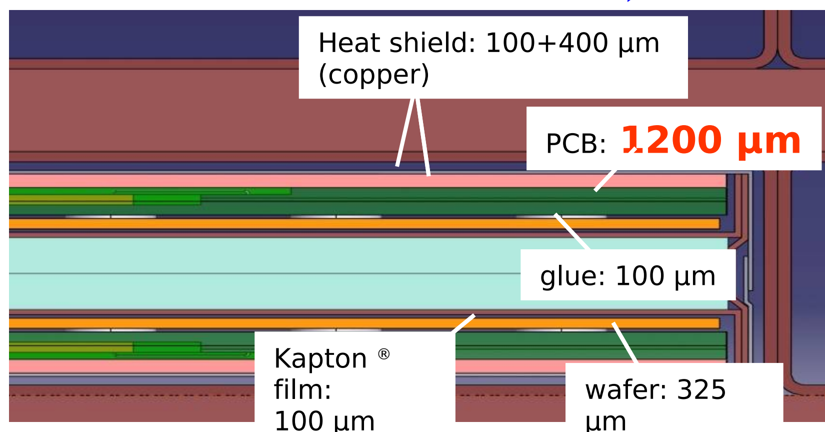
- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

EUDET Module – Design





FEV board
Thickness ~1.1mm



- ⇨ Gaps (slab integration) : 500 µm
- ⇨ Heat Shield: **400 µm ?** Validation with the demonstrateur
- ⇨ PCB : ~~800 µm~~ **~1200 µm**
- ⇨ Thickness of Glue : 100 µm
- ⇨ Thickness of SiWafer : 325 µm
- ⇨ Kapton® film HV : **100 µm ?**
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

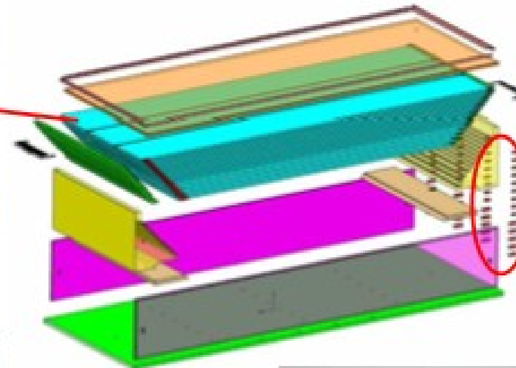
ECAL module – parts of Mould

CALICE Calorimeter for ILC

⇨ Validation & Thermal tests : **Feb 2011**
⇨ Alveolar structure : **March 2011**

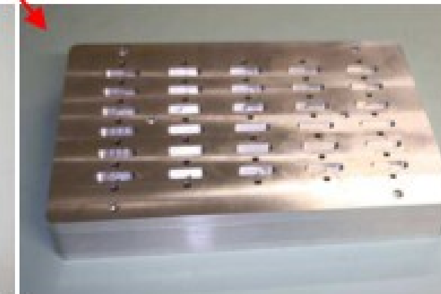
Alveolar layer production :
15/15 *structures are been moulded*
The production of one layer is now stopped because we waiting the FBG.
The reception of the FBG is expected this week

All the cores and layers are assembled for the thermal test



Joints production :
180/180 *joints ready*
Design and construction of 2 moulds according to lower and upper parts

All PVC parts for pre-compacting are completed



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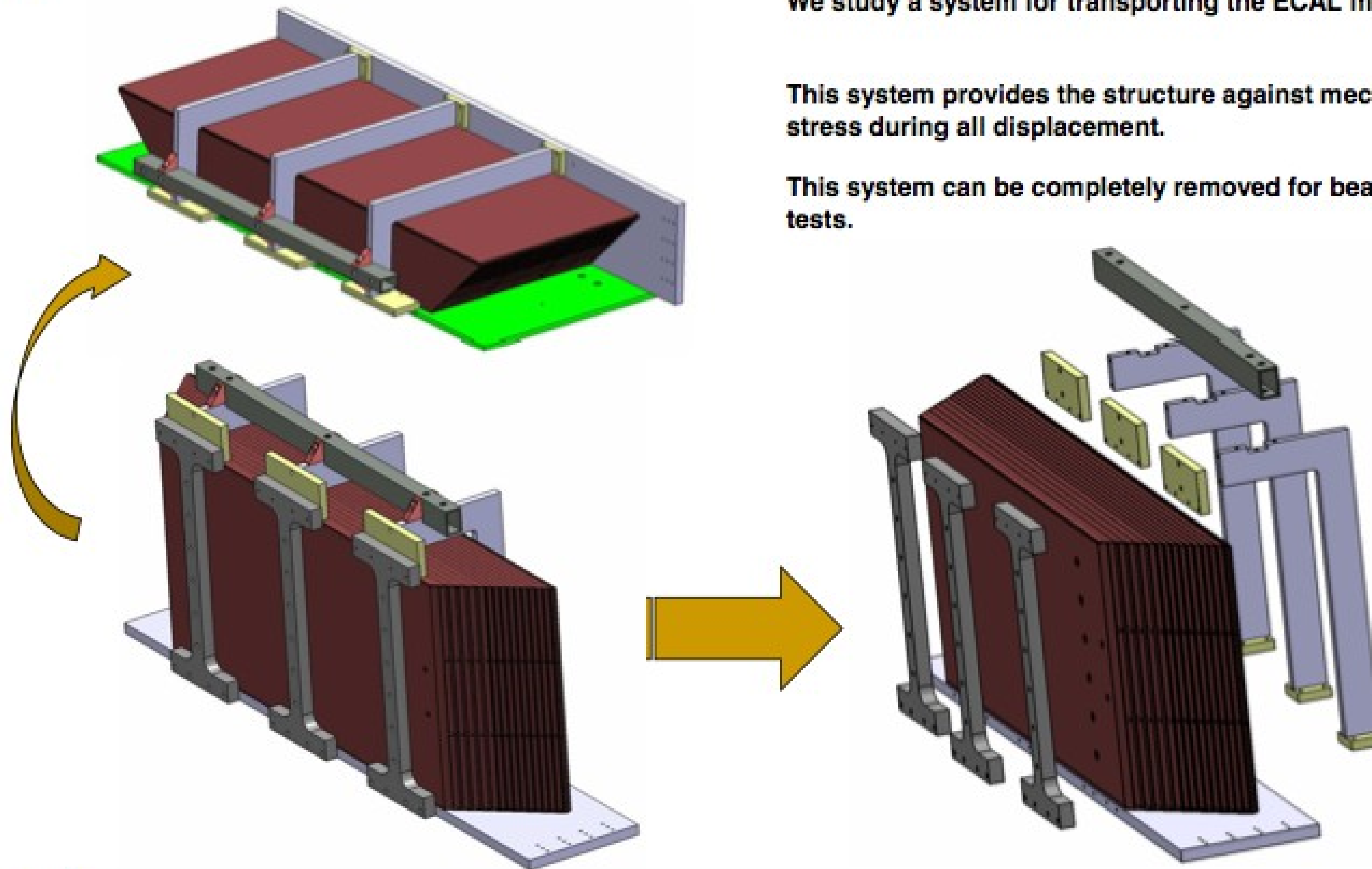
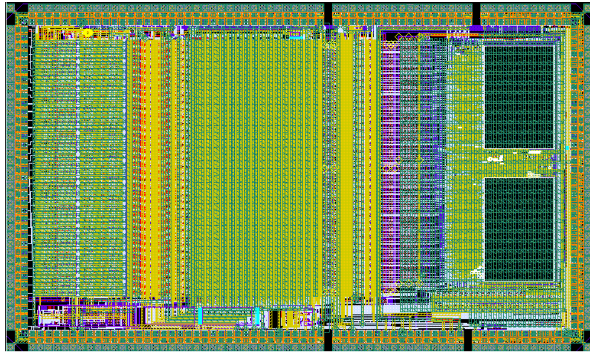


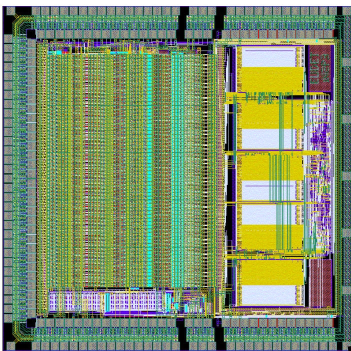
Preparing EUDET Module for testbeams

The ROC Chips

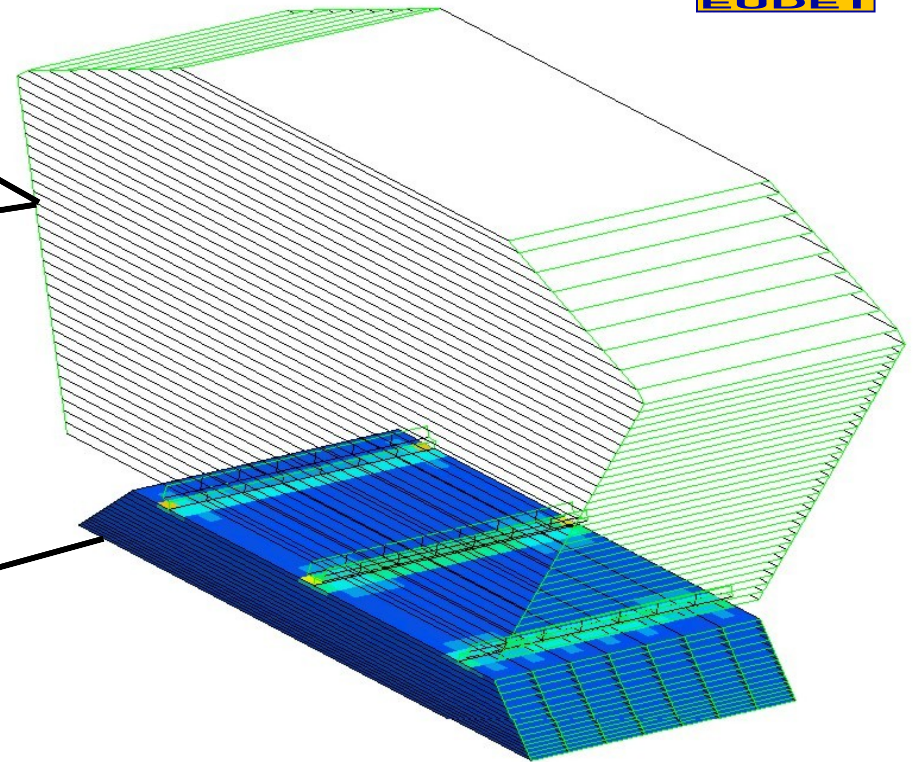


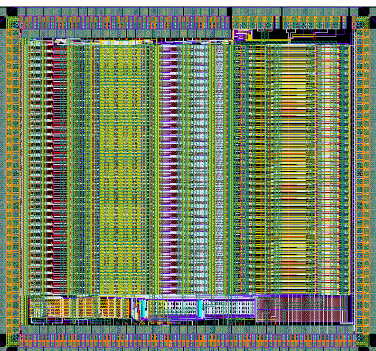
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07

- EUDET prototypes: large scale prototypes
- Financial support by EU (06-09)
- ECAL, AHCAL, SDHCAL



HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
128 ch. 16Mm²
Available since beginning ~2009





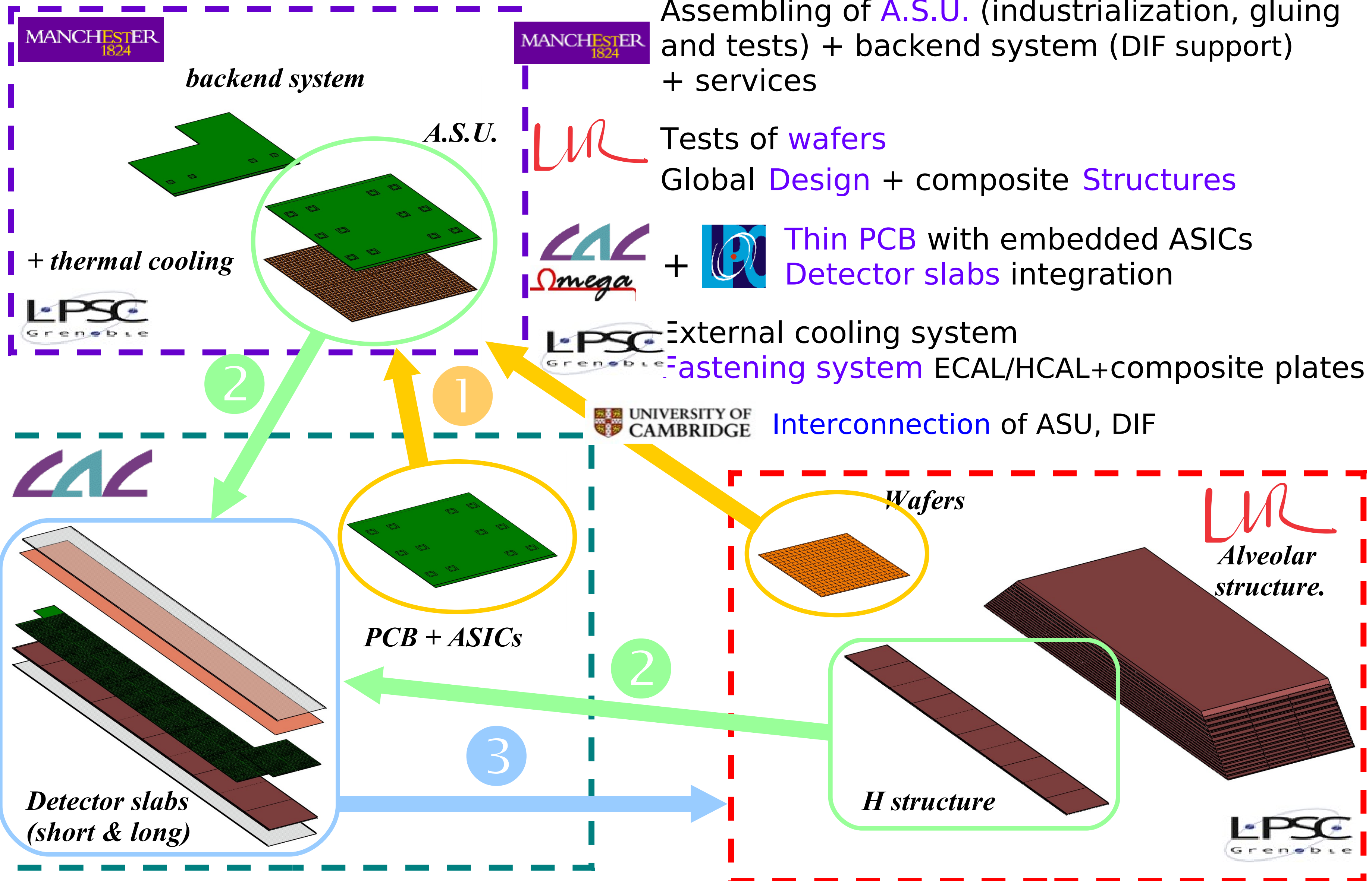
SKIROC
ECAL(Si PIN diode)
64 ch. 20mm²
October 2010

SKIROC most complicated chips but very similar to SPIROC
→ Verfication/Development of Ecal FEE Design with SPIROC2 chip

Parties Involved

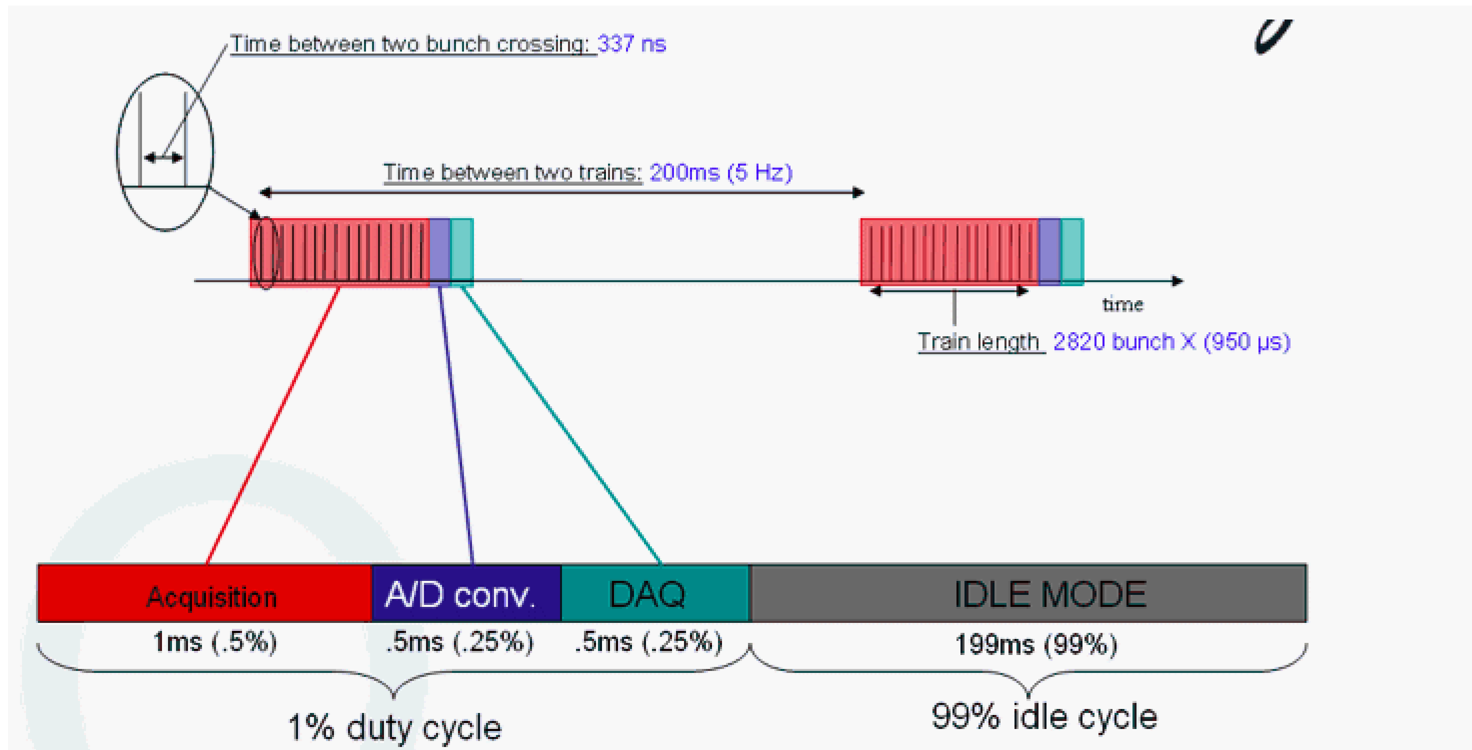
6 Laboratories are sharing out tasks in according to preferences and localization:

- MANCHESTER 1824: Assembling of A.S.U. (industrialization, gluing and tests) + backend system (DIF support) + services
- LLR: Tests of wafers; Global Design + composite Structures
- LAL + Omega + LPNHE: Thin PCB with embedded ASICs; Detector slabs integration
- LPSC Grenoble: External cooling system; Fastening system ECAL/HCAL+composite plates
- UNIVERSITY OF CAMBRIDGE: Interconnection of ASU, DIF



Power Pulsing

Main tool to control power budget of LC calorimeters



- Electronics switched on during 1ms of ILC bunch train and data acquisition
  Time constraints even more severe for CLIC

- Bias currents shutdown between bunch trains

FEV N Issues

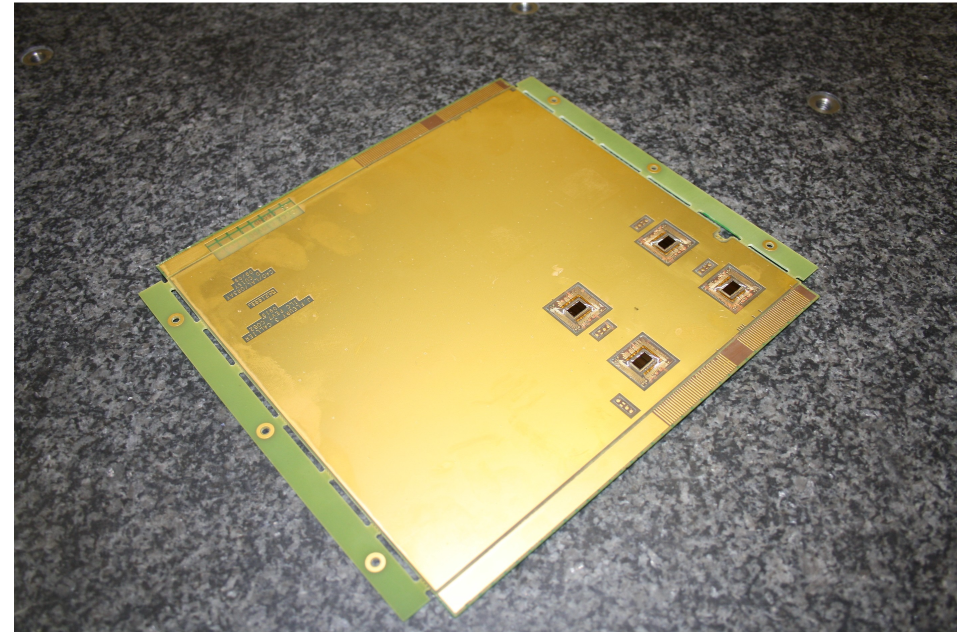
- FEV7 feature untolerable bending ~3mm

- Industrial standard is 1% of diagonal (30cm for FEV7)

- Would lead to mechanical stres to wafers during assembly

- Alternative assembly may reduce bending by 50% (still untolerable)

- Dedicated effort to reduce initial bending by ~50%

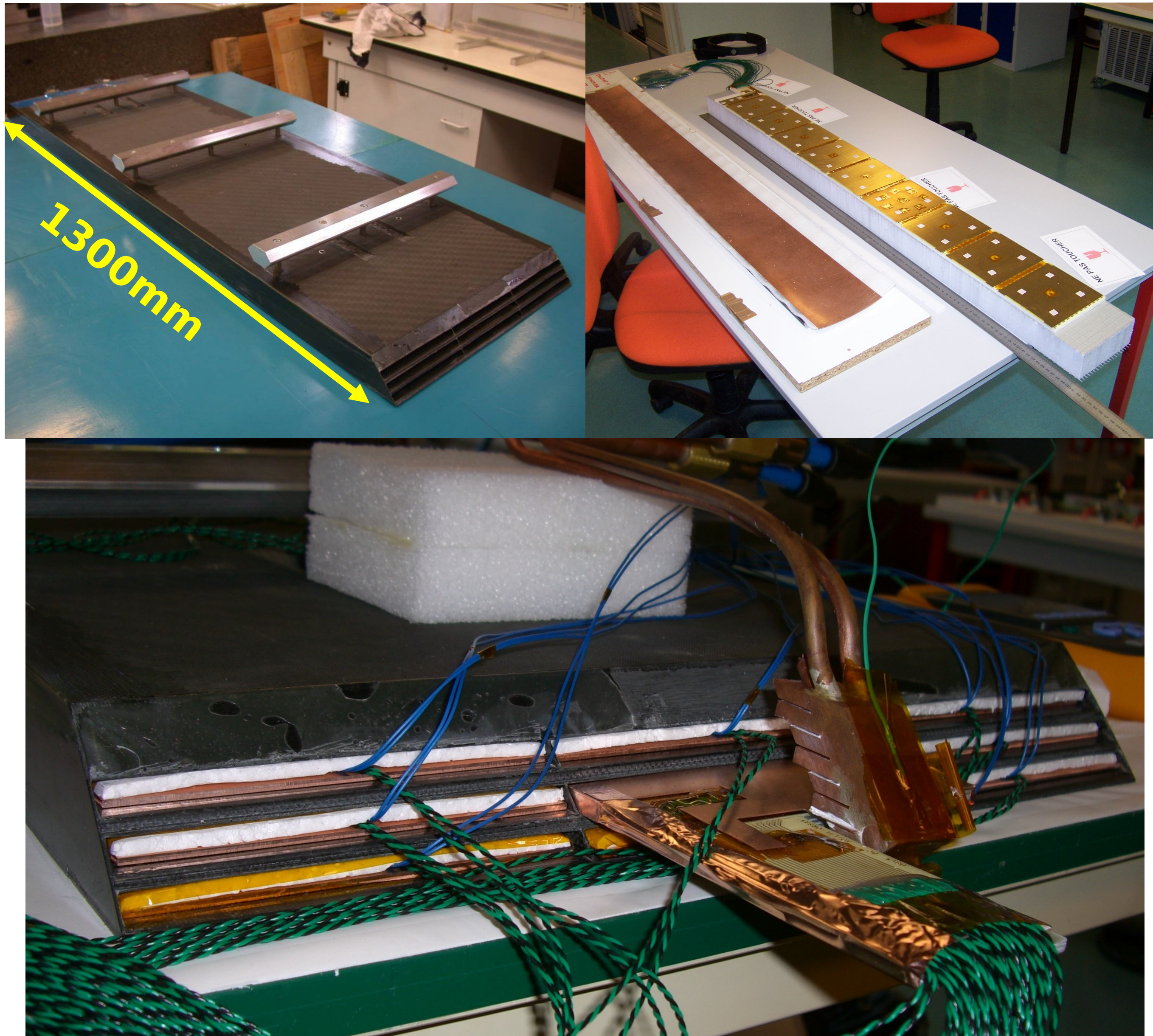


Remedies?: Contact with industry
Collaboration with corean groups
Contacts within AIDA?

Issue needs to be solved before before moving towards FEV8

FEV8 is actual board for SiW Ecal

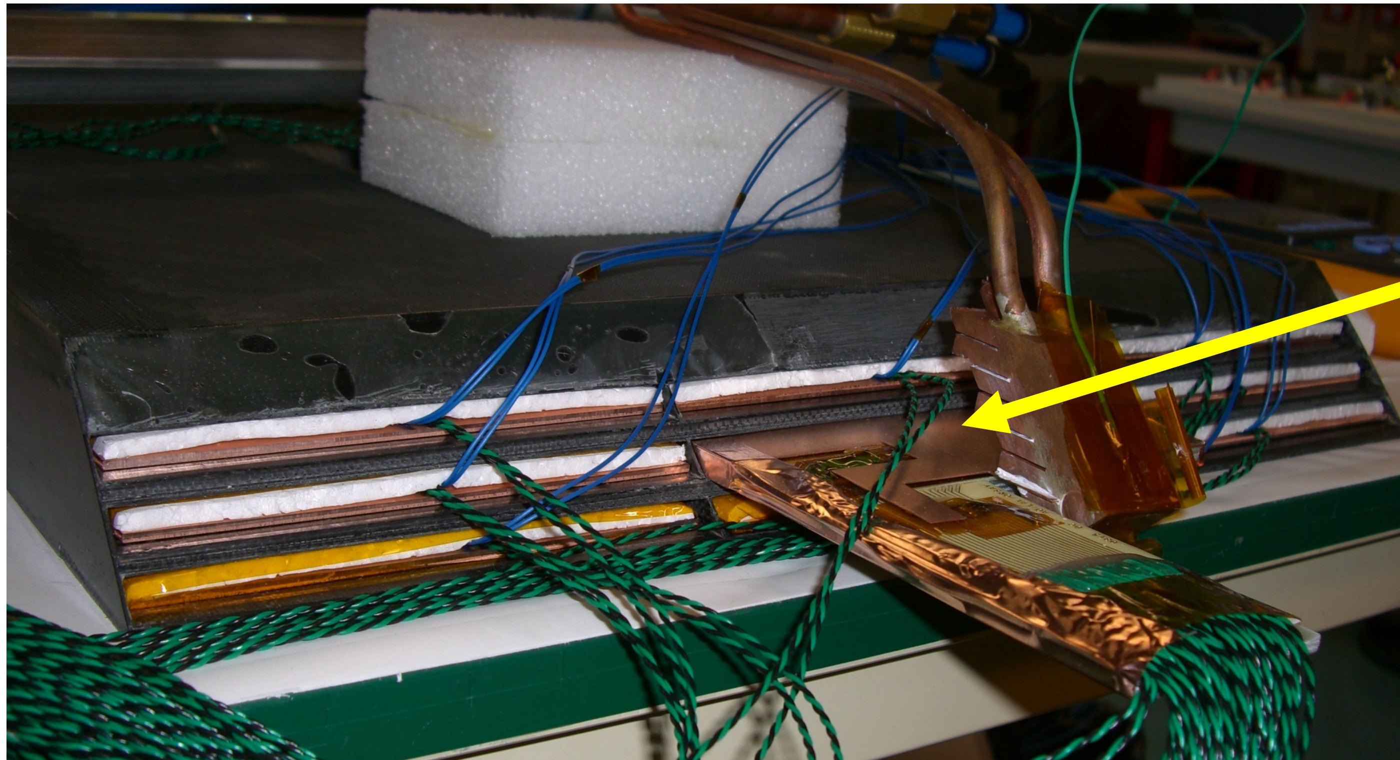
Assembly of Demonstrator



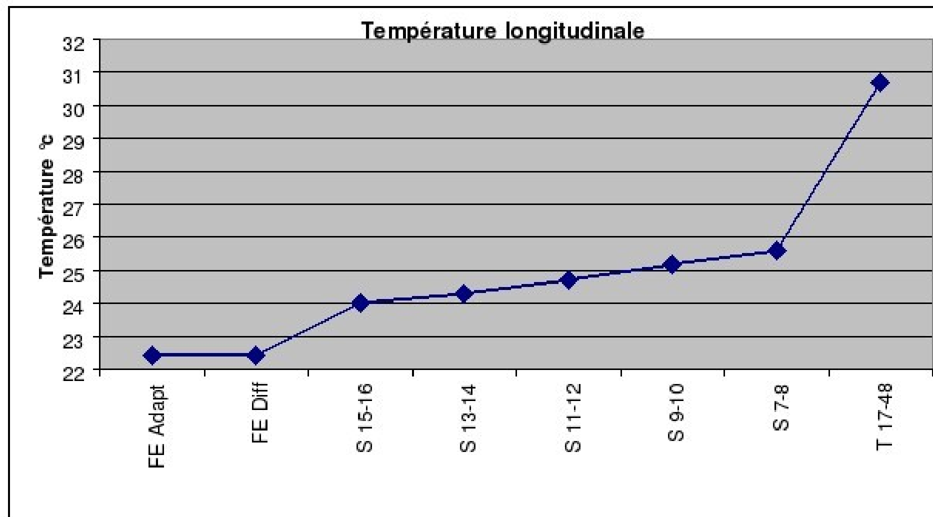
- Detector module realised (from mechanical point of view)
- Demonstrator subject to a thermal test

Thermal Test

To study thermal behaviour of detector module



Inserted Thermal Layer

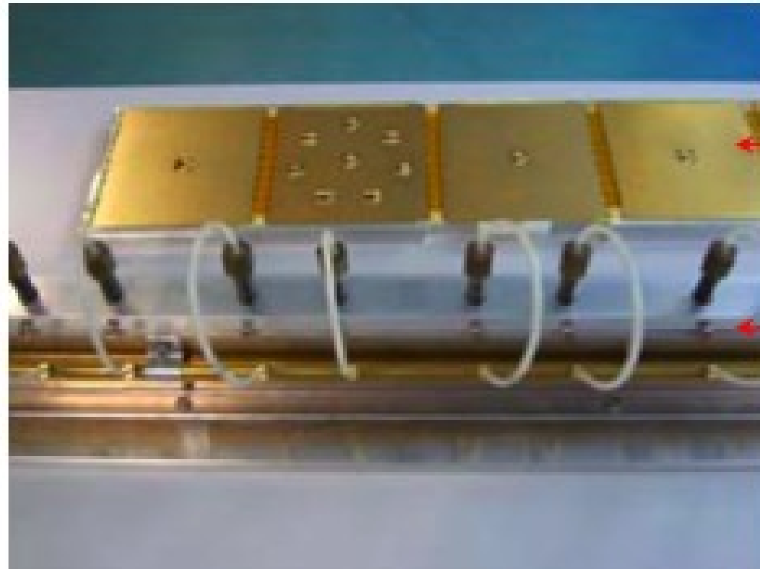


Ambient Temperature	22		
Alveolar Slot	Left	Middle	Right
External		23.5	
Upper	24.8	24.8	24.6
Lower	25	30.7	25.2
Bottom	25.1	25.2	25.1

- Detector Module realised from mechanical point of view
- Thermal test important for DBD

Assembly Tools – Handling of fragile layers

Handling by vacuum lifter



Line of ASU

Vacuum Lifter

Positioning of Vacuum Lifter on ASU Line

Vacuum Lifter

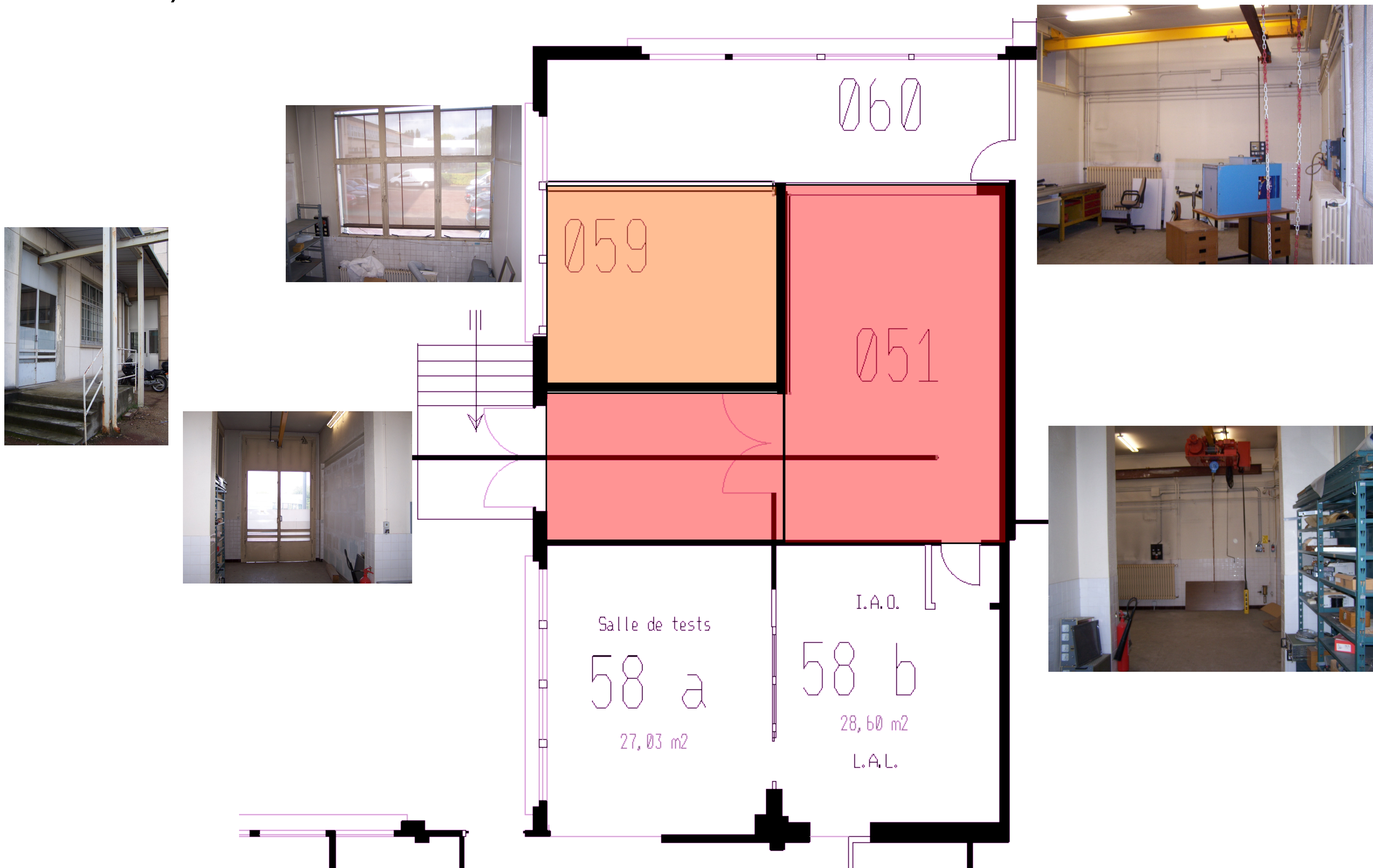
Line of ASU

(Careful) handling of ASU Line established

- Detector Assembly needs more tools and an assembly hall

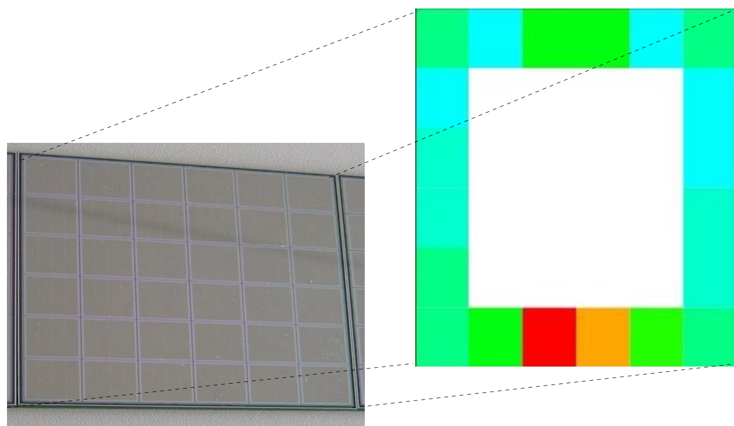
LAL allocated facilities for Ecal

Hall present state _(hall 051:47m2 and hall 051+ hall 059:64m2)

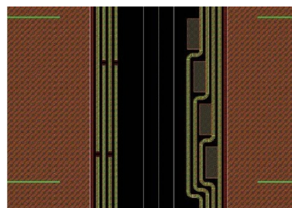


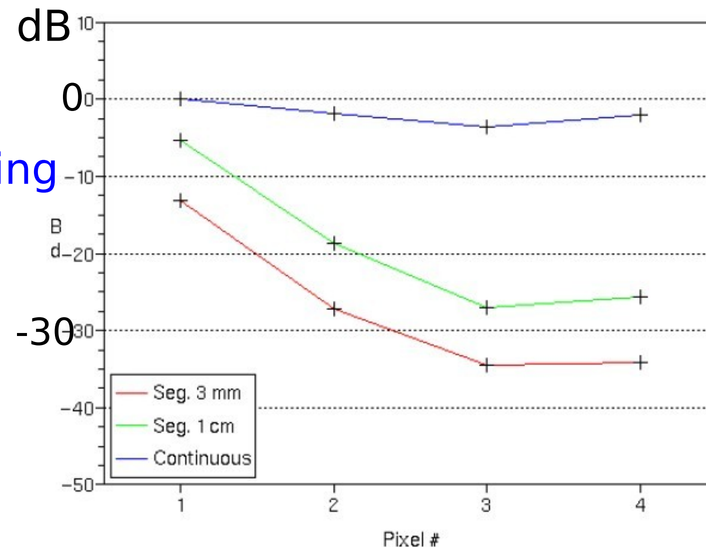
R&D for Silicon Wafers

Square Pattern in Wafer Response



Segmented Guardring



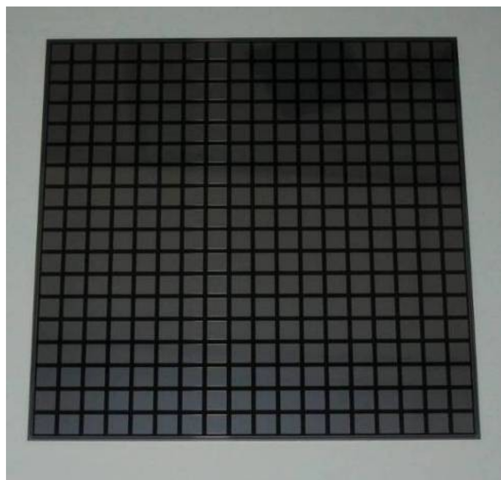


Xtalk Continous Guardring <-> Pixel

Attenuation of Xtalk

Beyond the Physics Prototype

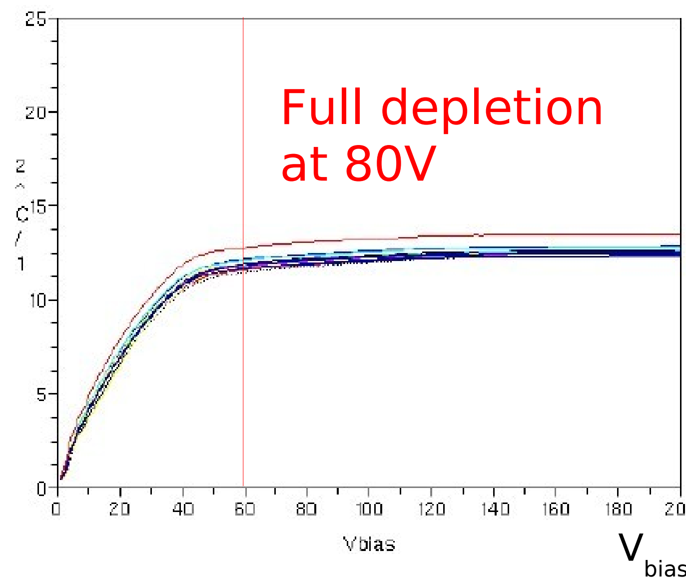
Wafers with smaller pixels



5x5 mm² pixels
~optimal "ILD width"

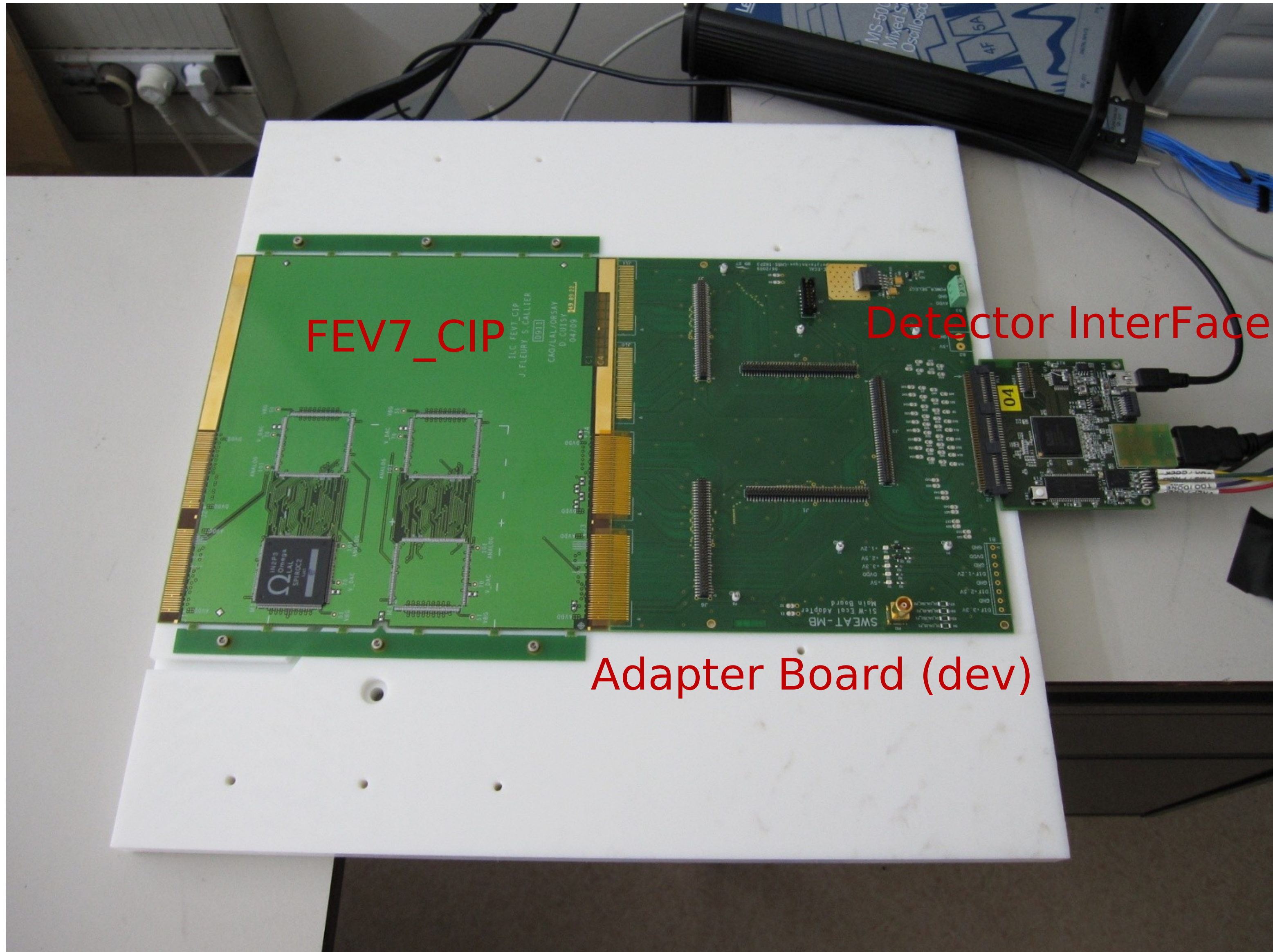
Thickness: 325 μm

Characterisation



Breakdown at ~500 V

First SLAB prototype (01/07/09)



Conclusion and outlook- Towards the EUDET Module

- Construction of alveolar structure for 'real' EUDET Module proceeds well

- Infrastructure for detector assembly about to be established
  Assembly hall with cosmics test bench at LAL

- Focus of getting the VFE accomplished

- “Shipping” signals out
  Interface to the DAQ is addressed

- Results with first ASU expected in the coming months
  Depends on development of DAQ interface

- (Crucial) Step from ensemble FEV7/SPIROC → FEV8/SKRIOC to be realised

- Cost for Silicon wafers is an issue (well beyond EUDET matters)

- Beam tests with EUDET Module (foreseen within AIDA)