Progress on FEV7/8 in France
Mechanical aspects

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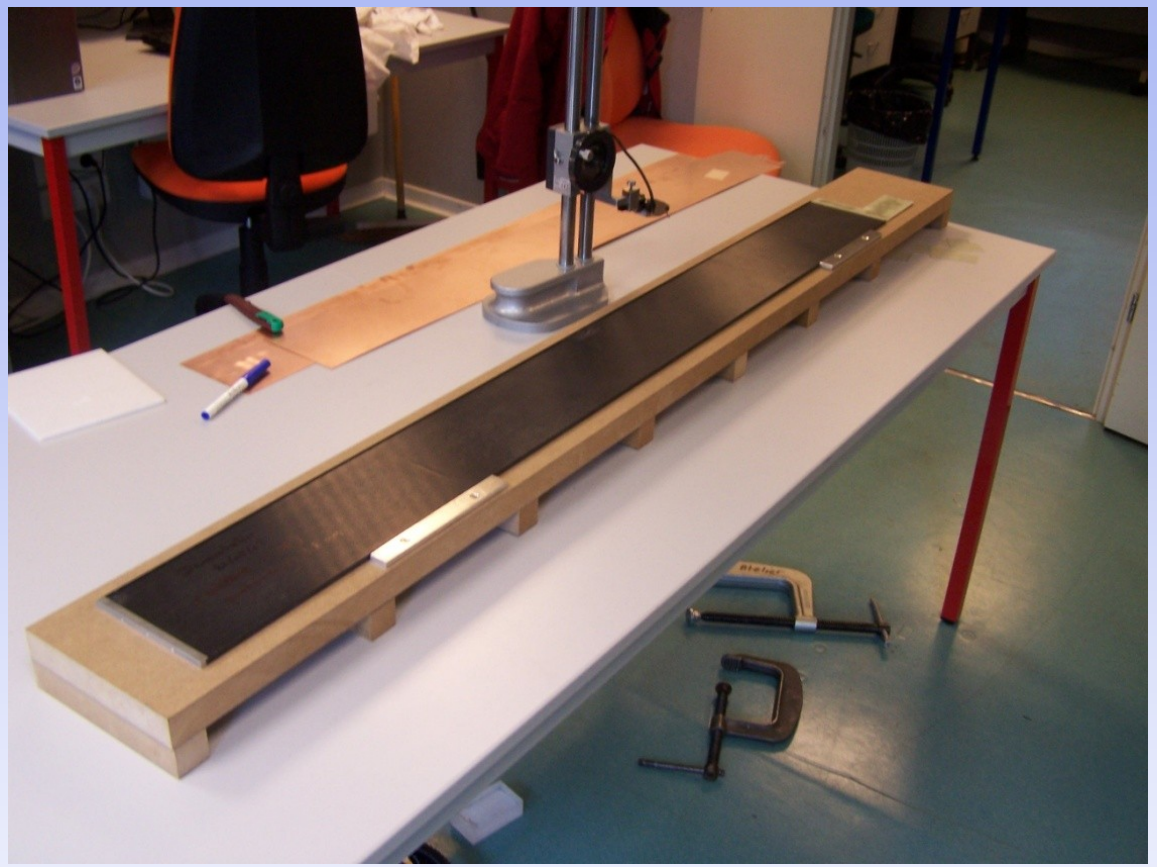
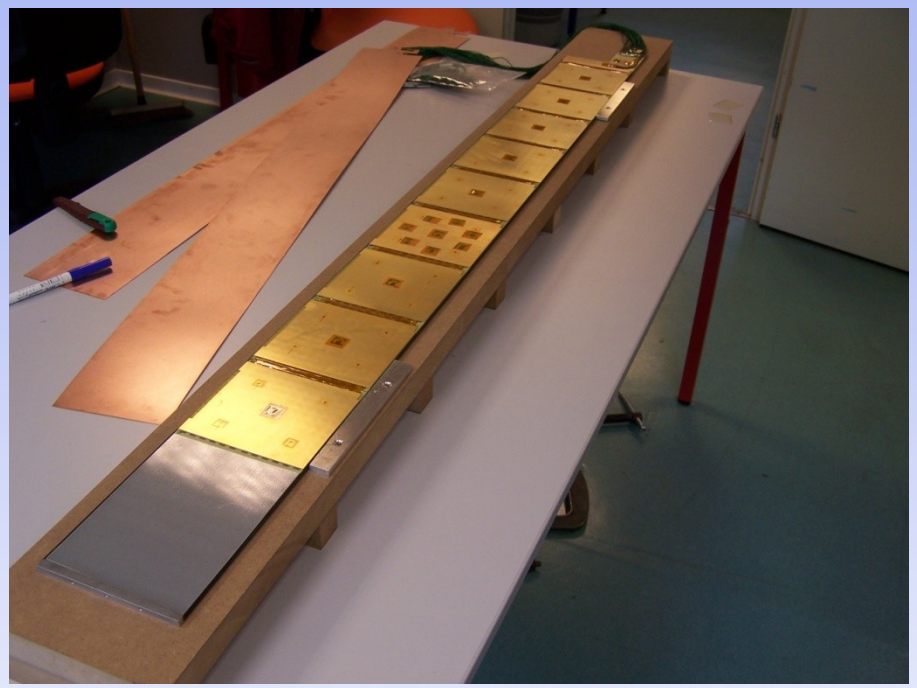
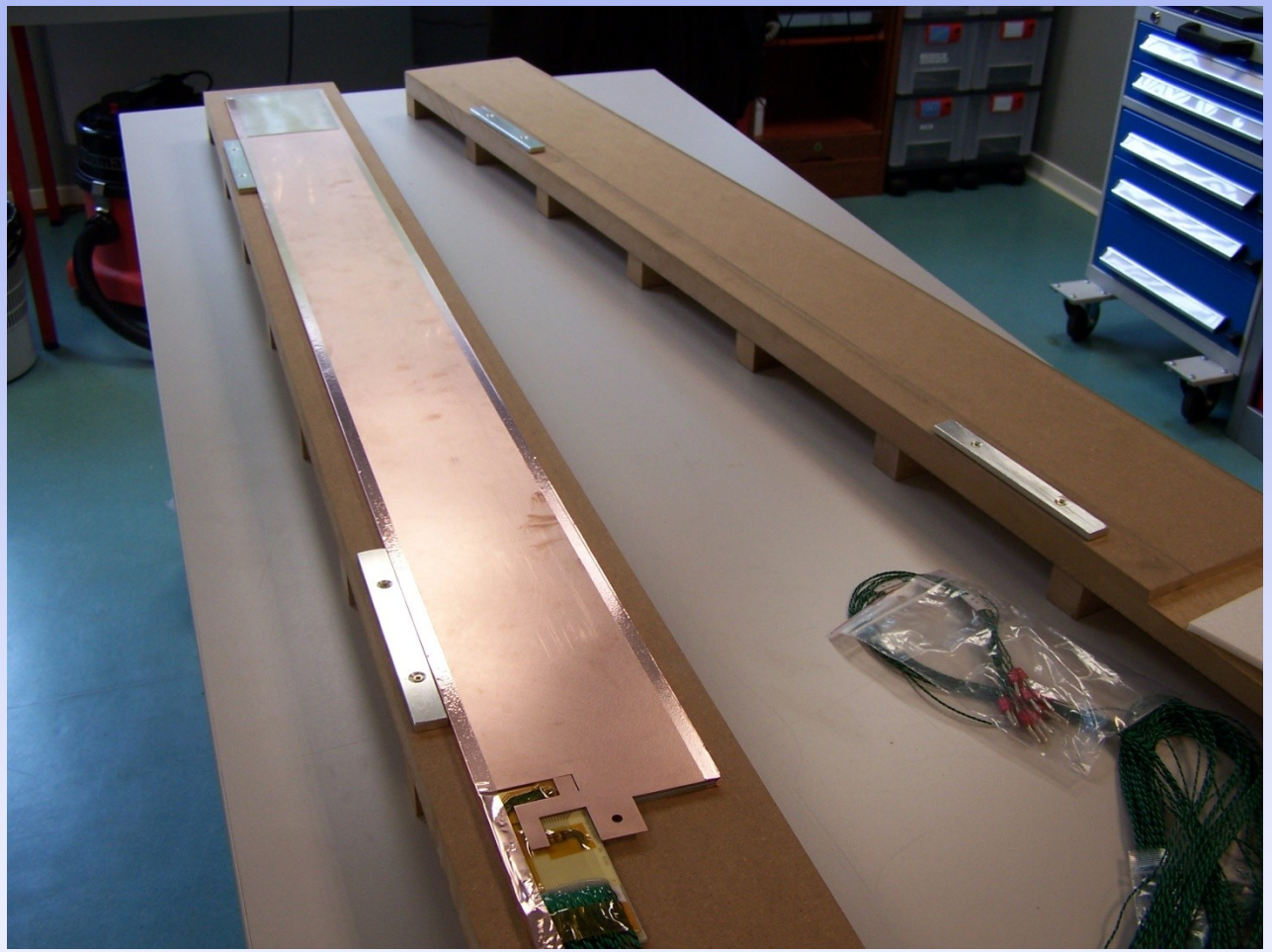
EUDET mechanics, General overview



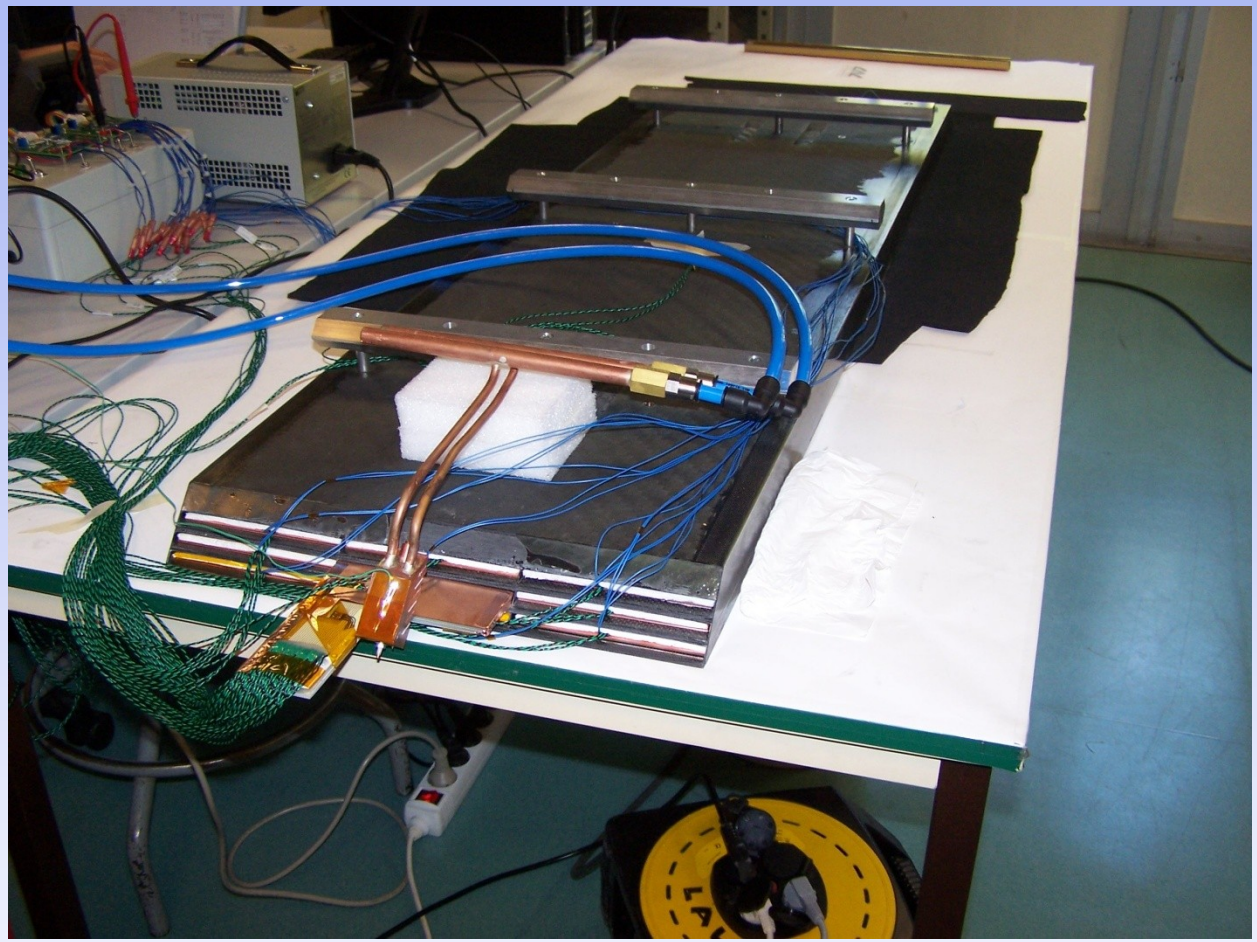
Tungsten Slab structure



Thermal test ASU (connected between them) inside Slab structure



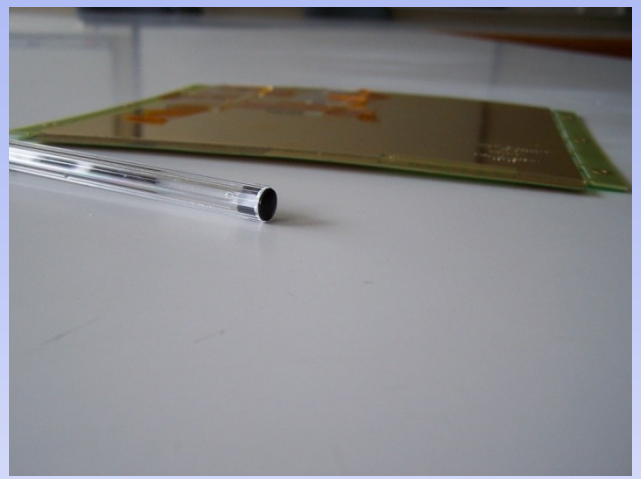
Finish thermal test Slab



Slab introduce into thermal test module

FEV7 Board, Mechanical current state

Planarity challenge



- **« Horse saddle shape » deformations**
- **2mm of deflection (order of magnitude)**

Causes

- **Bimetallic effect during elaboration**

(PCB = copper layers and composite layers)

Remark :

- *Elastic modulus or/and thermal expansion are differents according to direction in plane.*

(Horse saddle shape) .

Which consequences ?

Difficulties :

- Glue flat wafer on curved PCB.
- Connect bend out ASU between them
- Final Slab thinkness.

=> PCB must be hold flat during operations

Main issue was stress level in wafer and glue when PCB are release.

Question is : What PCB deflection was acceptable ?

Finite Element Methode modelisation of ASU

Objective : Estimate stress inside glue and wafer when ASU was released.

Materials proprieties

- **PCB**

Young modulus = 32 GPa

- **Conductive Glue** : EPO-TEK E4110

Young modulus = 3.6 GPa

Failure stress = 8.7 MPa

- **ACP** (Anisotropic Conductive Film)

Failure stress = 1O to 50 MPa

- **Si Wafer**

Young modulus = 185 Gpa

Failure stress = 140 MPa

Modelisation of PCB bending without wafer

•Only one quarter of PCB modelized : exploit symmetry of board.

•PCB separated in two pieces : 2 x 0.6mm = 1.2mm thickness
•(2 shells in model)

•Equivalent PCB material, E= 32 GPa, with unidirectional thermal expansion coefficient.

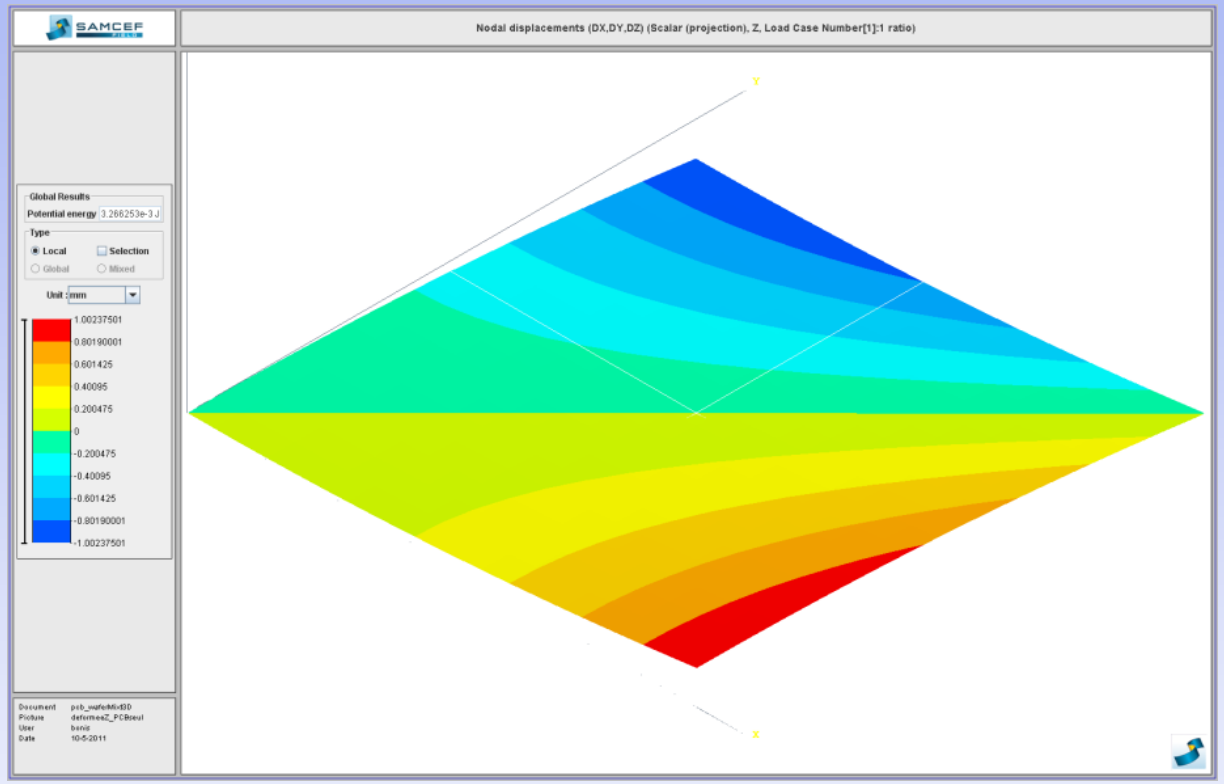
•The two shells are linked : nodes connected in all directions.

• Opposite variation of temperature was arbitrary imposed on shells: until deflection equal 1mm.

• The total PCB plan expansion is zero (no bimetallic effect with wafer when it will be added.

Preliminary results :

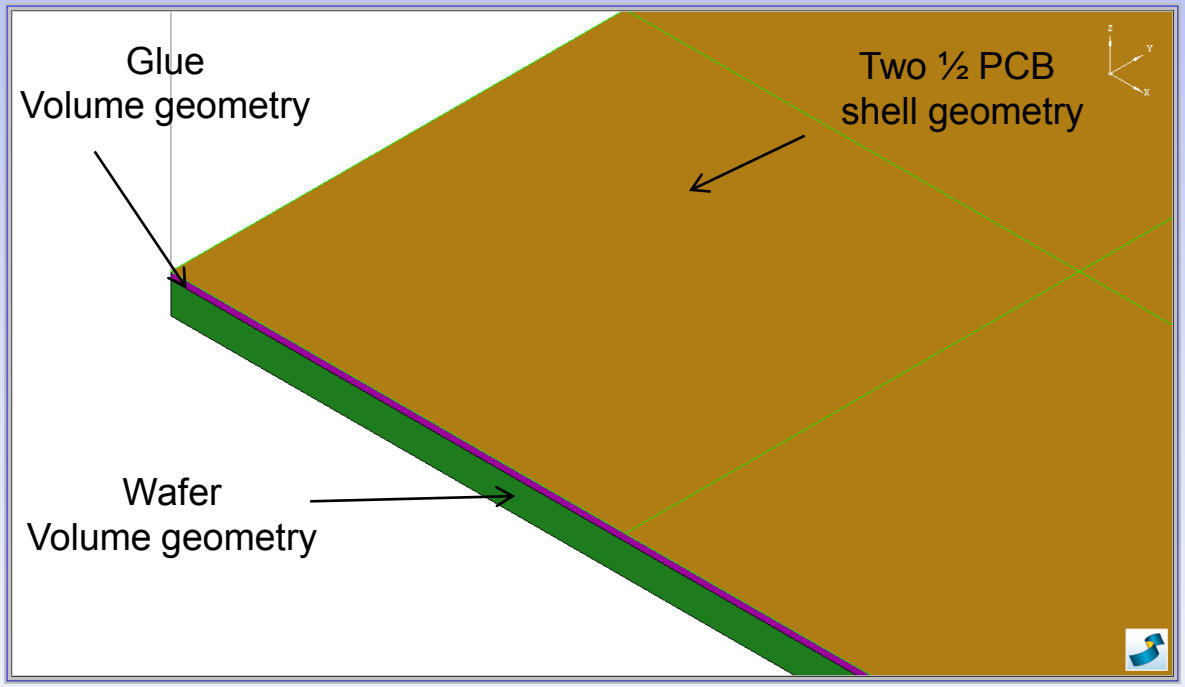
Simulate deformations and efforts of PCB



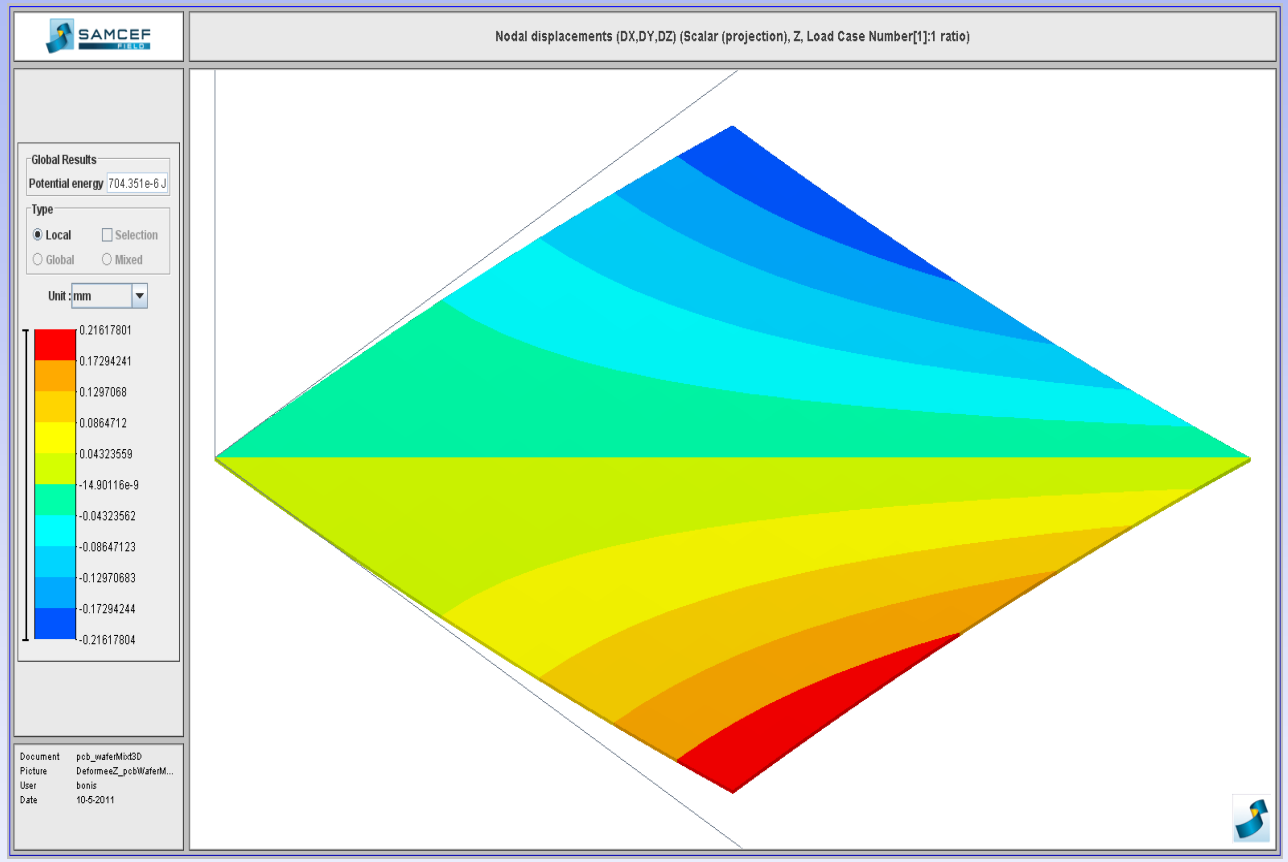
Deformations of ¼ shell PCB (2 symmetries applied).
Maximale Deflection was 1mm.

ASU modelisation

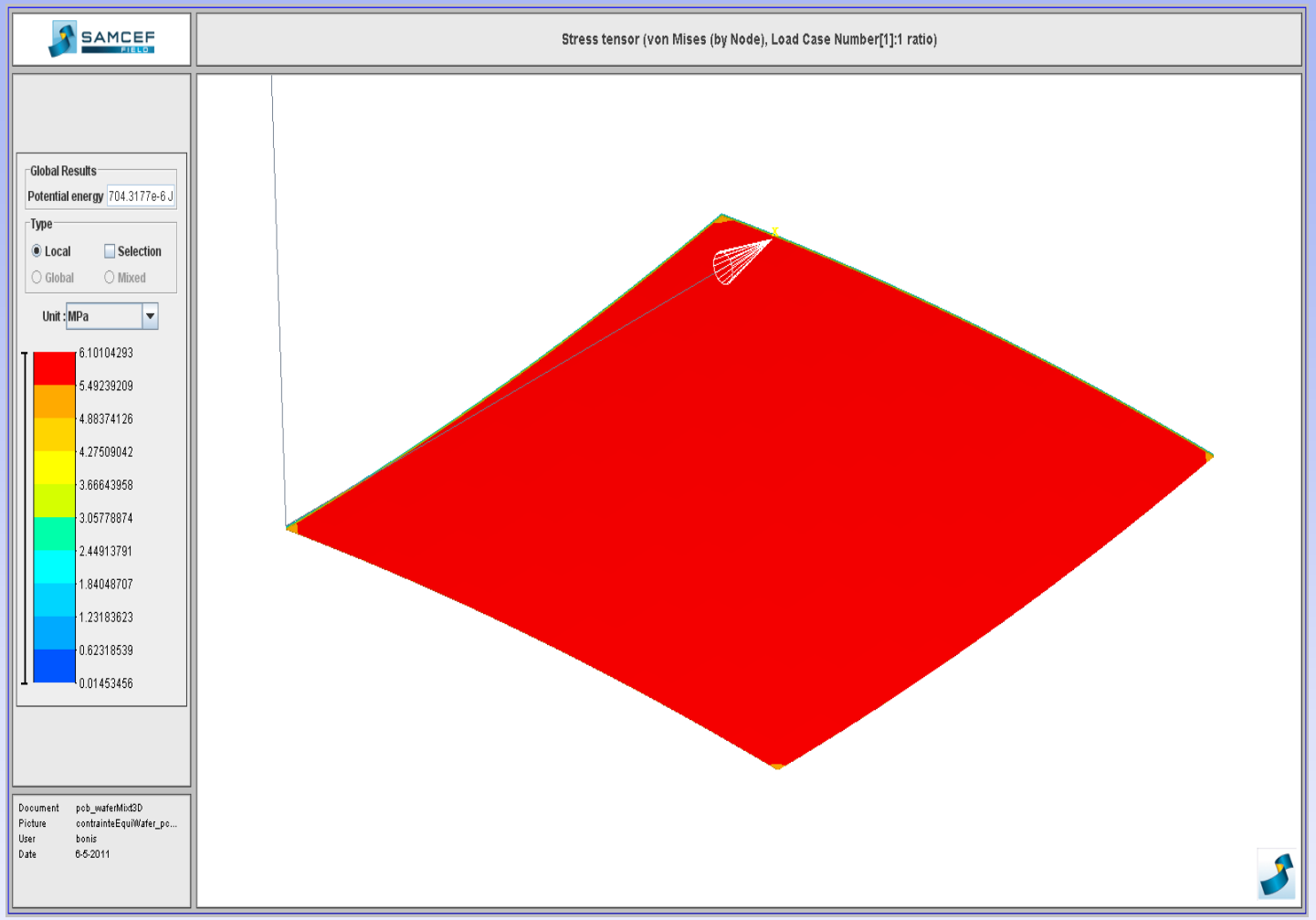
Glue and wafer (two 3D solid volumes) was connected to PCB shell.
Same variation of temperature than previously was imposed on the 2 half PCB shell.



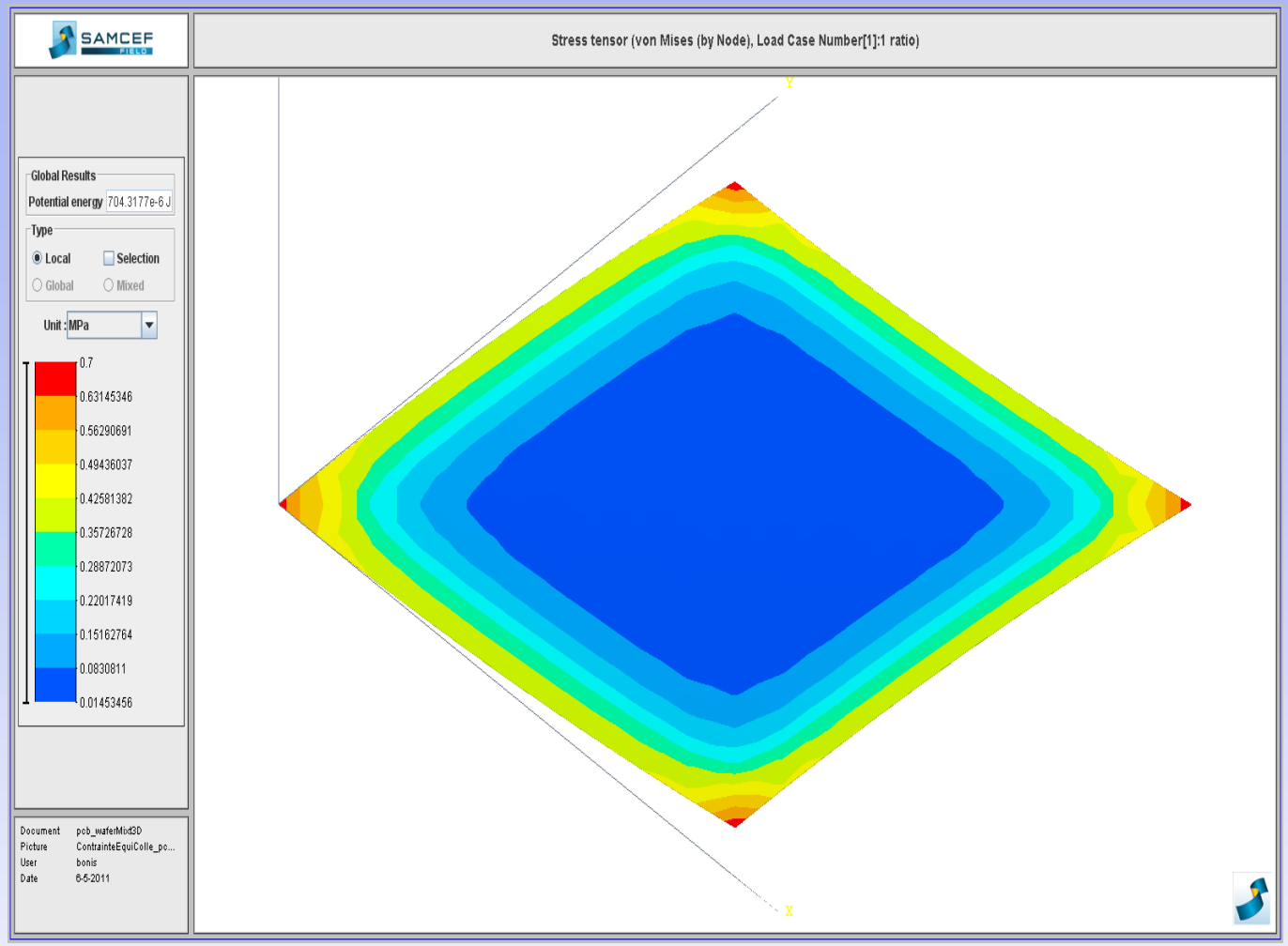
ASU simulation Results



ASU Deformations (in direction z) of ¼ PCB-wafer
Max deflection was 0.21mm



Von Mises Equivalent Stress in wafer
Max stress = 6.1mm



Von Mises Equivalent Stress in Glue
Max stress = 0.7MPa

With PCB initial deflection = 1mm

Stress in Wafer:

• Calculated Maximum stress is 6.1 MPa.

➢ Failure flexion stress of wafer is 140 MPa. => OK

Stress in Glue:

• Calculated Maximum stress 0.7 MPa.

➢ But in case of **points of glue**, totale glue surface was only 20% of wafer surface.
And, glue drop shape introduce a stress intensity factor (K = 2 or 3 minimum).
So, the **Effective stress in glue** become near **7 or 10 MPa**.
Failure stress of glue is 8.7 MPa. => OK !
With security coeffecient of 2, **initial PCB deflection must be less than 0.5 mm**

➢If **ACF** can be used for PCB-wafer connexion.
Failure stress of ACF is 1O to 50 MPa. => OK

Ways to minimize PCB deflection

- Balance :
  - Each core must be as symmetric as possible
  - Cores must be as similar as possible.
  - Cores with equivalent mechanical caracteristics.

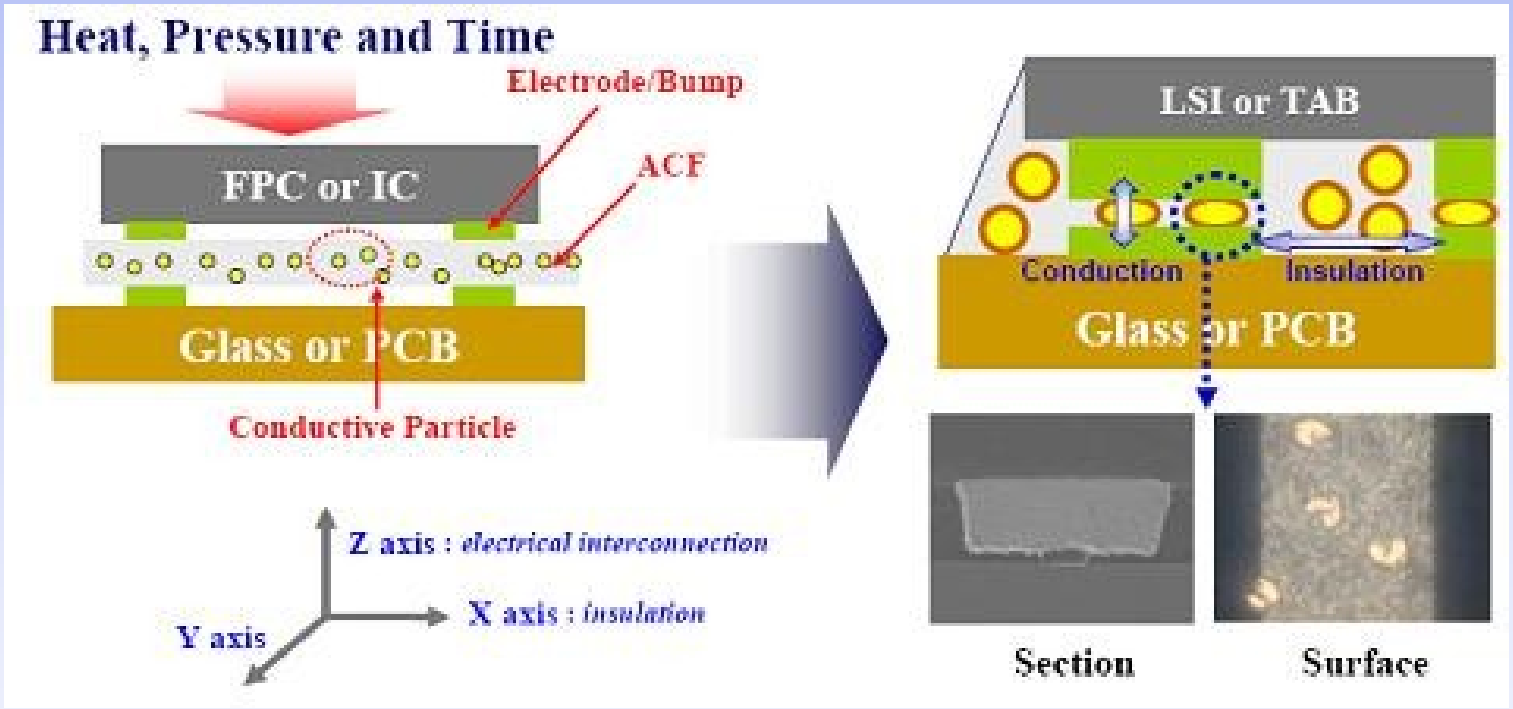
    FEV7 composition :
    • Cover part of PCB, on the top:
    300 micron of preg with 40 micron of copper
    => 13.33% of copper
    • Main pcb
    525 micron of preg with 231 micron of copper.
    ⇒44% of copper.
    ➢ It's perhaps better to introduce more copper in cover part of PCB

- Decrease process temperature when possible

=>Think about mechanical constraints during electronics design

Challenge : Less than 0.5mm deflection if possible.

ACFprinciple

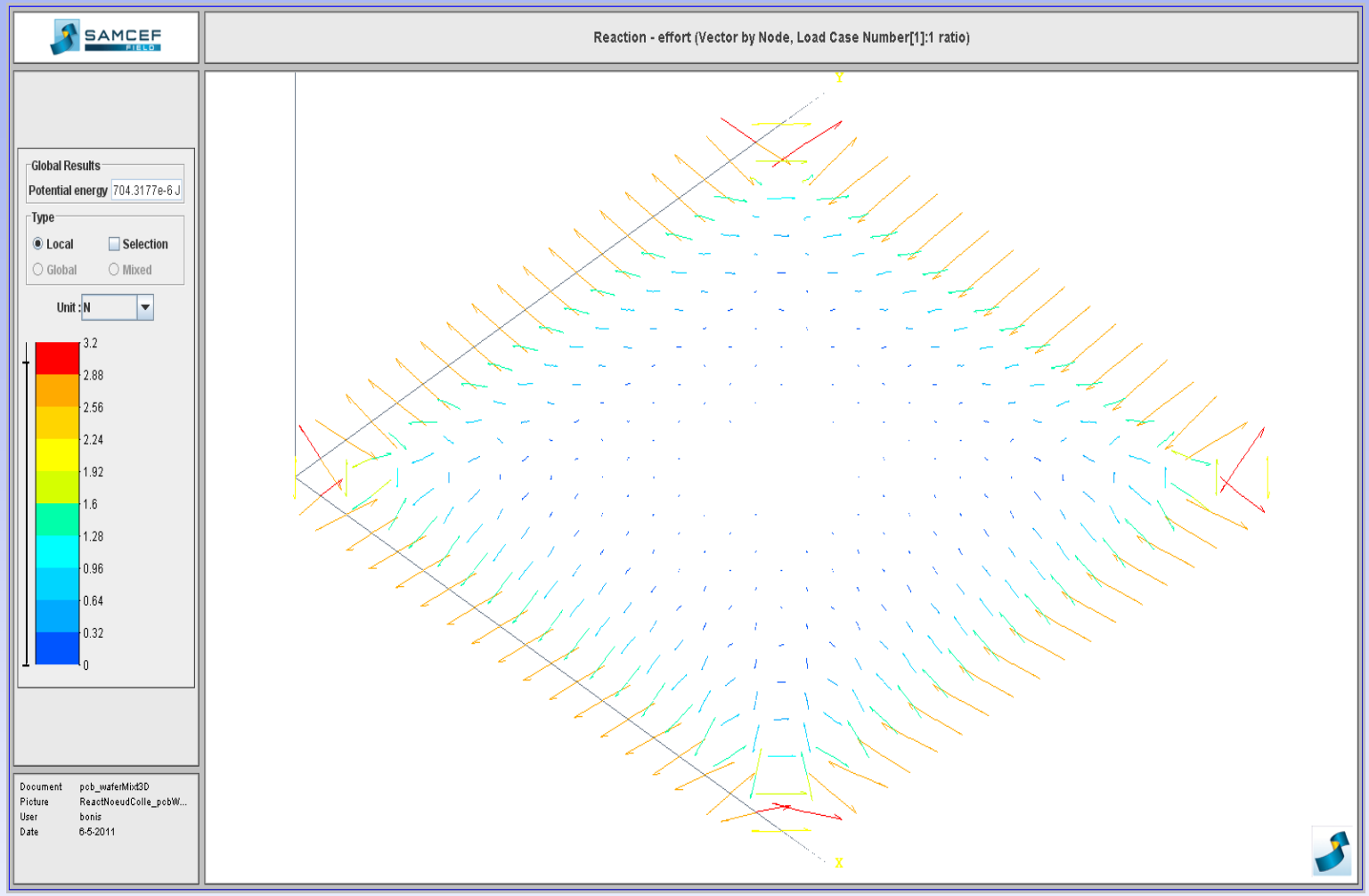


Common ACF parameters

Assembly Type	Adhesive Type	Time(Sec)	Temp (° C)	Pressure
Flex-on-Glass (FOG)	Epoxy	10-12	170-200	2-4MPa▲
Chip-on-Glass(COG)	Epoxy	5-7	190-220	50-150MPa※
Chip-on-Flex (COF)	Epoxy	5-10	190-220	30-150MPa※
Flex-on-Board (FOB)	Epoxy	10-12	170-190	1-4MPa▲
Flex-on-Board (FOB)	Acryl	5-10	130-170	1-4MPa▲
Flex-on-Flex (FOF)	Epoxy	10-12	170-190	1-4MPa▲
Flex-on-Flex (FOF)	Acryl	5-10	130-170	1-4MPa▲

Towards Chip encapsulation

- Bonding Wire were at 0.2mm from PCB surface.
- Resin Aradilte 20/20 used (the most flowing)
- Hopeful first test (flat surface aquieved)
- Next test under vaccum to avoid bubbles



Node reaction in glue points (equivalent pads positions)