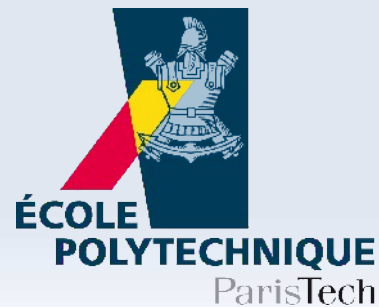


# DAQ2 status report

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**Calice meeting  
15/09/2011**

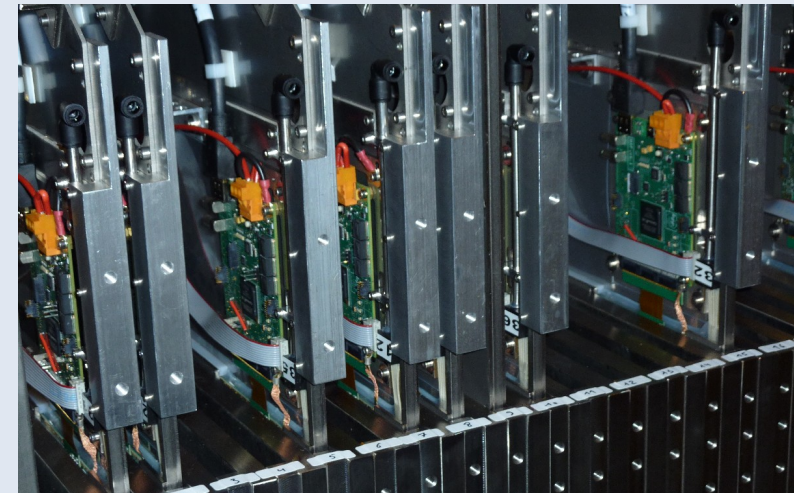
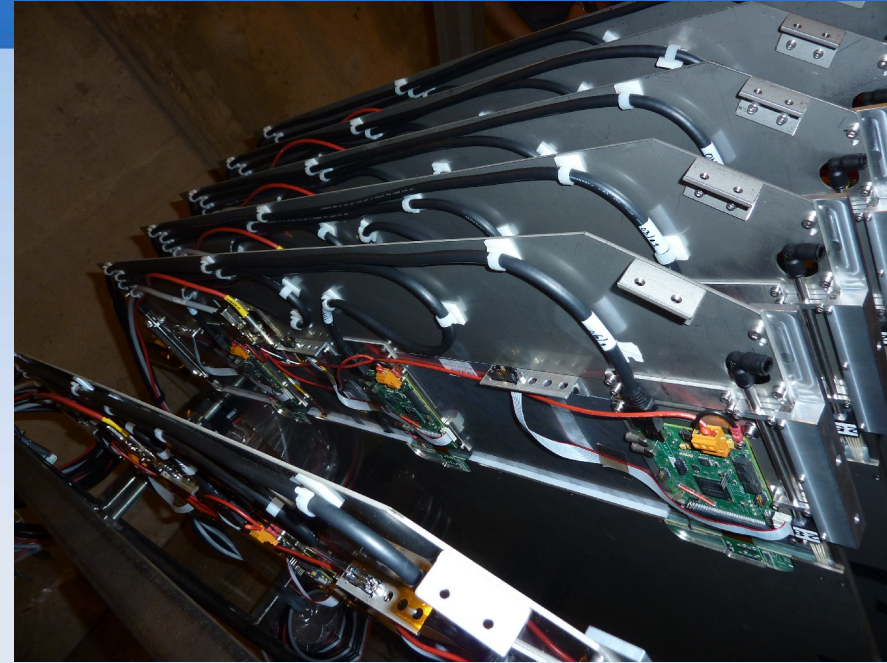


# Plan

- DAQ2 integration for SDHCAL
  - ▶ Some words on June TB
  - ▶ (Running) status of SDHCAL integration
- DAQ2 for ECAL
  - ▶ See Elmaddin Guliyev presentation
  - ▶ Development tools
    - ◆ images from Muriel
- Still missing Plans
  - ▶ SW plan...

# June test beam

- DAQ should have been ready for June SDHCAL TB
- All elements were ready
  - ▶ But without time for extensive tests
  - ▶ But not robust enough: blocking condition were just too frequent for a large system
  - ▶ Some critical bugs found afterwards (mostly in the SW)
- Effort put on USB readout
  - ▶ Required relinking of DIF by blocs of 6-7 chambers (21 DIF).
  - ▶ Synchronisation of data difficult
  - ▶ slow readout rate
  - ▶ but at least some data.
- All summer has been very busy improving the stability.
  - ▶ Huge effort from **IPNL, LAPP and LLR**
  - ▶ mid-August → running of 7 chambers in Lyon for > 24h without crash.



# DAQ2 for SDHCAL

- This week perspective:
  - ▶ SDHCAL moved to PS last monday
    - ◆ Not a single chamber broken
  - ▶ Cabling and mass checking done on Tuesday
  - ▶ Readout on 19 chambers was problematic with some of the DIFs. 1 DCC found unstable (PS problem ?)
  - ▶ Re-check from 6 chambers → 11 OK on Tuesday on 1 LDA
  - ▶ 21 chambers running on 2 LDAs during the night for long runs
    - ◆ Configuration loading instability
  - ▶ Improvement on stability with 2 LDAs
- Present focus (next days): Fast recovery of blocking conditions (reset of cards)
- To be done (lower priority)
  - ▶ Integration of DAQ1 code to access beam information
  - ▶ writing of LCIO files to grid (DAQ1 scripts available)
  - ▶ Running DB integration

# Running modes

- Running in «**test beam**» mode
  - ▶ All ASIC in acquisition mode (with auto-triggering)
  - ▶ on RamFull of ANY of the CHIPS
    - ◆ BUSY signal generate a reset of all ASIC (Centralised by the CCC)
    - ◆ Acq is resumed
  - ▶ On external trigger (beam hodoscope)
    - ◆ ASIC stops acquisition and sends data
    - ◆ Acq is resumed
- We are very sensitive to noise
  - ▶ non linear behaviour found vs # of chambers
  - ▶ Sequencing done by the CCC
- Running in ILC mode might be an alternative solution
  - ▶ Noisy parts (Elec or detector) would just be blind
  - ▶ Requires the BIF to work.



# DAQ2 for ECAL

- Readout made by a mix of libLDA line commands + Python scripts

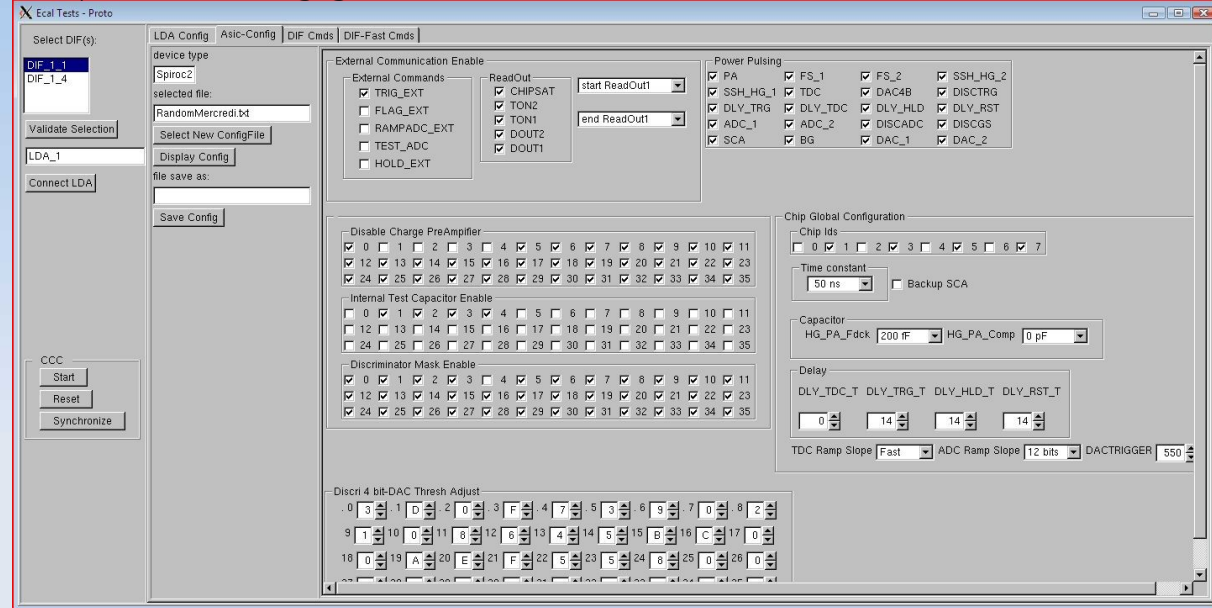


- ▶ See Elmaddin Guliyeu presentation tomorrow afternoon
- Soon to be replaced by debug tool (next slide)
- Integration with XDAQ in a few weeks (after stabilization for SDHCAL)

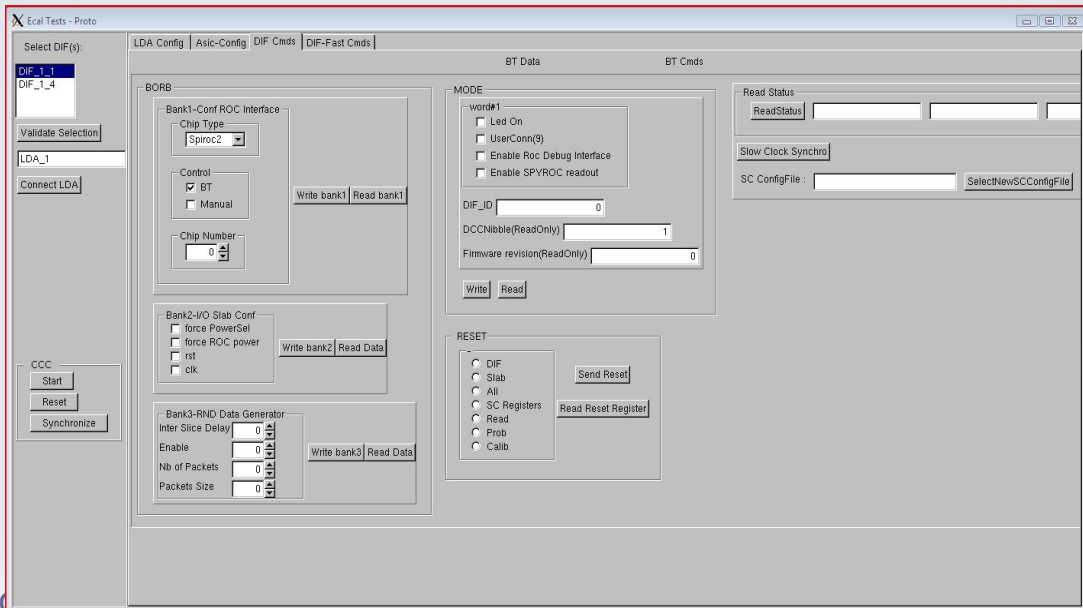
# DAQ2 for ECAL

- Development & low level debug tools (M. Cerutti, LLR) «GUI to libLDA»
  - ▶ Running modes
  - ▶ > config generator for SPIROC
    - ◆ Code for XDAQ integration
  - ▶ Bloc transfert & fast commands
  - ▶ (readout of data) → file
- Versatile debug tool
  - ▶ Tree of LDA/DCC/DIF

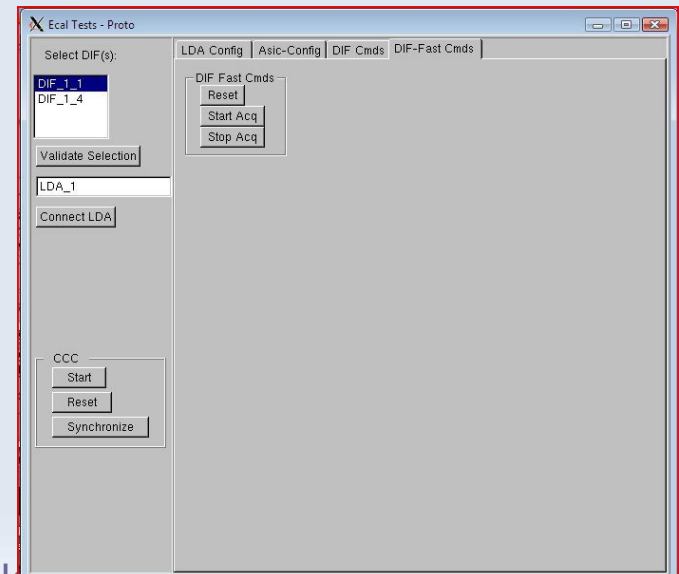
SpiROC config generator (~ S. Callier LabView translation)



Block Transfer Commands

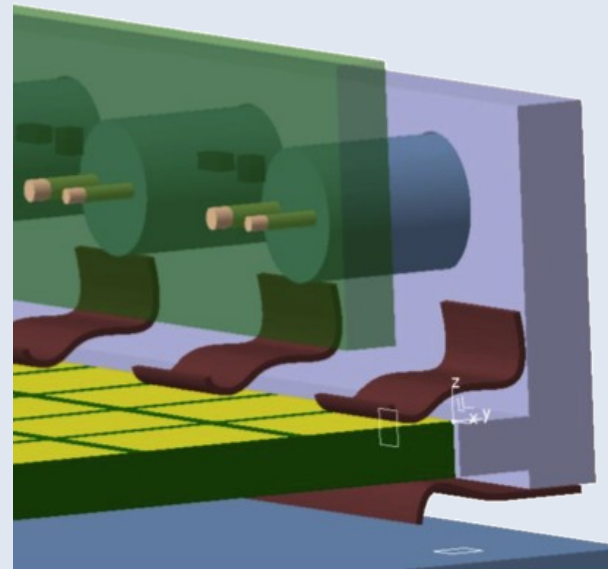
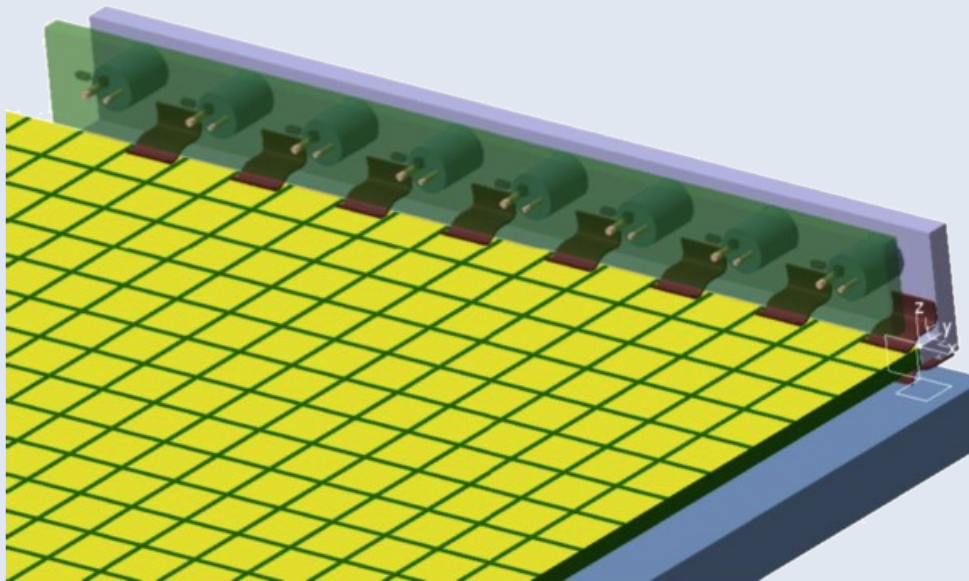


Fast Commands



# BIF

- Reminder: recording of hodoscope data(scint+ Č bits) in the same format that calorimeter → for back in time analysis
- Intermediate solution:
  - ▶ Use SDHCAL ASU to record hits with TimeStamp
  - ▶ Proof of principle this summer: NIM signal recorded on 1 PAD.
  - ▶ Injection HW being worked on:





# Longer term plans

- Clean-up code

- GigaDCC

- ▶ Replacement of LDA:

- ◆ Mechanics, CC coupling, licence

- ▶ many progress this summer thanks to S. Rateau (engineer student under Rémi's supervision) on the GigaEth bloc

- ◆ license free version to replace the no-more supported LDA one.

- ▶ Remains

- ◆ FW integration : GETH ↔ DCC (Franck Gastaldi)
- ◆ Card design (Mod of DCC) → VME format.

- Replacement for the CCC

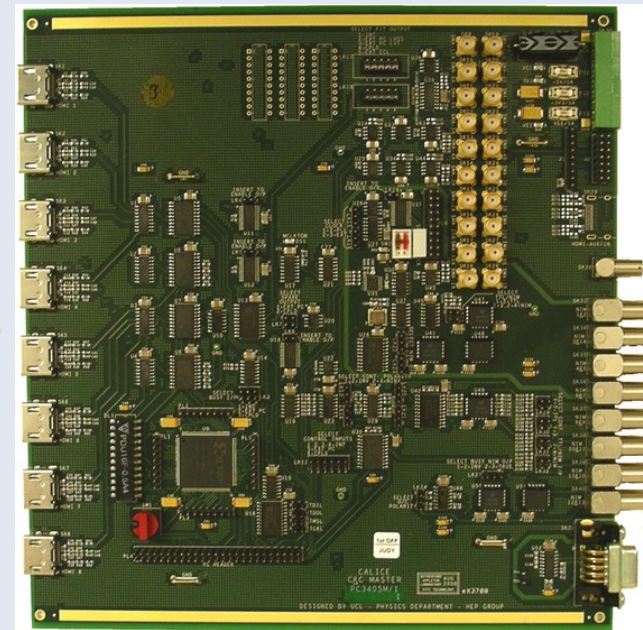
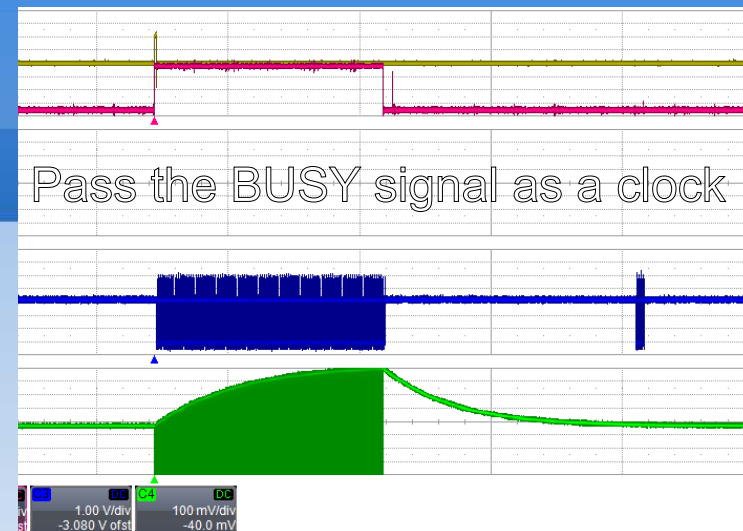
- ▶ CCC HW = mix of "Hard coded" path (clock & BUSY) & small CPLD

- ▶ Interface by RS232 (sic!)

- ▶ Current use (logic on BUSY signal, sequencing of system) ≠ from foreseen use.

- ▶ Should be redone for the AIDA DAQ

- ◆ Dialog with EUDET TLU (Trigger Logic Unit)



# Summary

- DAQ2 for SDHCAL works for ~2/5 of detector (more in the next days)
  - ▶ Focus is on stability improvement
    - ◆ Seek & destroy bugs
      - Electrical, Transmission, SW
- DAQ2 now usable for table top test (ECAL)
  - ▶ User friendliness improvement
- Integration in XDAQ
  - 1) Config Generation (“scramble” code for ASIC) Human params → bistream
    - ◆ Exists for SPIROC
  - 2) Ad-hoc sequencing (CCC coding)
  - 3) Decoding of RAW data for online monitoring
    - ▶ «wait for end of SDHCAL f work»
- Preliminary work on upgrade of HW has started
- Work on AIDA DAQ (compatibility with EUDAQ) to be started very soon [october] (report due in January).