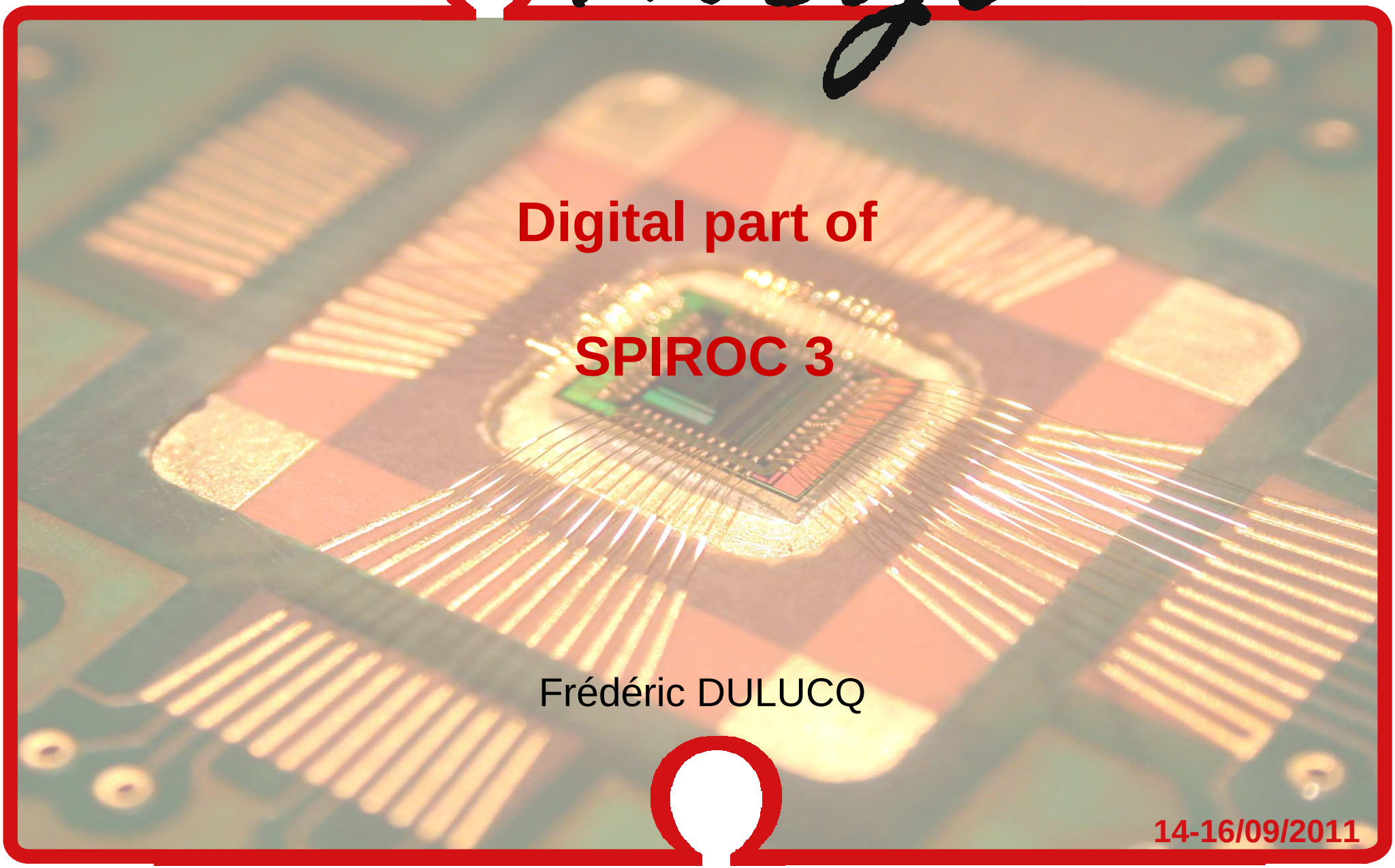
IN2P3 CSNSM LAL LPNHE IPN Orsay

Omega



Digital part of

SPIROC 3

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Orsay MicroElectronics Group Associated

Digital part outlines

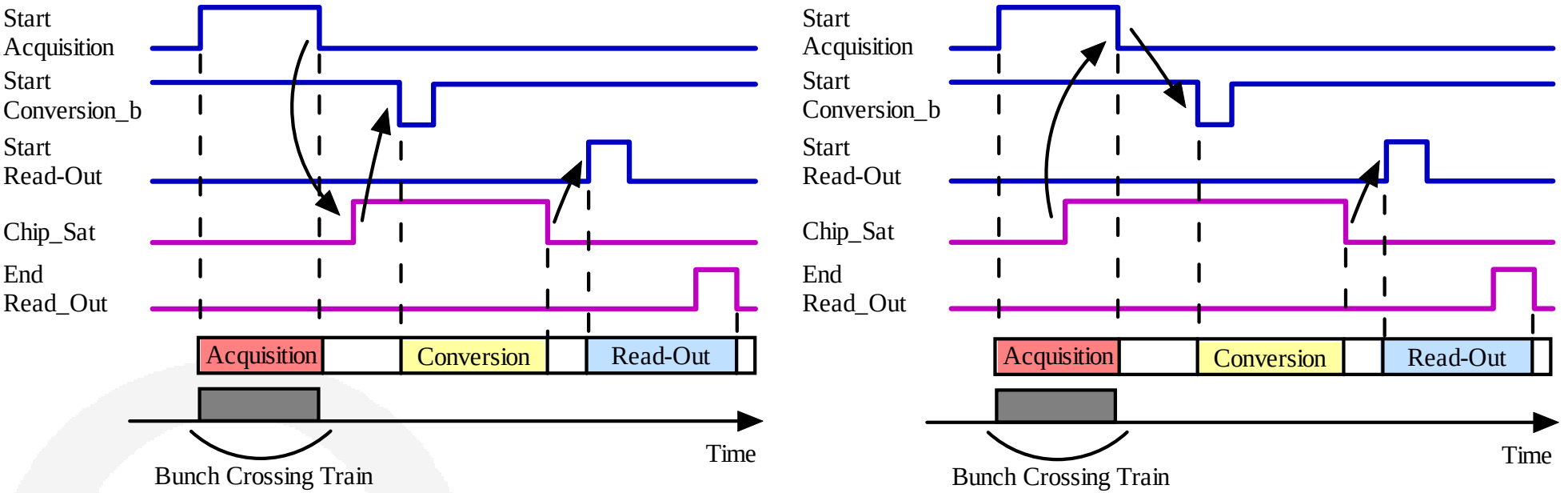
- **What's Not Changed (NC):**
  - Start Acquisition / Conversion / Readout sequence
    - Possibility to use a RazChn signal
    - Readout on a OC line

- **What's Changed/Improved (CI):**
  - New time measurement (PARISROC like)
    - New A/D Wilkinson conversion management
    - SCA depth decrease to 8

- **What's New (N):**
  - Independent channel management
    - New memory mapping
    - Only hit channels are readout (zero suppress)
  - I2C slow control
  - Possibility to use "roll" mode

(NC): DIF Management like all ROC Chips

- Same driving sequence for all previous ROC chips



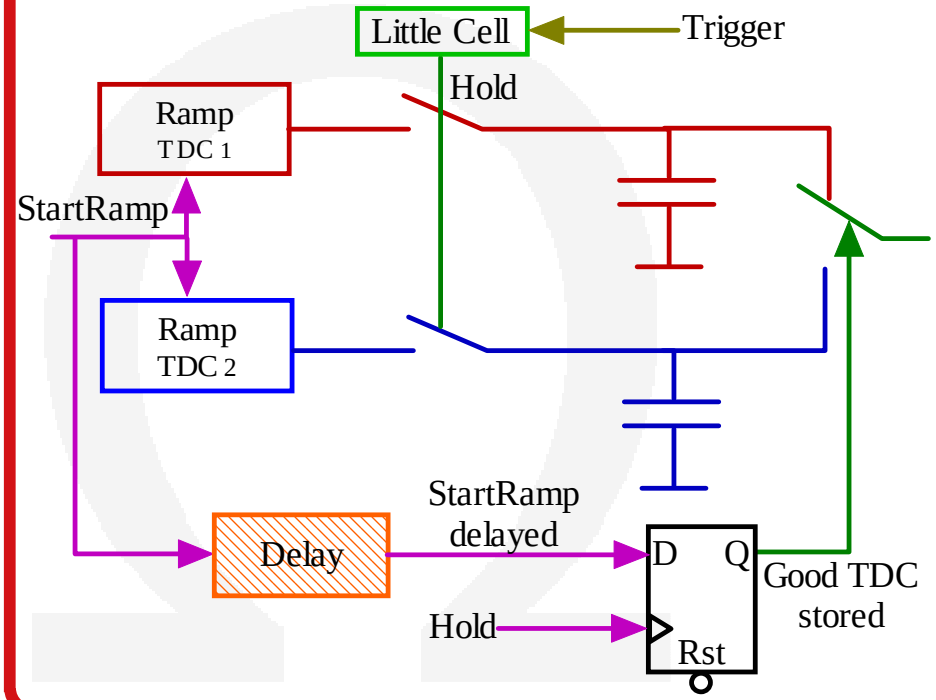
- ChipSat allows to know:
  - When to start the conversion after the falling edge of the StartAcq: ChipSat @ '1'
  - When the conversion is finished: ChipSat @ '0'

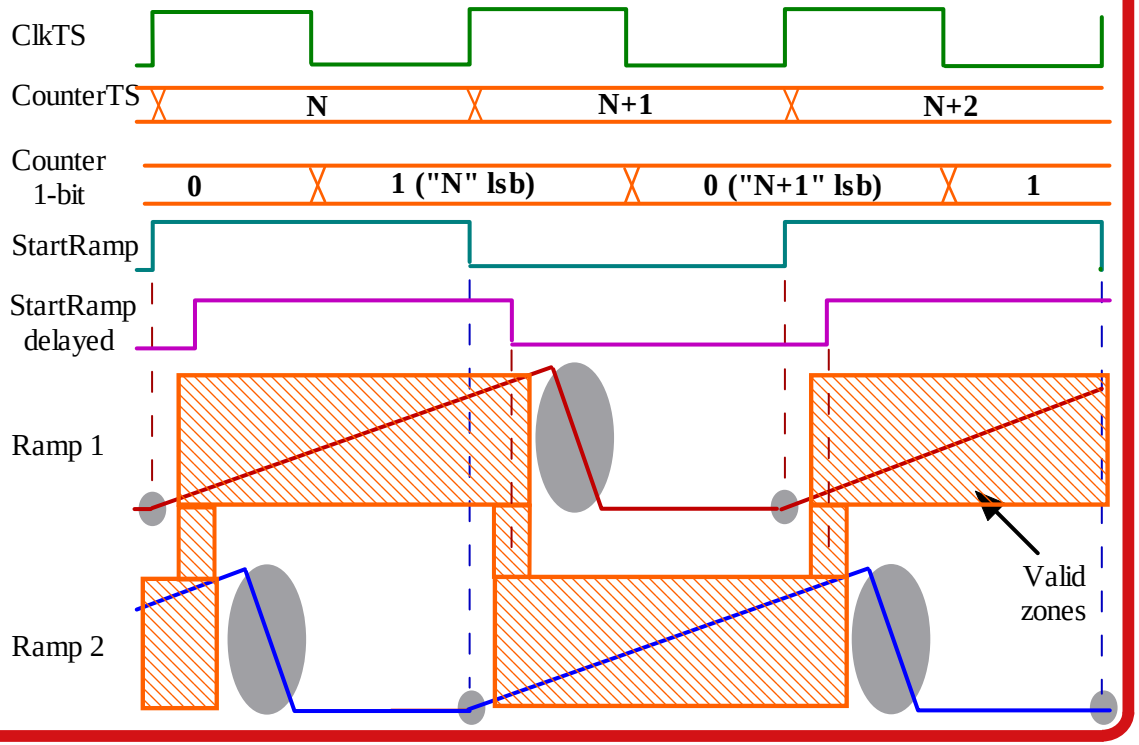
- If one chip stuck the ChipSat, DIF always has the possibility to use a timeout

(CI): New time measurement

- New fine time:
  - The 2 ramps are stored
  - Overlap between the 2 ramps and also the 2 counters
- Data readout:
  - 2 BCID counters (12+1 bits)
  - The good ramp selected internally (converted by ADC)

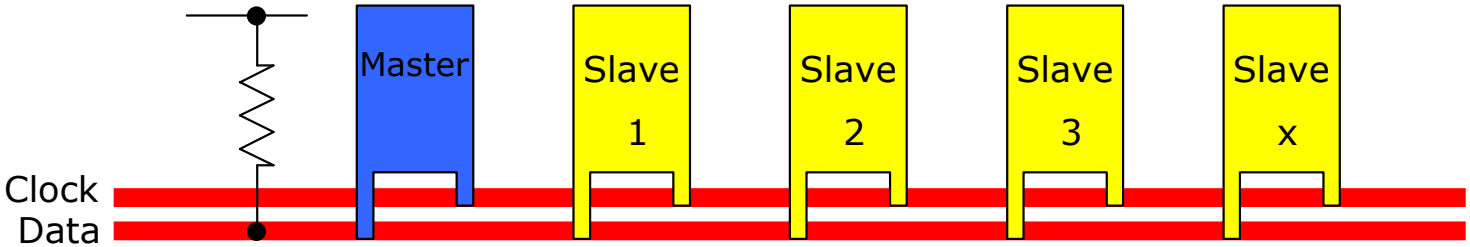
If "**Overlap zone**" and "**Lsb of 2 counters different**" then
Time = (CptTS-1) + Ttdc
else **Time = CptTS + Ttdc**





(N): I2C slow control

- Only 2 lines (Data et Clock) + GND (0V, 3.3V) + Reset
  - Unidirectional «Clock»
  - Bidirectional «Data» line : open collector with external pull up
  - 7-bit address + 1 general call address



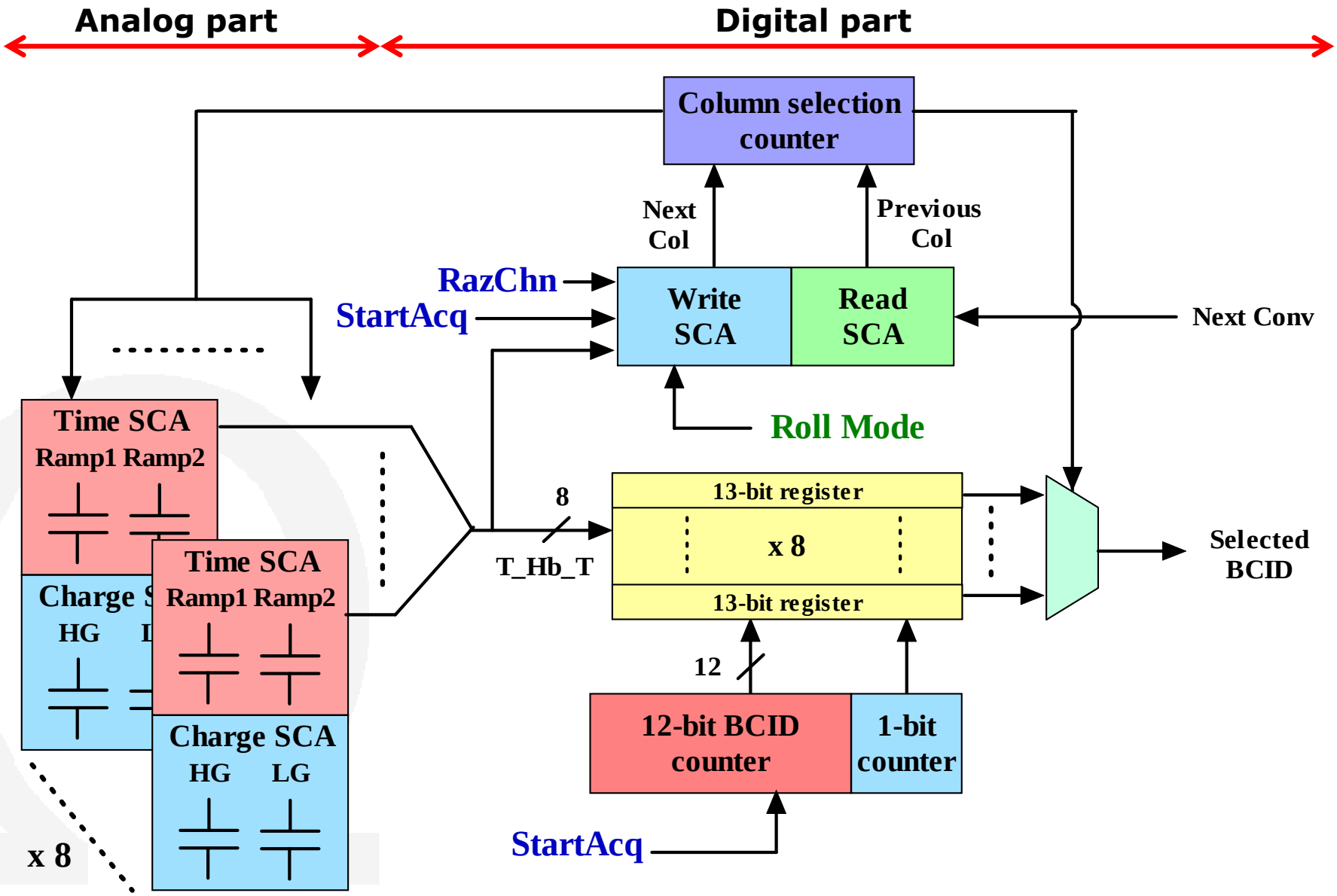
- Write frame:

- Read frame:

- Others:
  - Read back possibility (non destructive)
  - Possibility to use old slow control as a backup (shift register)
  - 2 x (I2C ports) / chip

(N): Independent channels

- Block diagram of the acquisition for 1 channel



(N): Memory mapping

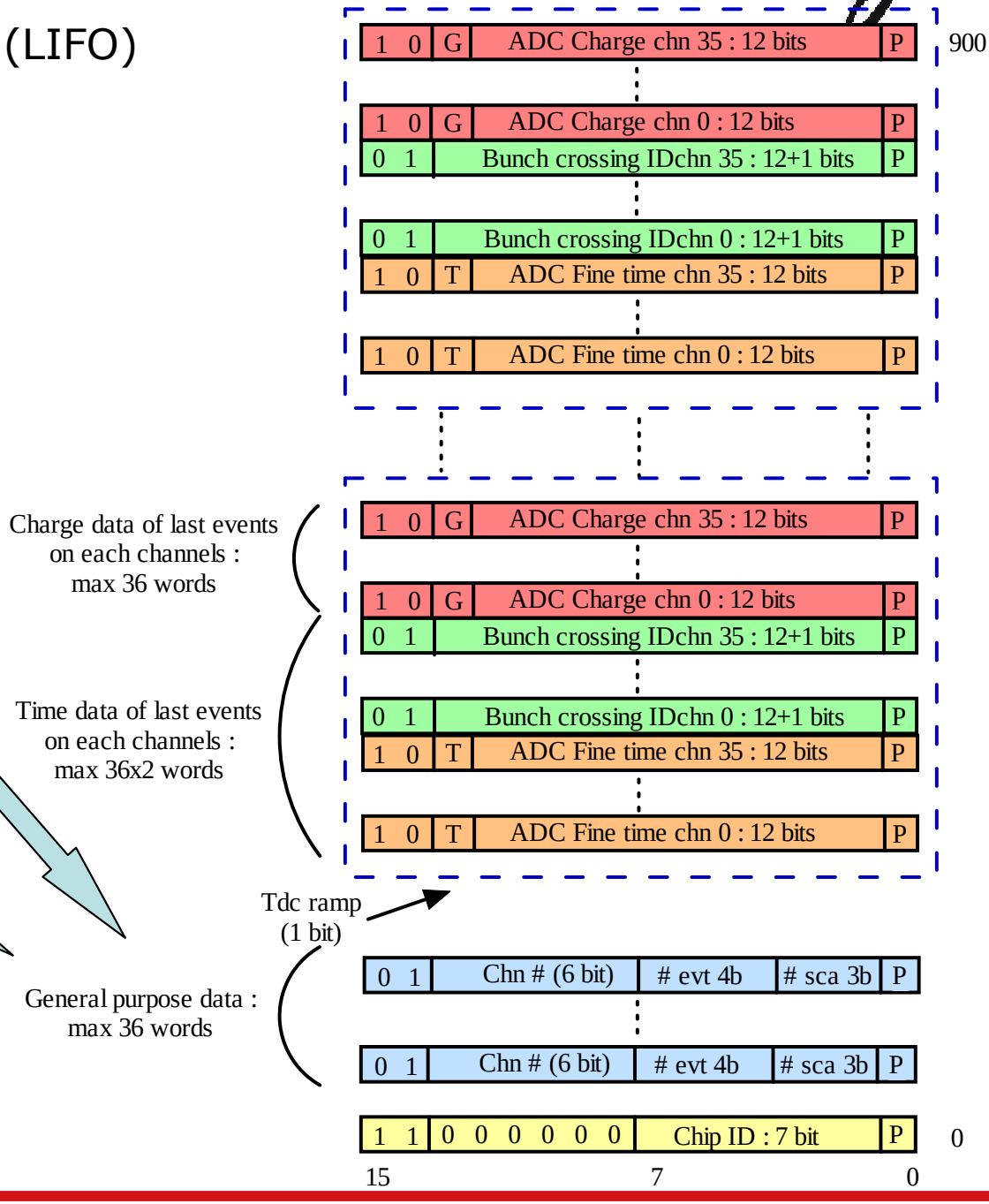
- Readout is MSB first and @ 0 first (LIFO)

- Amount of bits in memory:
  - No event ➔ no data
  - Even parity bit / 16-bit word
  - Else depends on general purpose data:
    - # channel hit = N
    - # events in chn = Evt_i

$$16*[1+N+\sum_{i=0}^{35}(3*Evt_i)]$$

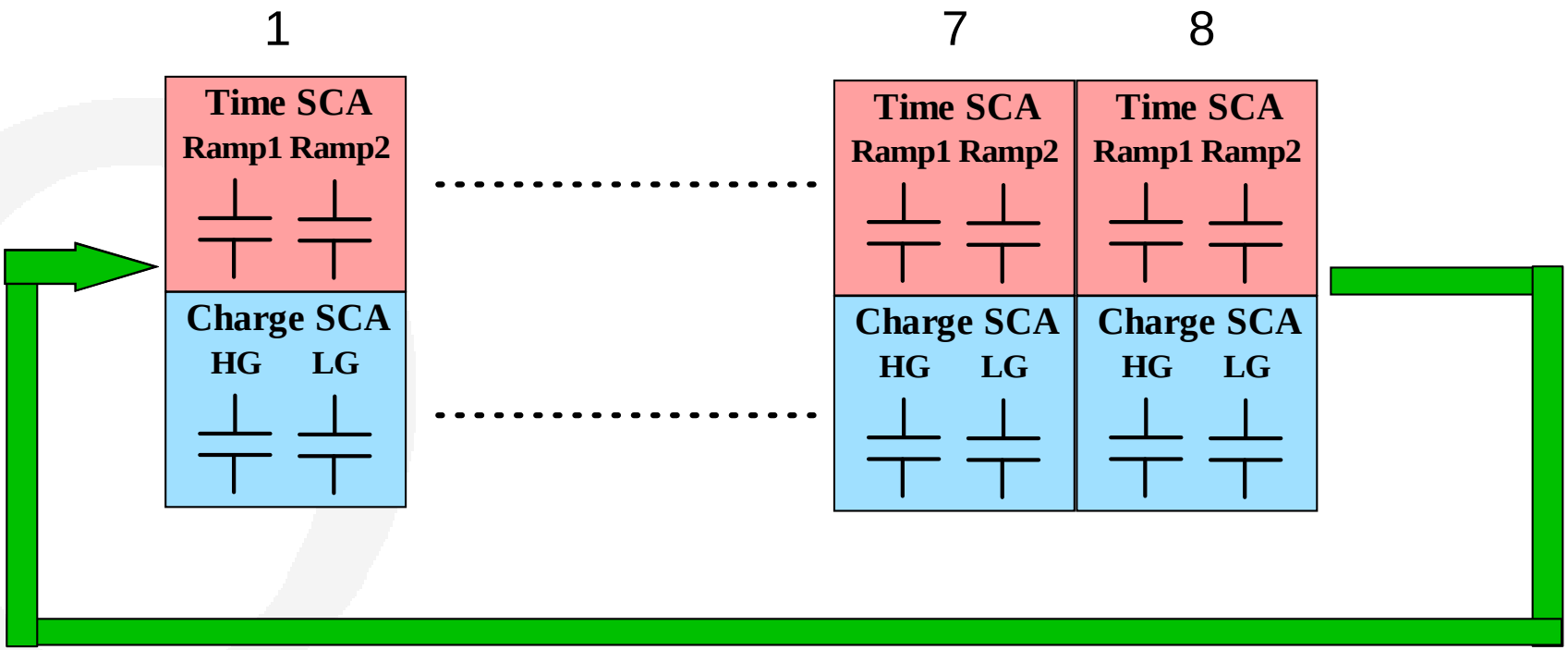
- 2 events comparison:

	Spiroc2	Spiroc3
2 evt	2352 bits	144 bits



(N): Roll Mode

- 2 behaviors selectable by Slow Control:
  - SPIROC 2 mode
    - Acquire up to 8 events / channel
    - ChipSat when 1 channel is full
  - Roll mode
    - Acquire all events but only keep the 7 last ones
    - SCA is used like a circular memory



Conclusion

- Trial layout shows that:

	Spiroc 2	Spiroc 3
I/O	195	530
Area / 1 SCA depth	0.26 mm²	0.90 mm²
# bits / evt on 1 chn	1168 bits	80 bits

- Synthesis is in progress / Layout + simulation will follow

- Future HARDROC chip ➔ some presented points will be the same in HR
  - No change of DIF sequencing (acquisition / readout)
  - Readout with zero suppress
  - I2C slow control access + old SR as backup

- Future SKIROC chip ➔ VHDL code is now standardized between SKIROC and SPIROC (only number of channels 36 ➔ 64 is different)