KLauS2v0
Characterization Measurements

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KLauS2v0

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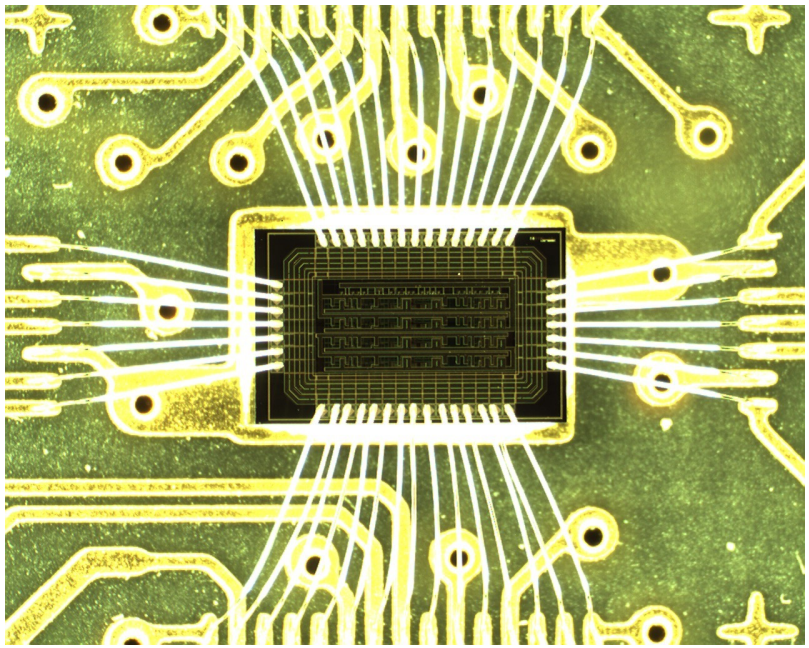
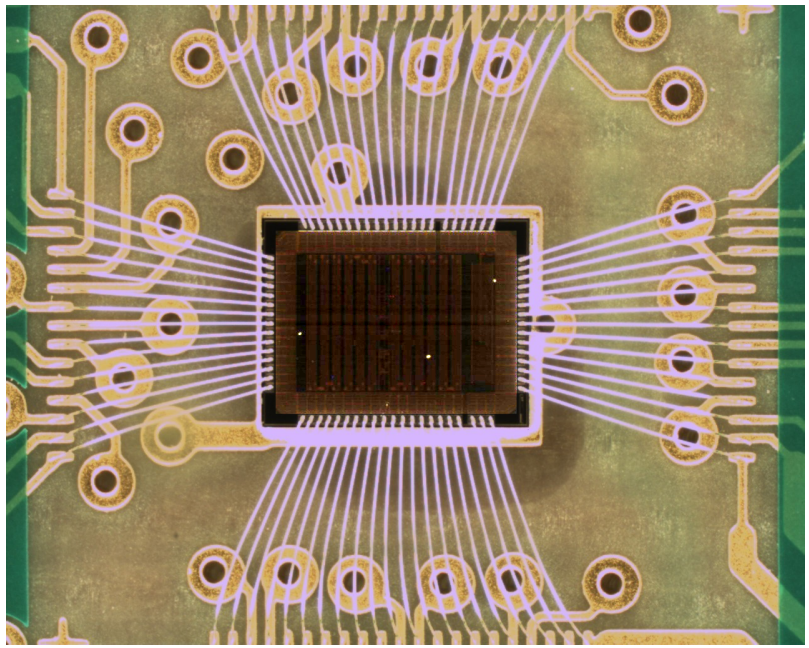
KLauS - Kanäle zur Ladungsauslese von SiPMs



KLauS1v0



KLauS2v0

KLauS is a silicon photomultiplier readout chip specifically designed for calorimetry applications.

Features of KLauS2v0

KLauS1v0 features	KLauS2v0 features
4 channels	12 channels
Power gating not supported	Power gating supported
10 mW/channel	Decreased power consumption
Dynamic range 150 pC	Increased dynamic range
Signal to noise ration > 10	Signal to noise ration > 10
SiPM bias tunable	SiPM bias tunable
AMS CMOS 0.35 μm	SiGe 0.35 μm
	Reduced digital noise

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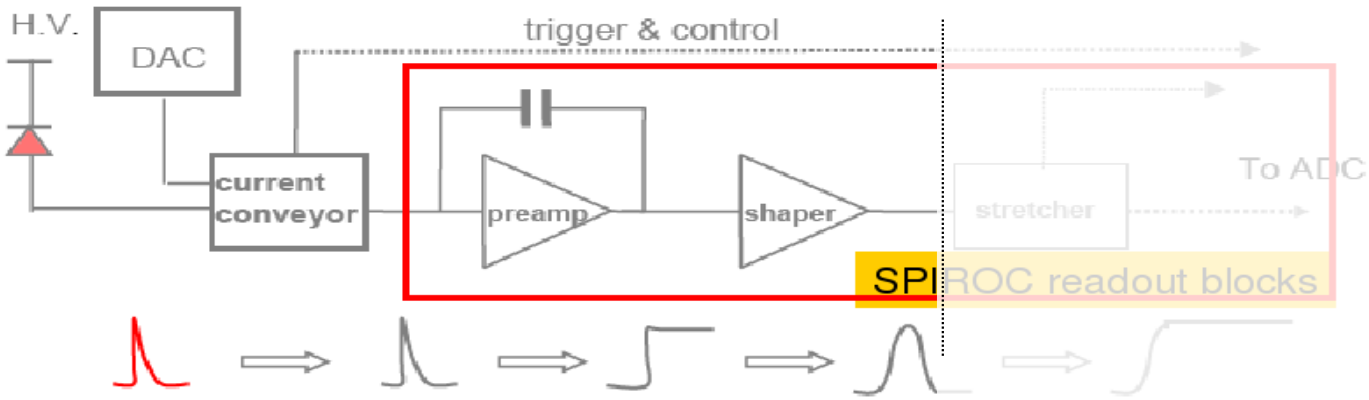
Power Reduction Scheme

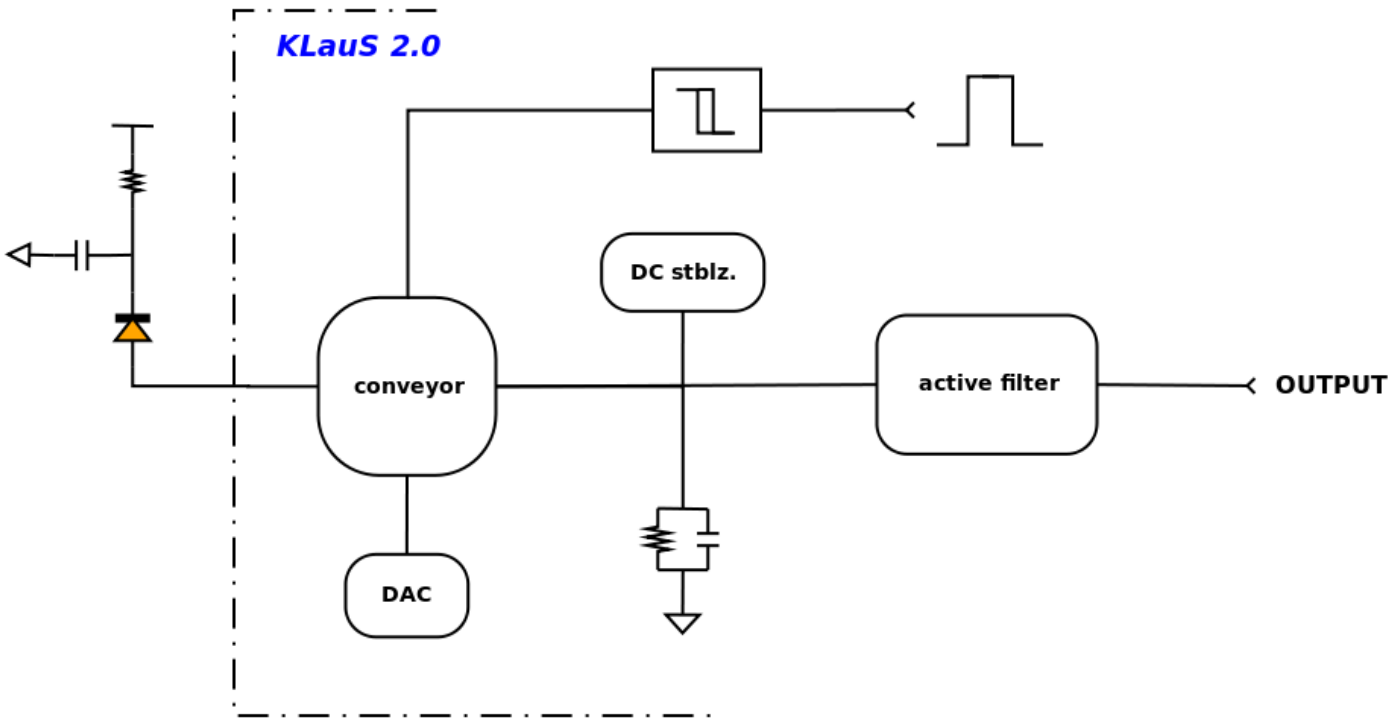


Channel diagram of KLauS1v0

Analog chain: preamplifier + 2 shaping stages

Power gating not possible

Power Reduction Scheme



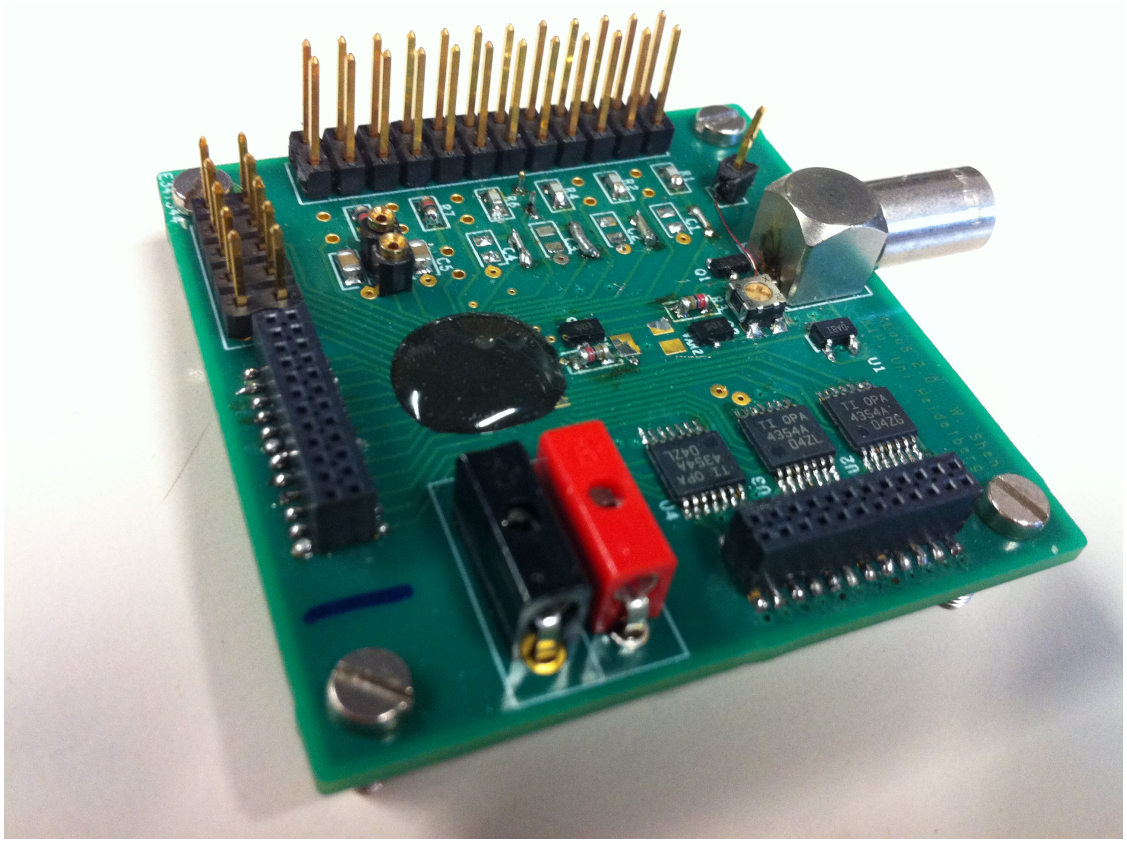
Channel diagram of KLauS2v0

Analog chain: passive integration + DC stabilization + active filter

Modified current conveyor supports power gating

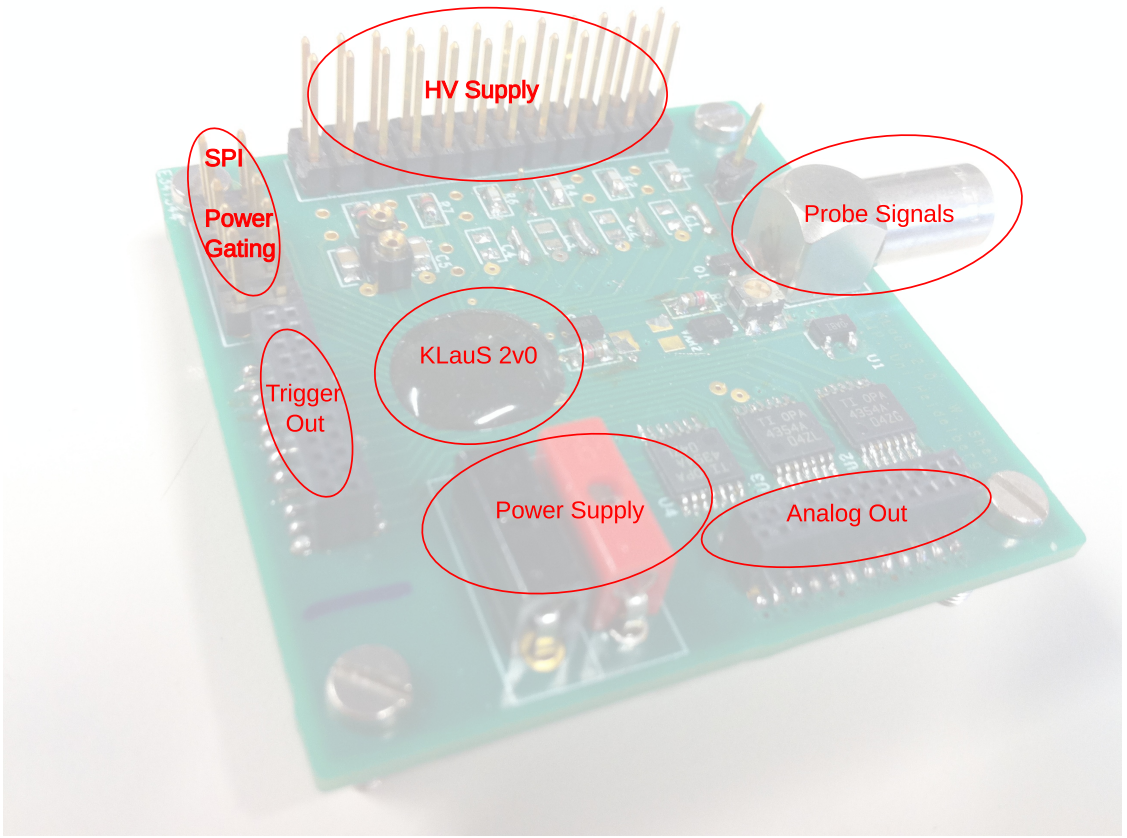
Characterization Measurements

Test Board and Setup



SiPM and charge injection measurements possible

Test Board and Setup



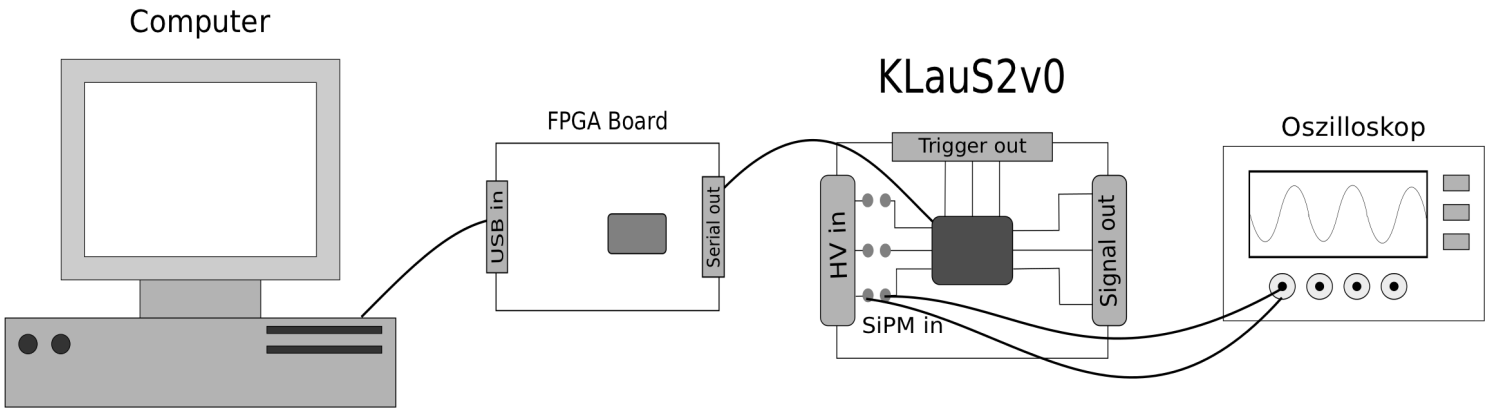
SiPM and charge injection measurements possible

Performed Measurements

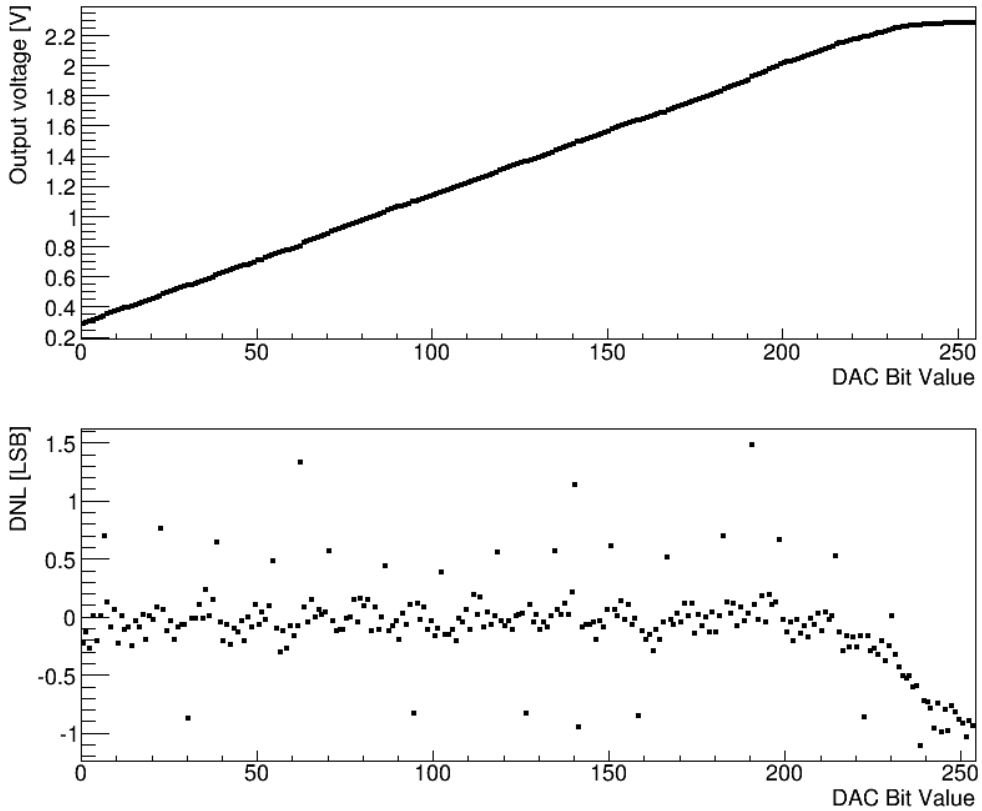
Input Bias Tuning	$\rightarrow$ DAC Linearity
Dynamic Range	$\rightarrow$ Analog Output Linearity
High Precision Timing	$\rightarrow$ Trigger Jitter and Charge Noise
Low Power Consumption	$\rightarrow$ Power Gating

DAC Linearity

Setup:

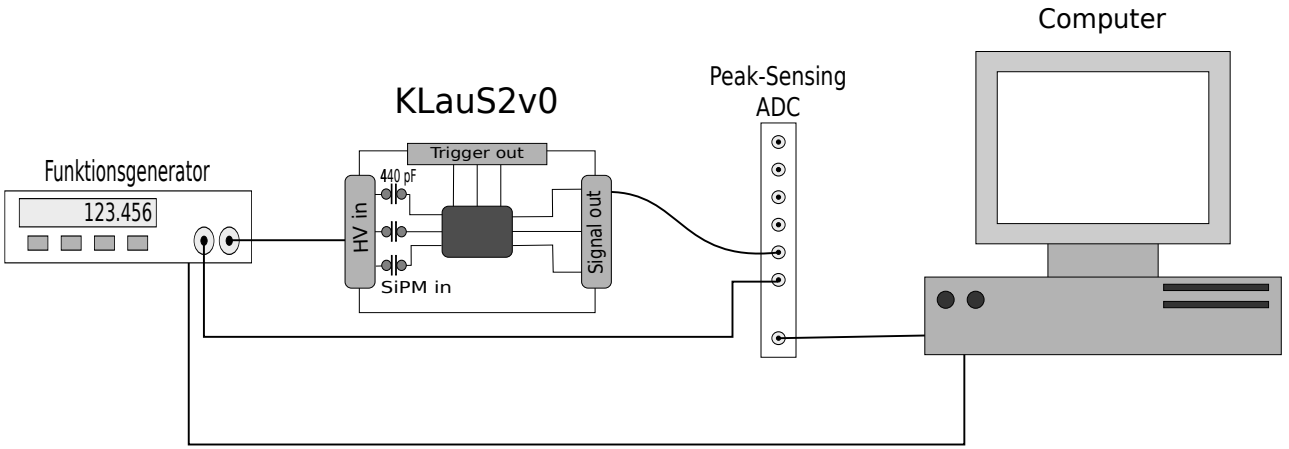


DAC Linearity



Linear range of voltage output $> 1.8\,\mathrm{V}$.
Periodic deviations caused by mismatch in the current mirrors of the DAC

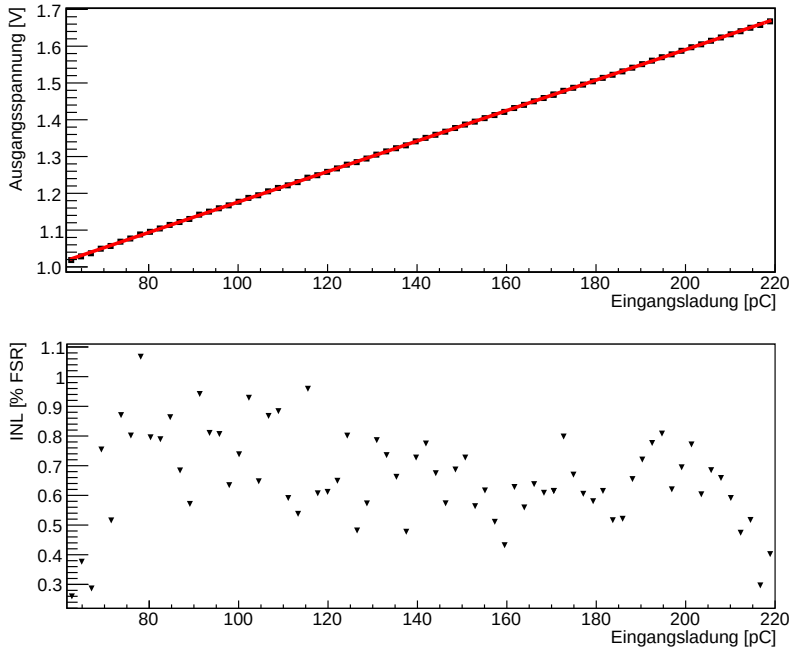
Dynamic Range



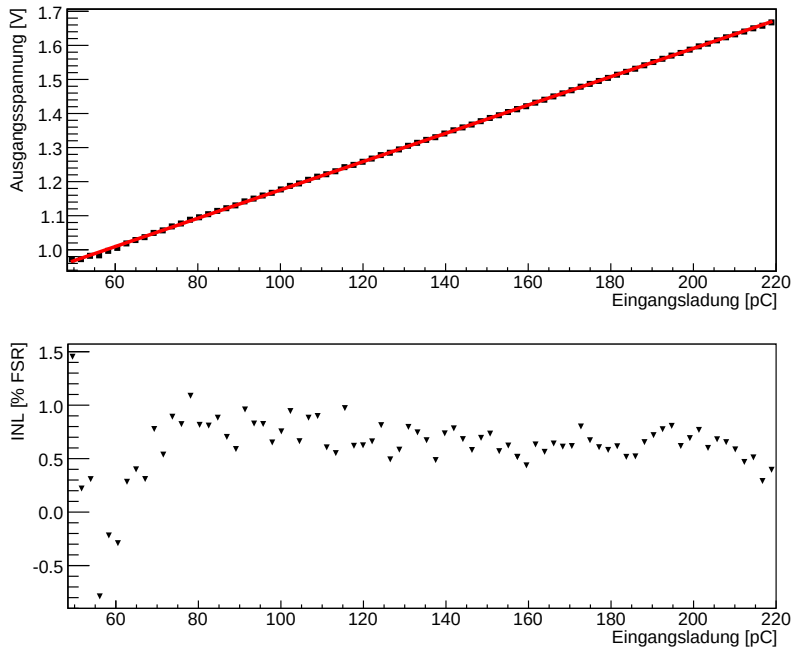
Charge signals from 40 fC to 220 pC are generated

Measurements with different shaping times and DAC values

Dynamic Range

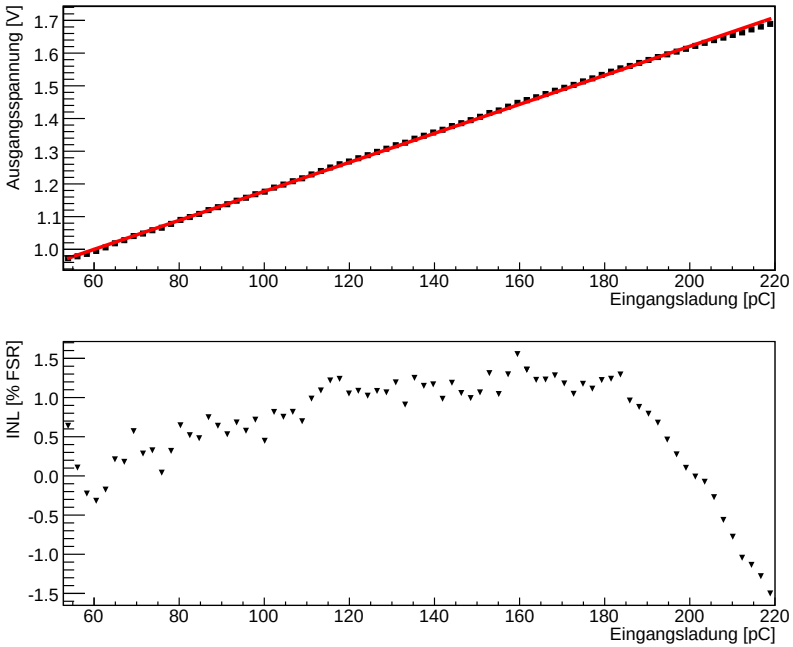


Shaping time 50 ns
DAC setting: 0

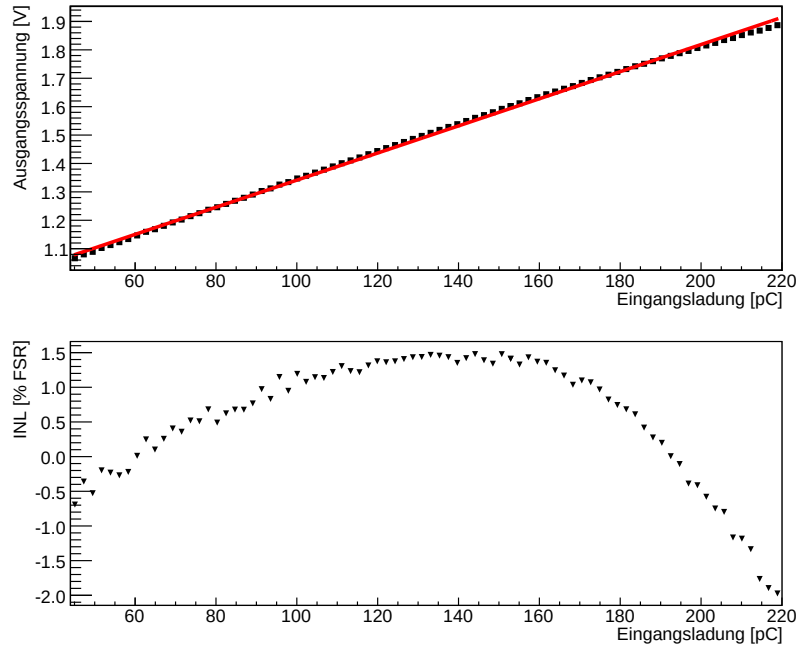


Shaping time 100 ns
DAC setting: 0

Dynamic Range



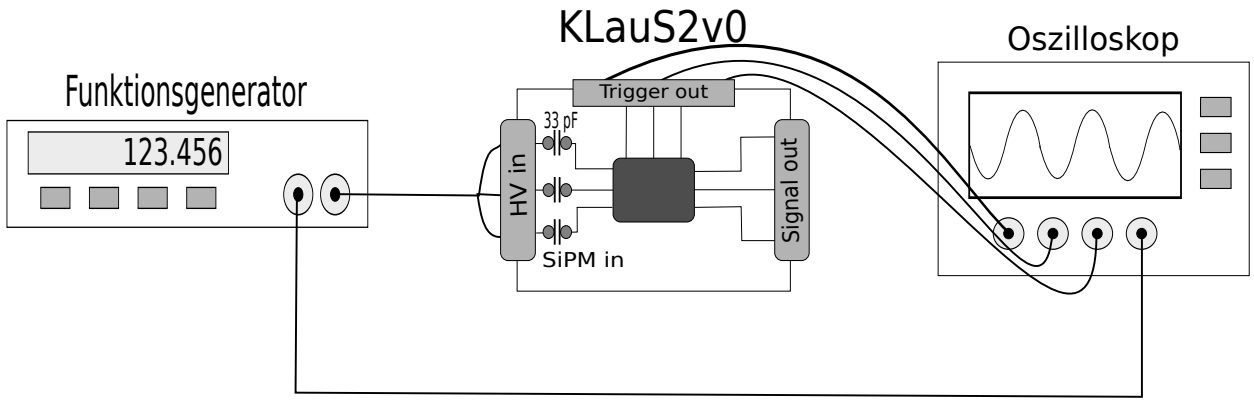
Shaping time 50 ns
DAC setting: 255

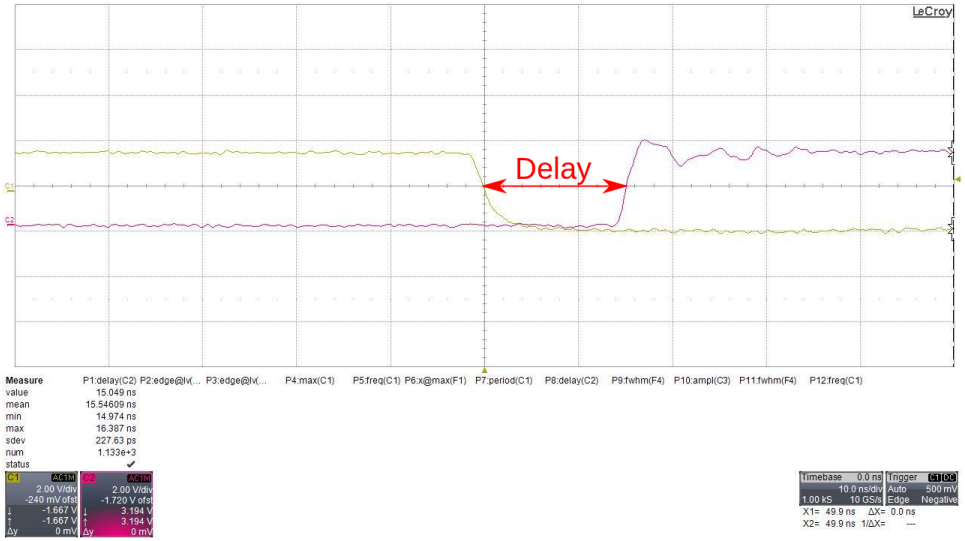


Shaping time 100 ns
DAC setting: 255

Maximum INL value $< 2.1\,\%$ for 100 ns shaping time.

Trigger Jitter





A signal charge corresponding to 15 fired pixels (660 fC) is injected.

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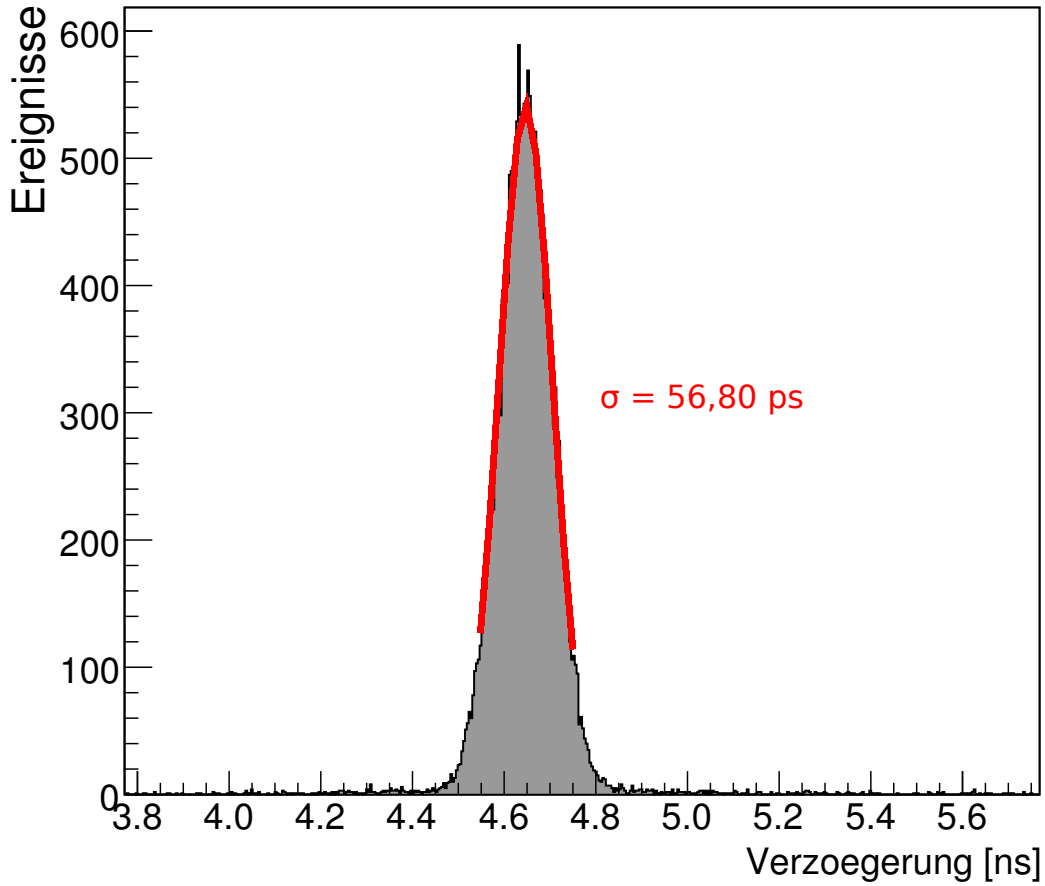
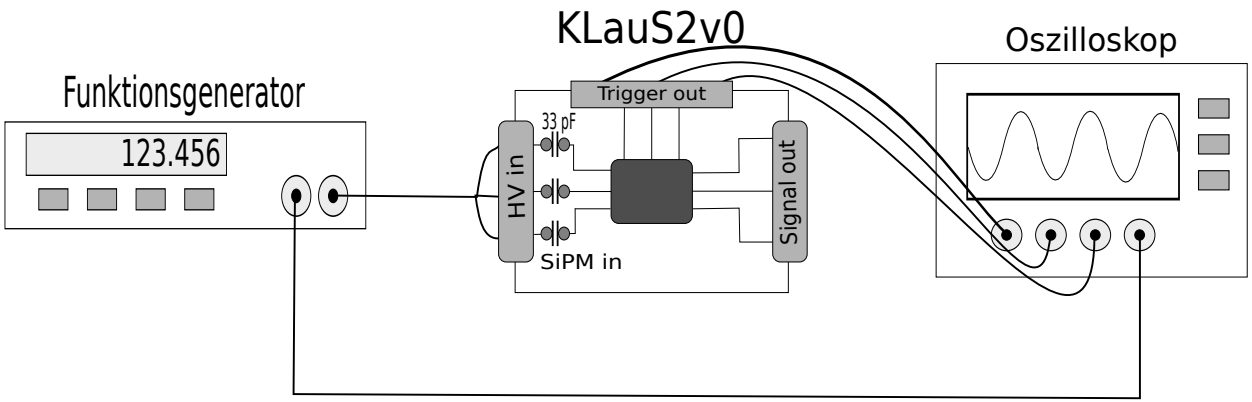
Trigger Jitter



Trigger Efficiency



Trigger efficiency and charge noise have been determined for trigger thresholds corresponding to 6,7,8 and 9 fired pixels.

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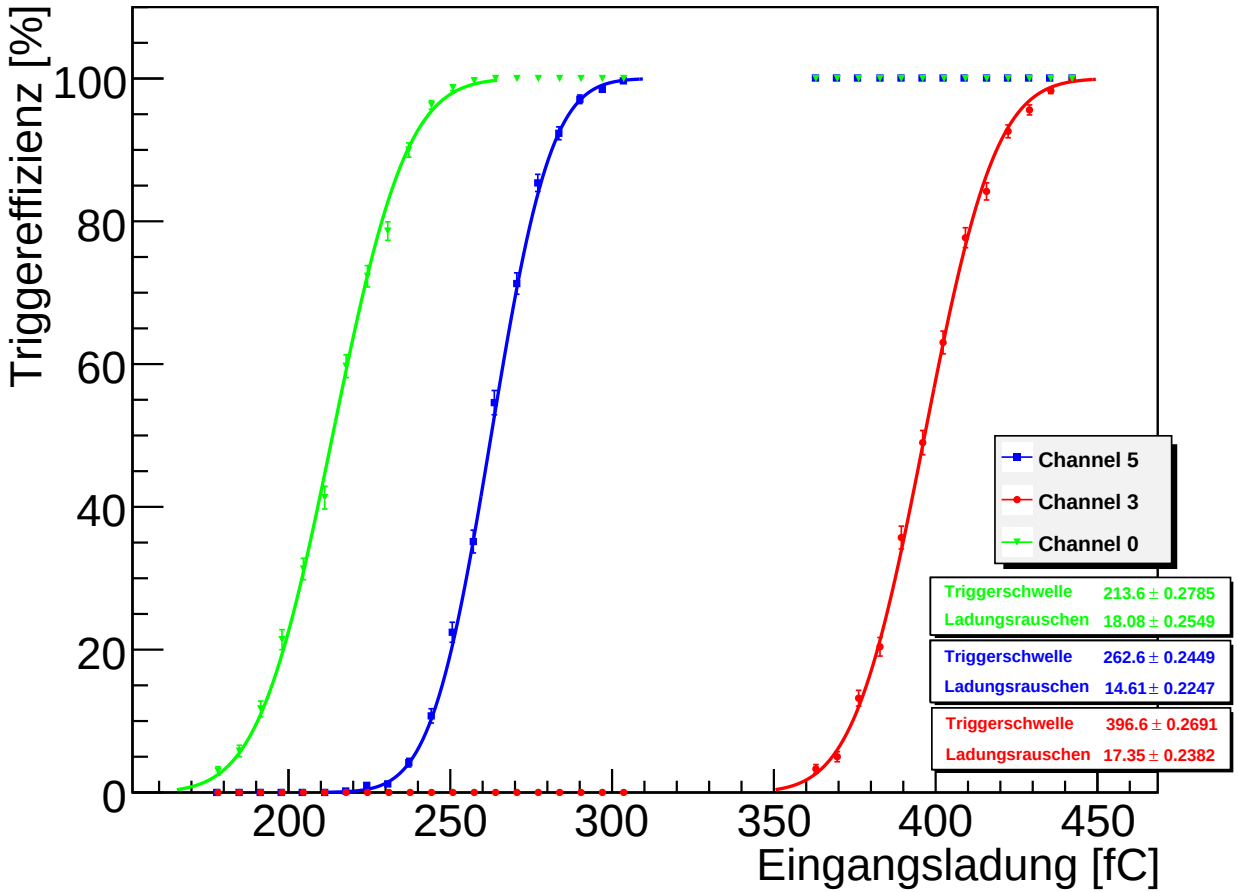
Trigger Efficiency



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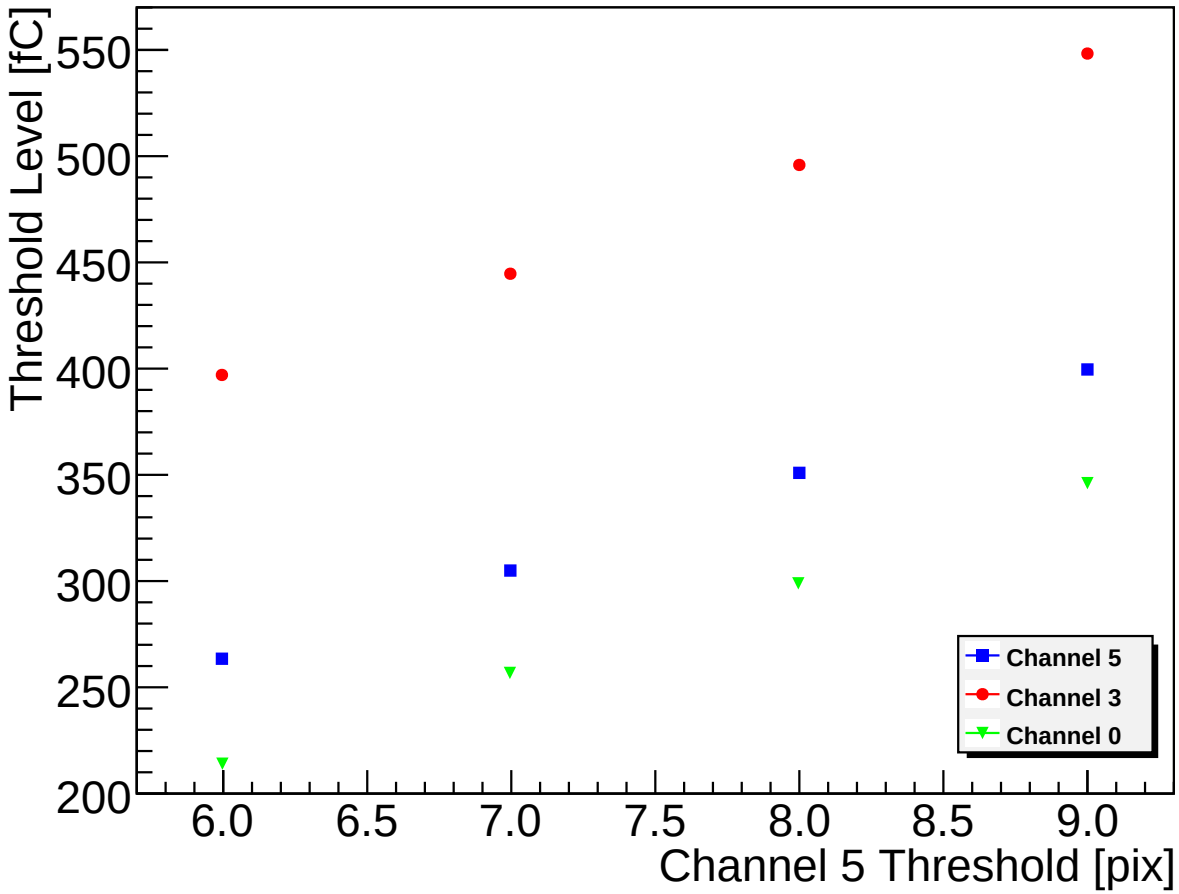
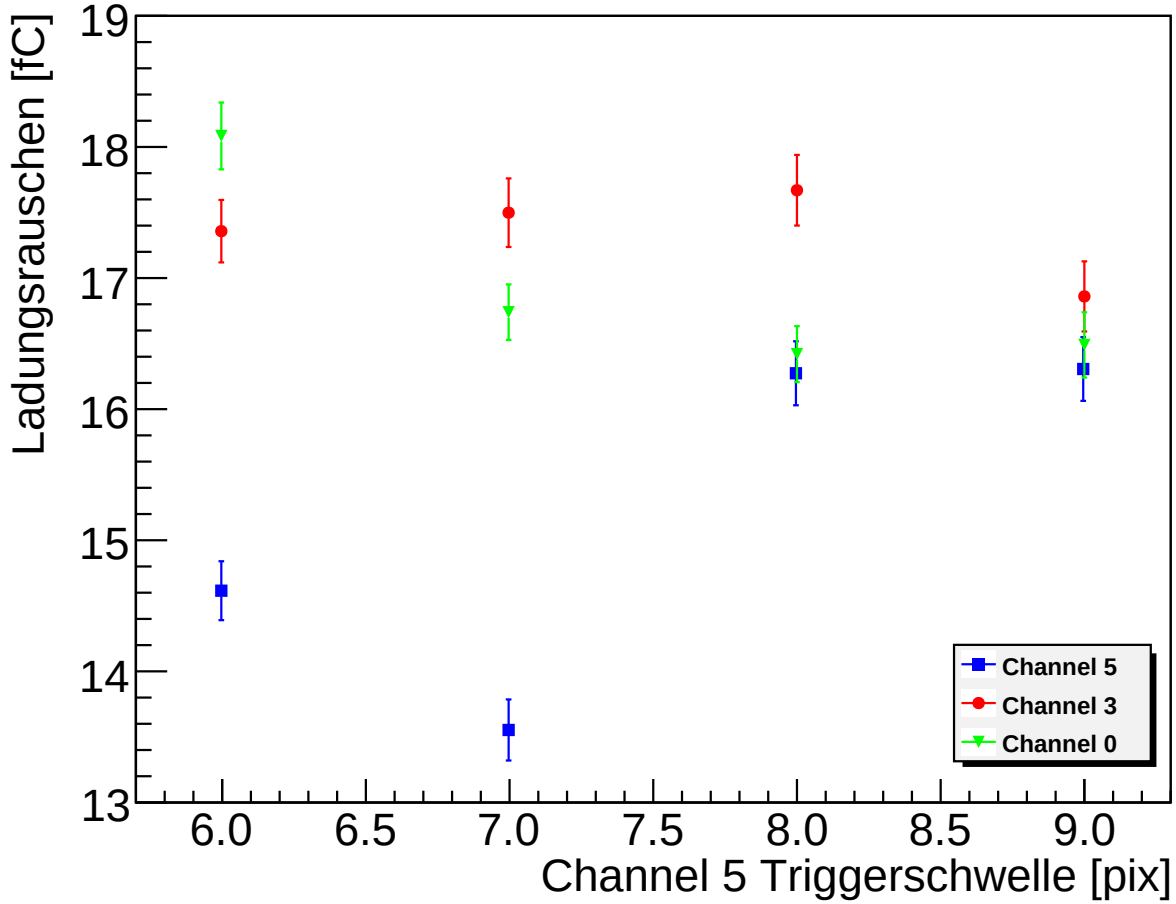
Trigger Efficiency

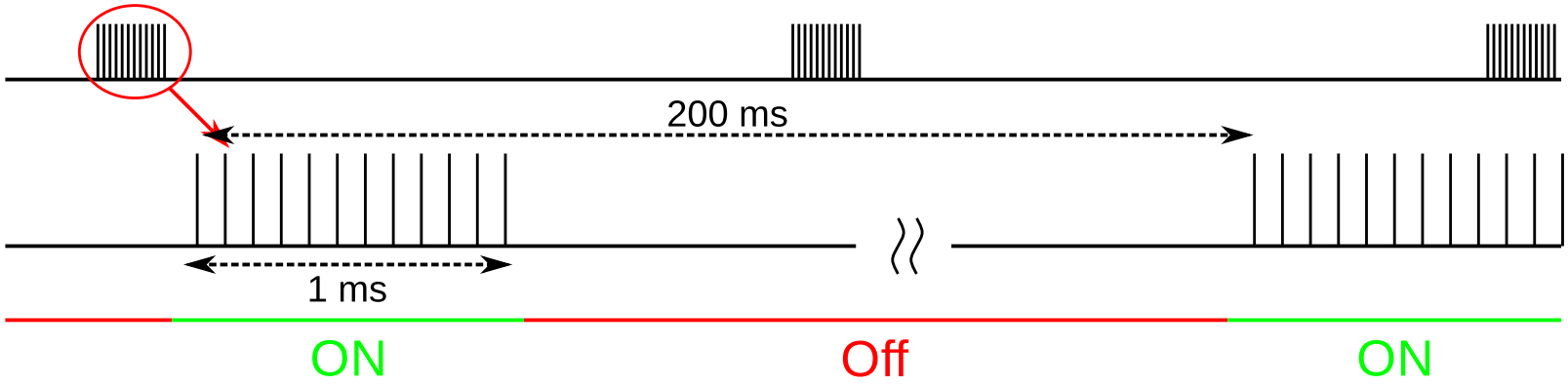


Trigger Efficiency



Maximum charge noise : $18\,\mathrm{fC}$

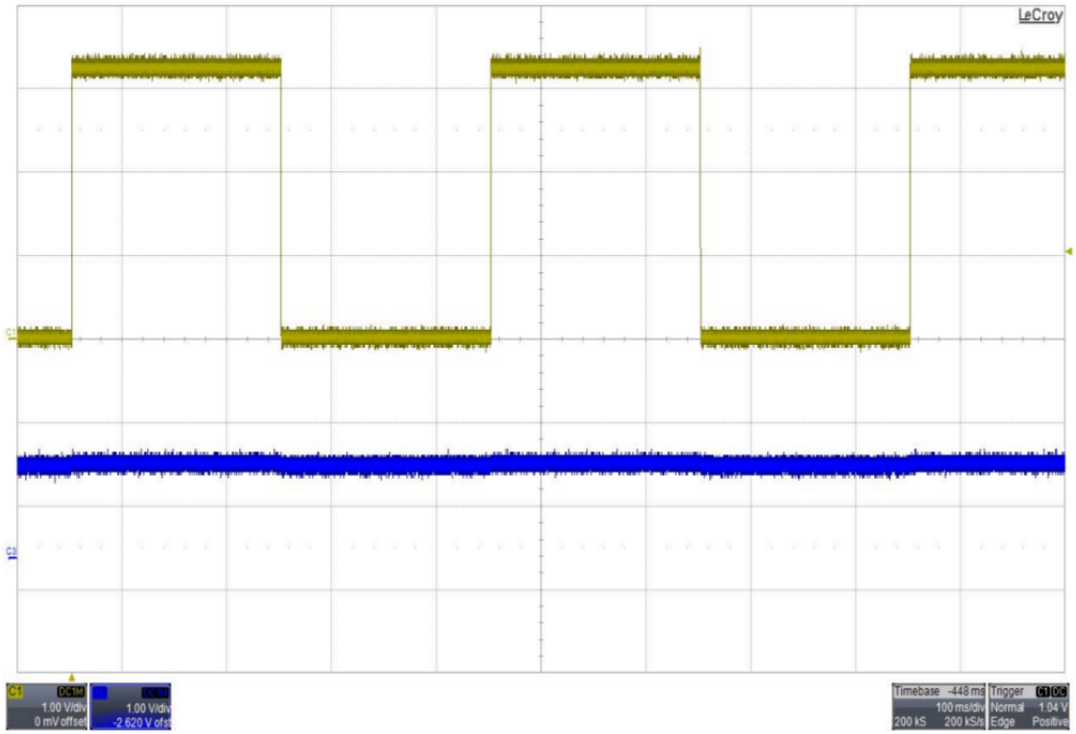
Power Gating



Power consumption reduced from $\approx 2.5\,\mathrm{mW/channel}$ to $< 25\,\mu\mathrm{W/channel}$

Power Gating

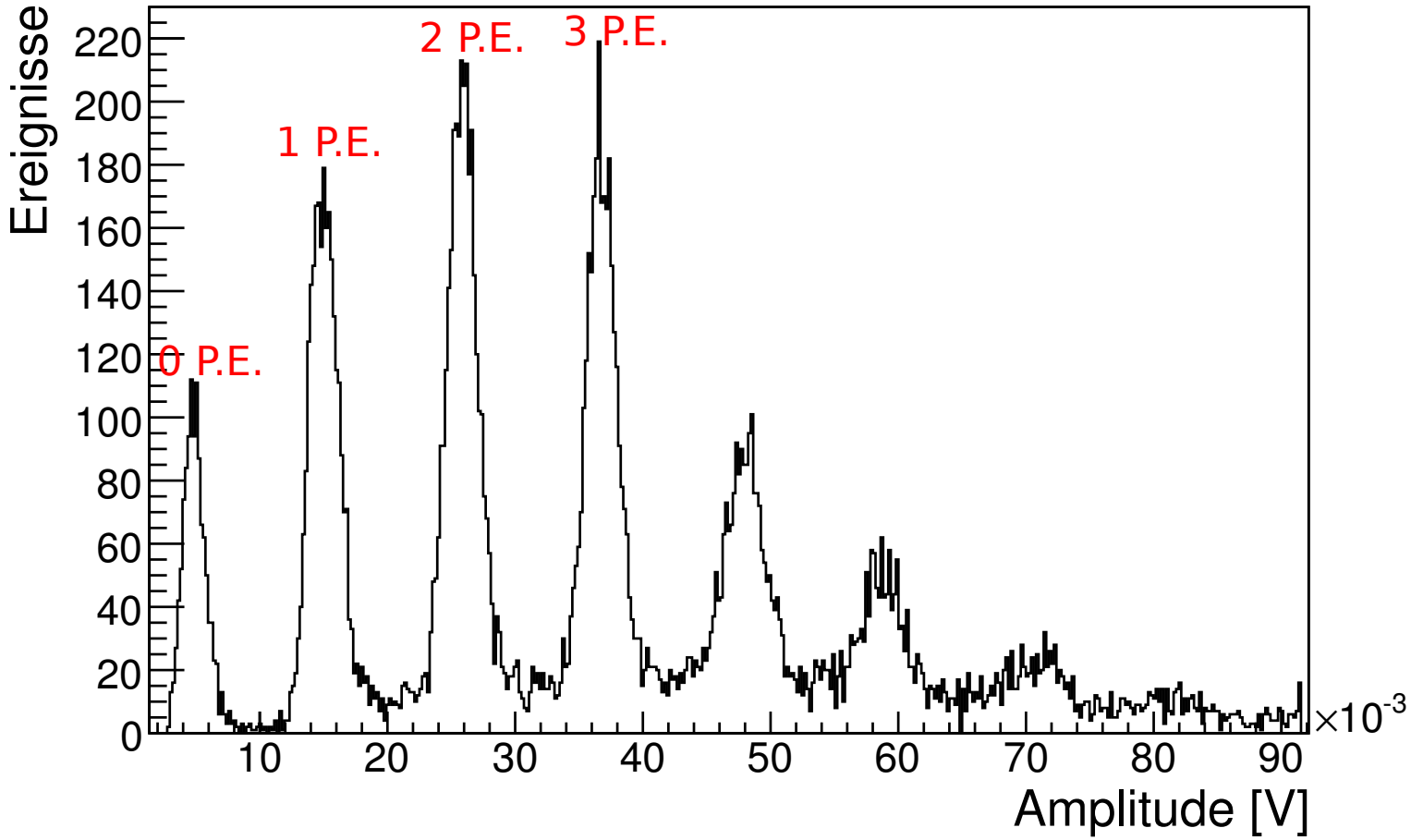
Influence of the power gating on SiPM bias has to be small



Observed bias variation less than $20\,\mathrm{mV}$ over the whole DAC range

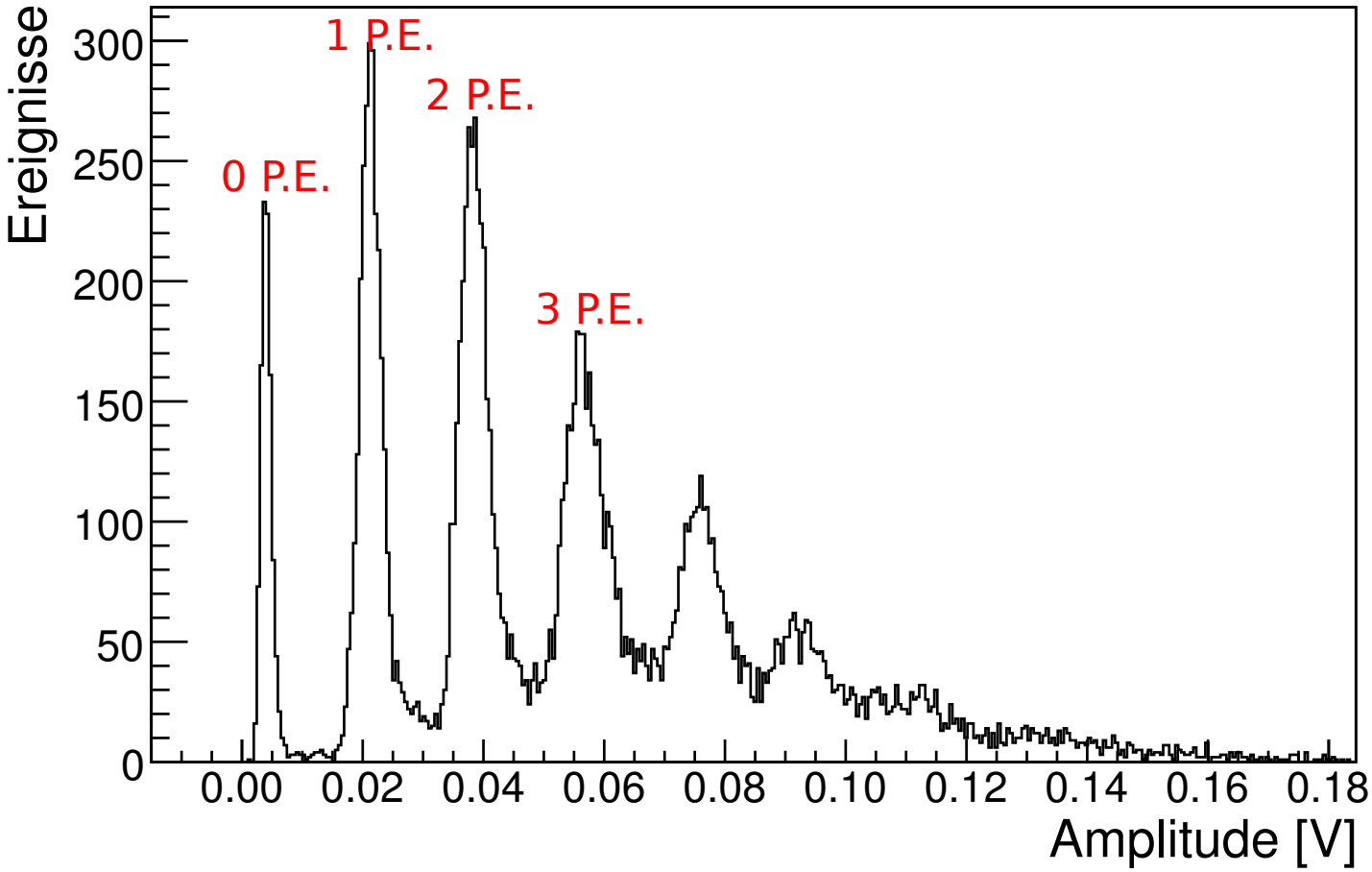
SiPM Measurements

Recorded Single Photon Spectra



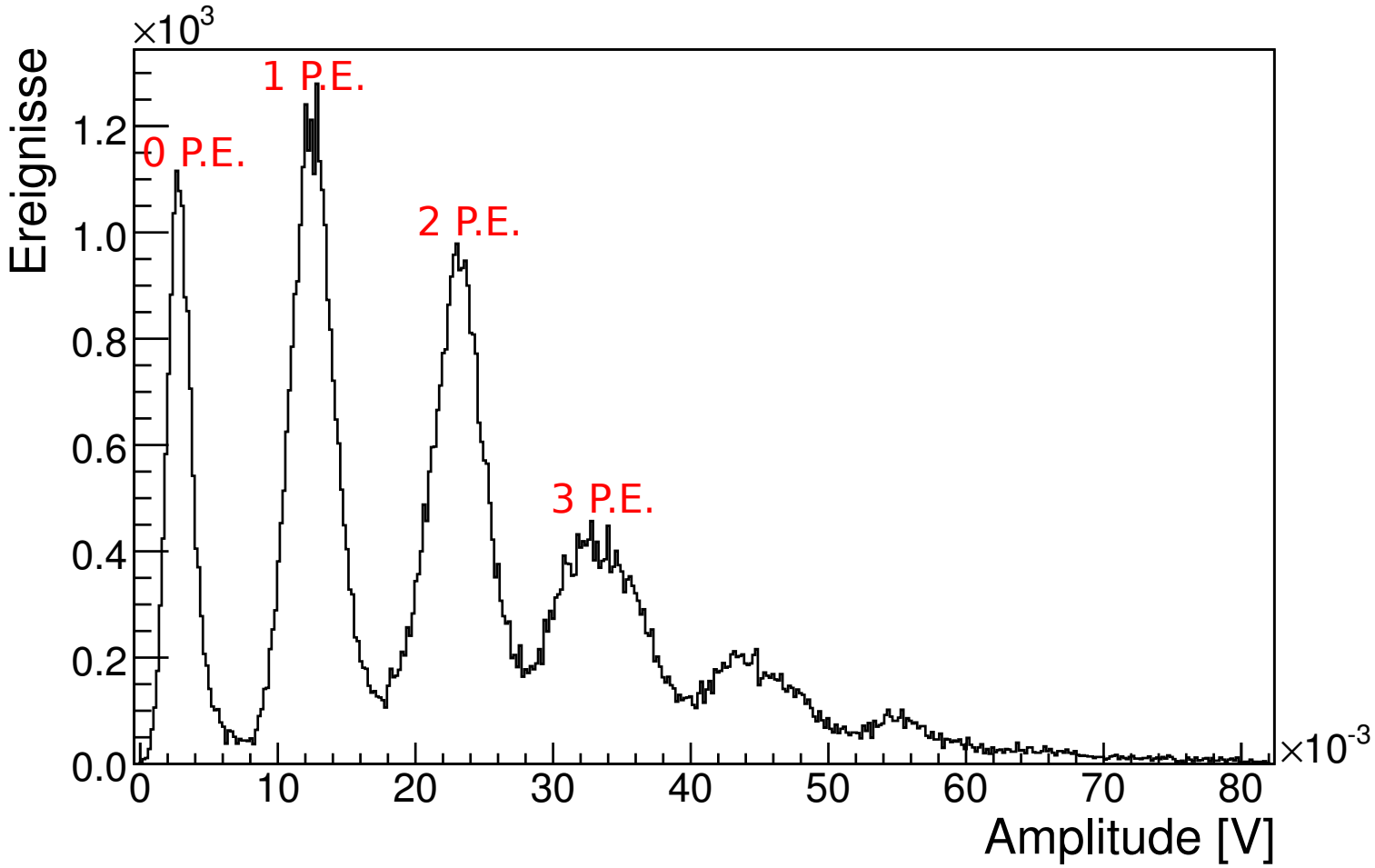
MPPC 25 um pitch at nominal voltage

Recorded Single Photon Spectra



MPPC 50 um pitch at nominal voltage

Recorded Single Photon Spectra



CPTA SiPM at low overvoltage

Conclusion

- KLauS2v0 has been built with additional features
- Characterization measurements were successful
  - Bias DAC linear in a range of 1.8 V
  - Dynamic range of 220 pC under all conditions
  - Trigger jitter < 60 ps for MIP signals
  - Charge noise < 18 fC
  - Power consumption < 2.5 mW/channel
  - Power gating functional
- Measurements with different SiPM types successful

Outlook:

- Further characterization of the power gating functionality
- Ready for integration into SPIROC.