

Omega

SPIROC Status

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IN2P3/OMEGA-LAL Orsay

France

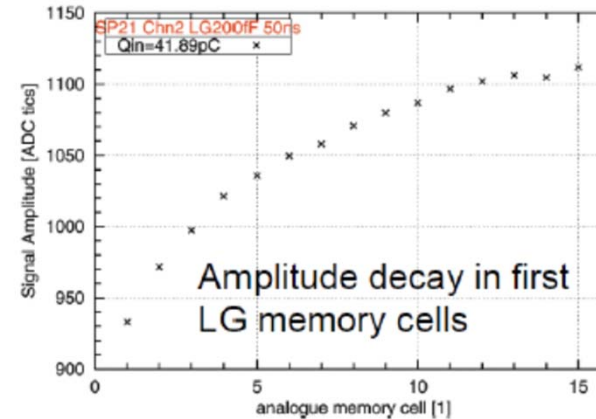
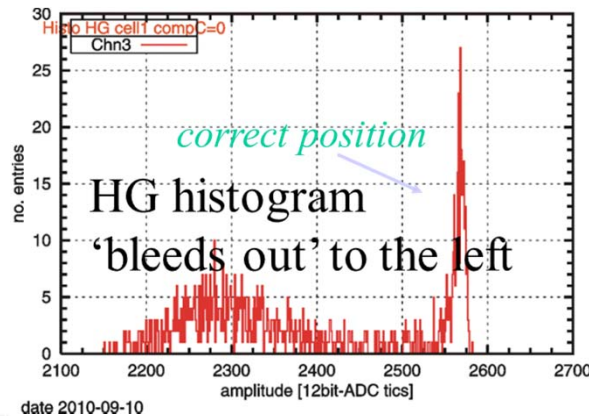
raux@lal.in2p3.fr



Orsay MicroElectronics Group Associated

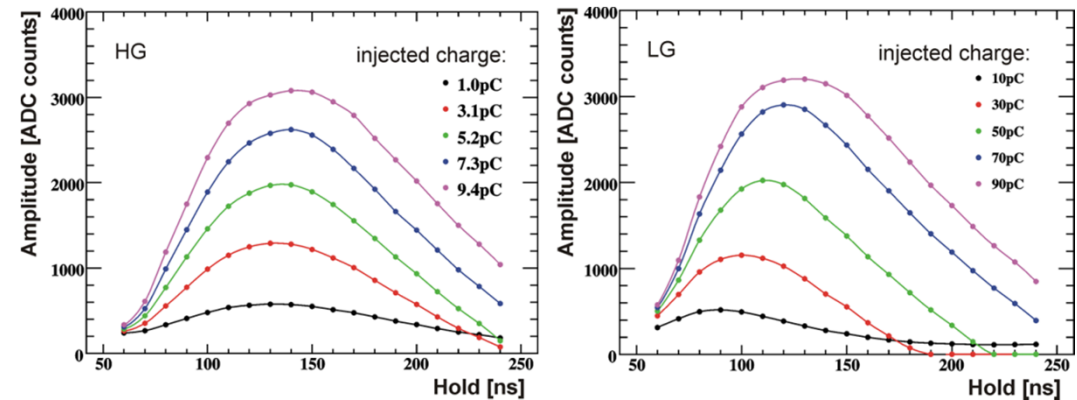
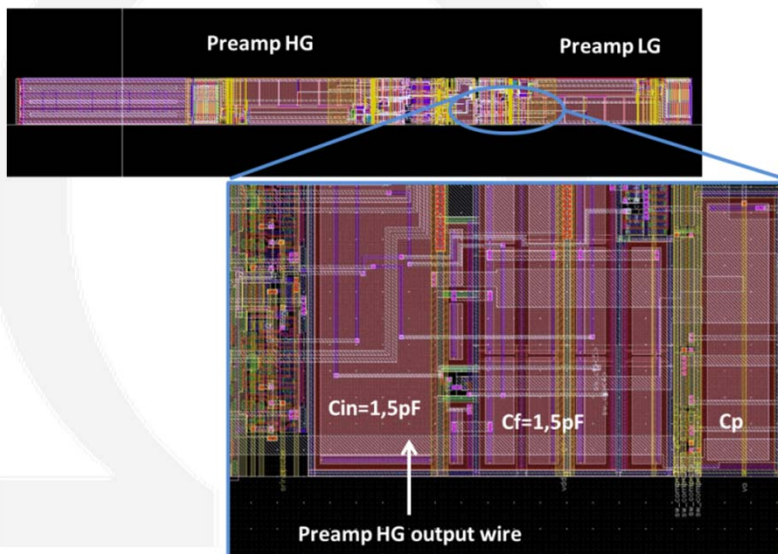
Status on SPIROC 2 major bugs (1/2)

- "Rate dependency" ➔ **Understood**
 - due to the switches on compensation capacitances when they are OFF, the signal is clamped with low rate signal



- Cross-talk between HG and LG ➔ **Understood**

One-channel layout



Capacitive Coupling between HG PA wire and C_{in}

Status on SPIROC 2 major bugs (2/2)

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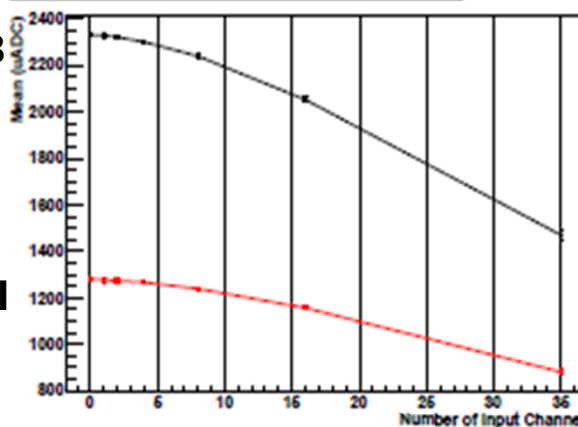
Problem when several channels are hit



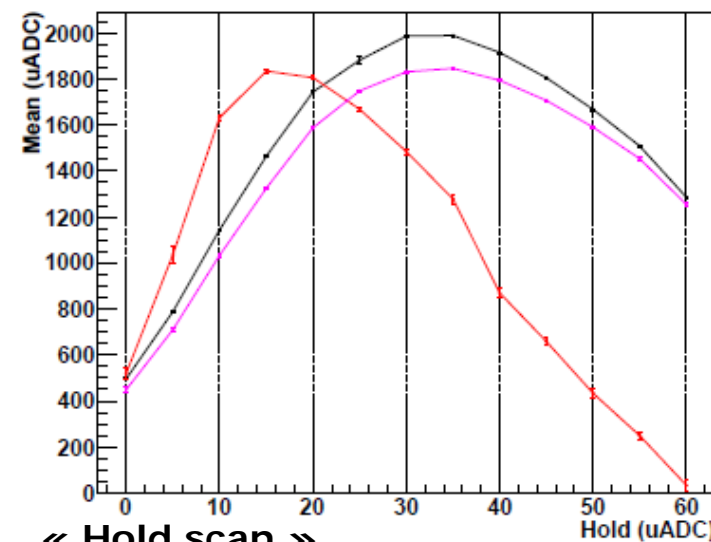
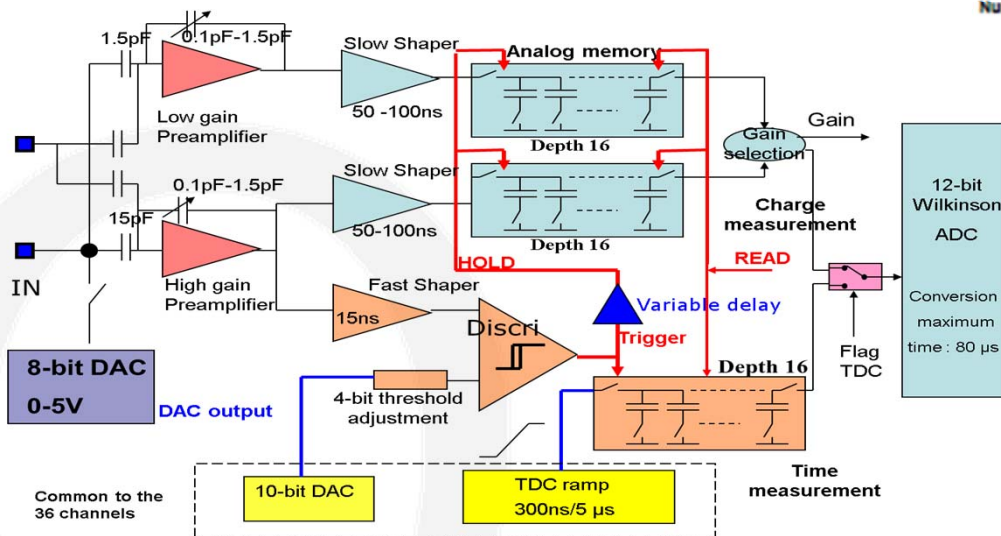
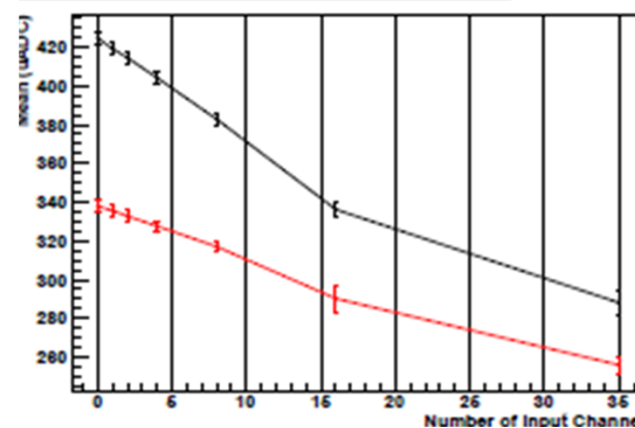
Understood

- Signal injected in channel 8 HG value when other channels are hit
- Decrease of the converted value when several channel are hit at the same time

Influencing of the Number of Input Channel (High)



Influencing of the Number of Input Channel (Low)



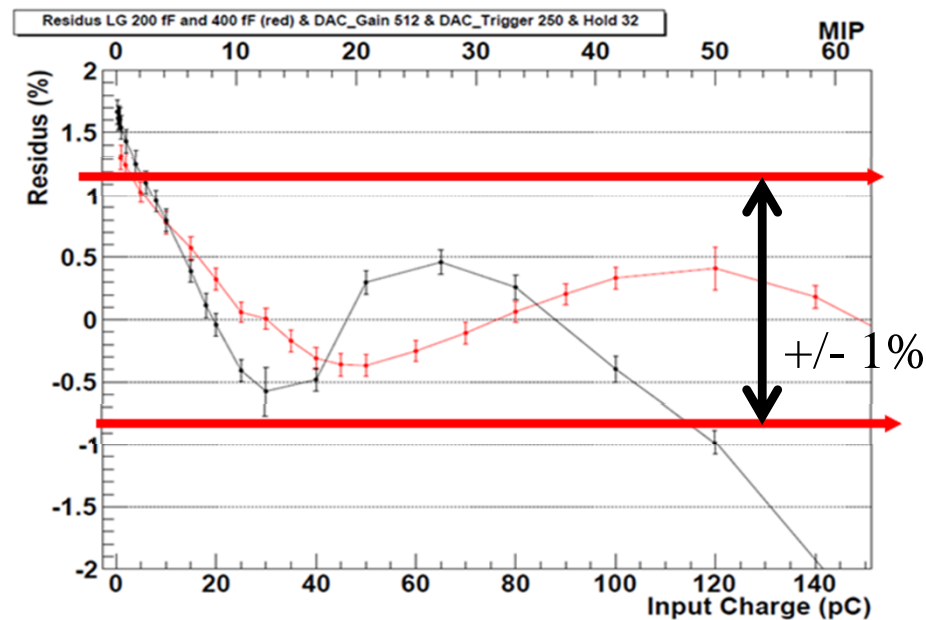
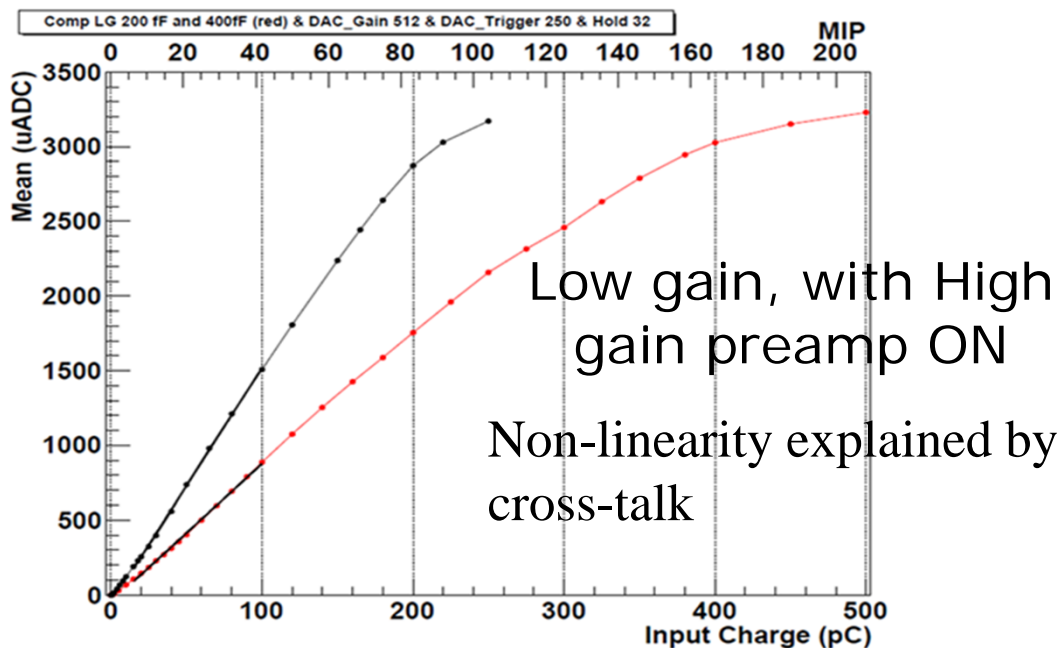
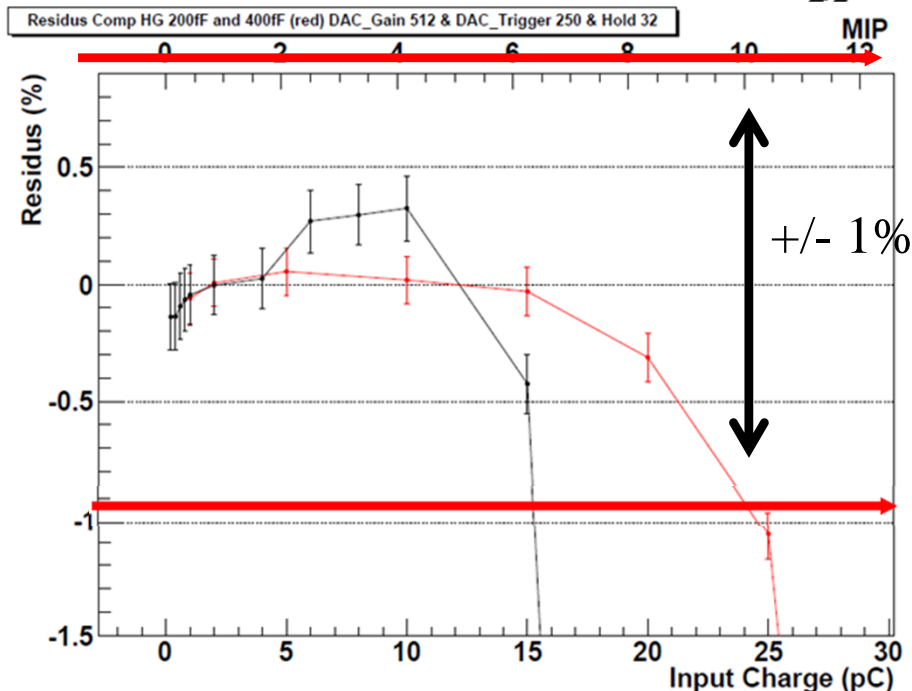
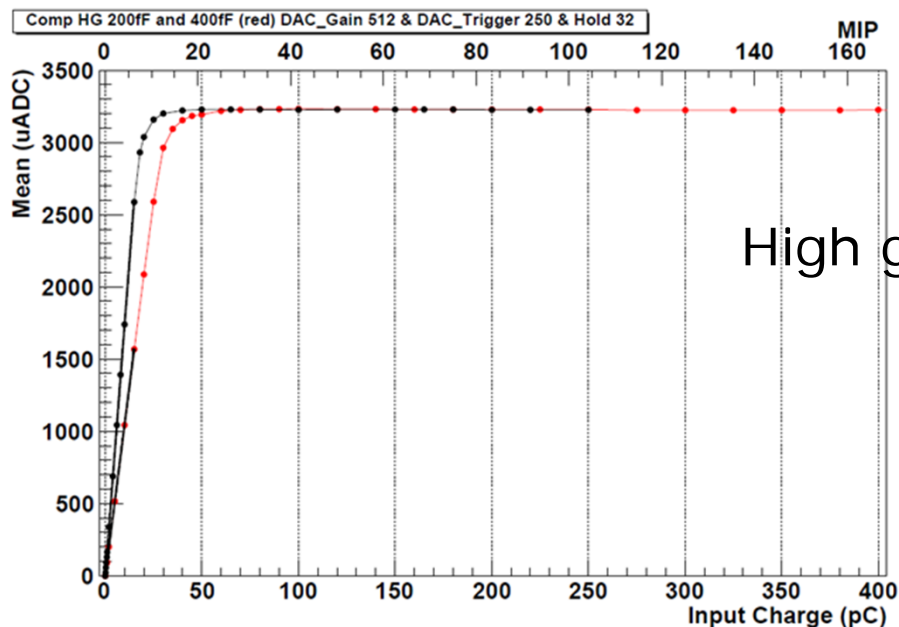
« Hold scan »

Conclusion:

Delay shift when several channel are hit. Delay box must be fixed.

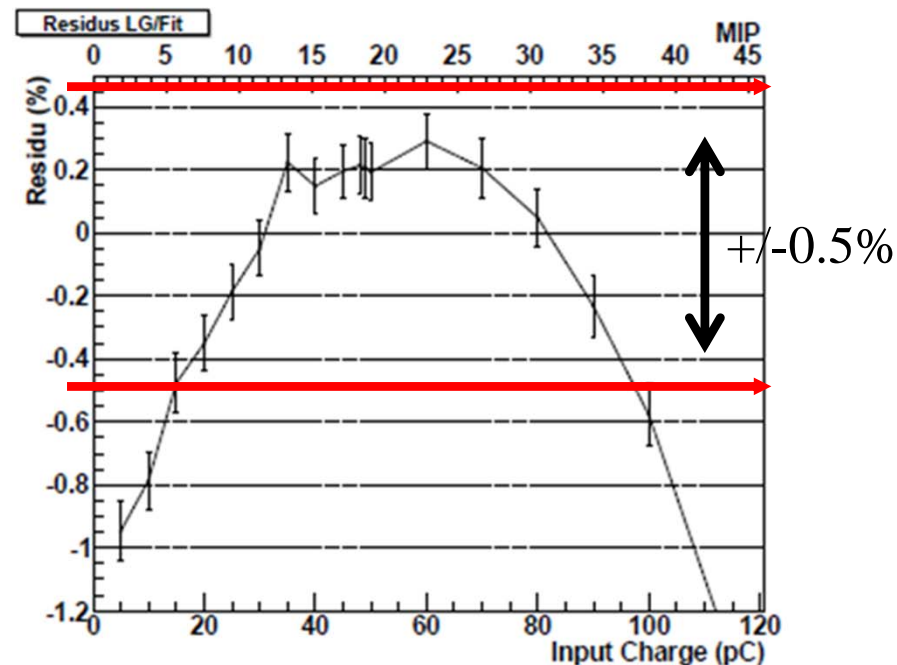
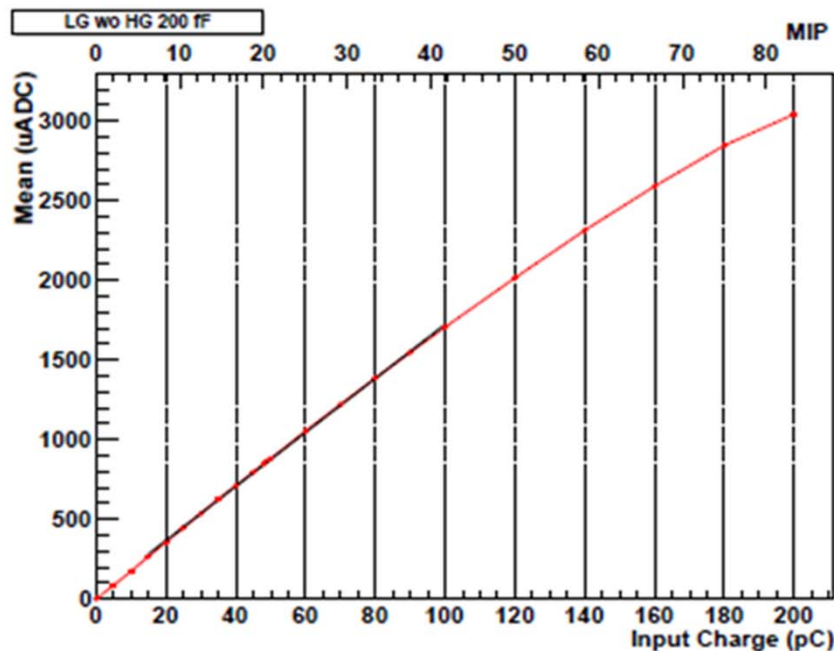
- **Black**: No signal in the 35 other channels
- **Pink**: The 35 other channels « hit » and « masked »
- **Red**: The 35 other channels « hit » and « not masked »

Linearity measurement (HG preamp ON)



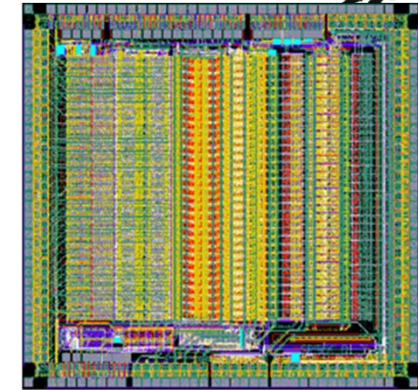
Linearity measurement (HG preamp OFF)

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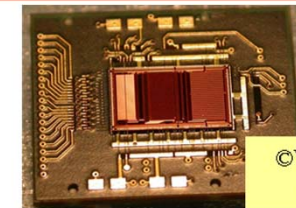


Low gain, with High gain preamp OFF

- EASIROC1a -> "light" version of SPIROC
 - conservative version of EASIROC
 - EASIROC/SPIROC x bugs corrected
 - Corrected « rate dependency »
 - Switches for Cp capacitances removed
 - Cp=1pF for HG
 - Cp=3pF for LG
 - Corrected cross-talk HG/LG
 - Default slow control setup extended
 - Right value for bias resistances implemented (ibm_pa_lg, ibmin_pa)
 - Submitted on the 2th September 2011
 - Delivery expected before 2012
- Should validate the correction of the two major problems on the preamps (« rate dependency » and cross-talk HG/LG)



Fabricated in SiGe AMS 0.35 μm
Submitted in September 2009
Delivered in December 2009
Chip area: 17 mm² (4.2 mm \times 4.1 mm)



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(Aachen)

**PEBS
experiment
Aachen
University**

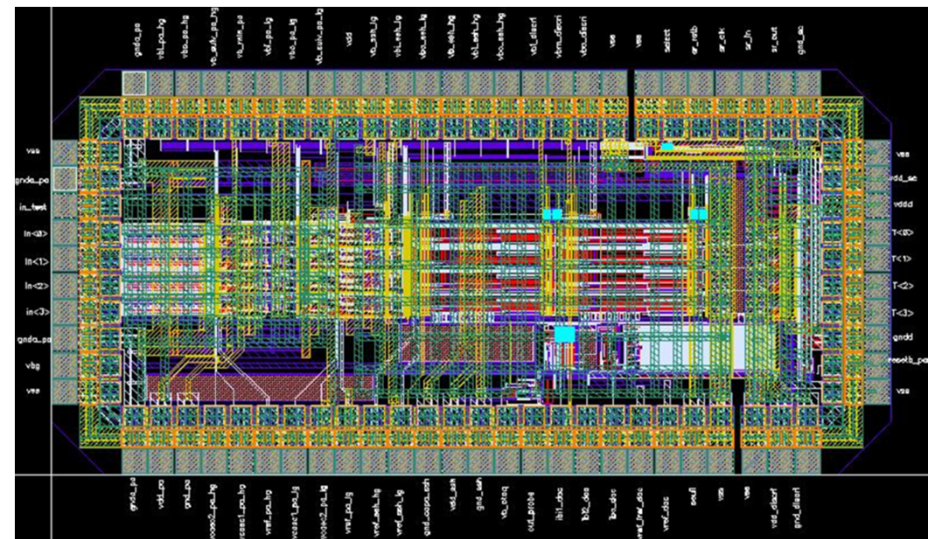
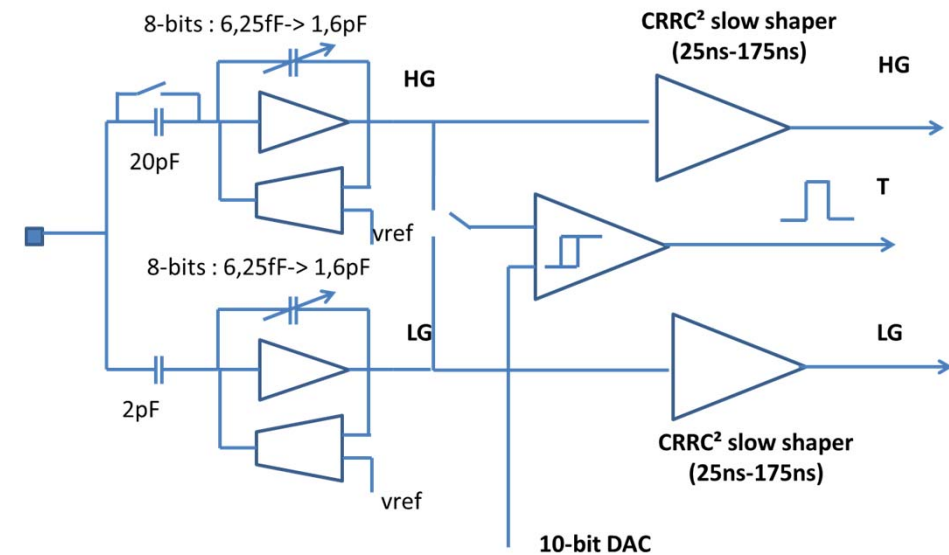


**MU-RAY
project
INFN
Napoli**

« Building block »

- Submission of a “Building block” in May 2011 (IN2P3 funding)
 - Delivery within a few days
- 4-Channel ASIC
- **New preamplifier** structure based on NMOS input transistor to be less sensitive to coherent noise
- Preamplifier gain tunable independently on 8 bits (minimum capacitance 6.25 fF)
- Discriminator connected directly to preamp
- If OK, could be used **SPIROC 3**

One channel schematic



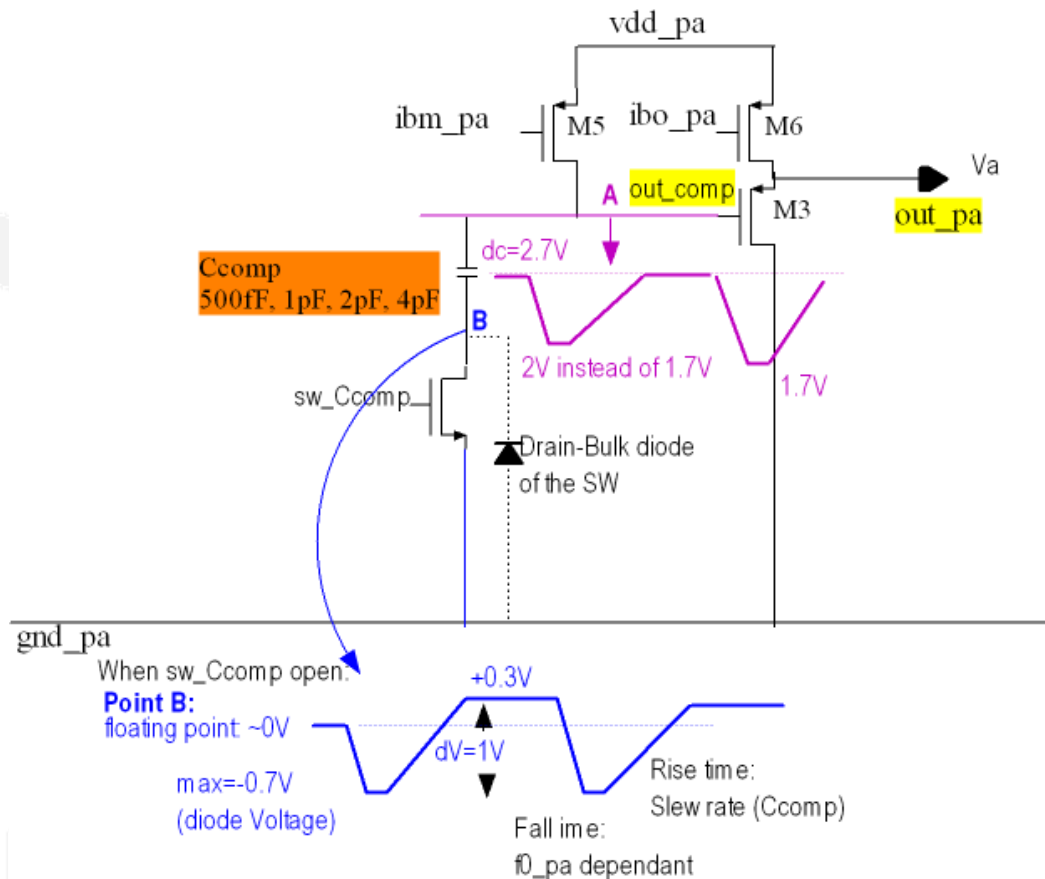
- New Chip SPIROC 3 submission expected in mid-2012 (AIDA funding)
- 5 major improvements:
 - **Preamplifier:** 3 options :
 - Corrected SPIROC 1 and 2 preamp (“Rate dependency”, HG/LG cross-talk)
 - New preamp tested in “building block”
 - “Klaus 2” preamplifier
 - **New SCA management** => real “zero suppress”
 - Channel managed independently -> Implied new digital part (see Frédéric’ talk)
 - SCA Depth will be reduced (from 16 to 8)
 - **New TDC** => avoid dead time
 - Already existed and tested in PARISROC 2
 - **Slow control by I2C:**
 - Developed in collaboration with IPNL (see Frédéric’ talk)
 - **Possibility to have a “circular memory mode”**
- Other minor modifications, corrections or improvements
 - Bandgap, delay box, latch on auto-gain discriminator, 4-bit DAC, etc.

- **Major bugs are understood:**
 - « Rate dependency » and HG/LG cross-talk
 - The bugs comprehension should be validated before the end of the year
- **SPIROC 3:**
 - SPIROC 3: **new generation**
 - Independent channel management
 - New TDC
 - Slow control by I2C
 - Prototype run expected in mid-2012
 - Digital part design and layout in progress
 - Analog part will start as soon as possible



Rate problem: understood

- Due to the switches of the Compensation capacitors when they are OFF
- SW OFF but Drain Substrate diode which prevents the voltage to go down to voltages lower than -700 mV
- ALL the Ccomp must be set ON to avoid this effect



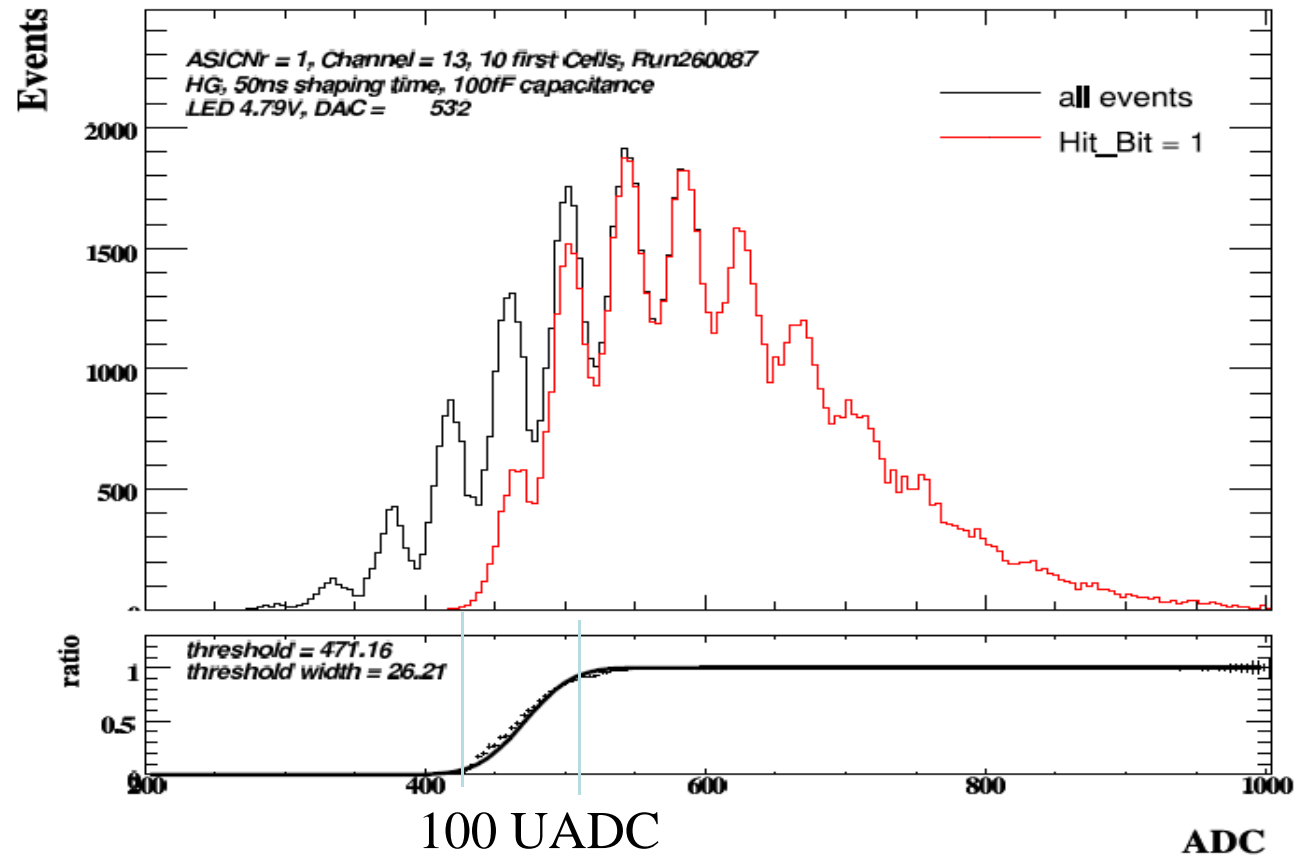
DESY measurement:

HG, LED 4.79V, DAC=532

ALL events in black

Hit bit in red

slope=100 UADC



→ Try to reproduce the same measurement in Orsay

Injected charge from 0.25pC to 0.5 pC – step = 10 fC

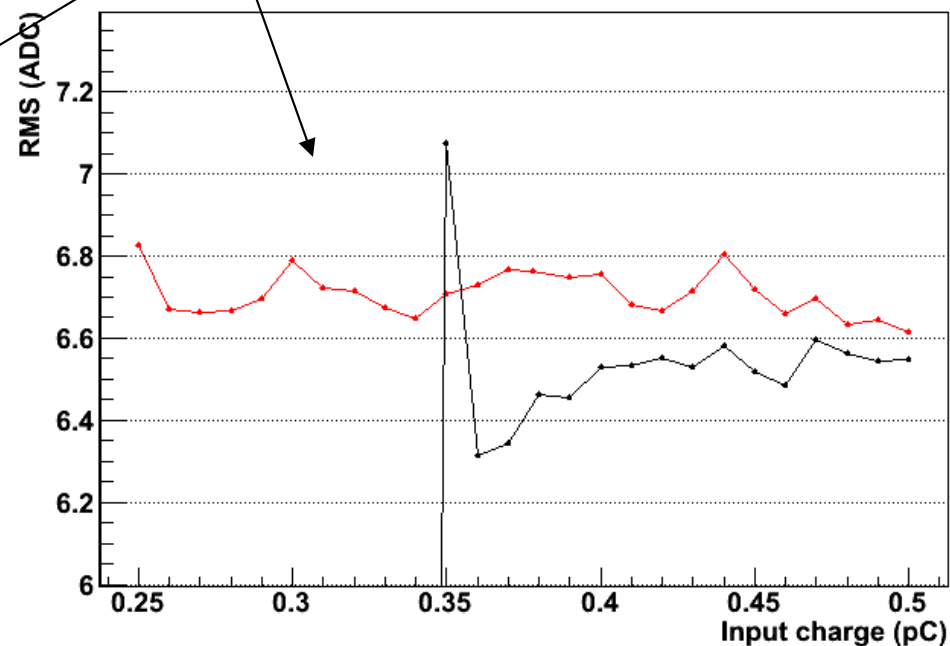
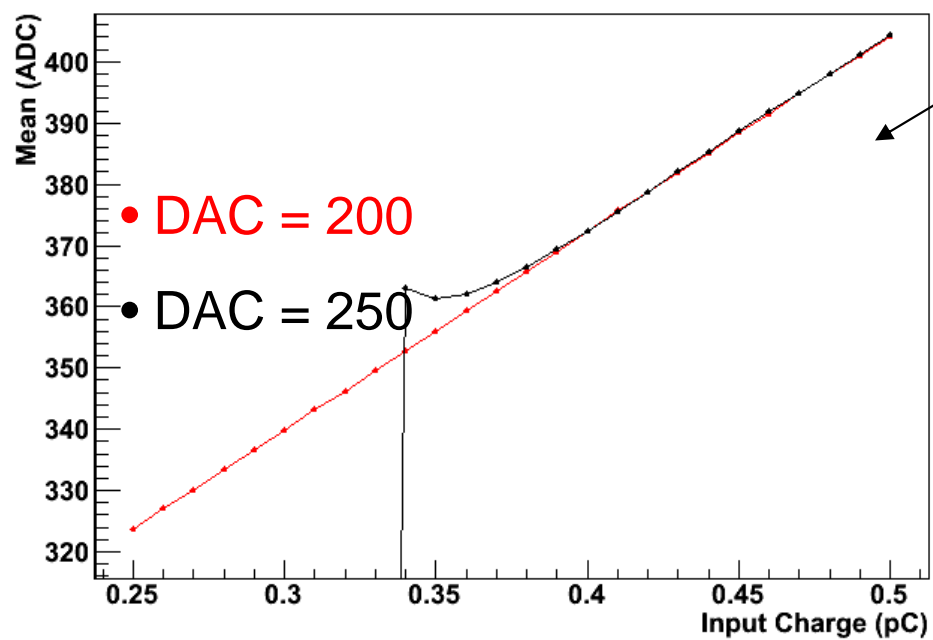
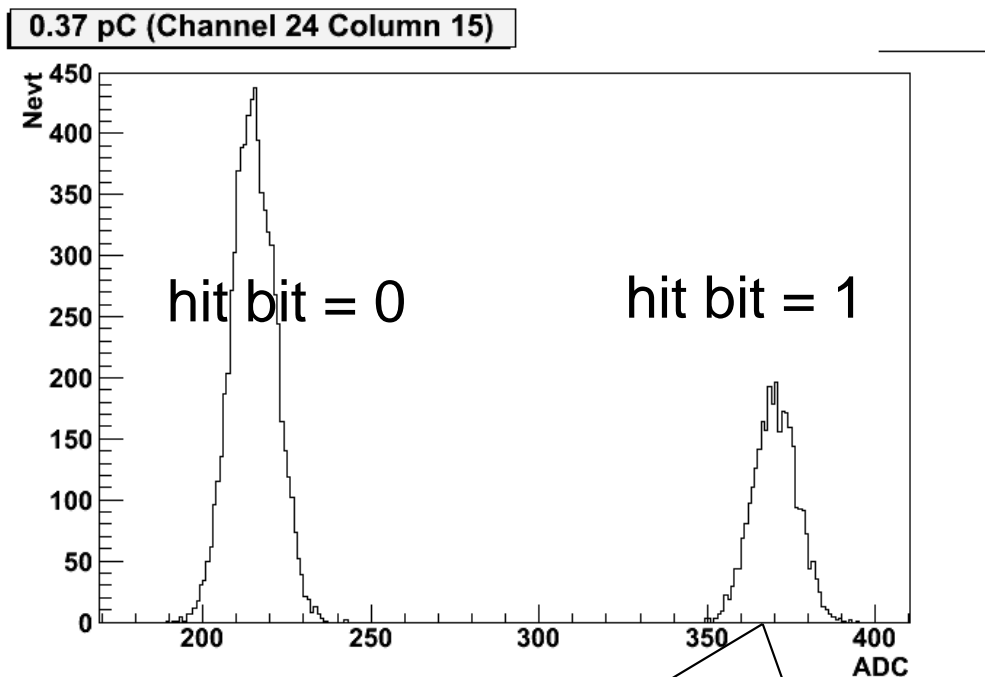
2 data samples:

1 UADC=250 μ V

- DAC value = 200 (all events triggered) → reference sample
- DAC value = 250 → studied trigger threshold

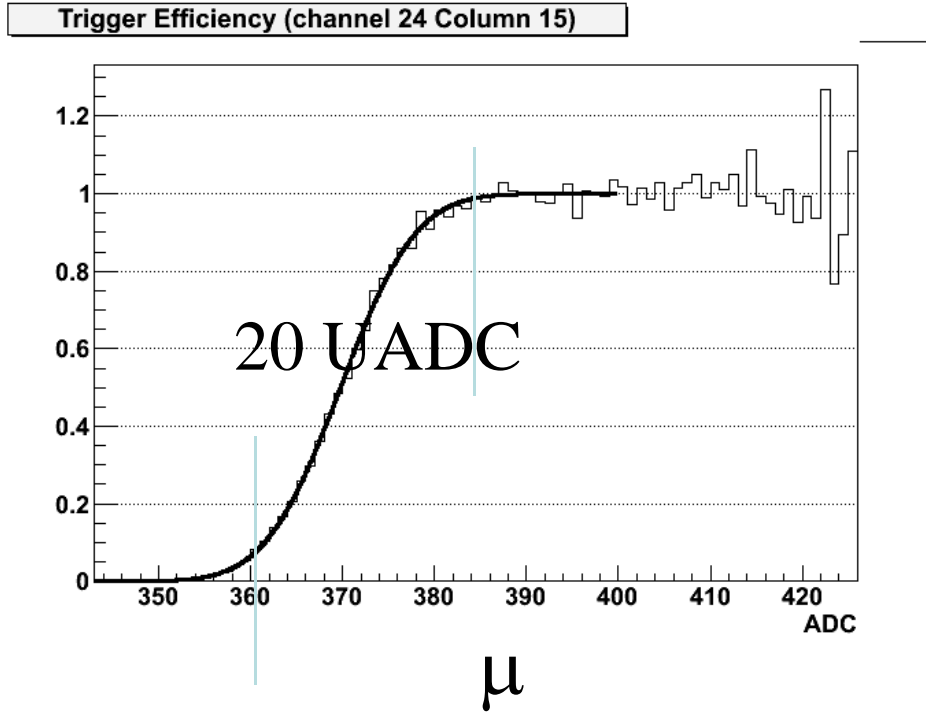
Trigger efficiency

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Trigger efficiency in function of the converted value

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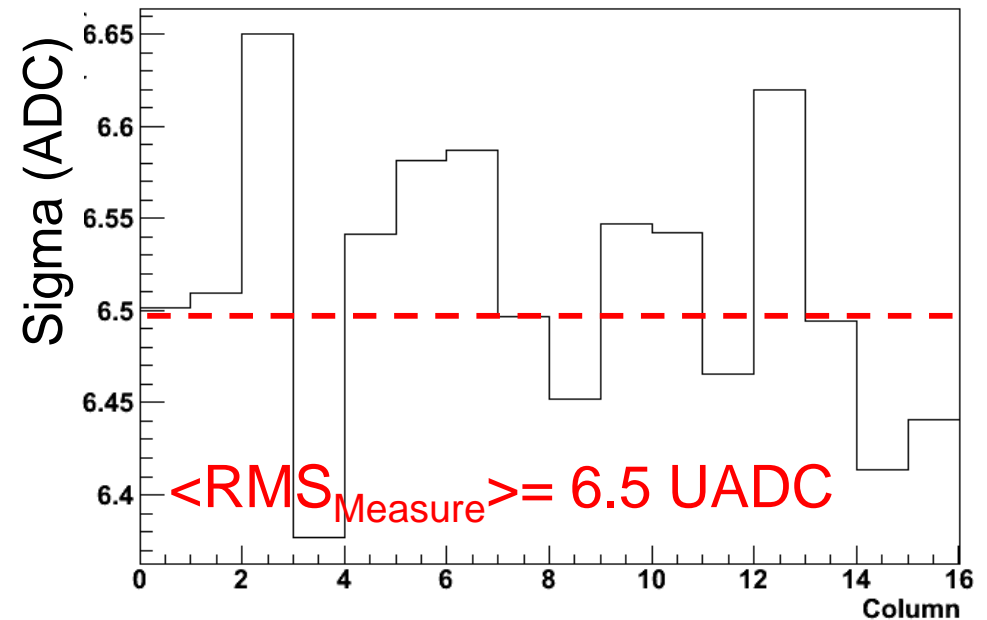
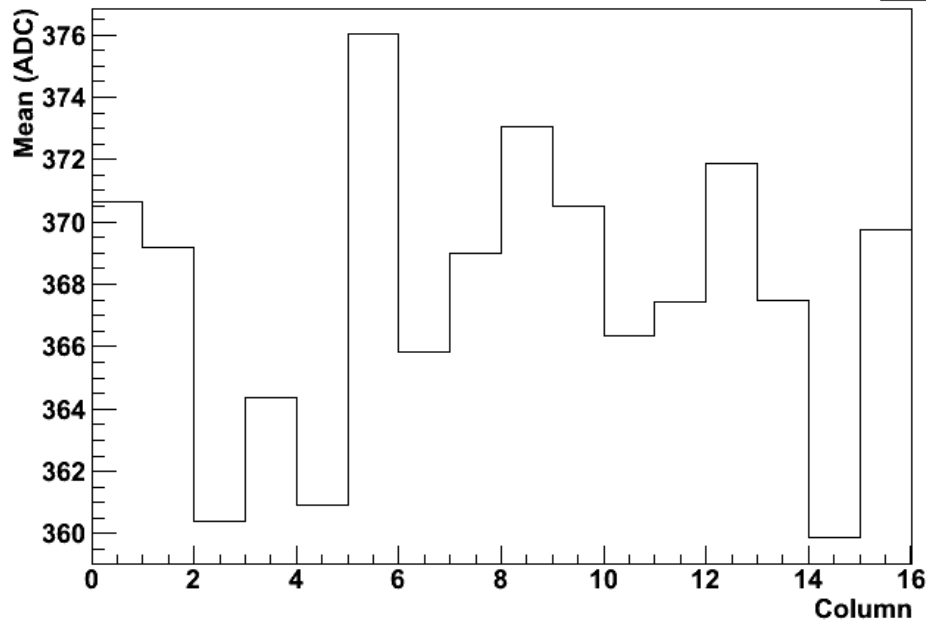
$$f = \frac{1}{2} \cdot \left[1 + \text{Erf} \left(\frac{x - \mu}{\sigma \cdot \sqrt{2}} \right) \right]$$

ORSAY: 20 UDAC

DESY: 100 UADC

measurements with SiPm → Noisier.

σ



Next step: stability of the efficiency in function of the DAC threshold