Status of the AHCAL engineering prototype

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CALICE collaboration meeting

Heidelberg, September 15th, 2011

- Tiles
- First SPIROC2b tests
- New HBU
- DAQ
- Summary and outlook

Tiles

- Signal sampled by scintillating tiles

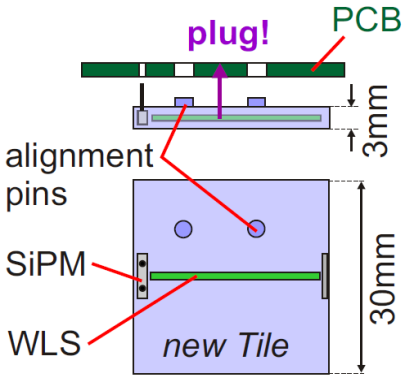
  → 3x3x0.3cm^3, 2592 tiles per layer
- First version of HBU/tiles:
  - Gain/Noise ~ 4
  - MIP/Noise ~ 30 (in high gain mode, 2 GeV electrons)
- No large sample of tiles available at DESY (only ~20 from last year)
- ~800 at ITEP, ~400 tested

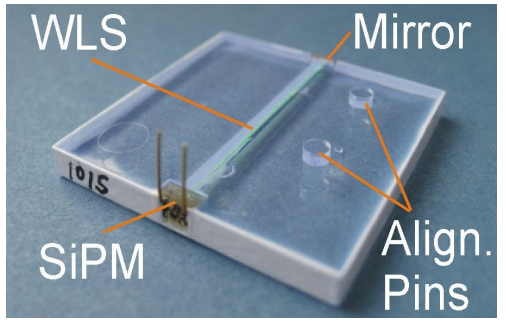
  → ~3 weeks to test all

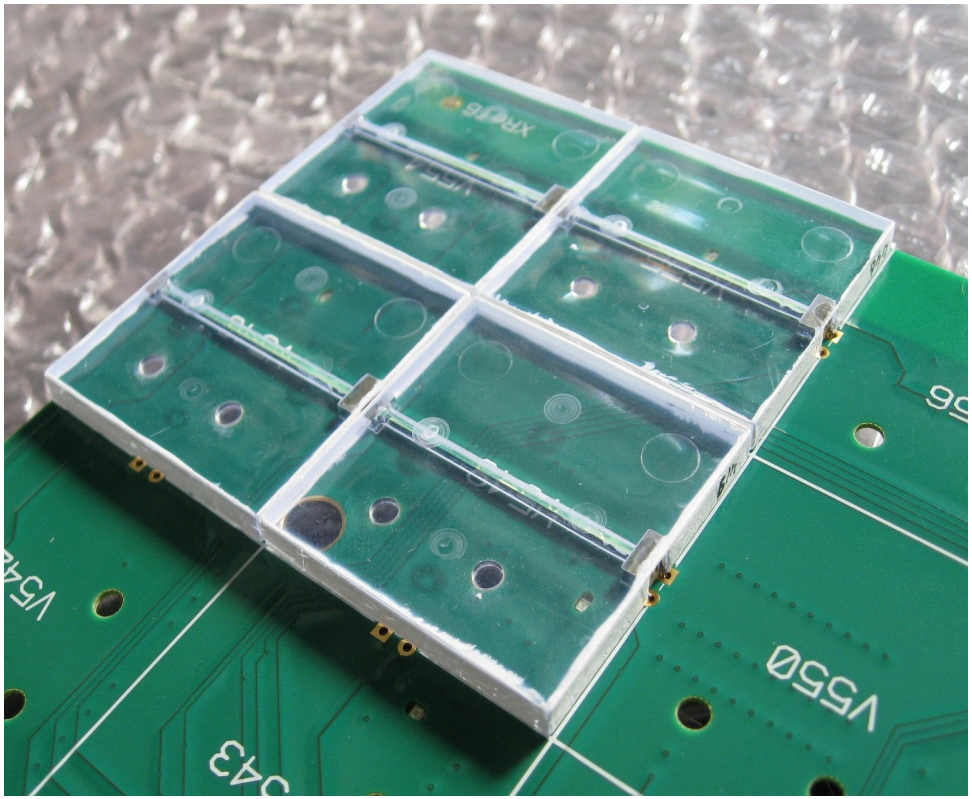
  → Selection (groups of same bias voltage and set of other criteria)

  → ~600 new tiles to be sent to DESY end of September

  → Equip 4 new HBU2s







Selection of new tiles

- ITEP proposed selection criteria for new tiles

  - HV such that we have 13 pixels for Sr90 signals

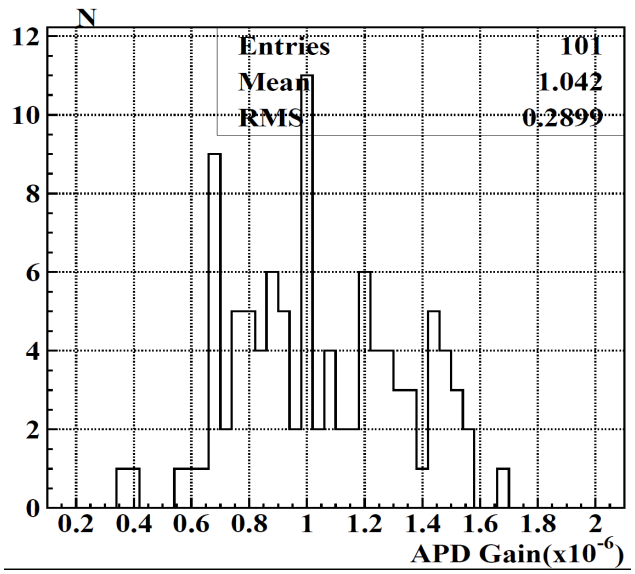
  - Gain larger than 450000 for 140ns gate, >400000 for 100ns gate (~50ns shaping)

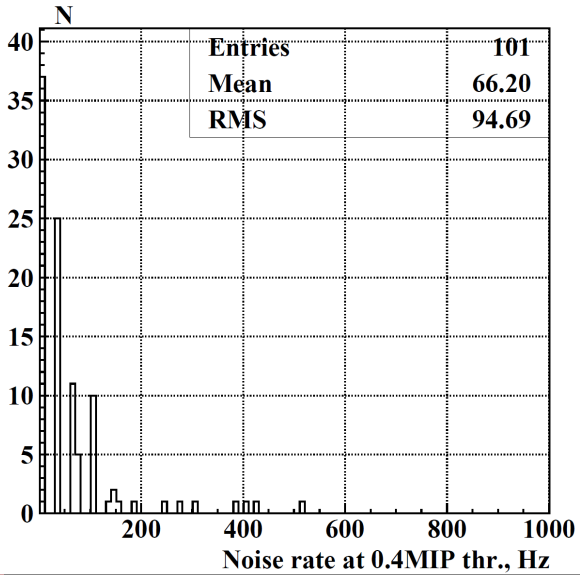
  - Noise at 0.4 MIP smaller than 500Hz → <100Hz at 0.5 MIP

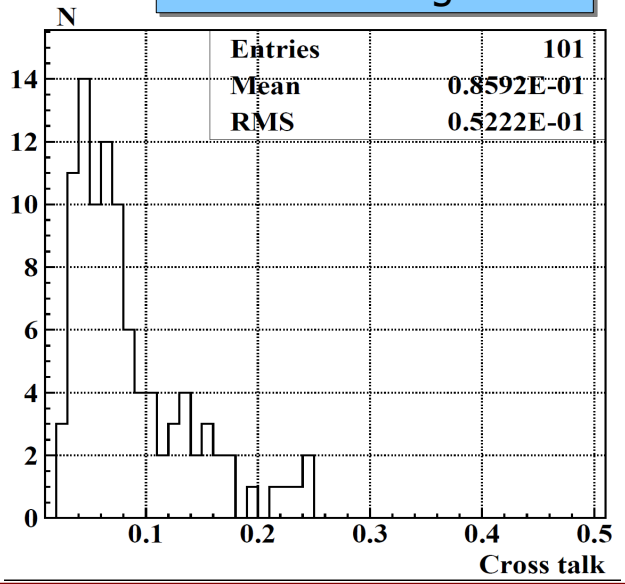
  - Cross talk less than 20%

  - Number of pixels at maximum light >700

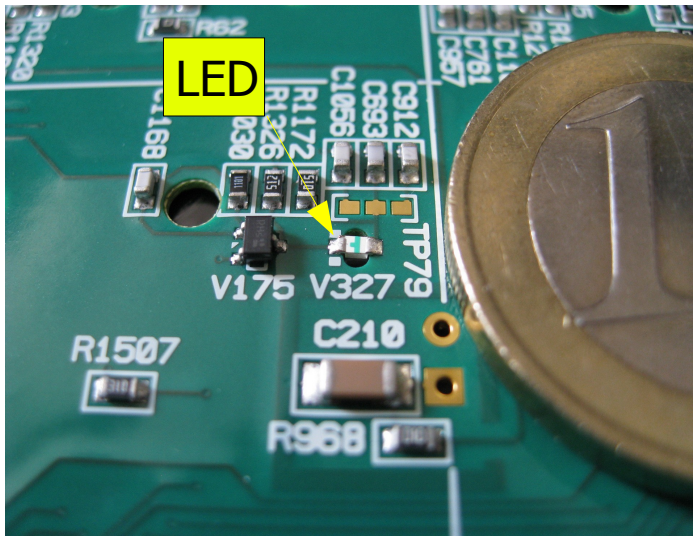
Plots shown by Misha at last meeting

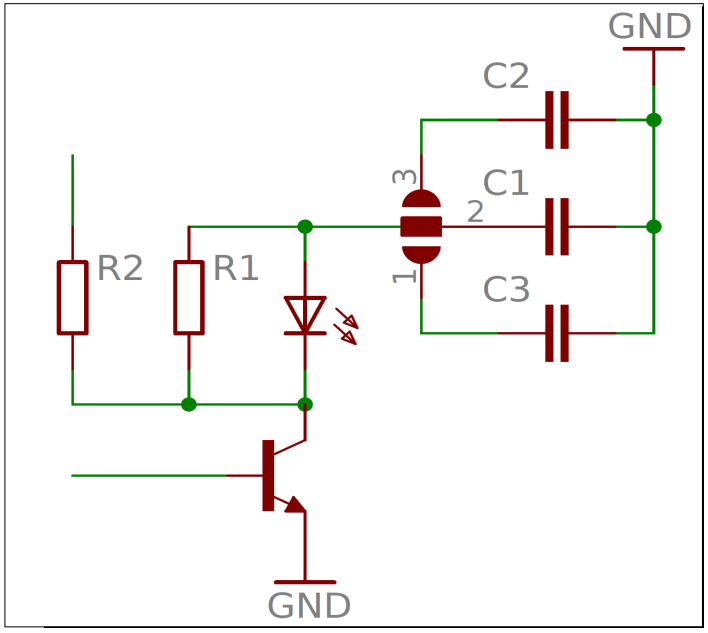






LED calibration system





Wuppertal solution:

- Light directly coupled into tile by 1 integrated LED per channel
- Light output equalization via C1 - C3
- New design implemented in new HBU2 and will be tested extensively by new Master student

Prague solution:

- Light coupled into tile by notched fiber
- Mechanical integration difficult

  → First tests in multi HBU2 setup end of the year at DESY
- See talk from Ivo

SPIROC2b

Specific chip for SiPM readout:

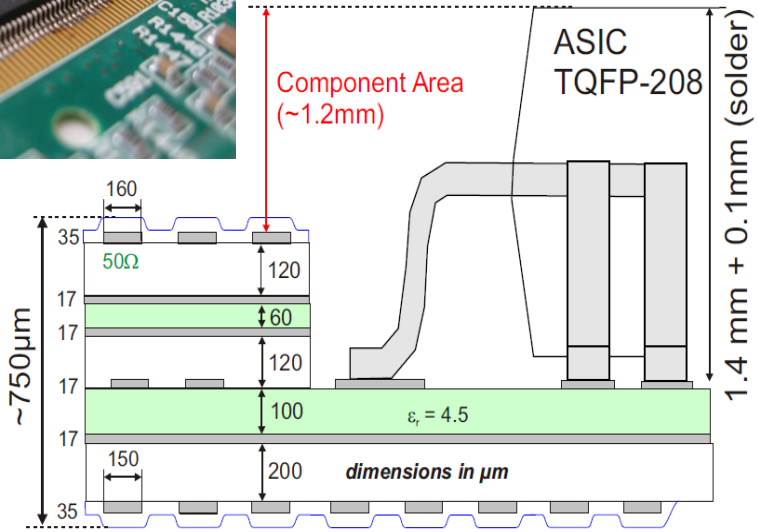
- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

- Power pulsing → 25µW/ch
- Dual-gain setup per channel

  → high gain/low gain ~ 10

  → 25fF – 1575fF per channel
- Auto-trigger and auto-gain mode
- Time stamp (12-bit TDC)



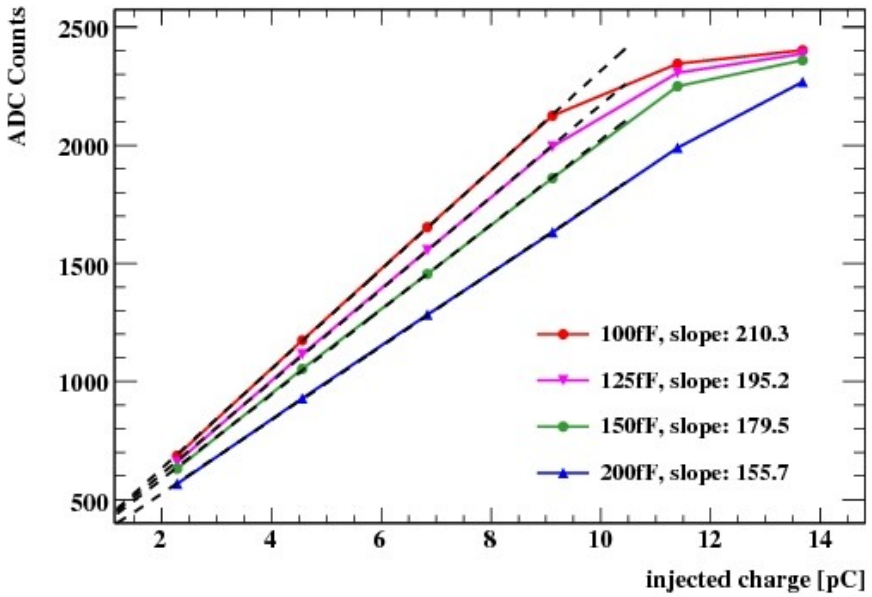
Placement of components in PCB cutouts

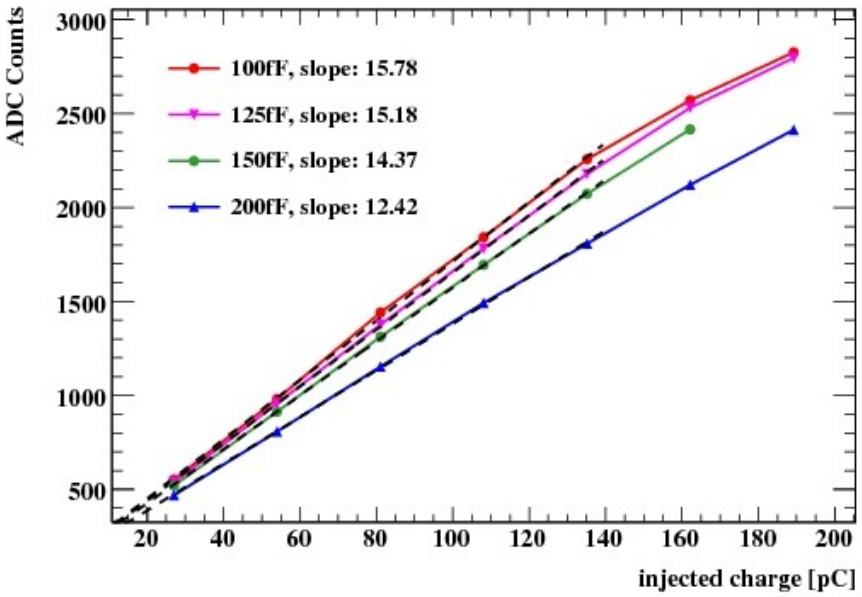
→ 500µm/layer

→ 50mm in total!

Although SPIROC3 is in the pipeline we will most probably use SPIROC2b for first tests with multi-HBU setups and testbeam!

SPIROC2b – First tests

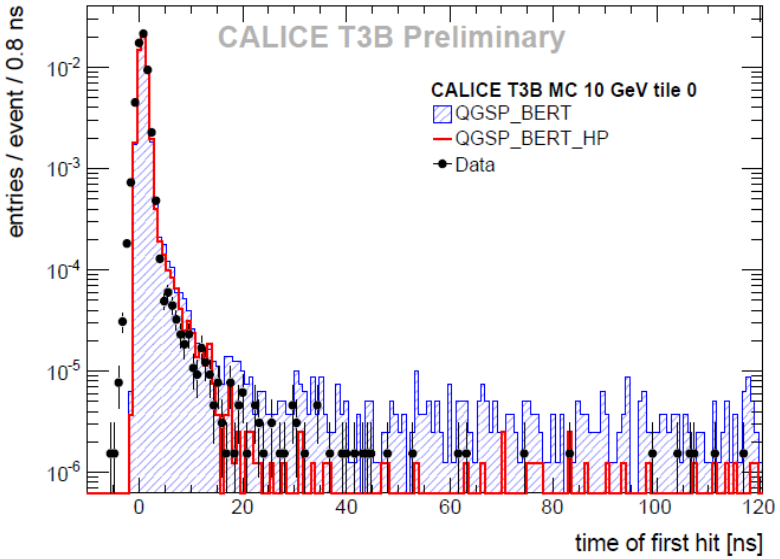


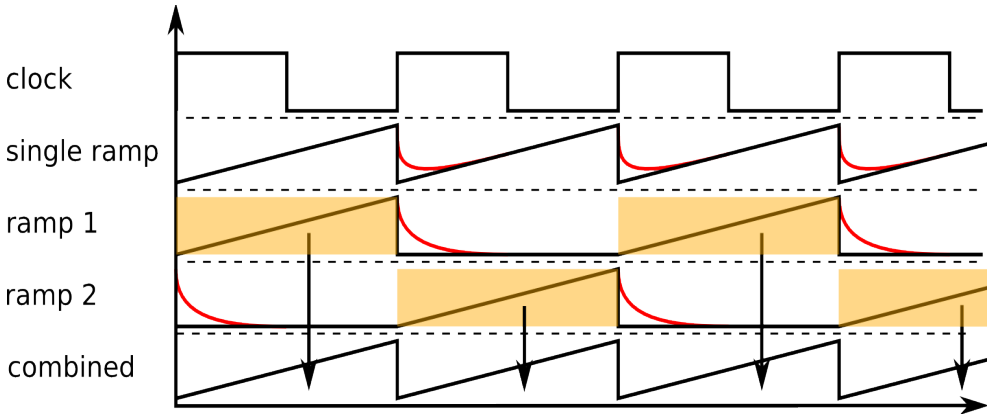


- SPIROC2b integrated in old HBU for first tests
- First measurements on linearity, preamplifier gains, auto trigger and TDC in old HBU
- We see first signals in HBU2!

→ Slow control programming, data taking with external trigger and readout works

SPIROC2b – Time measurements





- T3B measured radial development of shower in time in one row of last layer

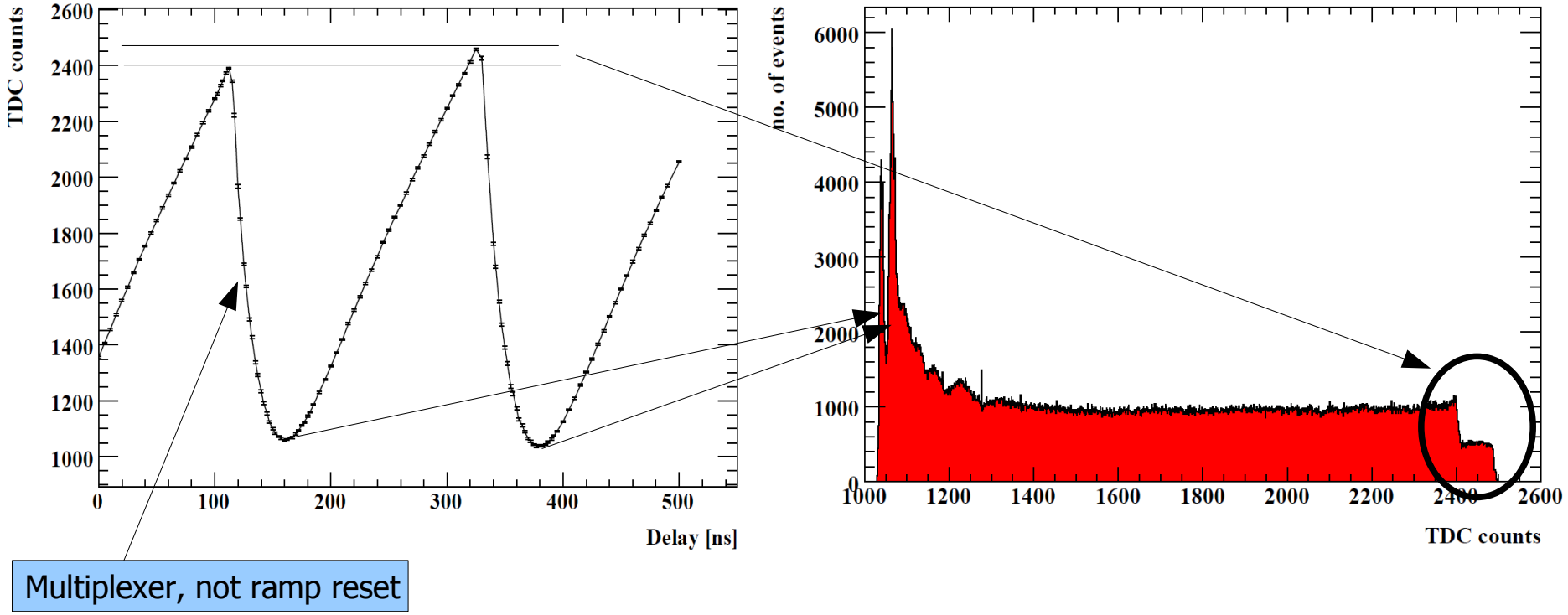
  → Repeat measurement with full layer or even multiple layers
- SPIROC2b measures time in auto-trigger mode relative to bunch clock

  → 2 ramps to reduce deadtime due to ramp reset

  → ILC mode = 200ns ramp, testbeam mode = 5µs ramp (less dead time)

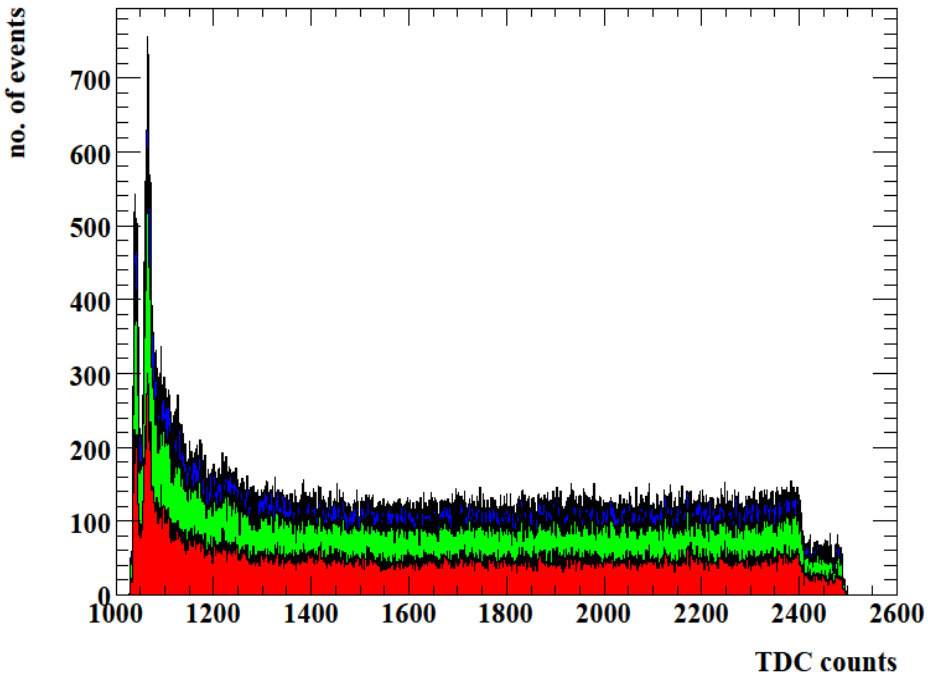
  → Investigate time resolution to optimize ramp slopes (and lengths)

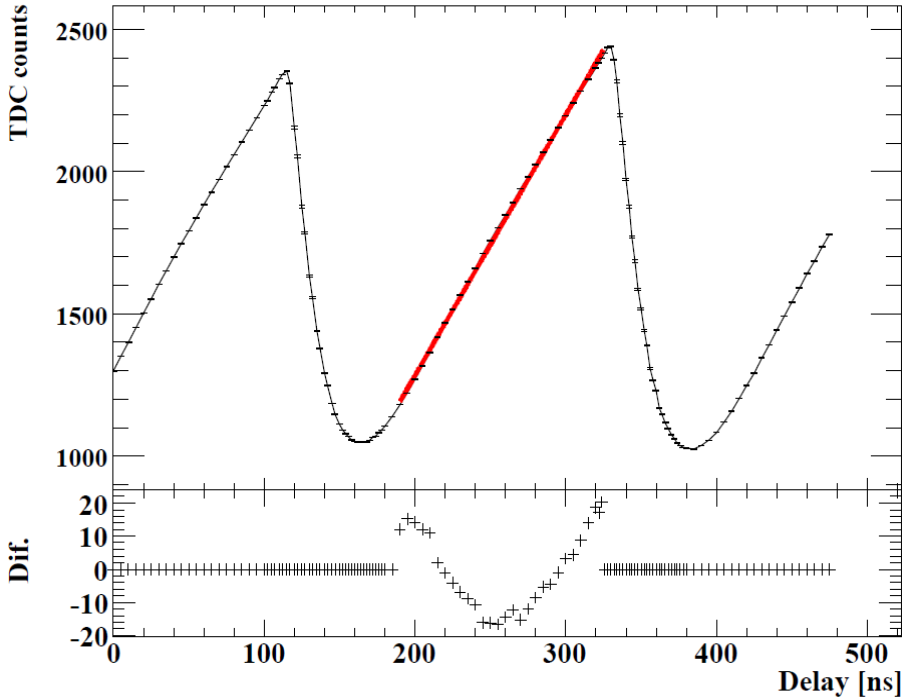
SPIROC2b – TDC (ILC mode)



- First tests of TDC ramps in SPIROC2b show promising results
- Resolution in ILC mode: ~250-350ps (dominated by linearity)
- The 2 ramps have different slopes/heights in ILC mode
- A few aspects will change in SPIROC3 (see Frederics talk)

SPIROC2b – TDC (ILC mode)





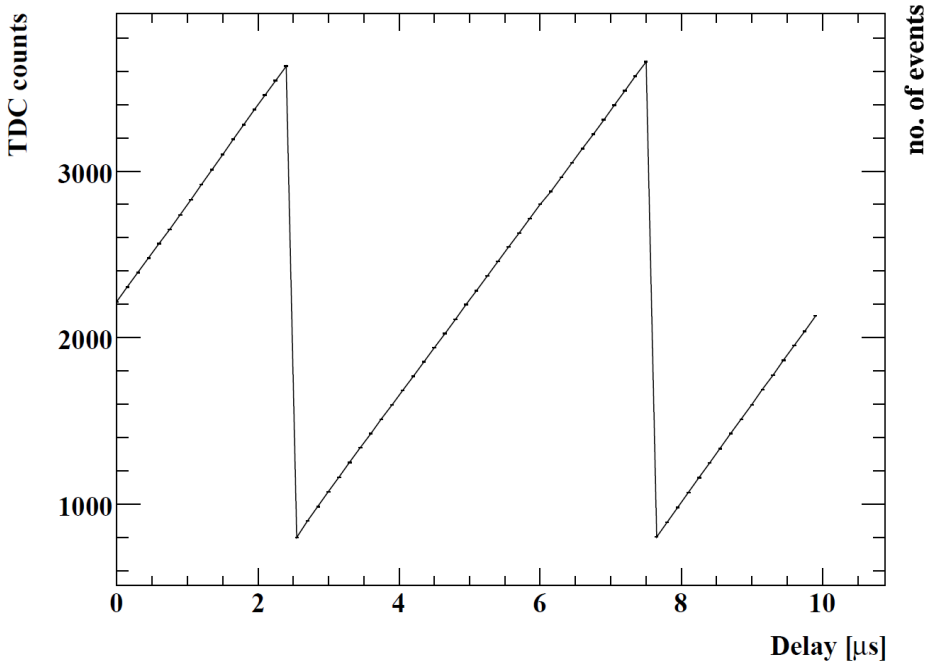
- No correlations visible between ADC and TDC measurements
- Resolution in ILC mode limited by linearity (~1ns)

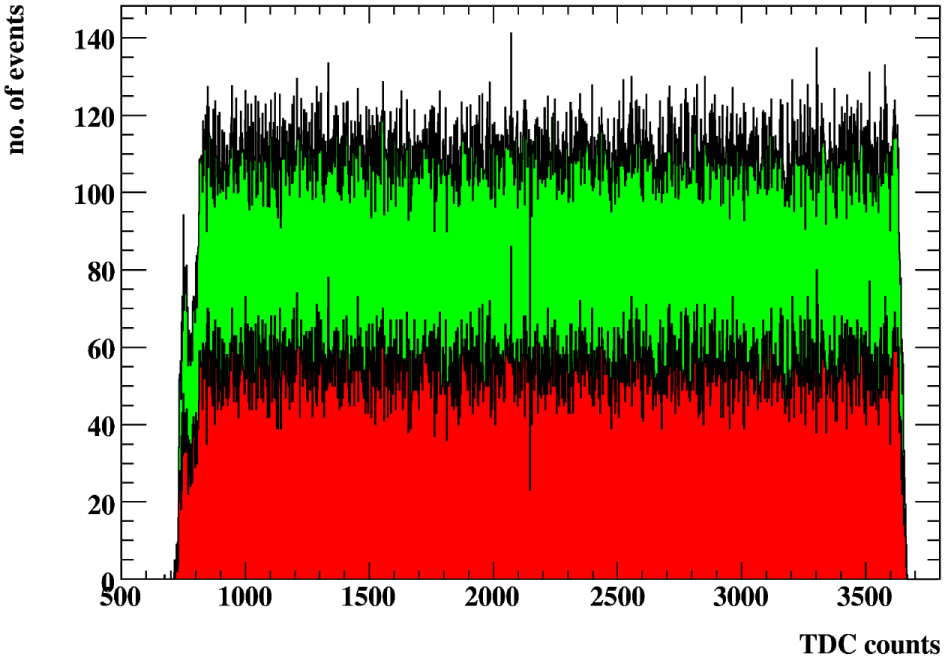
  → Linear fit reveals clear structure

  → Fit of 2 linear functions improves resolution (~300ps)

  → What is the most reasonable measurement/fit strategy?

SPIROC2b – TDC (testbeam mode)





- Multiplexer deadtime very small in testbeam mode (longer ramp)
- Resolution in testbeam mode: ~3ns
- Very small (no?) differences for the two ramps in testbeam mode
- Resolution of ~1ns possible by optimizing ramp slopes (and dynamic range)

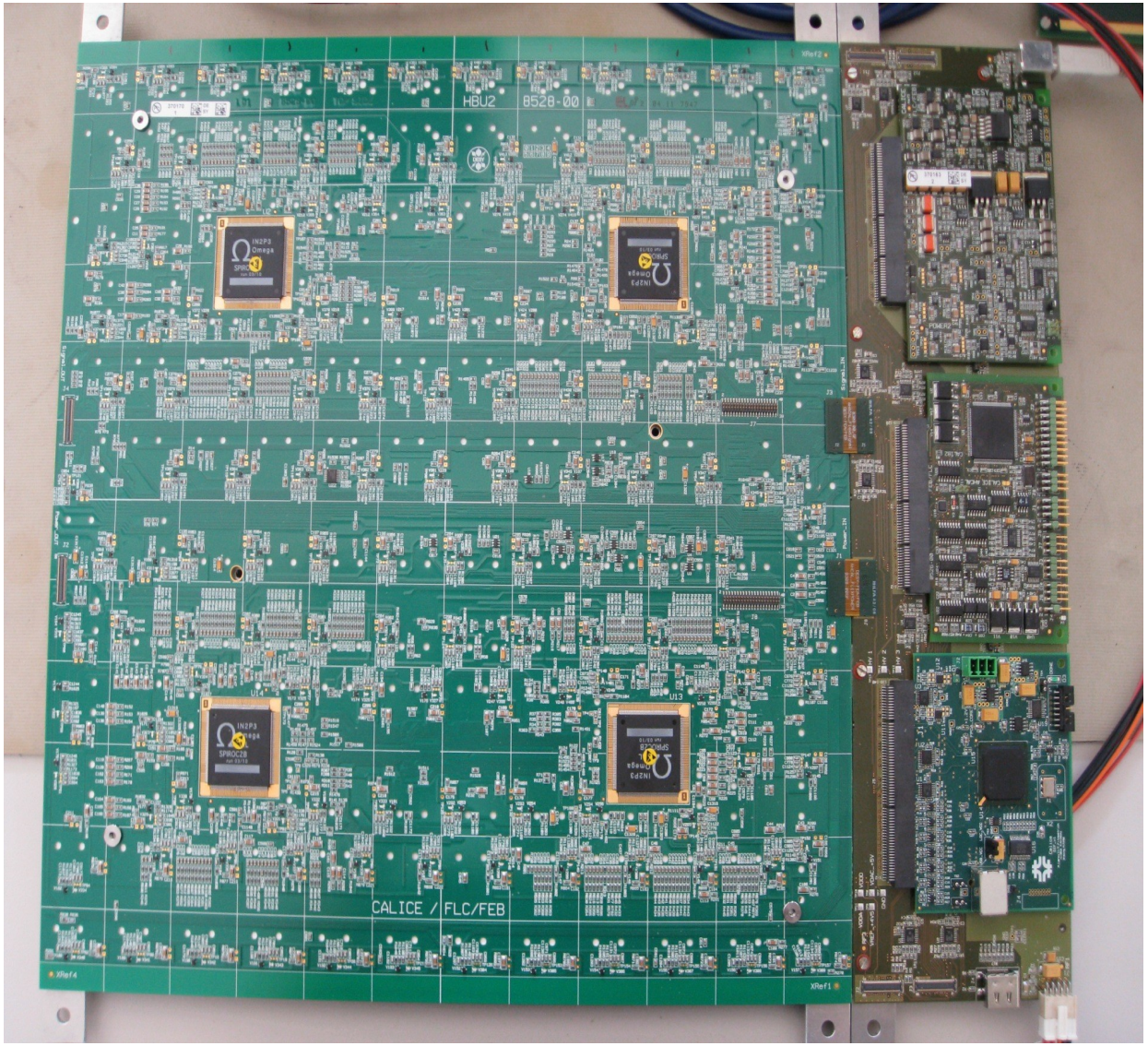
  → Tests with 1.25µs ramp promising

New HCAL Base Units (HBU2)

- 4 prototypes of new HBU in DESY lab
- 1 HBU2 connected to DAQ modules for first tests

  → so far fully functioning!
- No new tiles yet!
- Plan is to have 6-8 HBU2s at end of year

  → New SiPM production at ITEP to be started
- As soon as 1 HBU2 is fully working/equipped with tiles, we can go to DESY testbeam

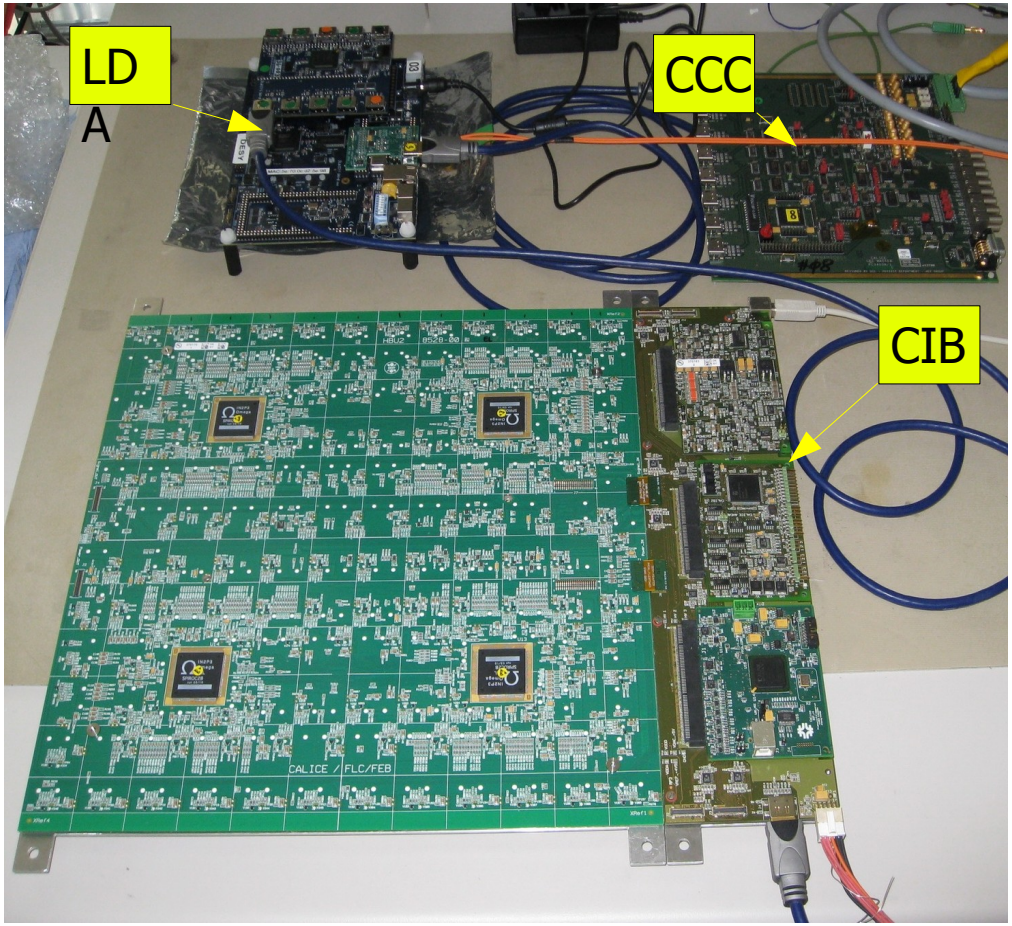


Data acquisition

- All components working at DESY
- 2 options:
  - Labview based DAQ for SPIROC2b tests and single HBU testbeam (finished)
  - XDAQ for full detector operation

    → to be started
- Currently 3 DIFs from NIU

  → Duplicate setups for more students, for Wuppertal, testbeam etc.



Summary and outlook

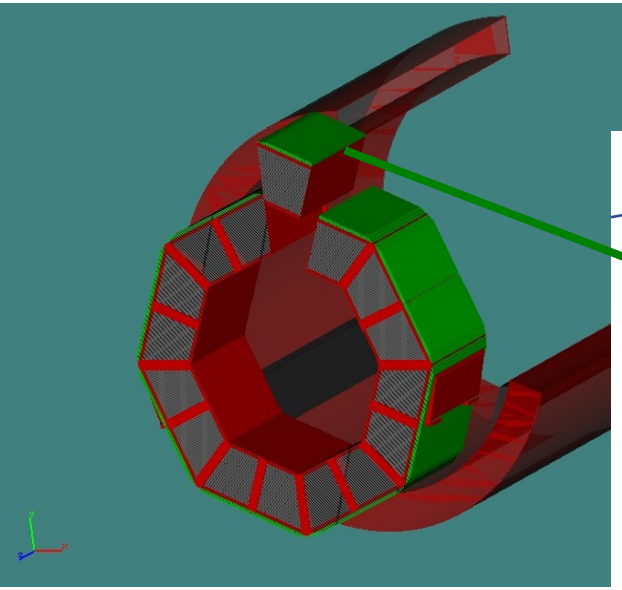
- HBU2 under test at DESY, so far fully functioning!
- First SPIROC2b tests in (old and new) HBU environment
  - Channel-wise preamplifier gain setup works
  - TDC measurements show promising results, both in ILC and testbeam mode
  - First successful data taking in HBU2 environment
- Tiles to be sent to DESY soon

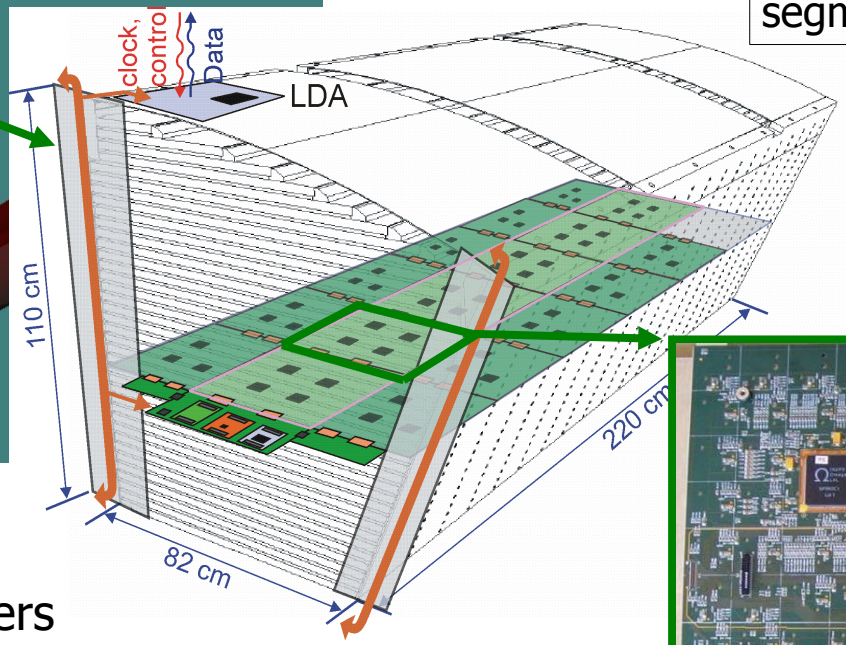
To do

- System tests of calibration system
- Plenty of SPIROC2b tests in HBU2 environment
- Continuing tests of power pulsing (see Peters talk)
- Assembly of multi-HBU2 setup (~6 HBU2s at end of the year?)
- DAQ development
- etc. etc.

The engineering AHCAL prototype

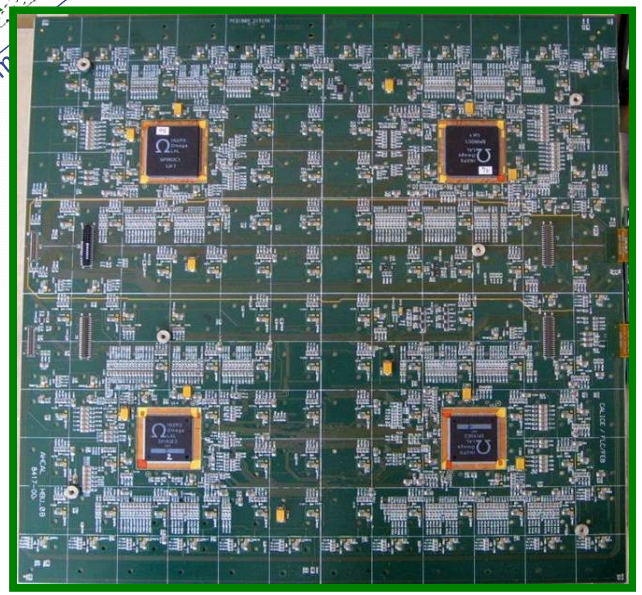
Development of scalable LC detector based on successful experience with physics prototype





Octagonal shape, 16 equivalent wedges, segmented in two along z

PCB with 4 SPIROCs, 144 scintillator tiles, SiPM readout

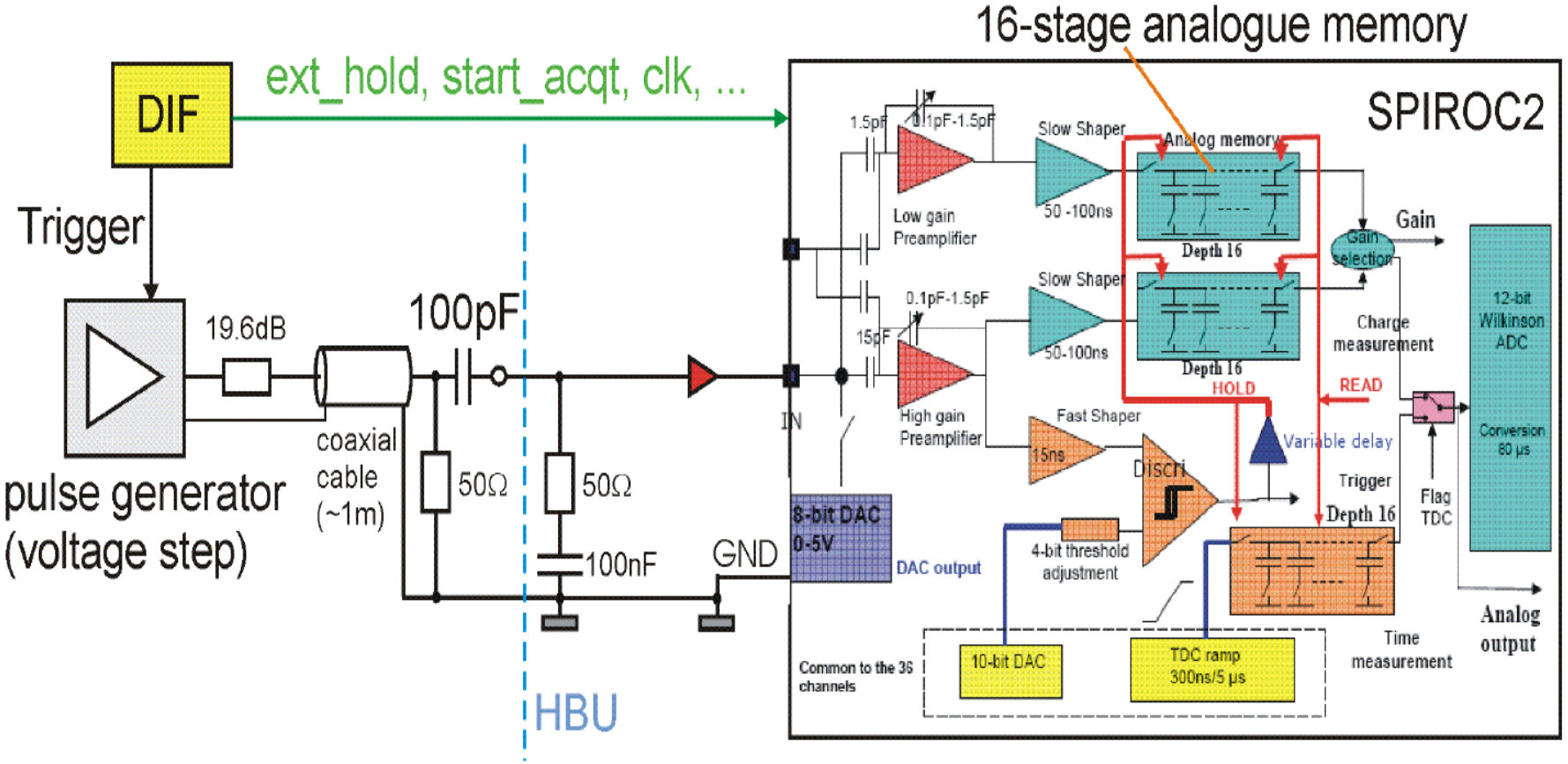


Challenges:

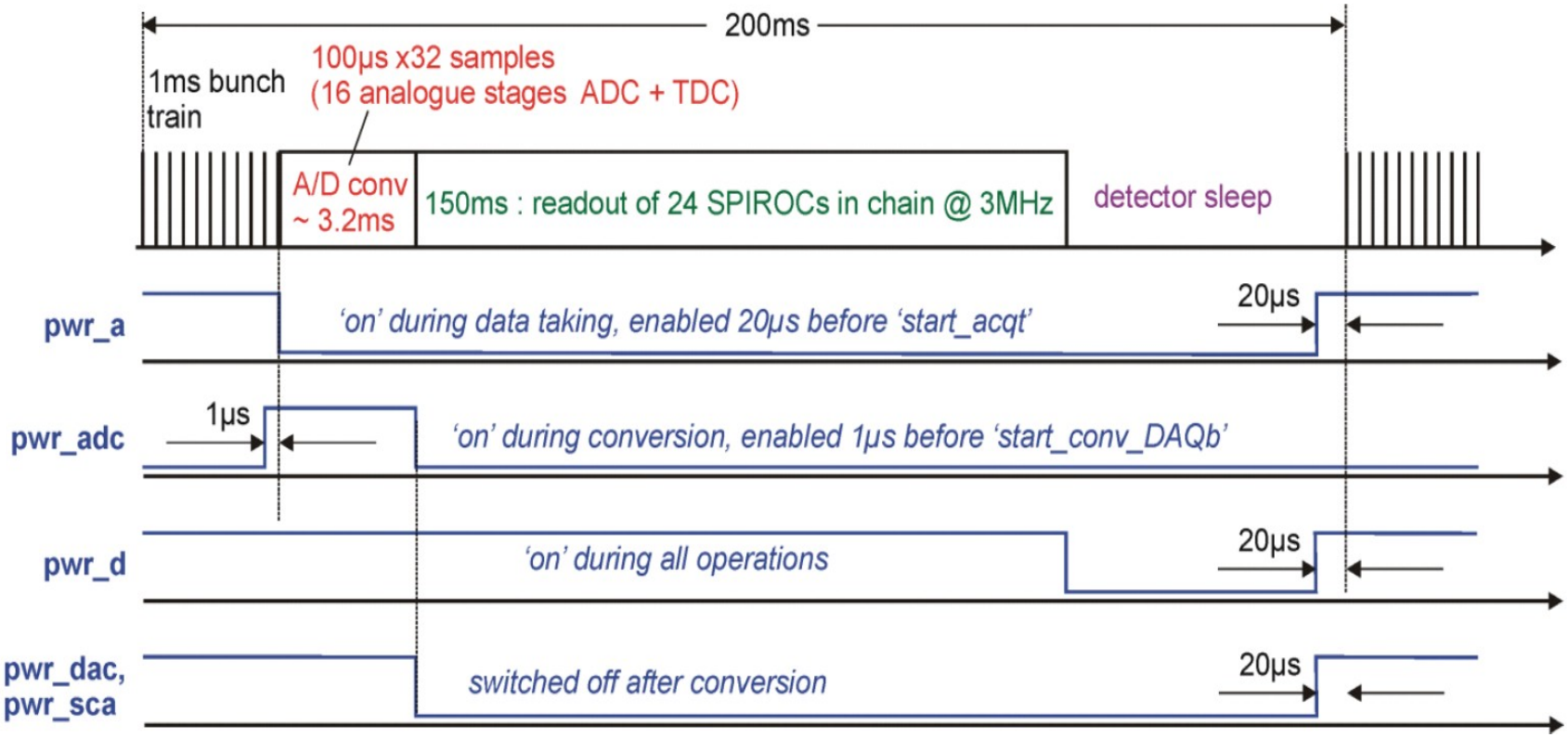
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

→ Integrated readout electronics

SPIROC2b

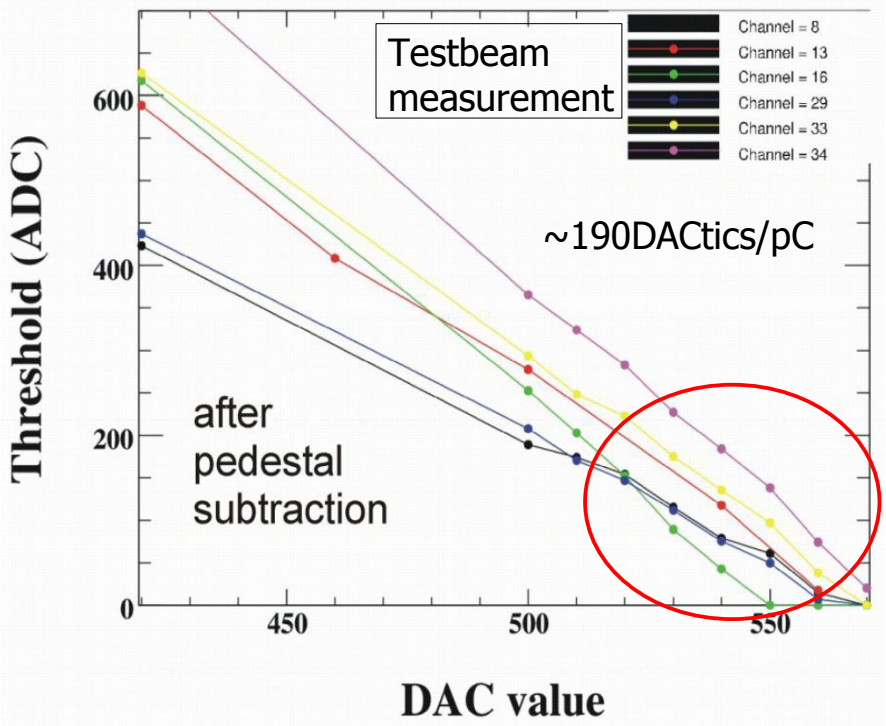

16-stage analogue memory
DIF
ext_hold, start_acqt, clk, ...
Trigger
19.6dB
100pF
coaxial
cable
(~1m)
50Ω
50Ω
100nF
GND
pulse generator
(voltage step)
HBU
IN
SPIROC2
1.5pF
0.1pF-1.5pF
Low gain
Preamplifier
Slow Shaper
50 -100ns
Analog memory
Depth 16
Gain
Gain selection
Slow Shaper
0.1pF-1.5pF
15pF
50-100ns
Depth 16
Charge
measurement
HOLD
READ
12-bit
Wilkinson
ADC
Conversion
80 µs
High gain
Preamplifier
Fast Shaper
15ns
Discri
Variable delay
Trigger
Depth 16
Flag
TDC
8-bit DAC
0-5V
DAC output
4-bit threshold
adjustment
Analog
output
Common to the 36
channels
10-bit DAC
TDC ramp
300ns/5 µs
Time
measurement

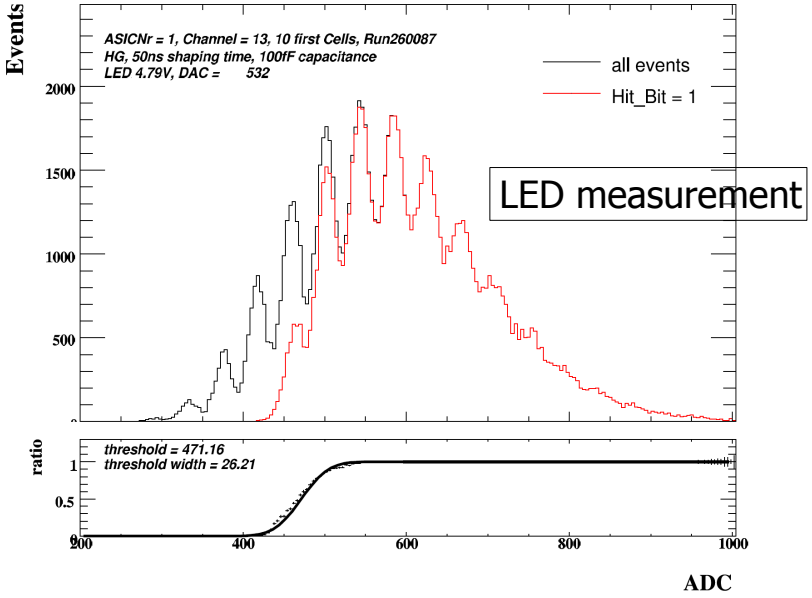
Power pulsing

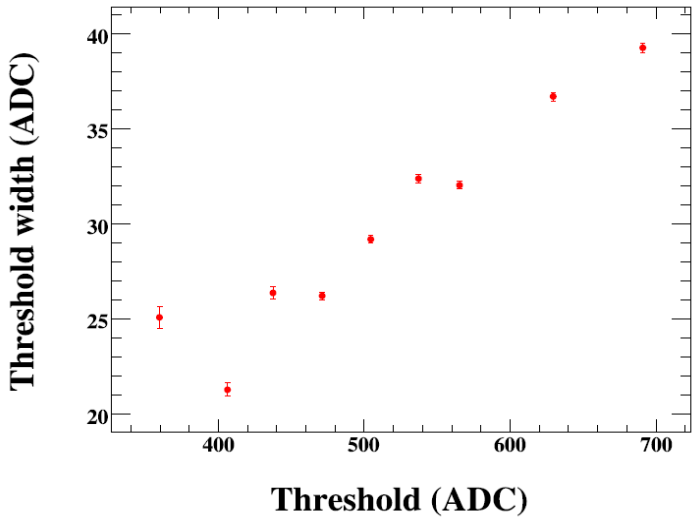


Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency

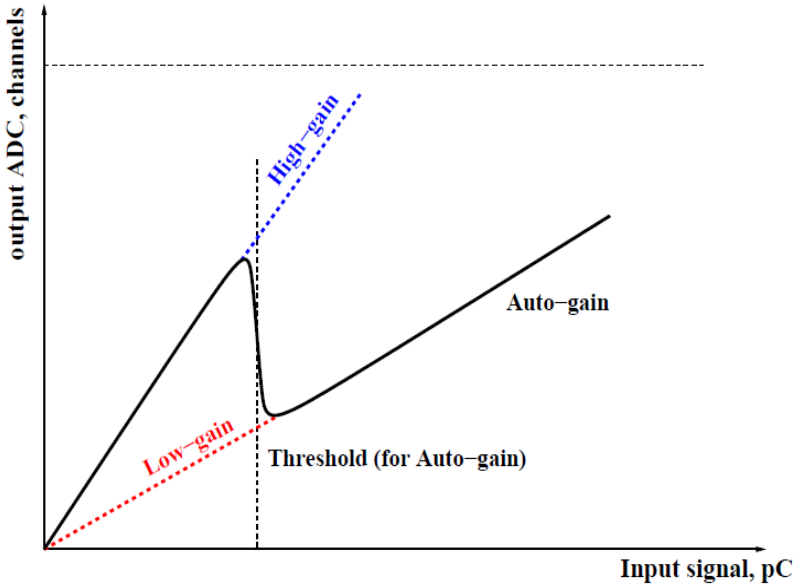


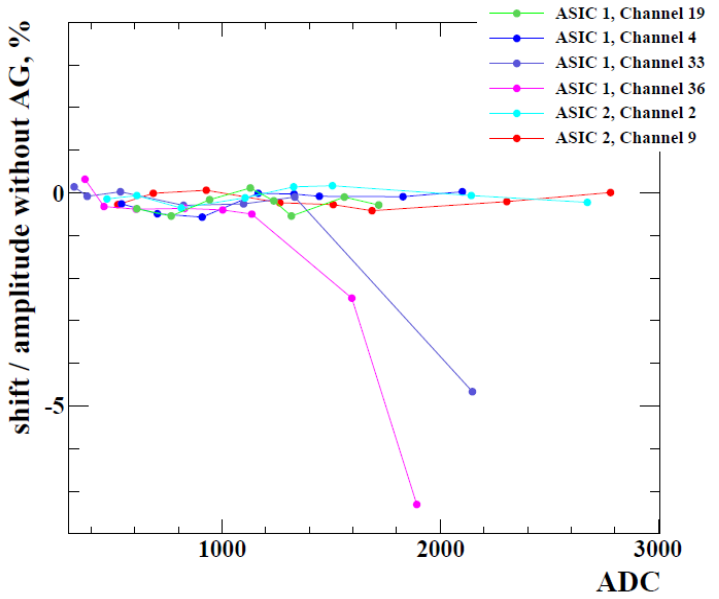


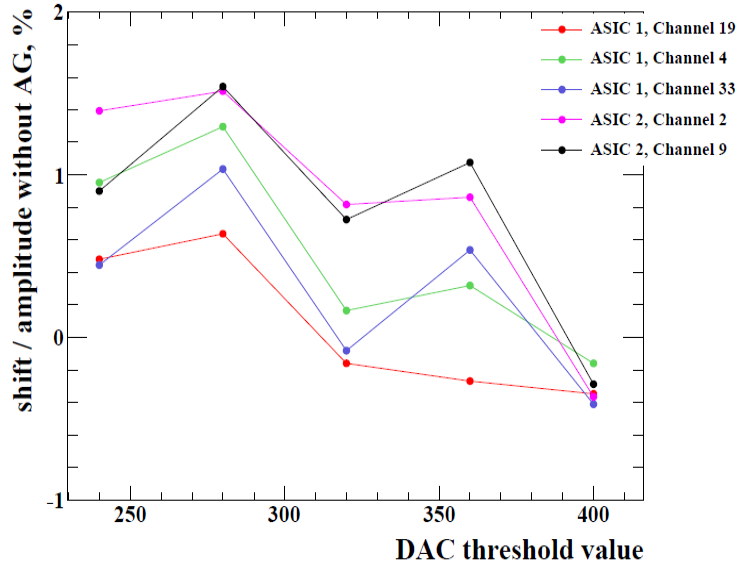


Autogain performance - Linearity

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, but still slightly depends on:
  - Amplitude
  - Distance to threshold

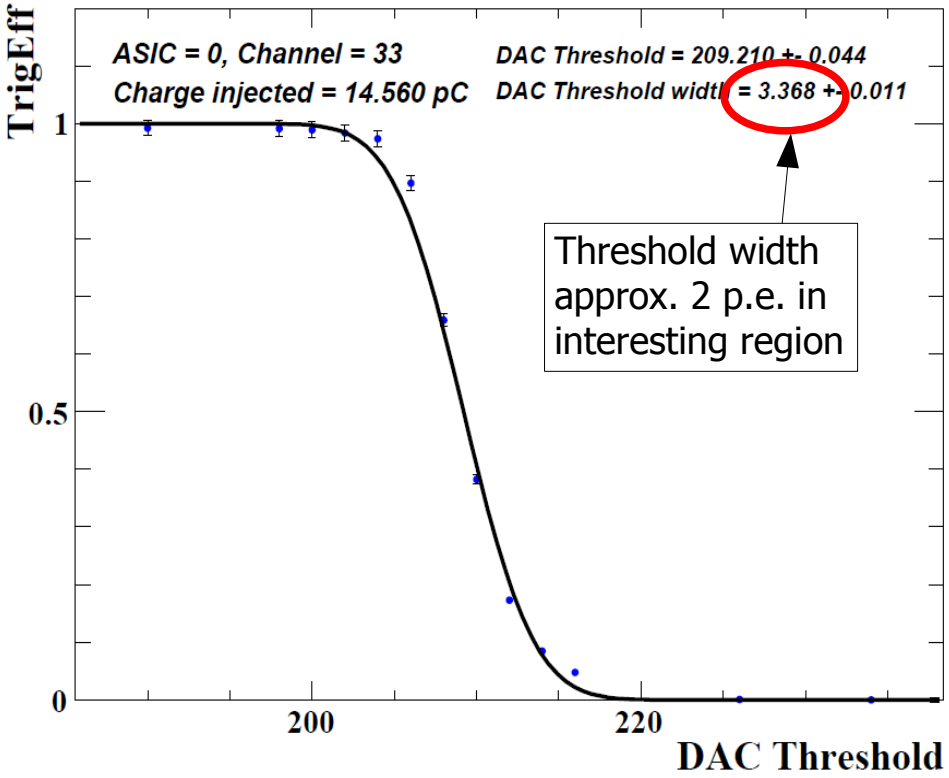


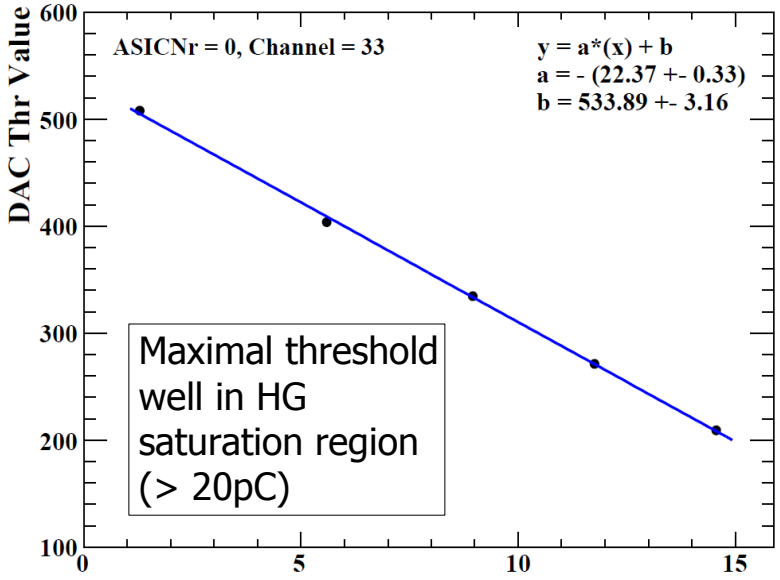


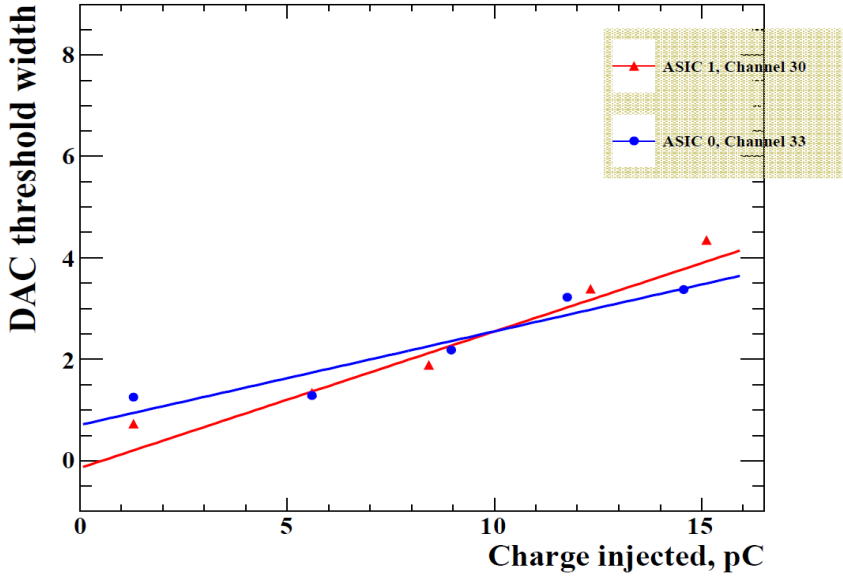


Autogain performance - Thresholds

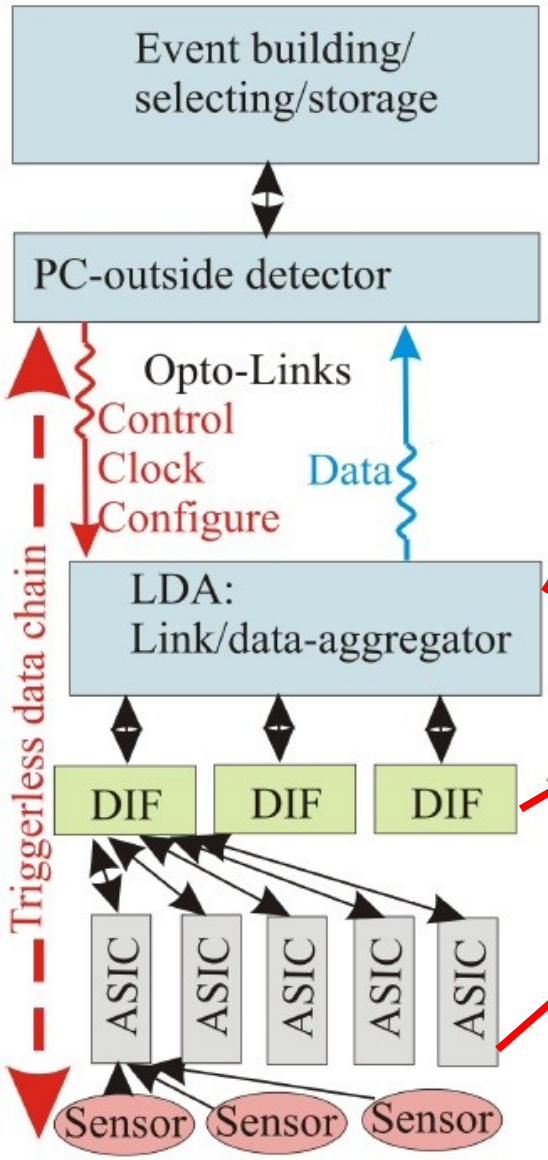
- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Similar performance as for autotrigger

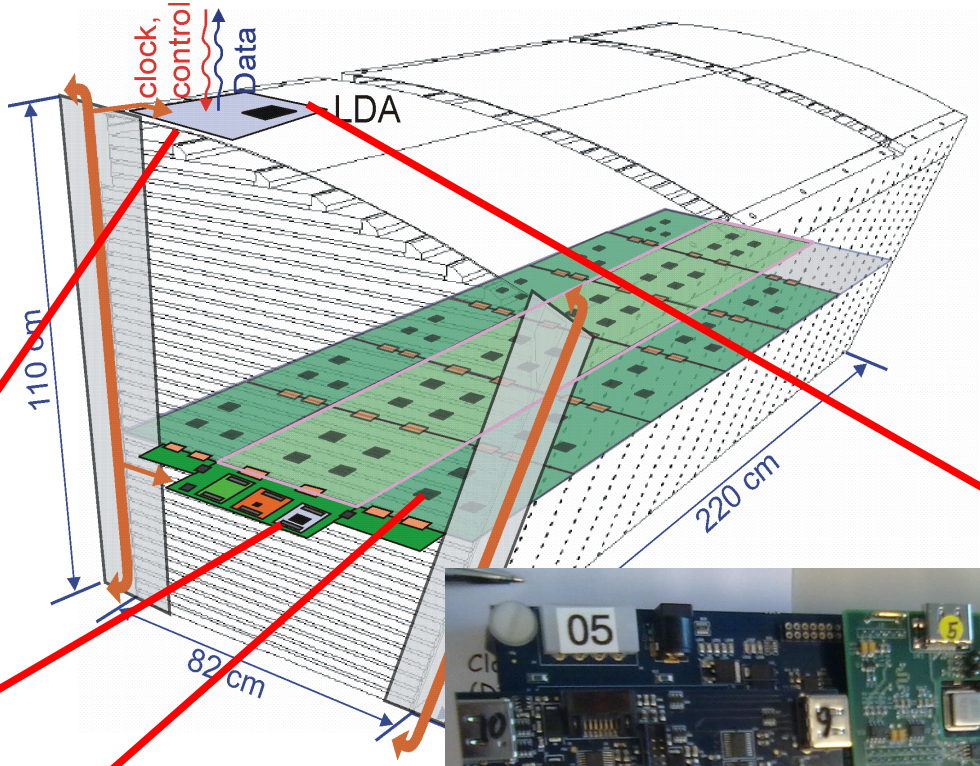


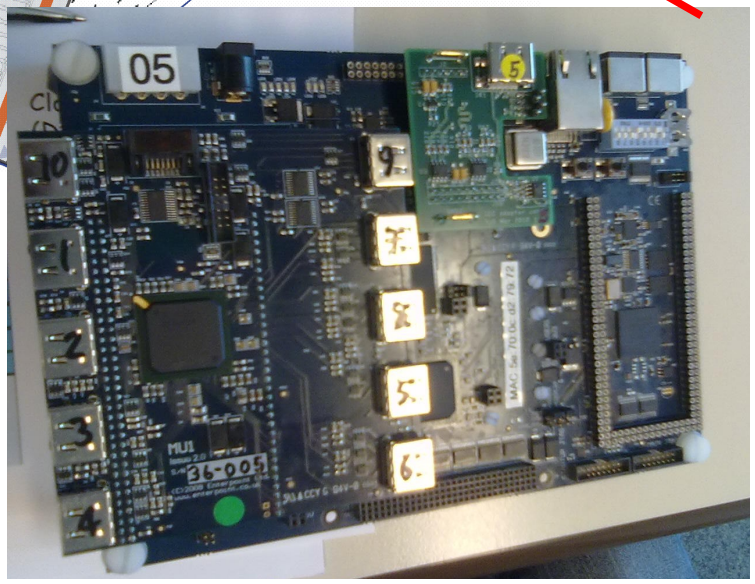




Data acquisition







DAQ data rates