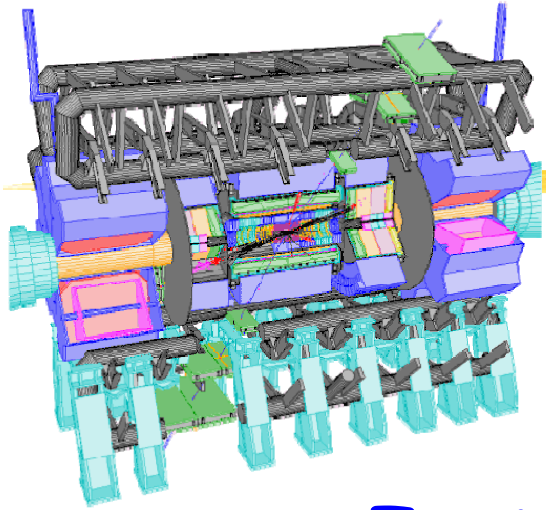


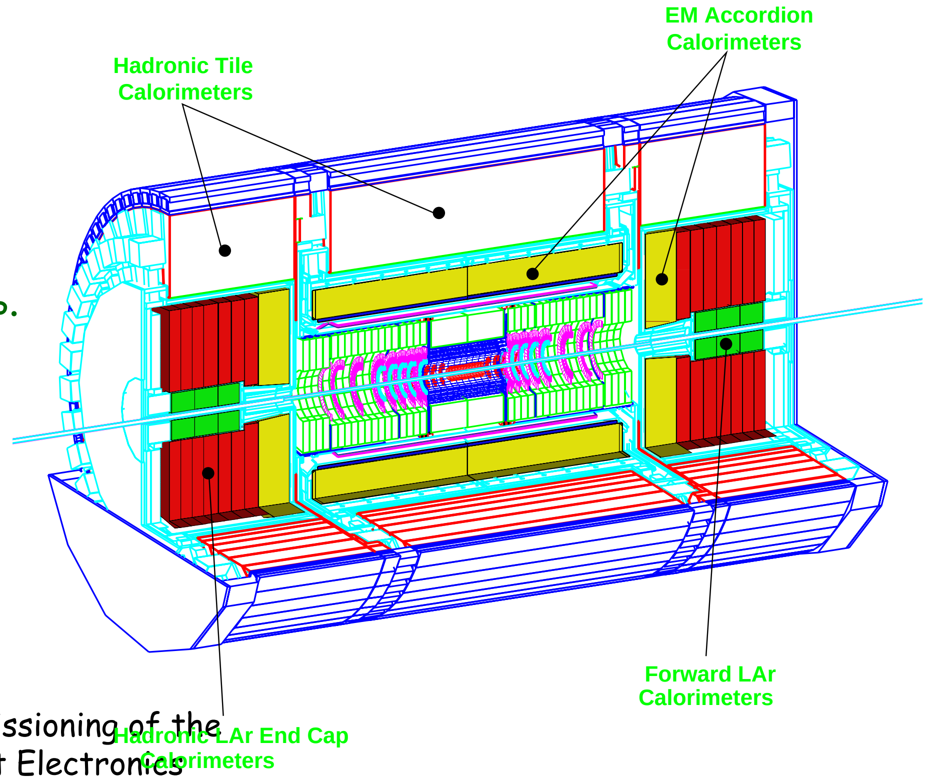
Installation and Commissioning of the ATLAS LAr Readout Electronics

Jingbo Ye
Southern Methodist University
For the ATLAS Liquid Argon Calorimeter Collaboration

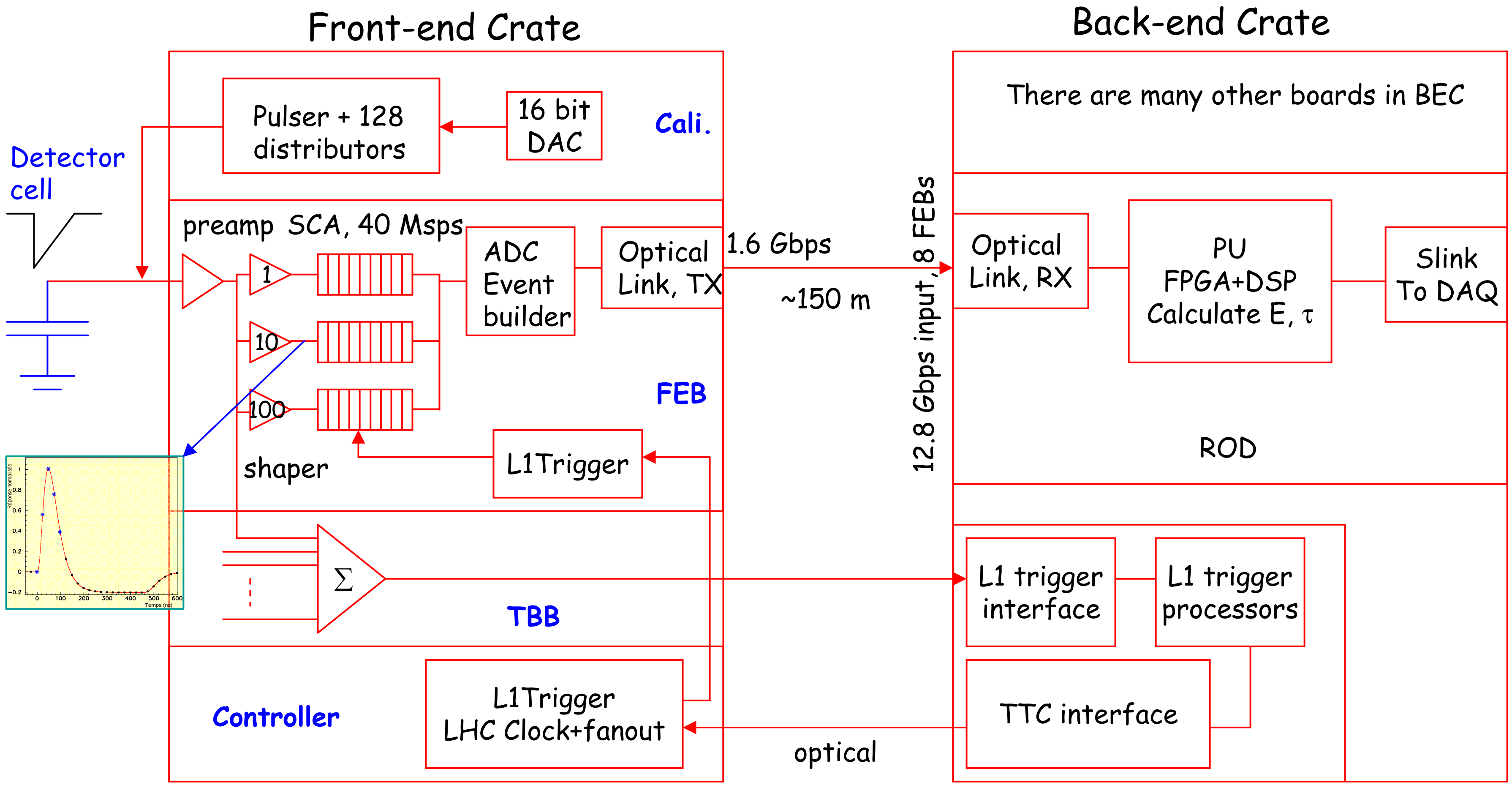
ATLAS LAr Calorimeter

- Physics goals dictate the calorimeter design
  - Higgs search in *$H \rightarrow \gamma\gamma$, $H \rightarrow ZZ \rightarrow 4$leptons (lepton = e, μ) requires* precise measurement of photon and electron.
  - SUSY search using missing E_T needs precise measurement of visible energy.
  - Low event rate in searches for Higgs and other new physics (*$W' \rightarrow e\nu$, $Z' \rightarrow ee$*) require high efficiency, high resolutions (E and spatial).
  - High (20 MeV to 2 TeV) dynamic range to maximize discovery potential.
- The ATLAS LAr calorimeters
  - Almost hermetic: $|\eta| \leq 4.9$
  - High granularity: ~190 000 cells
  - EM Accordion (Pb/LAr)
    - e/γ: $\sigma(E)/E(GeV) = 10\%/\sqrt{E} \oplus 0.7\%$.
  - Hadronic Endcap (HCAL)
  - Forward Cal (FCAL, Cu/LAr)

ATLAS Calorimetry (Geant)

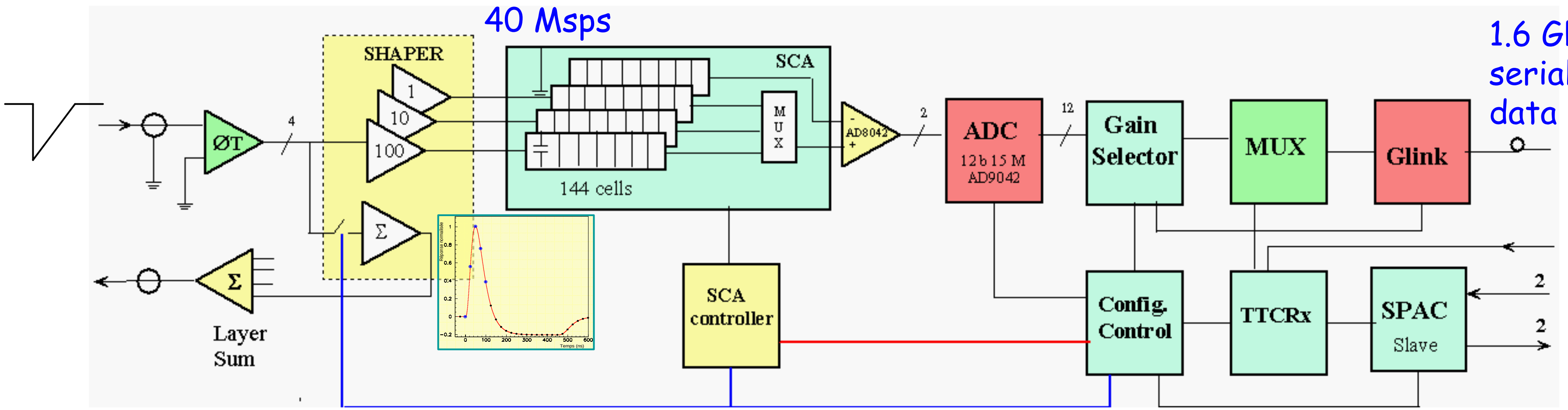


ATLAS LAr Calorimeter Readout



ATLAS LAr Calorimeter Readout

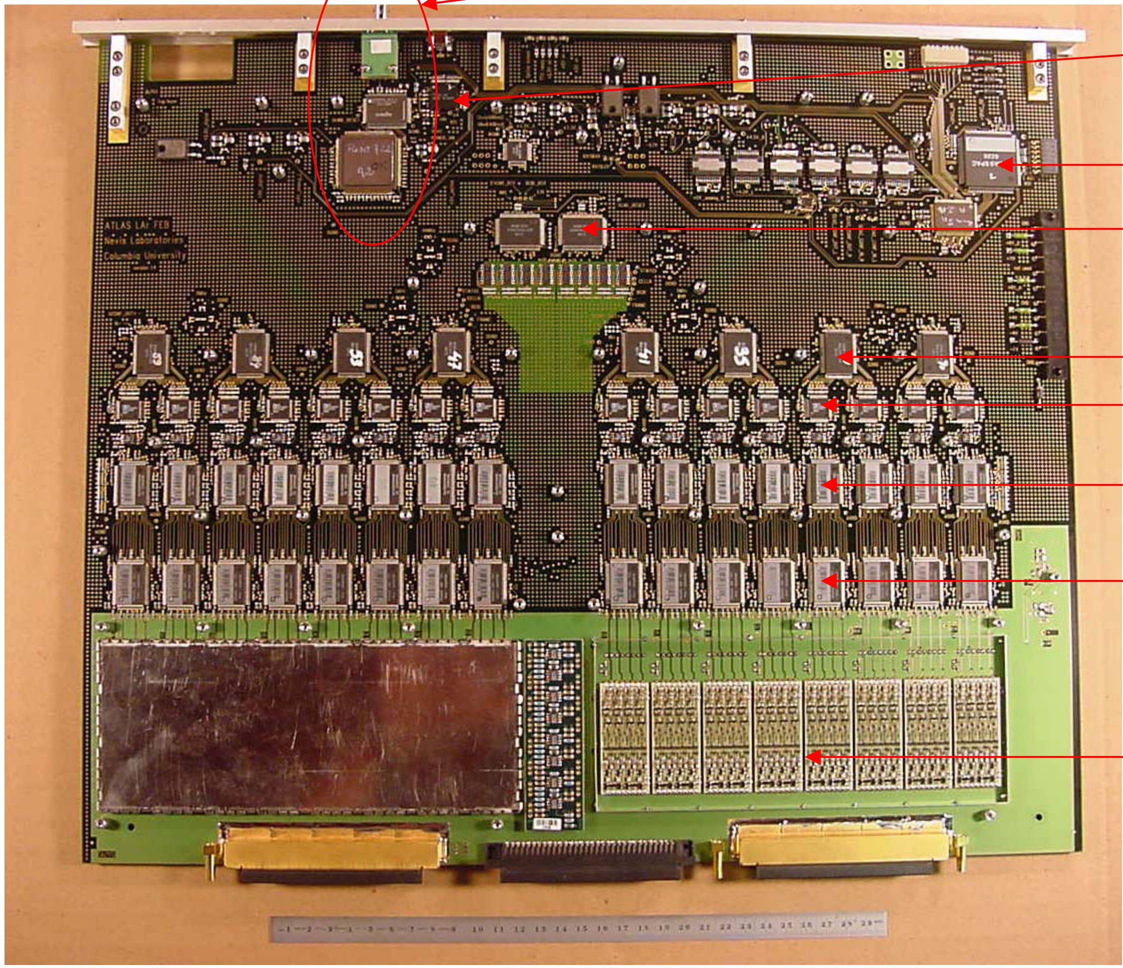
❖ Front-end readout



❖ Requirements

- Readout channel: ~ 190,000
- Dynamic range: 16 bits (3 gains plus 12 bit ADC), signal shapped to prevent electronics pileups.
- Data rate: 40MHz sampling and analog storage (SCA); L1 trigger on board up to 100 kHz.
- Rad-hard requirements (with safety factor):
  - **TID 850 Gy**
  - **NIEL 1E13 n/cm2 (1 MeV eq.)**
  - **SEU 4E12 h/cm2 (E > 20 MeV)**

ATLAS LAr Front-end Board



Optical link TX (Sub. System, DMILL, COTS)

TTCRx (DMILL)

SPAC (DMILL)

SCA Controllers (DSM)

GainSel (DSM)

ADCs (COTS)

SCAs (DMILL)

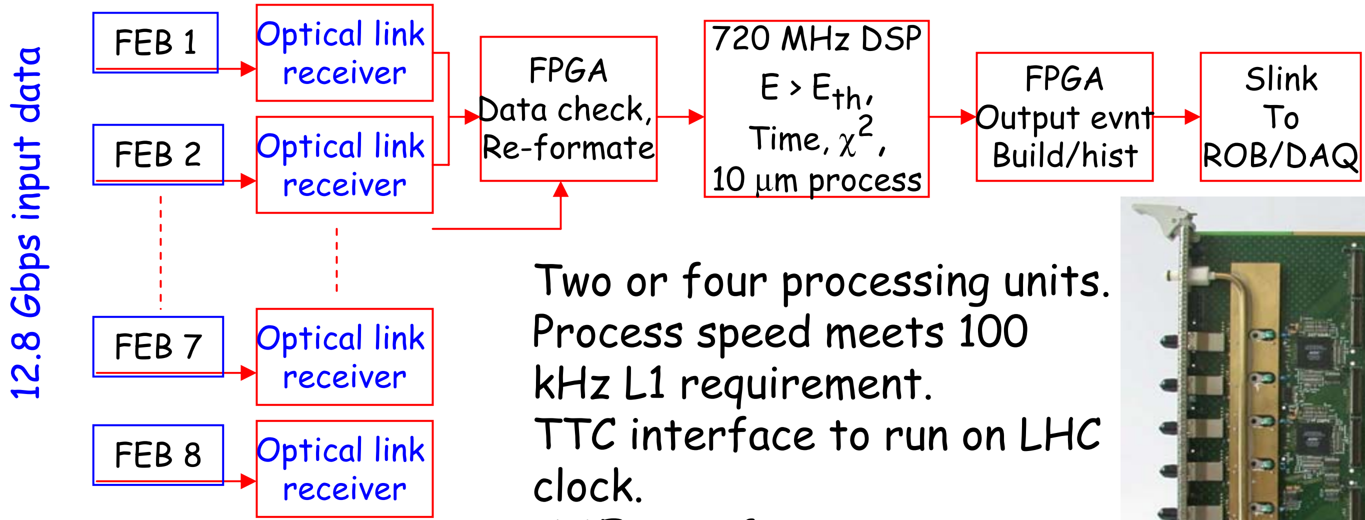
Shapers (AMS)

Preamps (sub. System)

Mix of three rad-hard technologies,
16 pos. Vreg, 6 neg. Vreg.

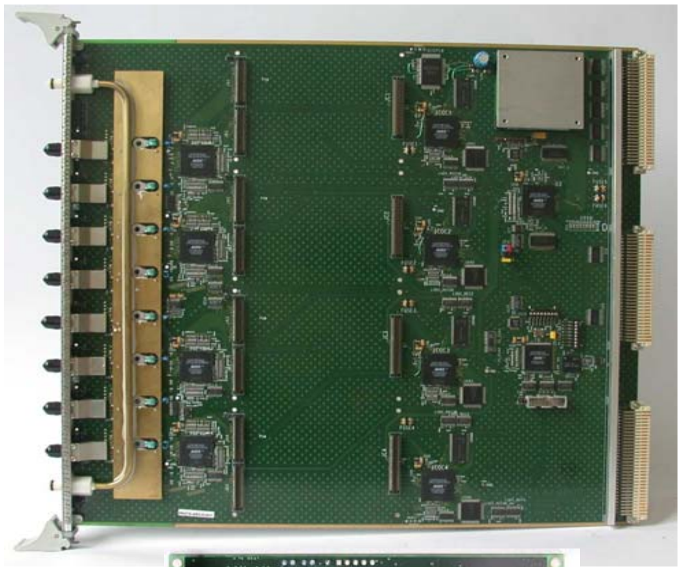
ATLAS LAr Calorimeter Readout

❖ Back-end readout



Two or four processing units.
Process speed meets 100 kHz L1 requirement.
TTC interface to run on LHC clock.
VME interface.

ROD motherboard



❖ Requirements

- Input data rate at 12.8 Gbps from 8 FEBs
- Data processing speed meet 100 kHz L1 trigger requirement.
- On-line monitoring, histograming and control request signal generation.

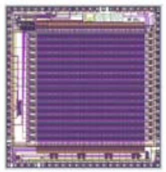
PU

Front-end Electronics Design challenges

- Large readout channels (~190k). High density frontend boards (128 channels per board).
- Low power (~ 0.8 W) per channel, but ~100 W per FEB → water cool.
- Large dynamic range (16 bits resolution achieved by 3 gains with a 12 bit ADC).
- Measure signals at bunch crossing frequency of 40 MHz.
- Store signals during L1 trigger latency of up to 100 bunch crossings.
- Digitize on board and read out 5 samples/channel at a max. L1 rate of 100 kHz.
- Event build and data serialization on board. Send 1.6 Gbps data through optical data link to backend. Optical data link used to reduce coherent noise.
- Mixed small analog and MHz to GHz digital signals on the same board.
- Very low jitter clock (<20 ps) for high speed serial data transmission.
- High reliability over expected lifetime of > 10 years.
- Components and subsystems must tolerate expected radiation levels of 10 yrs LHC operation ➔ large number of rad-hard ASICs development and extensive rad-hard evaluations on both ASICs and COTS.

ASICs

- SCA
  - the 144 cell analog pipeline used on FEB to provide analog signal storage during L1 latency of up to 2.5 μs (100 bunch crossings).
  - Design and developed in rad-soft technology, and then migrated to rad-hard using the DMILL technology.
  - Production tests: robotic test station to test 50000+ chips.



FEB

Technology	Components
AMS BiCMOS	shaper (32)
DMILL	SCA(32), SMUX, TTCrx, CFGCTRL, SPAC_slave,
DSM (0.25μm)	GainSele(8), QPLL, CLKFO, SCAC(2), DCU2(2)
RHBip 1	VREG (19)

Calib. board

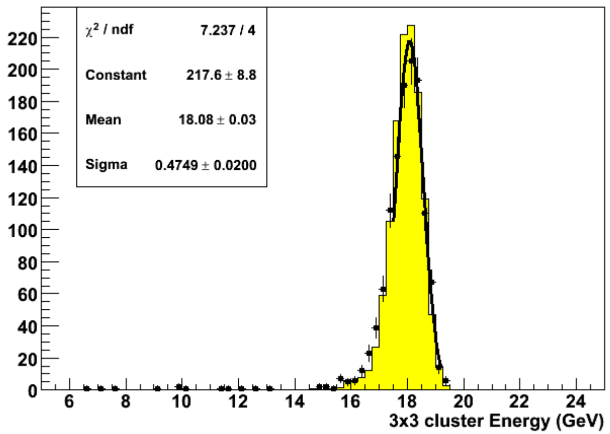
Technology	Components
AMS BiCMOS	HF Switch (128)
DMILL	Opamp (128), DAC, CALogic(6), SPAC_slave, TTCrx, delay(2).
RHBip 1	VREG (5)

Production Close to Completion

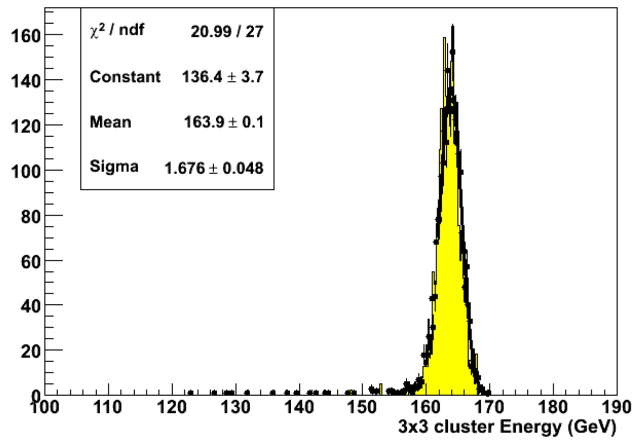
- FEB:
  - 1619 boards delivered with 1611 needed (with spares).
  - Each FEB went through 6 hours Highly-Accelerated-Stress-Screening test to simulate the first few weeks of LHC operation and to weed out "infant mortality".
  - All tests (digital and analog) have been completed at Nevis, BNL and LAL (Orsay).
  - Meet clock jitter < 20 ps requirement for high speed data transmission.
- Calibration board:
  - About 80 boards have been produced, tested and delivered to CERN, enough for the barrel commissioning.
  - The rest boards (~40) are still been worked on in lab and will be delivered to CERN soon.
- Controller board:
  - All 123 boards have been produced, tested. Most of them have been delivered to CERN.
- Tower builder board:
  - All 135 boards have been produced, tested and delivered to CERN.

Beam Test Results

- Beam tests using a real detector module with the production version of the readout electronics have been carried out.
- Preliminary data indicate the electronics system is working up to its design spec:



20 GeV electron



180 GeV electron

Data MC comparison

Installation and Commissioning Status

- EM barrel front-end crates (32) fully equipped except two half crates. Tests are under way and "fast" tests have been successfully carried out.
- Endcap front-end crates start to be equipped and readout.
- Cabling, including optical fibers are in place for the barrel; for the endcaps, we are waiting for the cable chains.
- Cooling (both air and water) and other services are either done or catching up.
- Problems on the LVPS are been closely monitored and worked with the vendor.
- Back-end electronics installation matches well with front-end.
- Long term stability is being checked on a 3 full crates readout configuration and has been running for one month. With more LVPS coming in, this test will be expanded to all equipped crates.

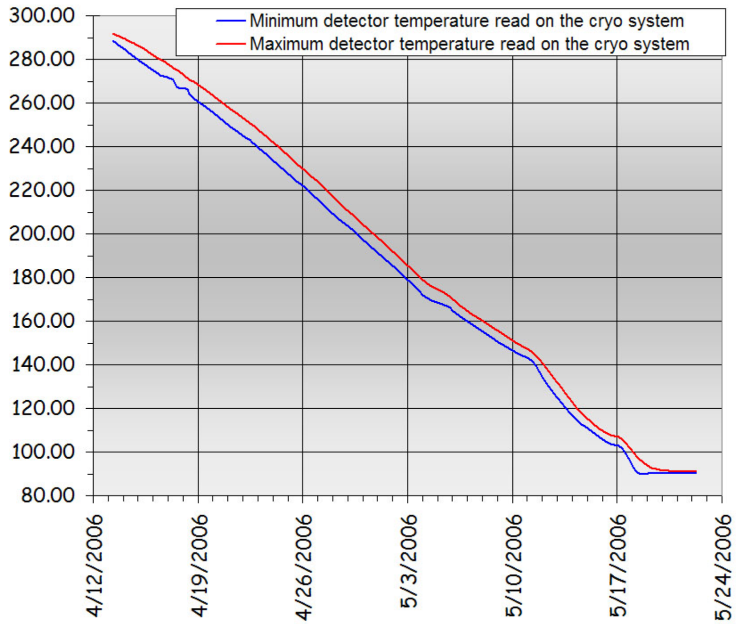
Equipping the front end crates

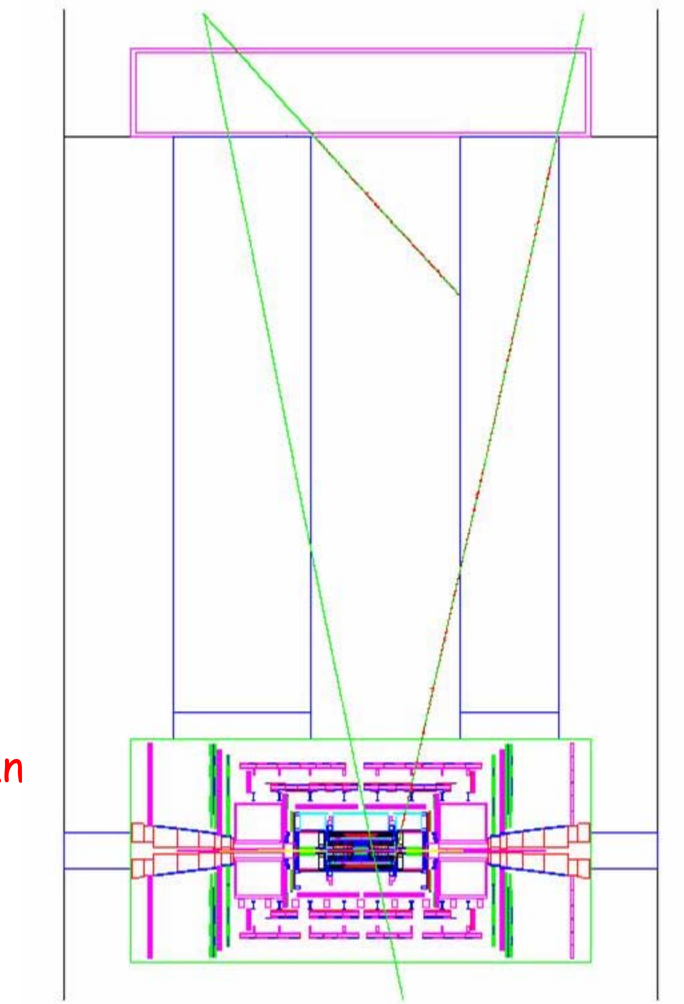
Endcap in place

Racks and crates for ROD system, powered, tested with the Injector. Connection with FEBs in progress.

LAr Commissioning

- Barrel cryostat is cooling down, now cold and filled with LAr, ready to raise HV.





- Cosmic muons run to commission the detector an the readout system.
  - Will start in summer 2006
  - Cosmic muons will be recorded with LAr + Tile.
  - MC and analysis tools are prepared.
  - Results: stay tuned.

Conclusions

- The ATLAS Liquid Argon calorimeter readout electronics system is in its installation and commissioning stage.
- This readout system is designed to fulfill the requirements from physics goals set for the ATLAS experiments.
- In order for the front end electronics to work on the detector, in radiation environment, large number of ASICs have been developed using various rad-hard technologies.
- This system has reached its design goals through tests from past beam tests.
- More results will come soon from the cosmic muon runs this summer. These results will further test the system design goals with the whole system working together.