Development of Readout ASIC for FPCCD Vertex Detector

2011.9.13 Kickoff meeting

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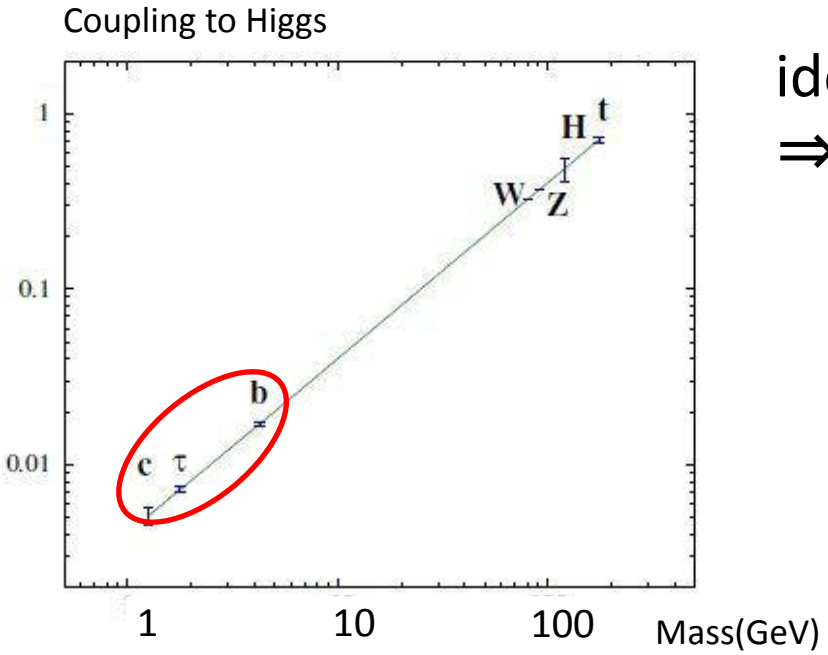
FPCCD vertex detector motivation

Verifying Higgs mechanism



identify b and c quarks

⇒excellent flavor tagging is needed!

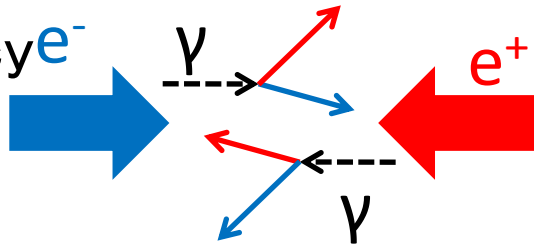
Impact parameter resolution

$$\sigma = 5 \oplus \frac{10}{p\beta \sin^{\frac{3}{2}}\theta} (\mu m)$$

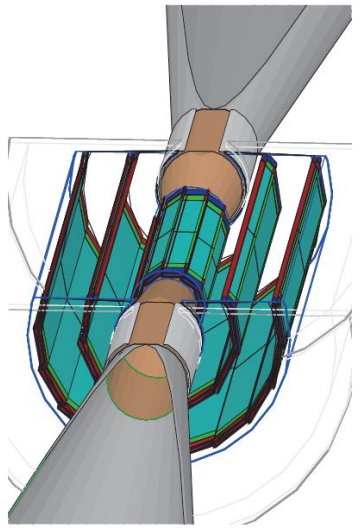
High resolution for vertex detector is needed!!

FPCCD vertex detector

- Pixel occupancy < 1%
  - Pair background increases pixel occupancy

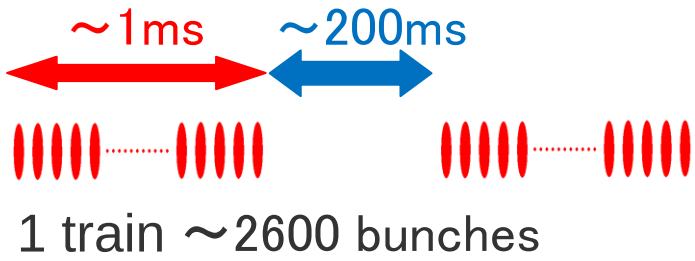


- Small pixel size
- Fine Pixel CCD(FPCCD)
  - Pixel size : **5 ×5 um^2**
  - sensitive thickness: 15 um (Fully depleted)
  - **20,000 × 128 pix/ch**
  - 8ch/ASIC
  - Total #ch ～6,000ch
  - ladder geometry: 3 double-sided layers

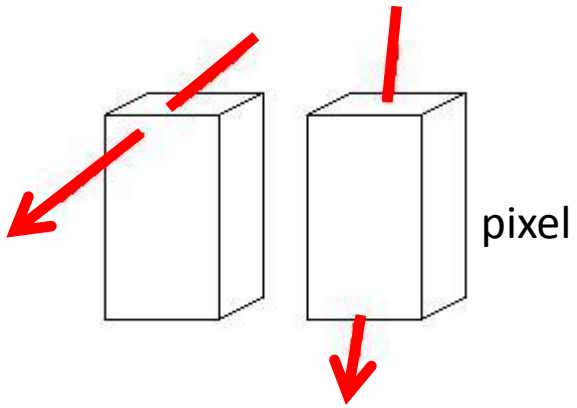


Requirements for readout system

- Readout speed> 10Mpix/sec
  - Readout in inter-train time(200ms)
  - 20,000x128pix/200ms



- Noise level < 30e-
  - Small signal level: ~500e-



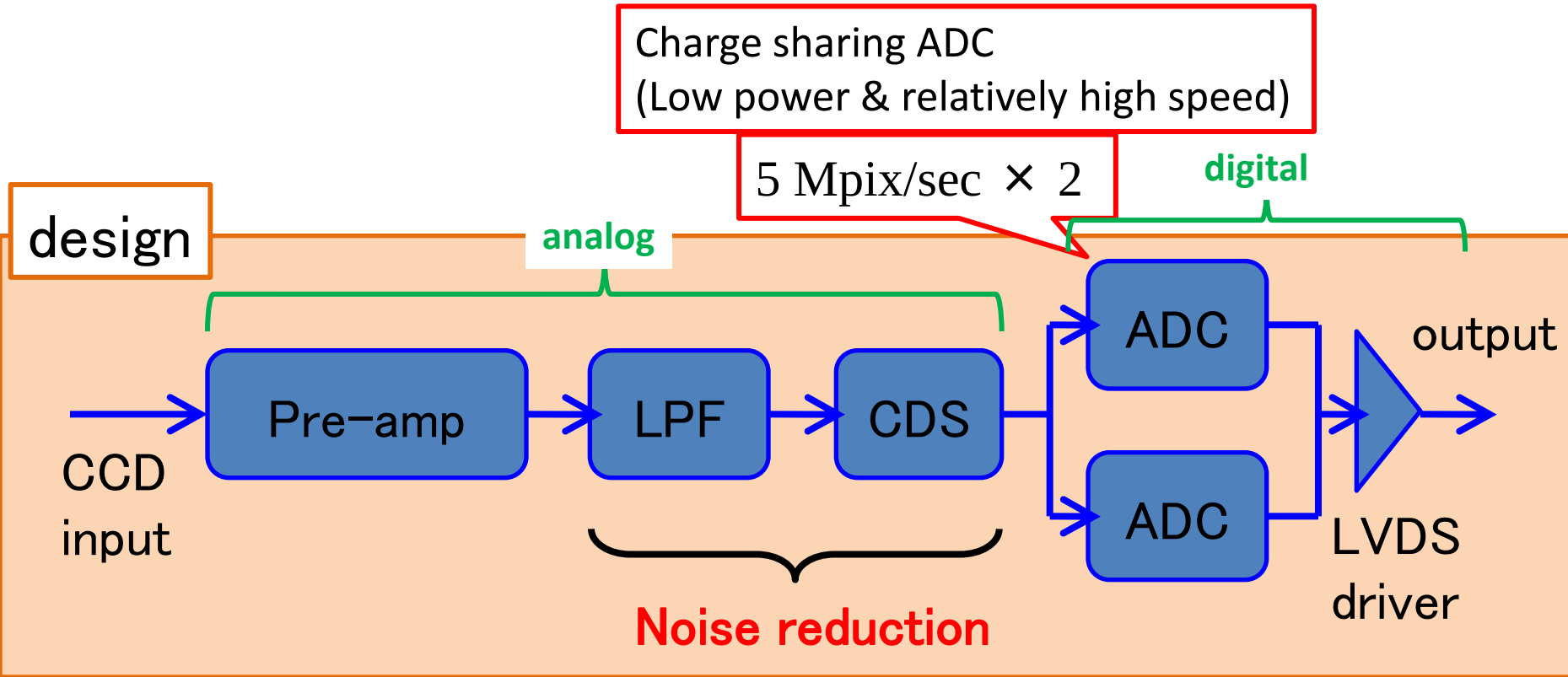
- Power consumption < 6mW/ch
  - Total power consumption<100W

➢ Design readout ASIC to meet these requirements

Design concept of readout ASIC

■ 2nd prototype readout ASIC focus

- Readout speed > 10Mpix/sec
- Noise level < 30e-



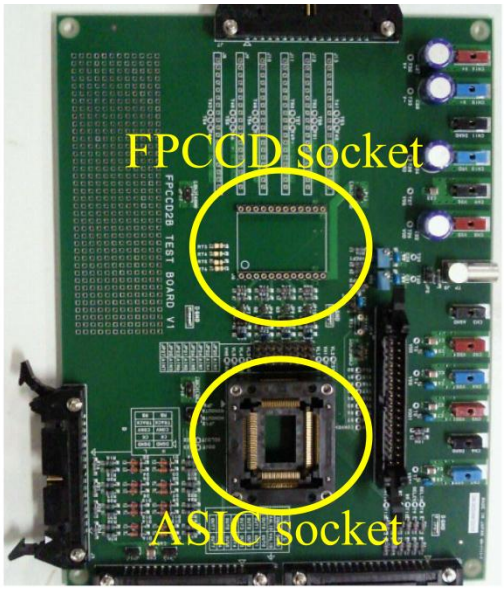
2nd prototype readout ASIC

2nd prototype readout ASIC

- Produced by TSMC
- Process : 0.35mm CMOS
- Number of channel : 8 ch
- Chip area size : 4.3mm × 4.3mm
- Signal 8 bit (10CK/conversion)

2nd prototype ASIC packaged

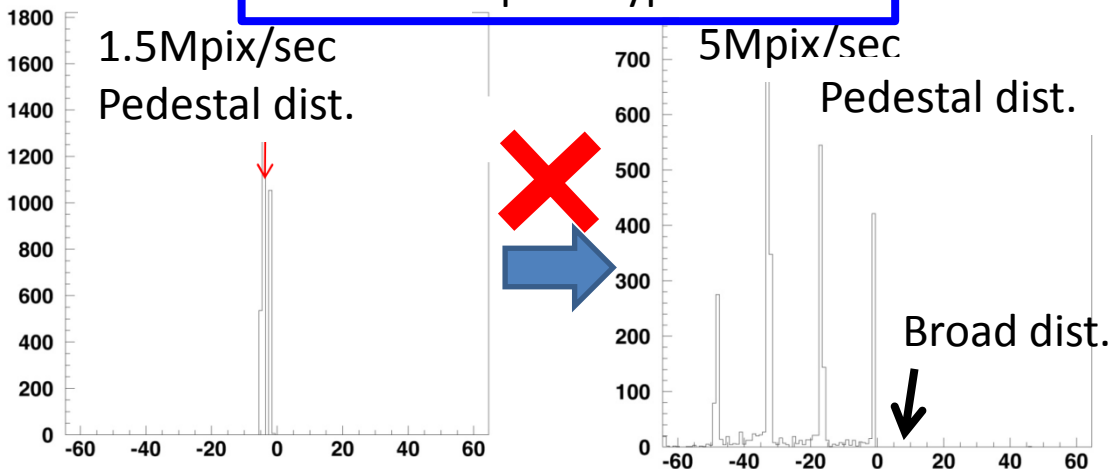
Test board for 2nd prototype



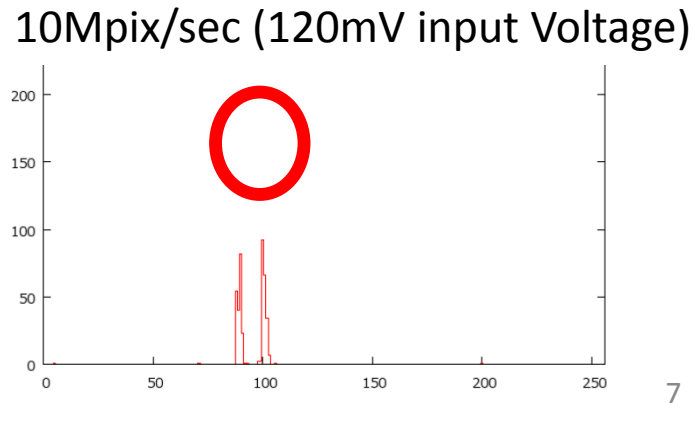
Readout speed

- 1st prototype readout ASIC
- Limited readout speed(1.5Mpix/sec)
  - Shortage of current for comparator. & Stray capacitance
  - ➢ Redesigned ADC, comparator
- 2nd prototype readout ASIC
- Operates under 10Mpix/sec.
  - 2 peaks emerge from the difference of 2 ADCs. (can be corrected in the back end.)

1st prototype

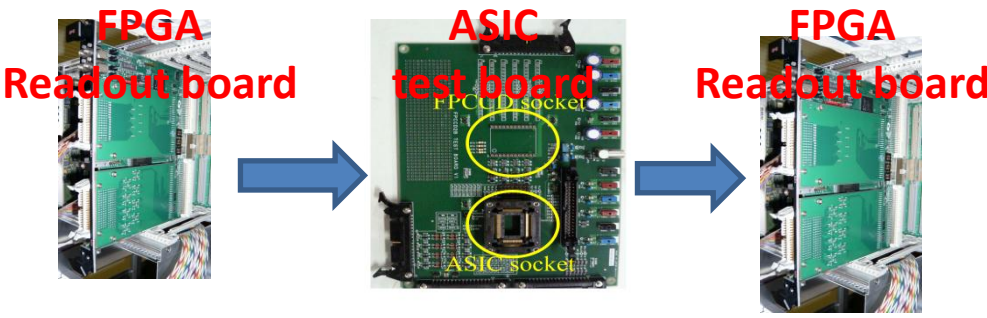


2nd prototype

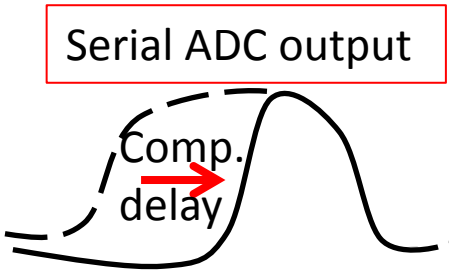


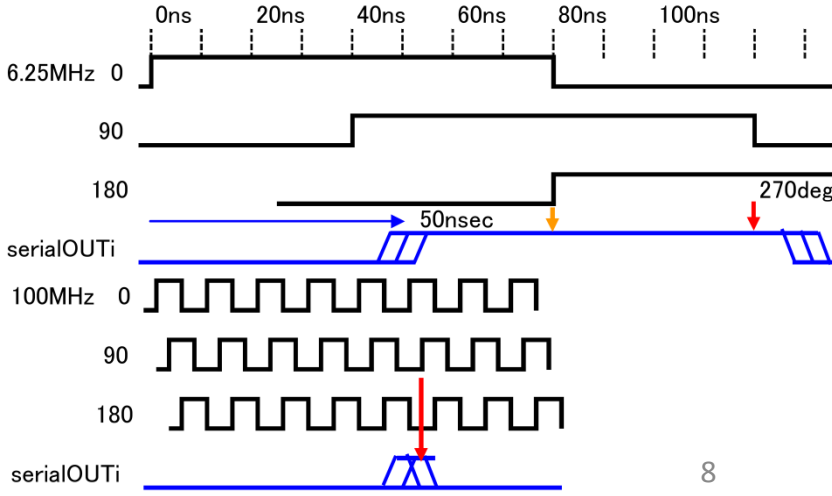
Difficulty of 10Mpix/sec readout

- Delay
- It takes over ~50ns to travel FPGA→ASIC→FPGA
- (~50ns=5CK for 100MHz)



- comparator delay
- ADC Comparator delay causes pulse width to shorten.
- Used effectively 400MHz sampling using 4 phases of 100MHz clock.
- Sampling timing extremely difficult.

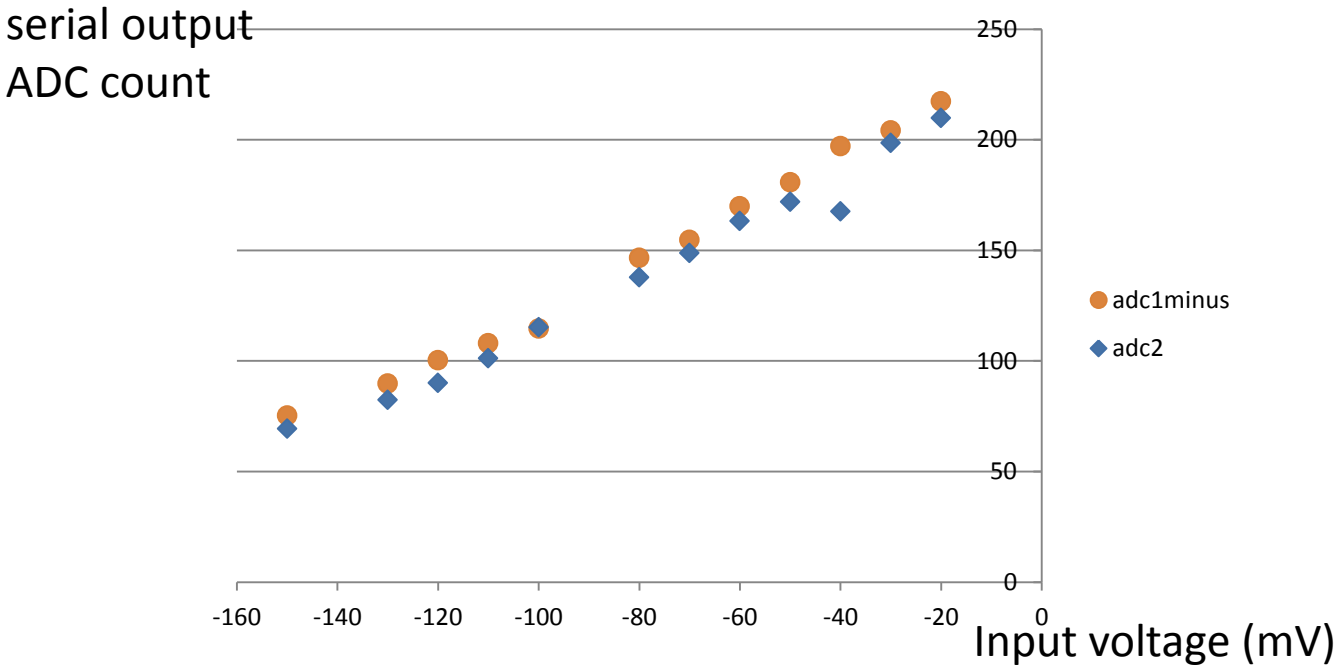




➢ Plan to improve in next prototype.

10Mpix/sec readout linearity

- We were able to see linearity of ADC @ 10Mpix/sec(100MHz CK)
  - Accuracy of linearity will be obtained.
  - ※There are individual differences between ADC1 and ADC2



Power consumption

- Requirement < 6mW/ch
- 2nd prototype readout ASIC: power consumption needs to be reduced to 1/5.
- Digital and analog are in comparable order.
- ➢ For next prototype, meeting power consumption requirement will be one of our major goals.

Measured Power consumption [mW/ch] |V|=1.65(V)

Ibias(uA)	Pss(mW)	Pdd(mW)	Pss1(mW)	Pdd1(mW)	合計
100	5.94	6.52	9.80	8.56	30.8

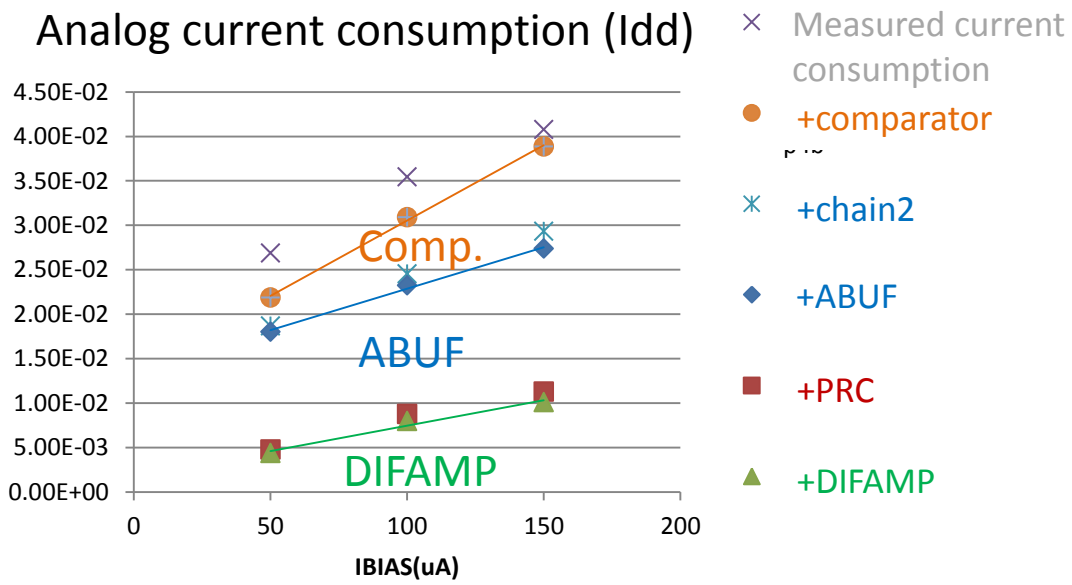
Simulated avg. power consumption [mW/ch] |V|=1.65

Ibias(uA)	Pss(mW)	Pdd(mW)	Pss1(mW)	Pdd1(mW)	合計
100	10.3	9.6	6.8	6.70	33.3

analog digital

Analog current consumption

- IBIAS dependence current consumption
- 10Mpix/sec ,Vdd ,Vss=1.65V
- Most of the current is consumed in ABUF, DIFAMP, comparator.



Design for next ASIC (analog part)

- ABUF(Analog Buffer)
  - Used for monitor circuit and buffer before ADC.
  - ➢ Change design so that we can turn off monitor when not needed.
- DIFAMP(Differential Amplifier)
  - Used in LPF and CDS
  - ➢ Replace with ABUF.

➢ extensive simulation/study will be done in near future.

Design for next ASIC (digital part)

- Measured digital current for 10Mpix/sec
- 48 mA
- simulation
- LVTTLR … low voltage receiver that receives signals in order to set Amp, LPF parameters.
- Will not use after parameter setting
  - Input voltage 0(V): 1 cell 1.3mA
  - Maximum current consumption: 22mA

➢ Change design so DC consumption is minimized. Further simulation/study will be done.

- Change process: 0.35um→0.25um(or 0.18um)

➢ Reduction in dynamic supply current is expected.

summary

- 2nd readout ASIC prototype was made to meet 2 of the 3 requirements for FPCCD readout ASIC.

■ Readout speed

- We were able to acquire 10Mpix/sec data.

➢ sampling is extremely difficult and further effort will be spent so that we can acquire data more easily in the next prototype.

■ Power consumption

- Measured the power consumption of 2nd prototype. Power needs to be reduced to 1/5.
- Changes under consideration:

➢ Analog : turn off/reduce number of ABUF, DIFAMP.

➢ Digital: change so there is no DC current.

➢ change process 0.35um→0.25um(or 0.18um)

backup