TPC Electronics

13/Sep/2011 ILC Tokushin Kickoff MTG

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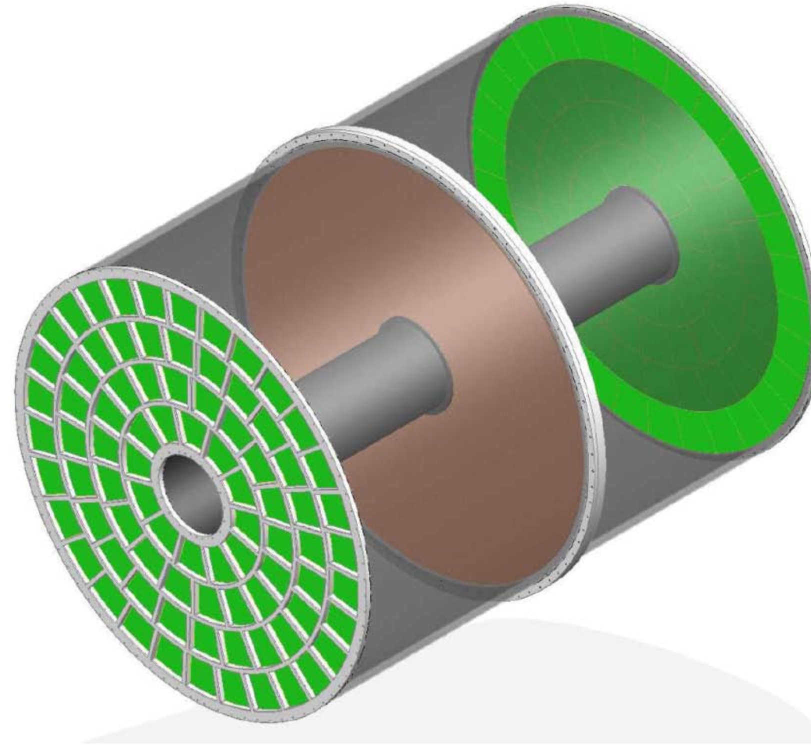
On behalf of the Japanese LCTPC group

TPC Endplate Requirement

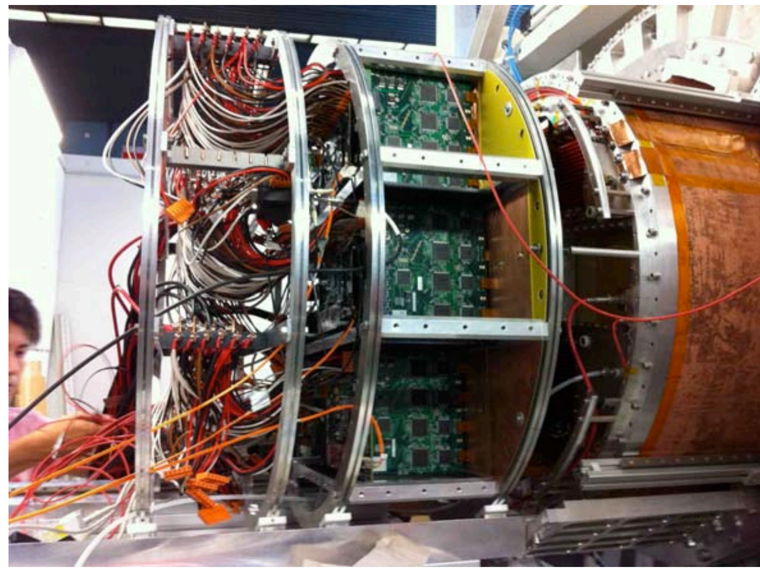


- ILD LOI constraints: TPC readout endplate < 15% X_0 in z.
  -> a recent PFA study shows that it may be relaxed.
  -> we now set the target at 25% X_0.
  -> anyway, “thin” endplate electronics is required.

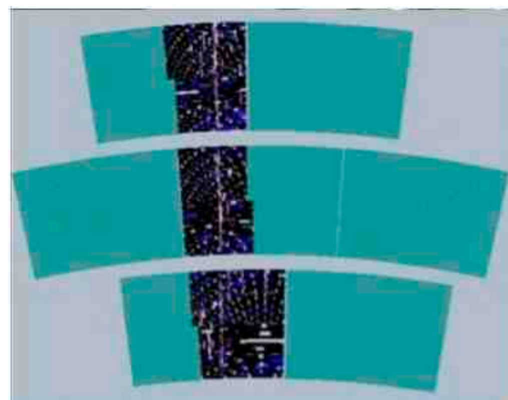
TPC Electronics Generations

Phase 2 (consolidation) Large Prototype

Readout cards perpendicular to the pad plane.
4PCA + 4ALTRO chips/Bd.

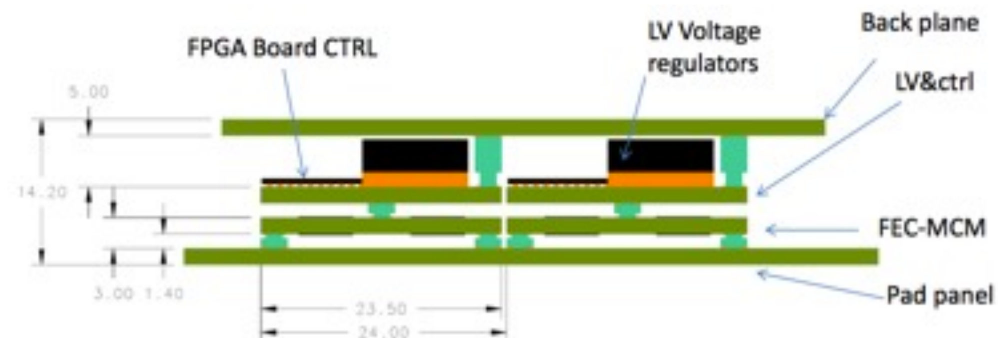


For GEM/MicroMEGAS pad readout

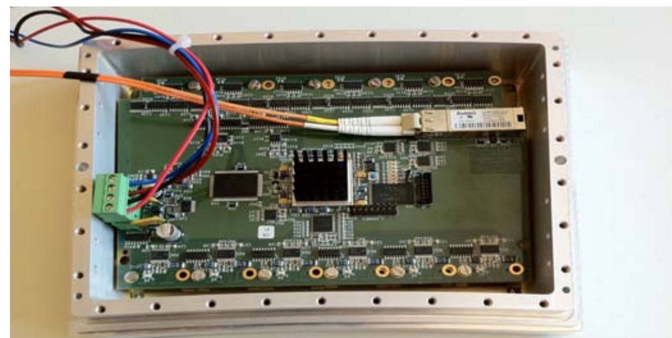


Semi-Advanced Endplate

Multi-PCB flat endplate.



S-ALTRO16 (demonstrator)
for GEM/MicoroMEGAS pad readout



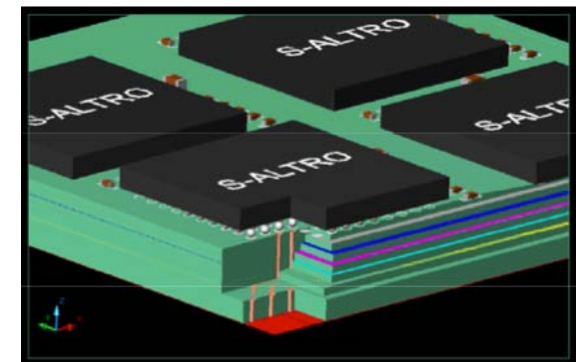
AFTER (T2K) electronics
for MicroMEGAS pad readout

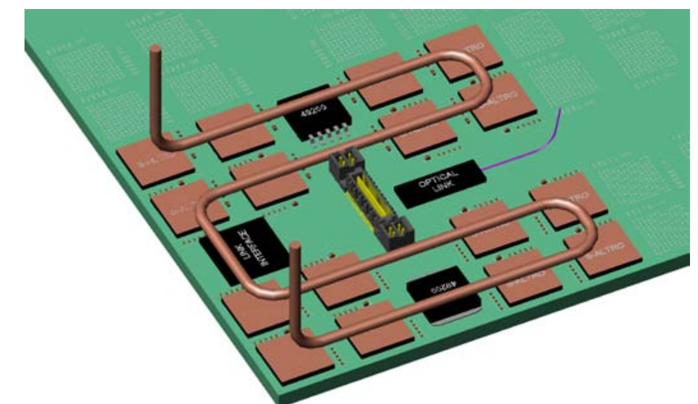
TimePix (pixel readout)

Phase 3 (design) Advanced Endplate

Final target:
thin endplate with single-PCB

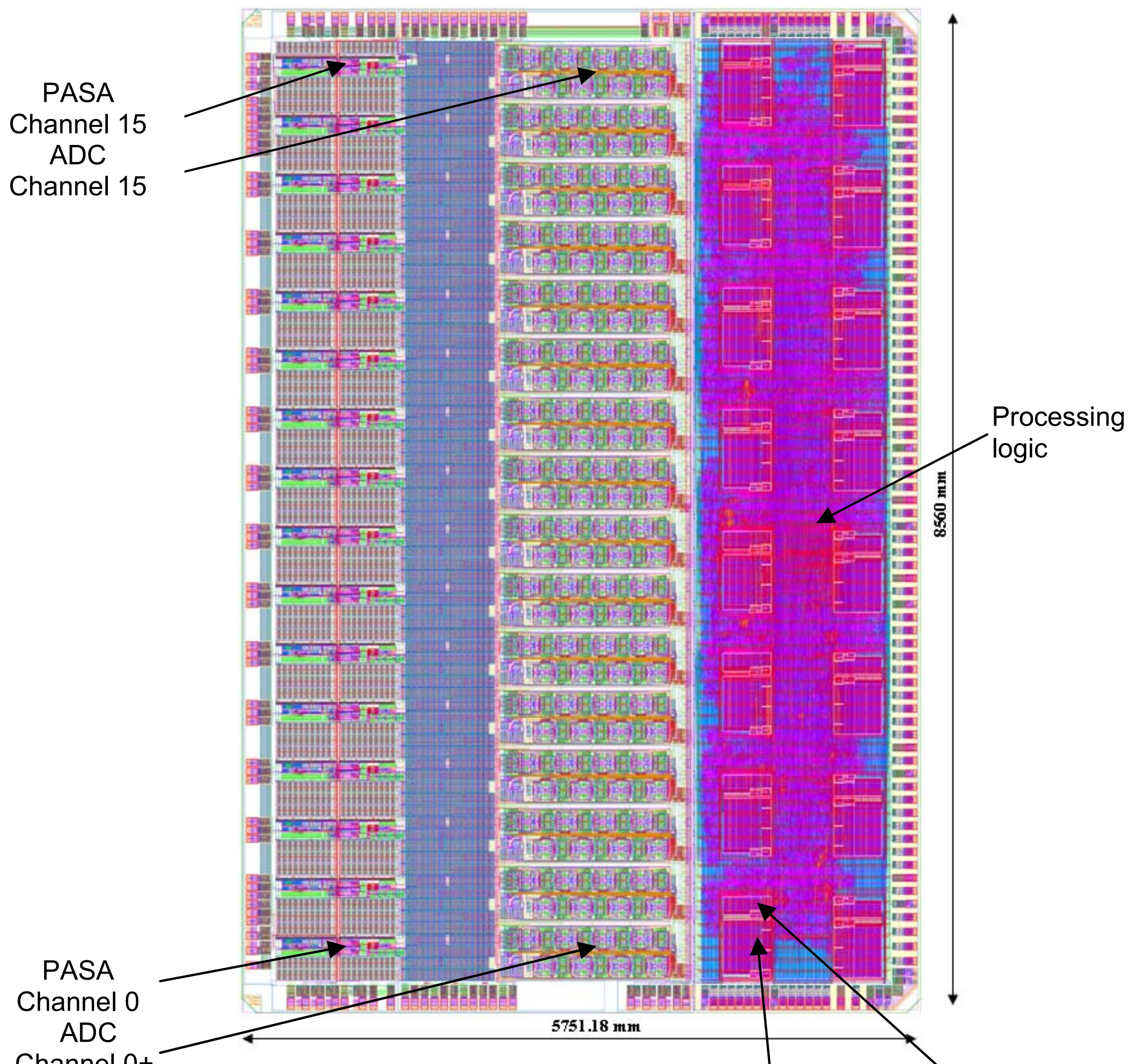
Candidate: S-ALTRO64
for pad reading

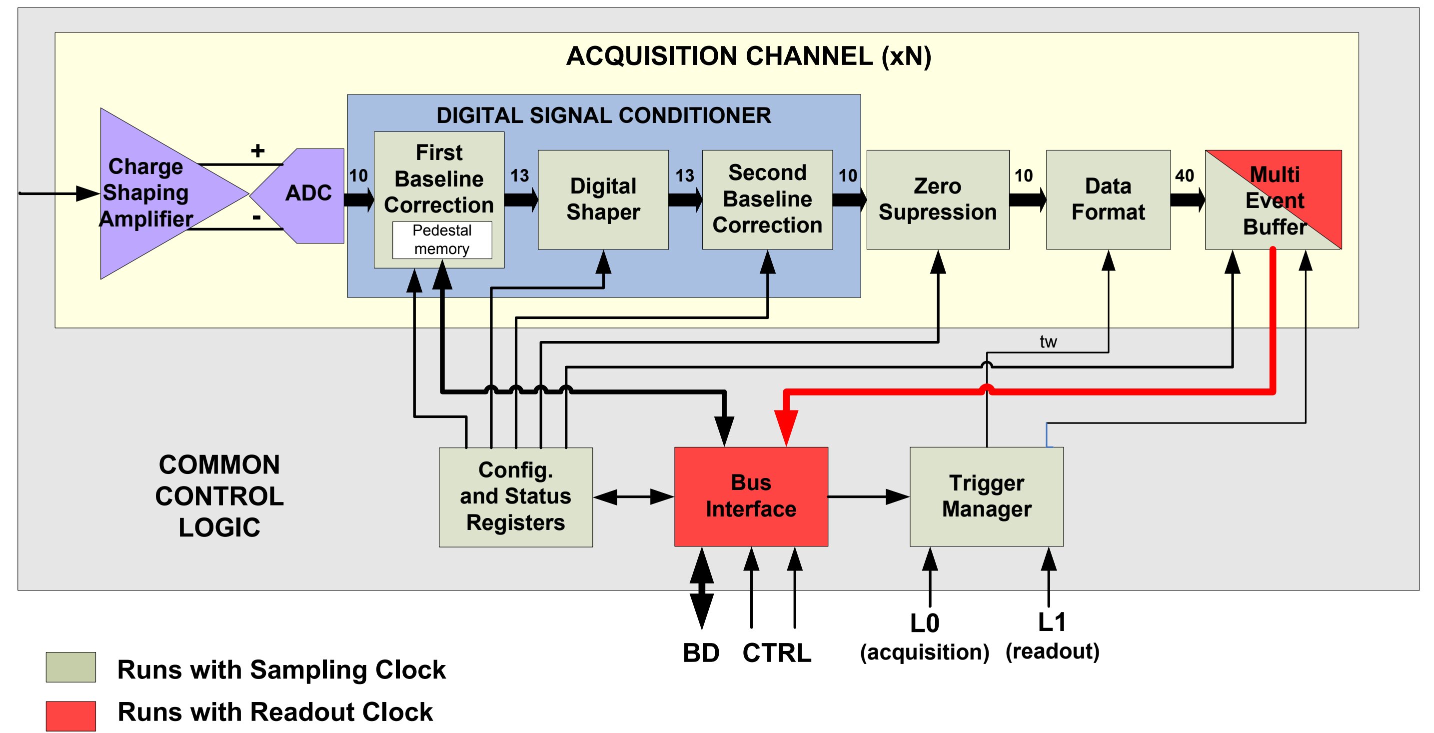




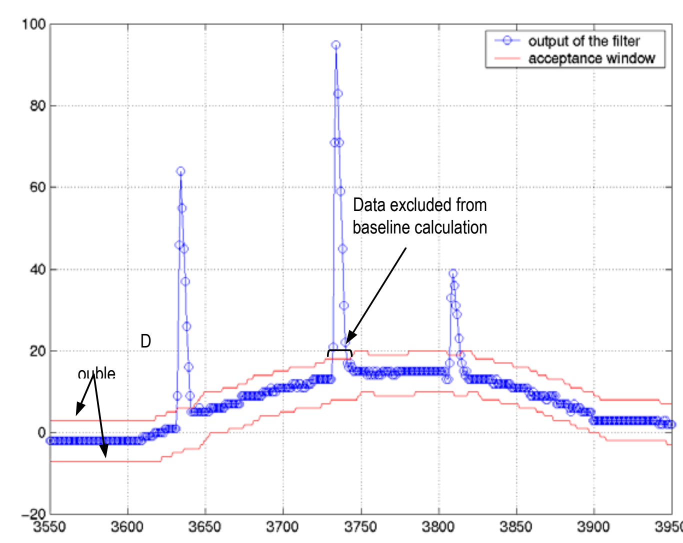
Candidate: TimePix
for pixel reading

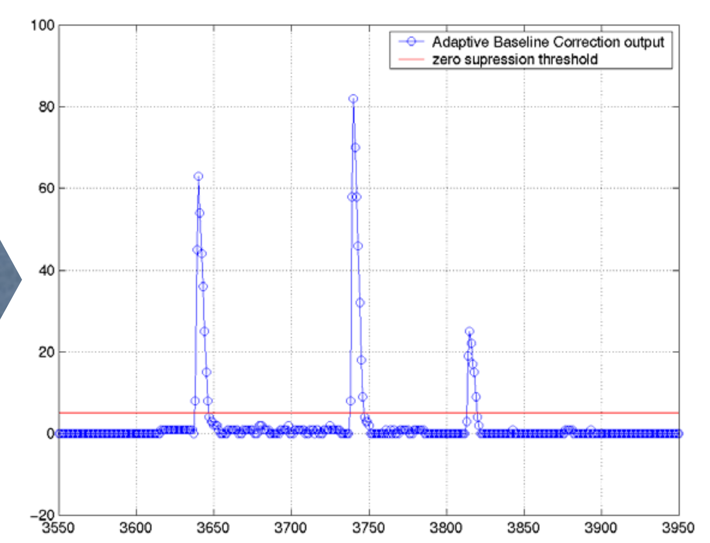
16ch S-ALTRO Demonstrator (CERN)





Wire bonding package
24mm x 24mm x 1.4mm





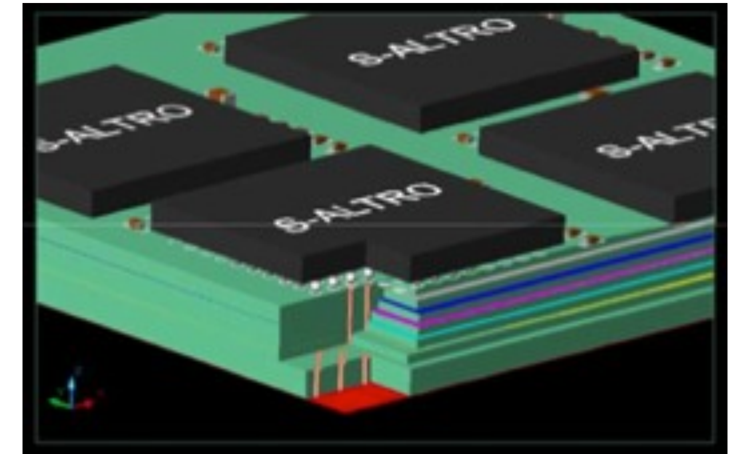
Example of baseline correction

- Fabricated May/2011.
- Characterization ongoing.

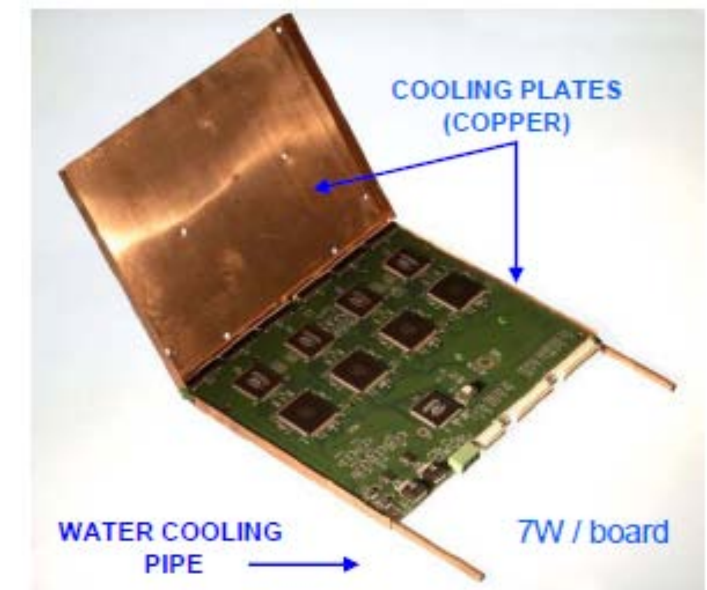
Reference:
“S-ALTRO prototype” 27.07.2010

Power Consumption of S-ALTRO and TPC Advanced Endplate

- At 10 (20) [40] Ms/s operation,
  - PASA (PreAmp&ShapeAmp) : 8 (8) [8] mW /ch
  - ADC : 20 (26)[34] mW/ch
  - Digital Processor : 2 (4) [8] mW/ch
  - Digital Links : 2 (4) [8] mW/ch
  - Power Regulators and Aux. : 11 (14)[20] mW/ch
- In total, one channel consumes : 43 (56)[79] mW/ch
- When the pad pitch is 1mm x 4mm, power density will be : 11 (14) [20] kW/m^2
- With power pulsing of 1.5% duty cycle : 160 (210)[300] W/m^2
- This number is comparable with ALICE TPC frontend. Difference: LCTPC endplate material budget <25% X_0, and we need different cooling mechanism -> CO_2 cooling.
- Half Cylinder of ILD TPC with inner Φ=0.65m and outer Φ=3.6m : 1.5 (2.1) [3.0] kW of which 88 (81) [72] % is analog.



↑ LCTPC AEP / ALICE TPC ↓

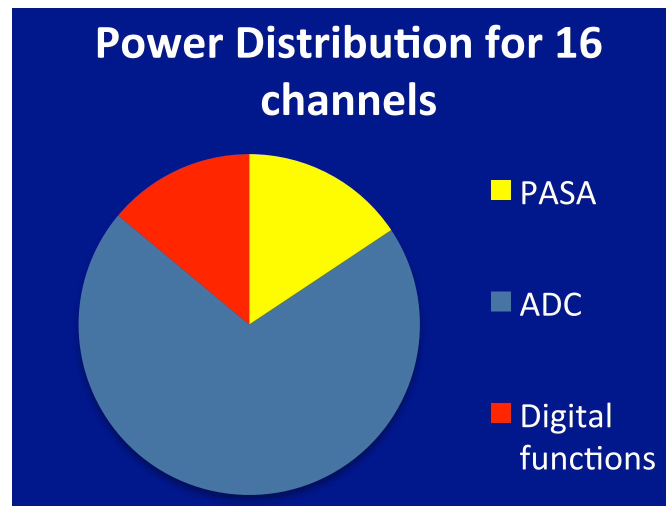


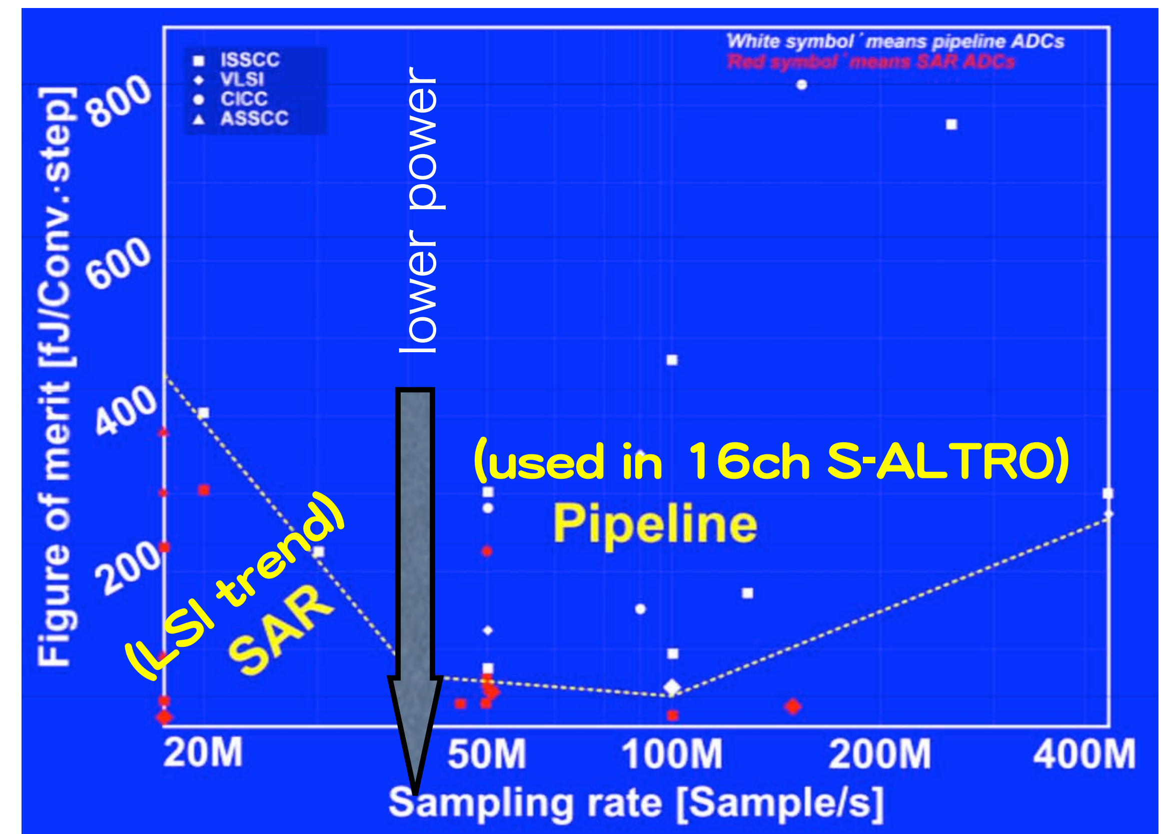
ALICE TPC Electronics
- PC board ~150µm Cu (0.1 X_0)
- 22mW / cm^2 ➡ 220W / m^2
- 0.3mm copper plate (0.2 X_0)

Future S-ALTRO idea

(Essentially, only after evaluation of 16ch S-ALTRO demonstrator, we can discuss final S-ALTRO design.)

- Optimization of pipelined-ADC or replacing it with different architecture (SAR ADC).
  Challenge: 4mW/ch @ 40Msps





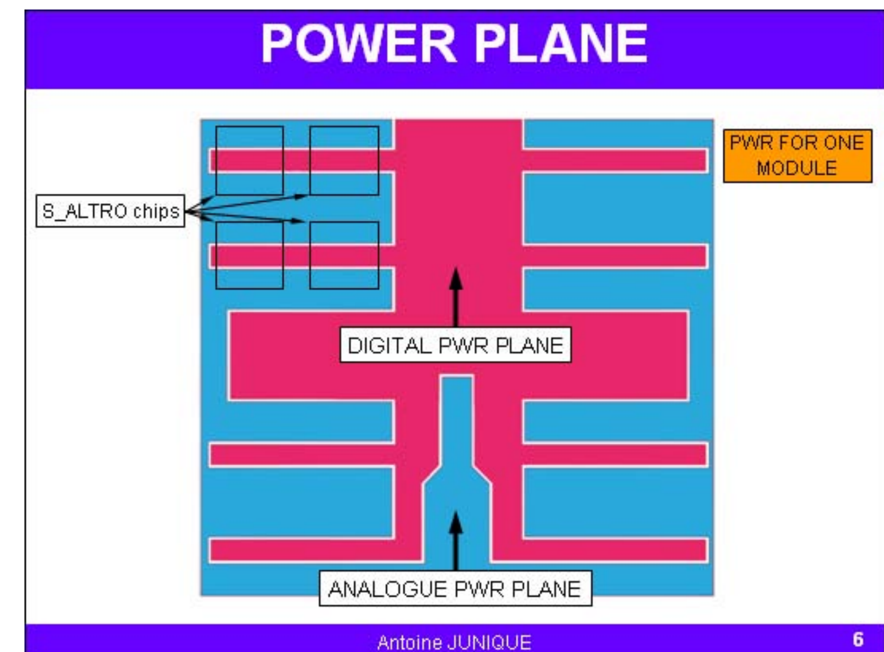
- Tuning of Front-end circuit power.
- Even with these power reduction, power pulsing is still necessary.
  Power management with multiple power domains for power pulsing:
  - Analog: Reduce current via bias control.
  - ADC: Stop clock and reduce current.
  - Digital: Reduce Vdd to minimum or 0V.

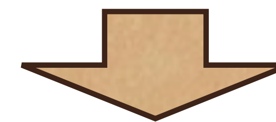
Advanced Endplate Test Board

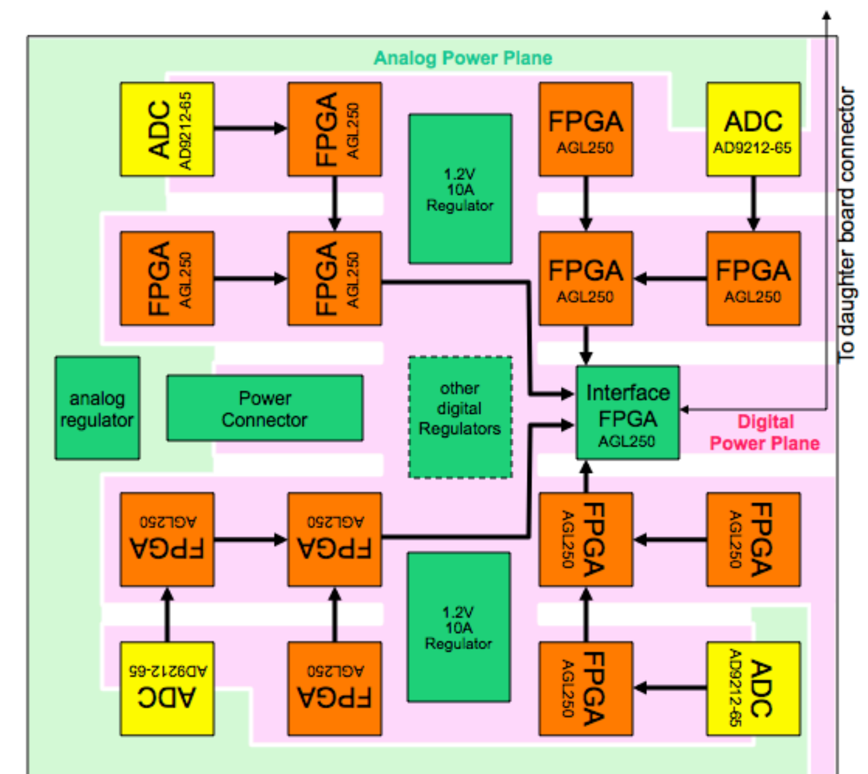
We have constructed Advanced-Endplate “test boards” to test:

- Liquid CO_2 cooling
  - Temperature of ASICs and pads.
- Power pulsing condition
  - Power line stability
  - Noise effect to analog signals
  - PP in strong magnetic field
- Fabricationability
  - Many SMT devices on a PCB

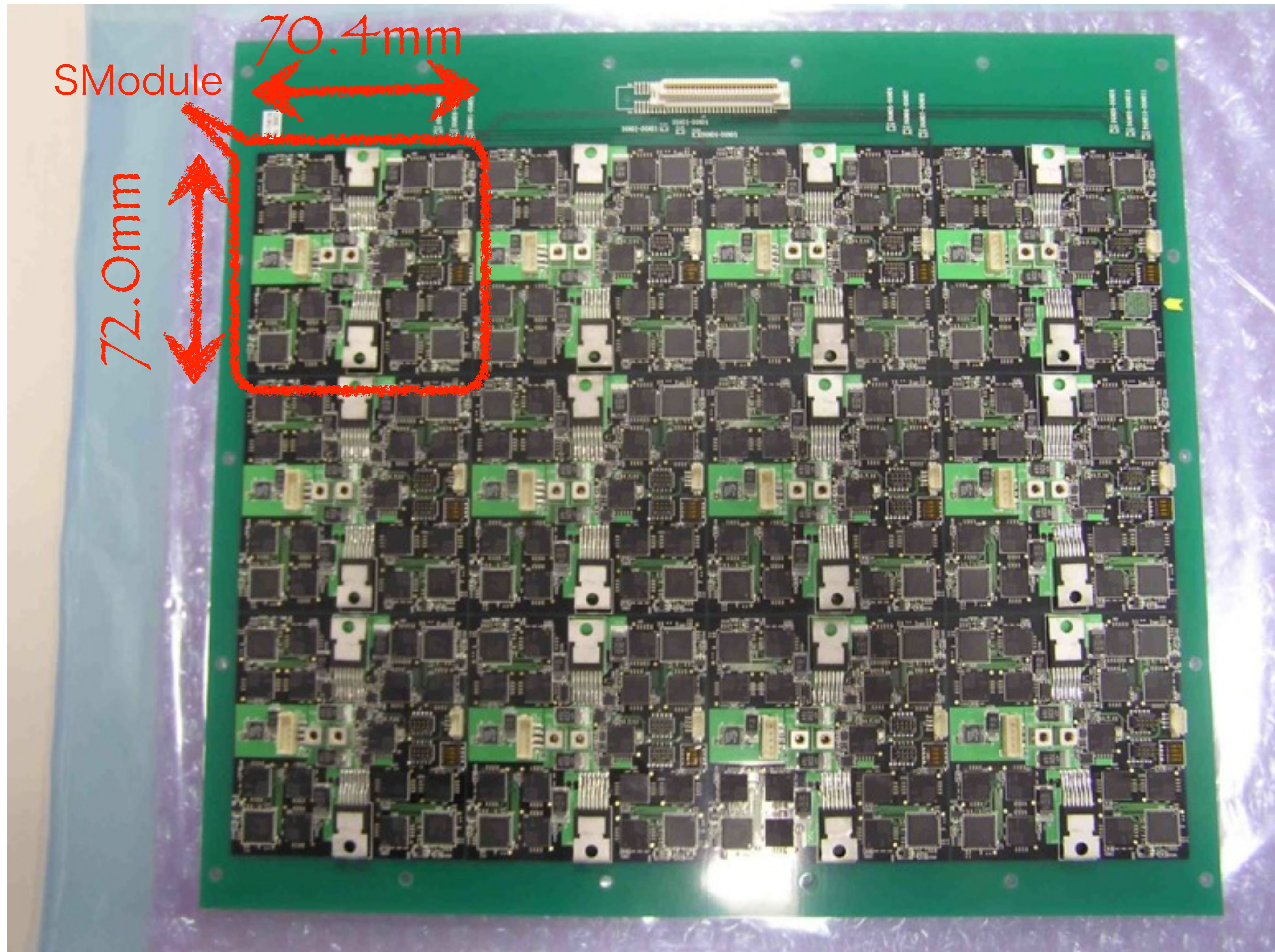
For these studies, surface-mounted FPGAs and ADCs are mounted instead of the future S-ALTRO.



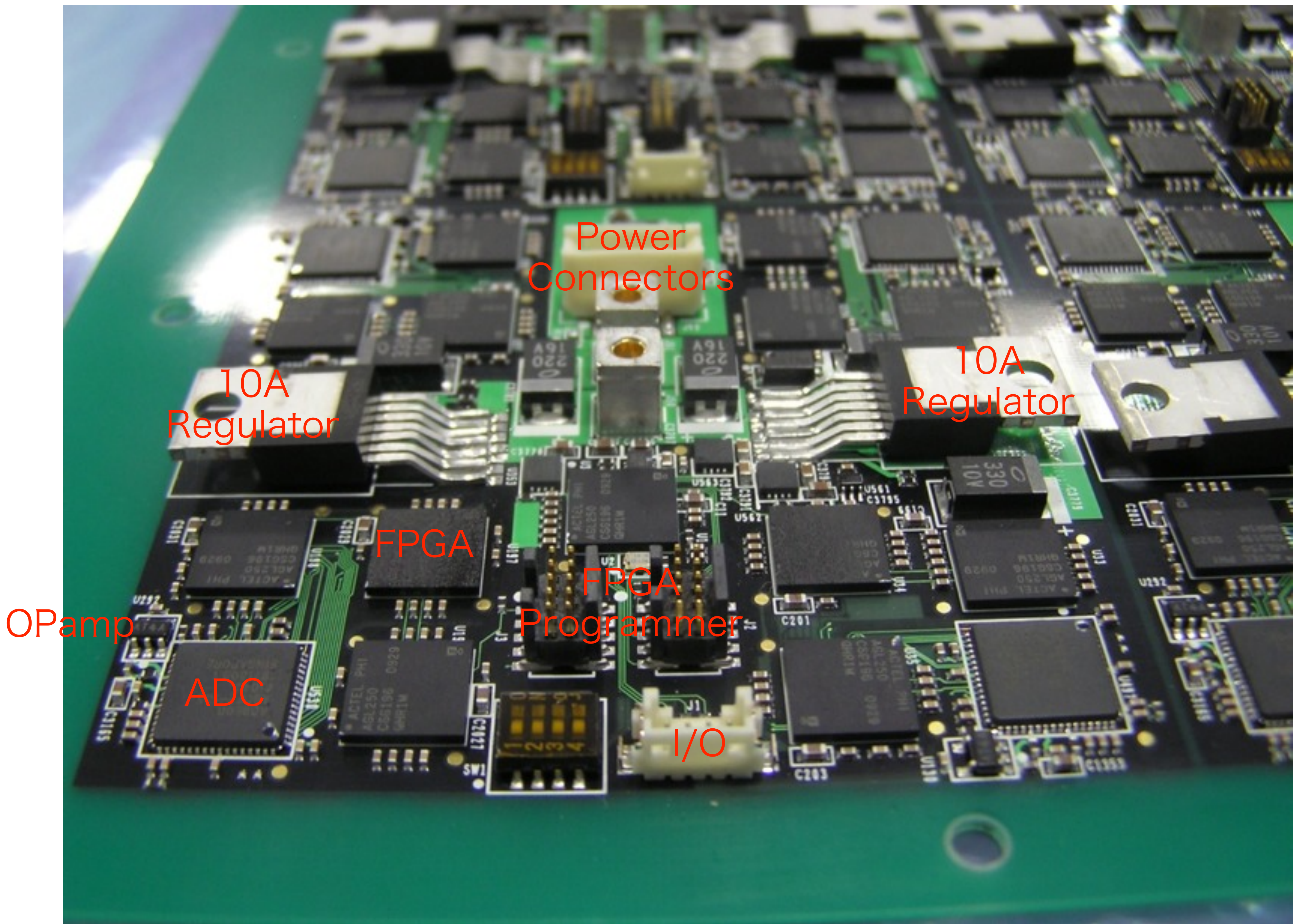




Advanced Endplate Test Board (parts-side view)

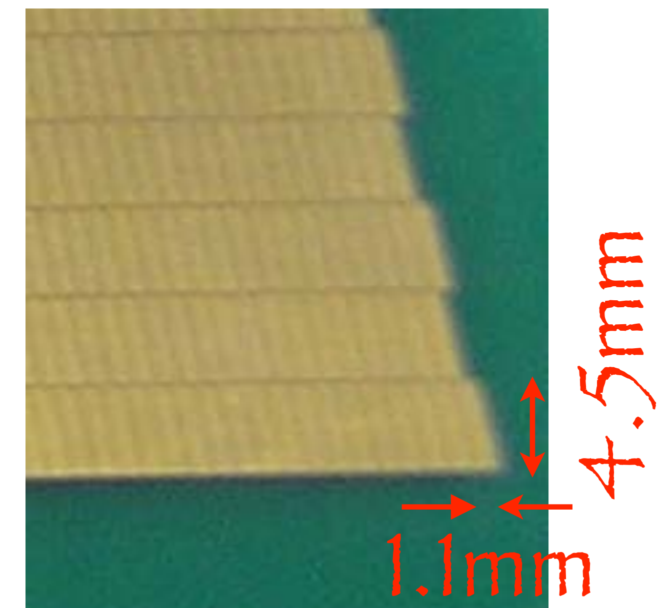


Advanced Endplate Test Board (SModule Zoom-up)



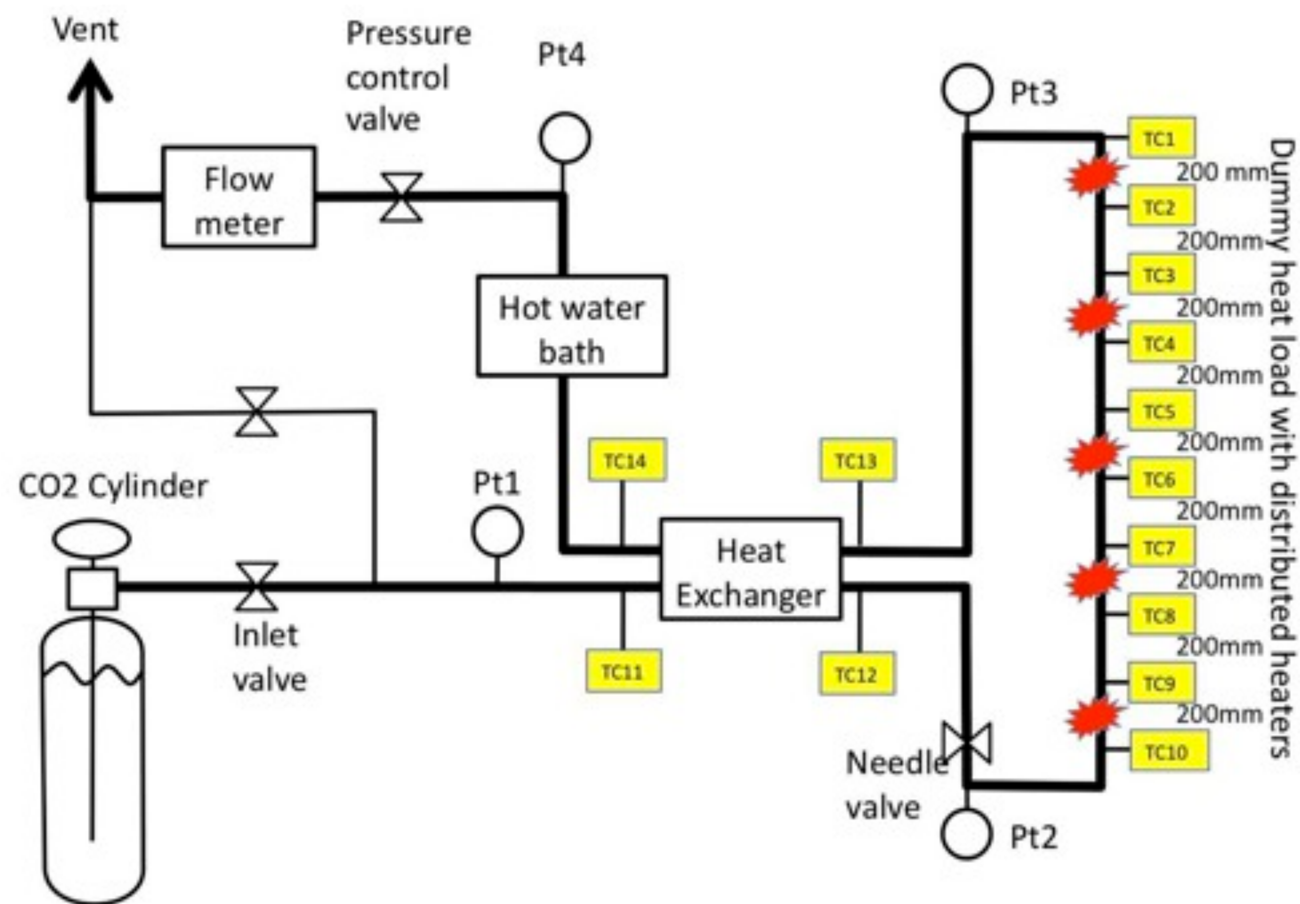
Advanced Endplate Test Board (Pad side)

Pads are prepared on the AEP test board and connected to FPGA pins in order to observe temperature change of pads, which can affect gas volume temperature.
Some pads are connected to ADC inputs via charge amps (OPamps), with which we aim to observe power-pulsing effect to analog circuits.



2P CO_2 blow cooling test bench

Blow system of 2 phase CO2 cooling was setup at KEK by the CO_2 cooling research group.
The AEP TB test with the system will be performed in FY2011.

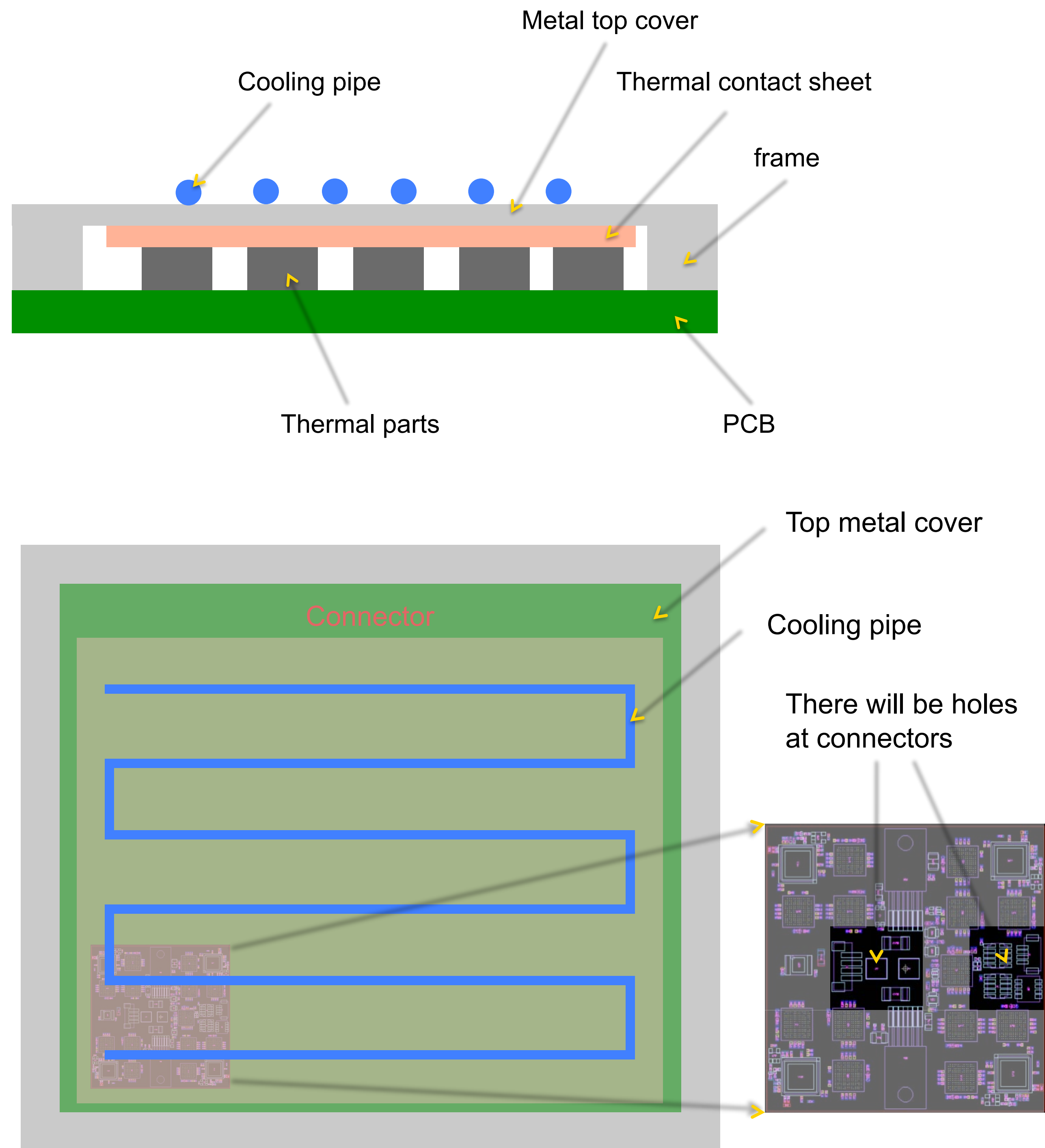


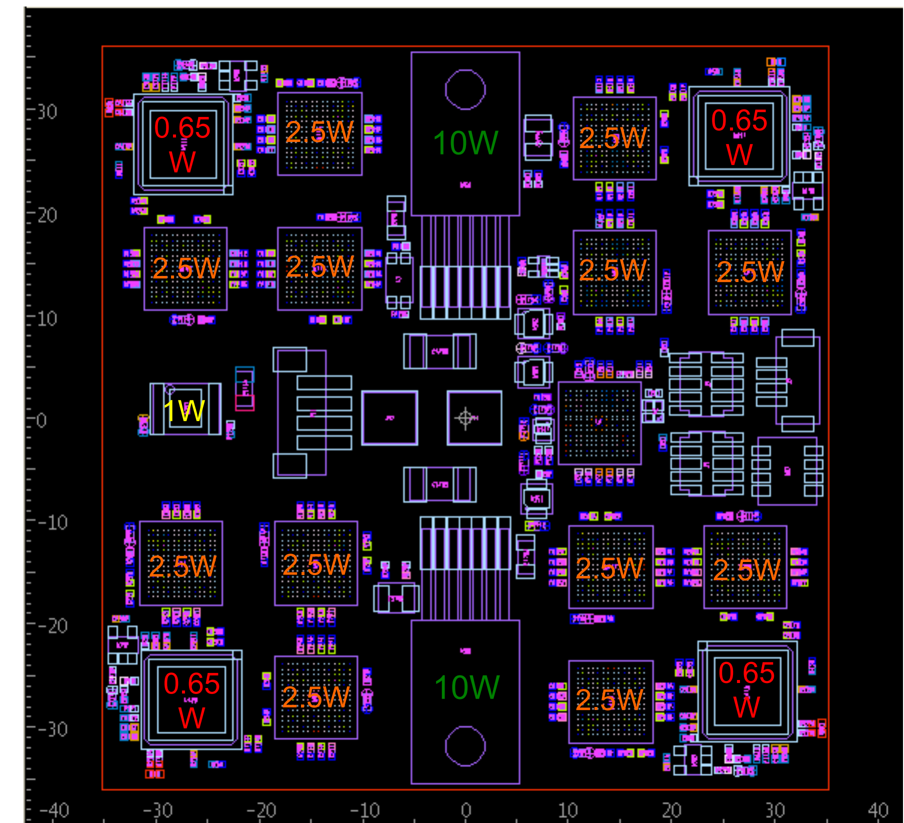
In the blow system,
CO_2 pressure defines temperature.
(+15 ～ -40℃)

First CO_2 cooling system constructed in KEK

First setup of TB for CO_2 blow system

With simple cooling device attached on top side,
temperature data will be taken under CO_2 cooling condition.

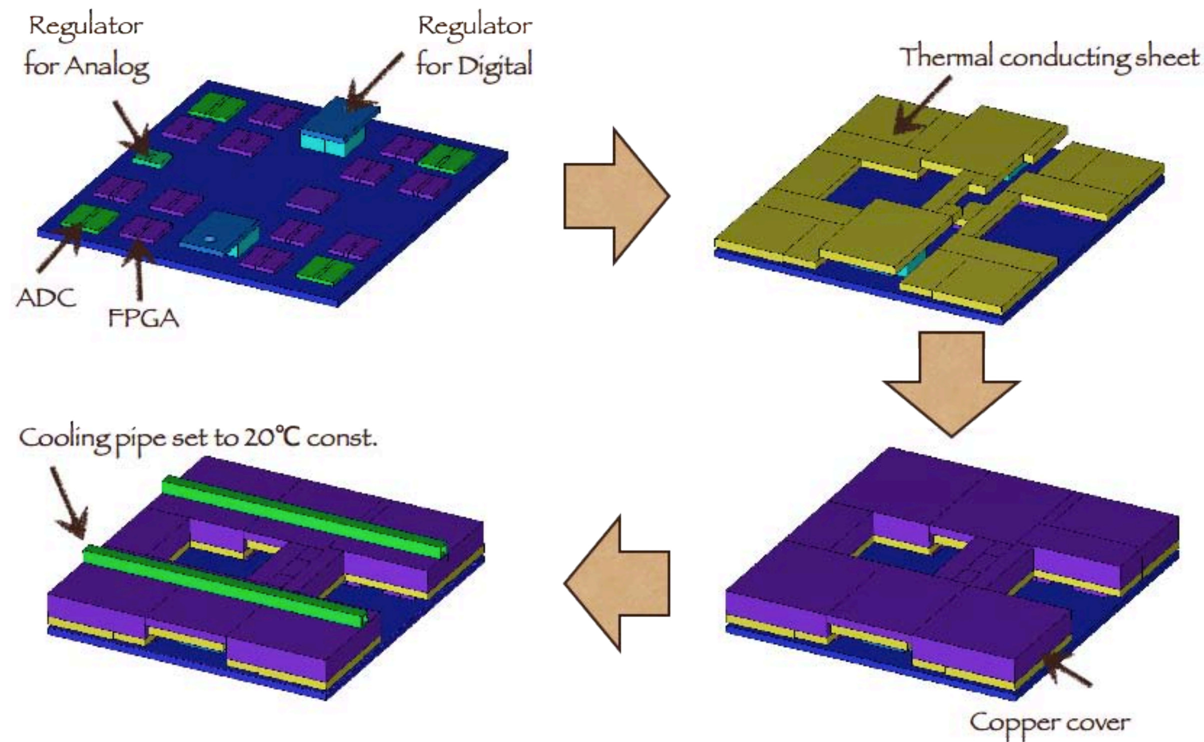




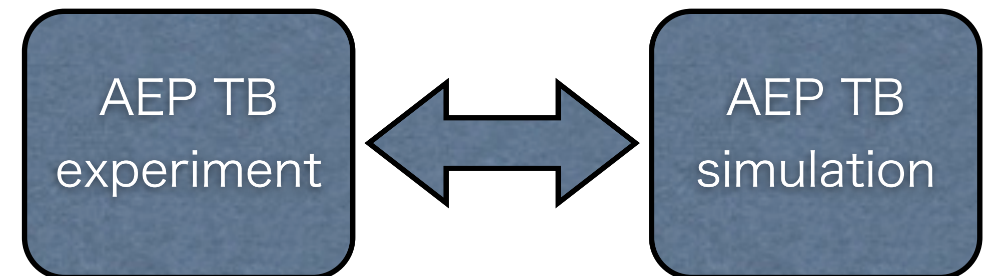
SModule power consumption
when w/o power pulsing

※ Calculation shows
1mm diameter is enough
for R.T. CO_2 cooling pipe

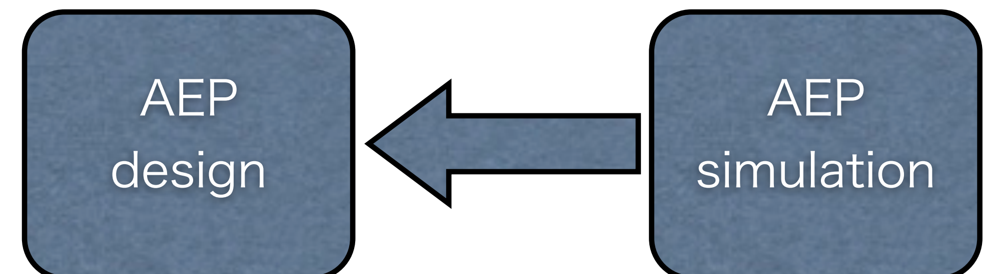
Simulation study of AEP test board



Simulation tasks:
- Include precise PCB model.
  The whole PCB data is too large to be processed by a heat simulator.
  --> trying simplification technique.
- The simulation shown here is “static”.
  --> go transient simulation.
  (heat capacity information is needed)



establish heat simulation method



Ideal shape of AEP cooling

AEP TB layer structure

Layer	structure	material (μm)	plate (μm)	grade	比誘電率	誘電正接	残銅率 (%)	finish (μm)
	SR	30		SR	3.7	0.02		30
Lay1		5	15					20
		pp60*1		FR5	4.3	0.022		70
Lay2		18	15					35
		core100		FR5	4.3	0.022		100
Lay3		35						32
		pp150*1		FR5	4.3	0.022		160
Lay4		35						32
		core100		FR5	4.3	0.022		100
Lay5		35						32
		pp150*1		FR5	4.3	0.022		160
Lay6		35						32
		core100		FR5	4.3	0.022		100
Lay7		35						32
		pp150*1		FR5	4.3	0.022		160
Lay8		35						32
		core100		FR5	4.3	0.022		100
Lay9		18	15					35
		pp60*1		FR5	4.3	0.022		70
Lay10		5	15					20
	SR	30		SR	3.7	0.02		30

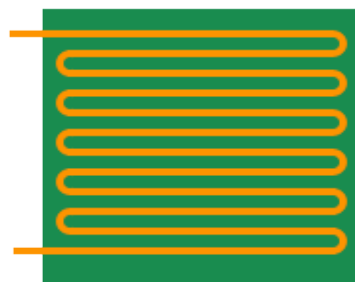
put cooling device in between PCB layers to block heat diffusion from electronics to gas volume

pad layer

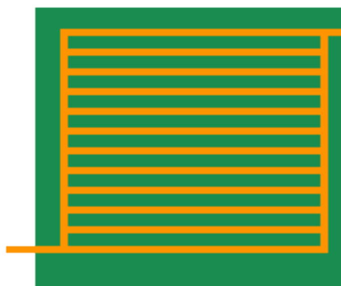
Channels are created by etching, then two Cu plates are bonded. Good thermal contact, but possible only up to 5 atm according to a company.

Channels are created by pipes, then sandwitched by two Cu plates. Good thermal contact, endurable to high pressure, but thick material.

Channels are created by pipes, then put in between PCB layers. Thin, endurable to high pressure, but how is thermal contact?



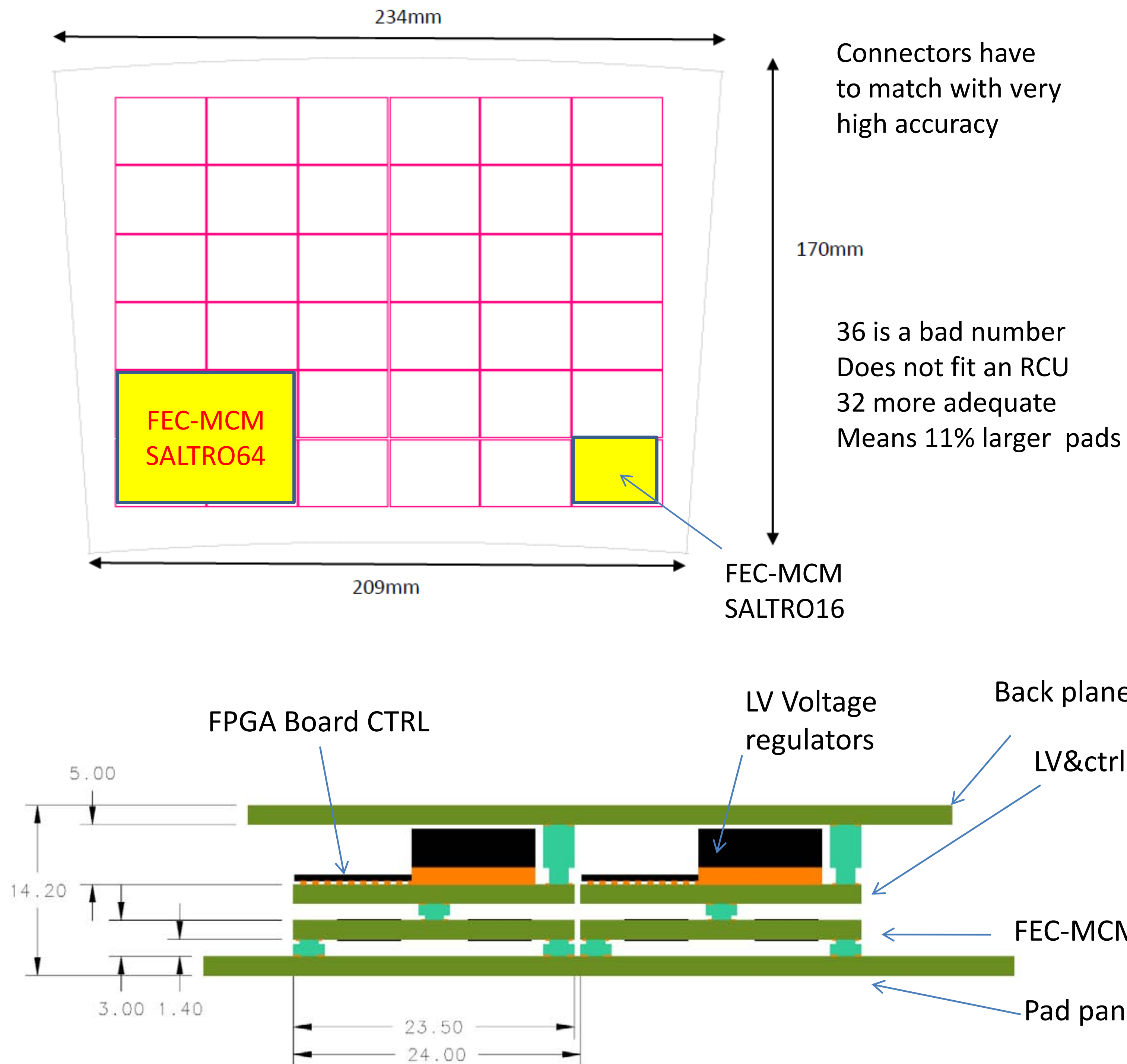
Thin and long piping → dry out!



How to branch?

looking for good industrial choice > 50atm

Daughter-board option for TPC readout
(Semi-AEP idea by Lund group)

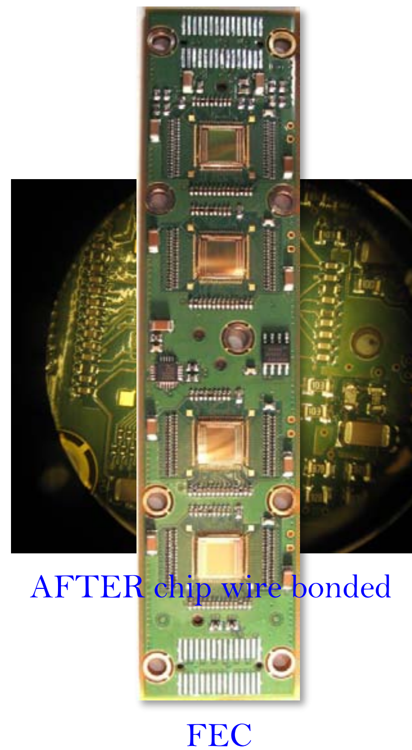


Good:
- Close to present solution.
- Shorter development,
- Lower risk,
- can keep RCU mostly as it is

Bad :
- difficult to mount the bricolage of cards.
- Many connectors
- Difficult access for cooling,
- geometry fixed by backplane
- Need many bus drivers (GTLs)
- Slowed down by noisy FEC-MCM

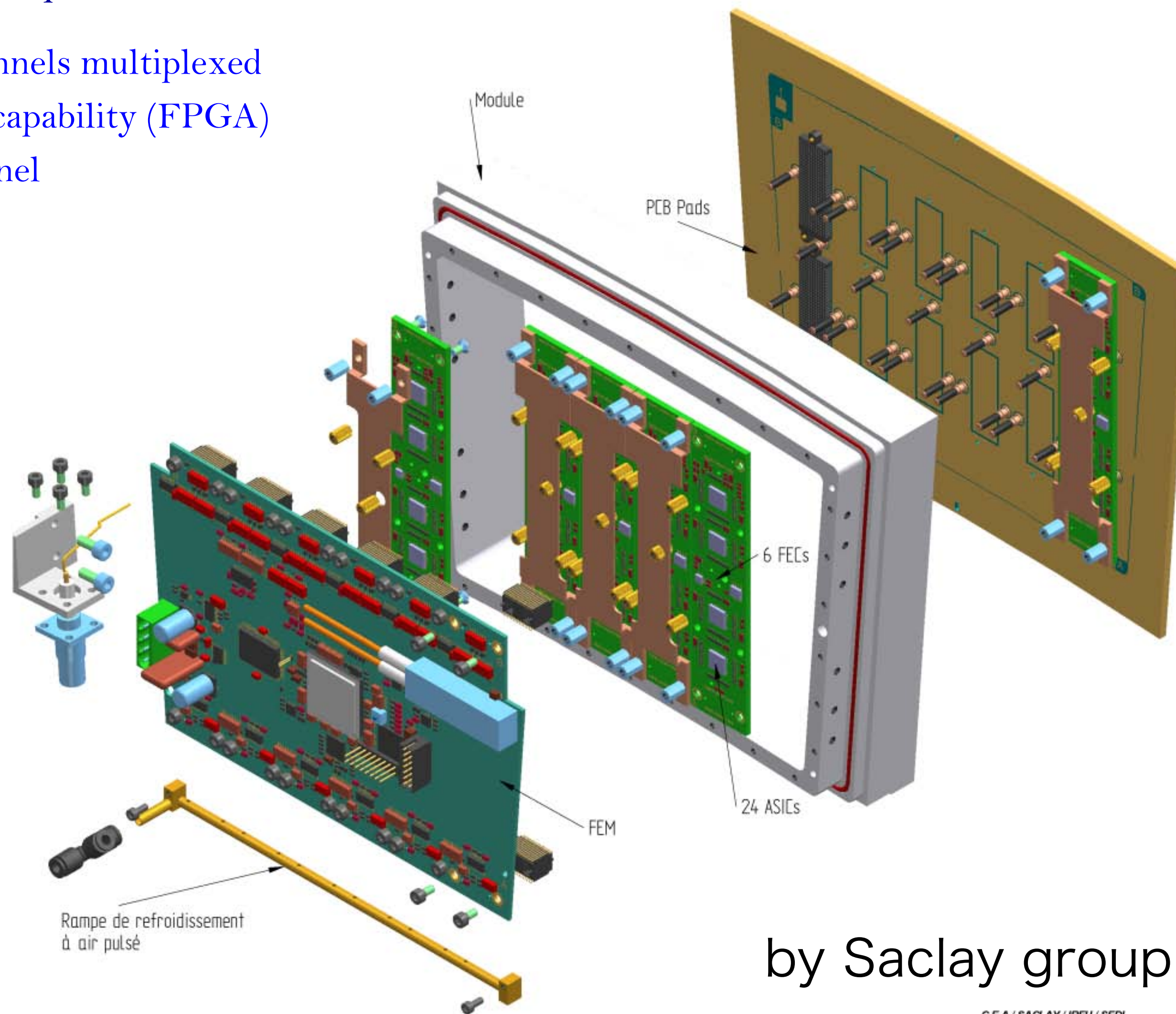
AFTER-based electronics

- 1 FEM, 6 FECs, 24 chips :1728 ch
  - 12-bit ADC, 6 channels multiplexed
  - Zero Suppression capability (FPGA)
  - ~14-25 mW/channel

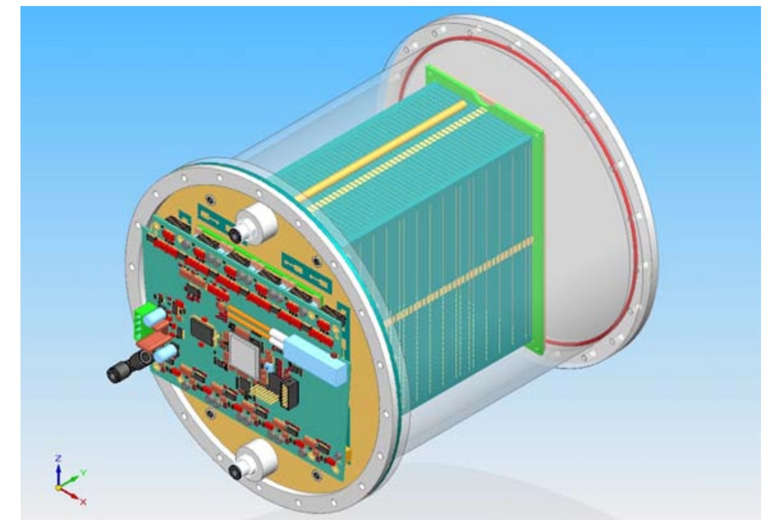


AFTER chip wire bonded

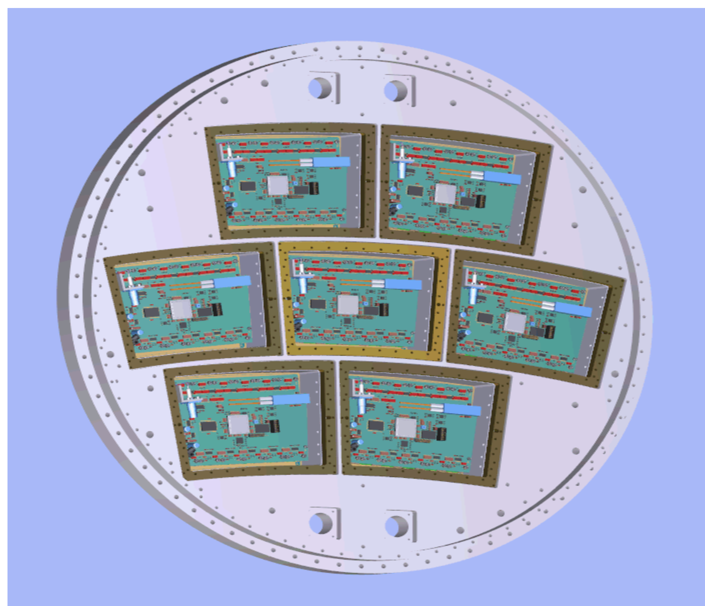
FEC



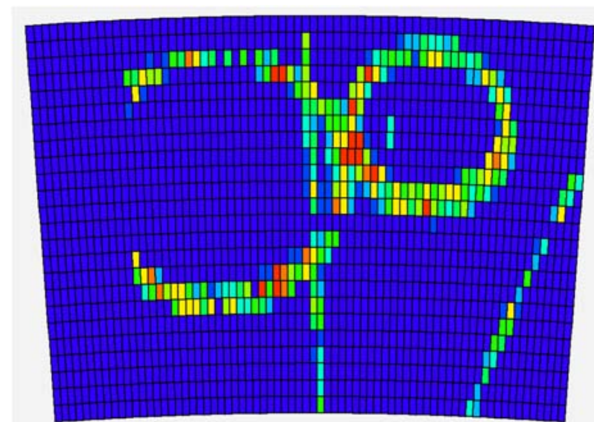
by Saclay group



power pulsing under 5T is planned



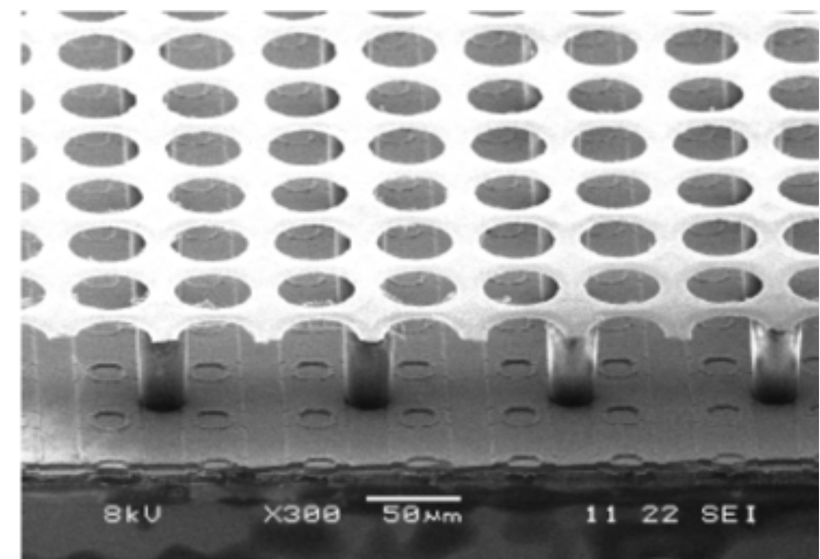
fits 7 module micromegas for the large prototype

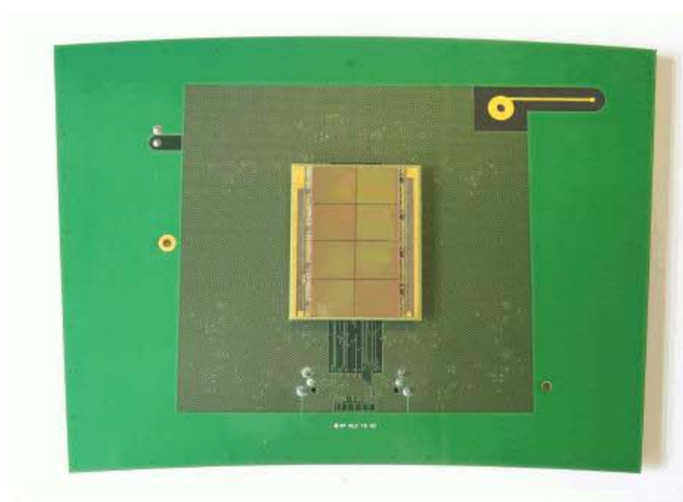


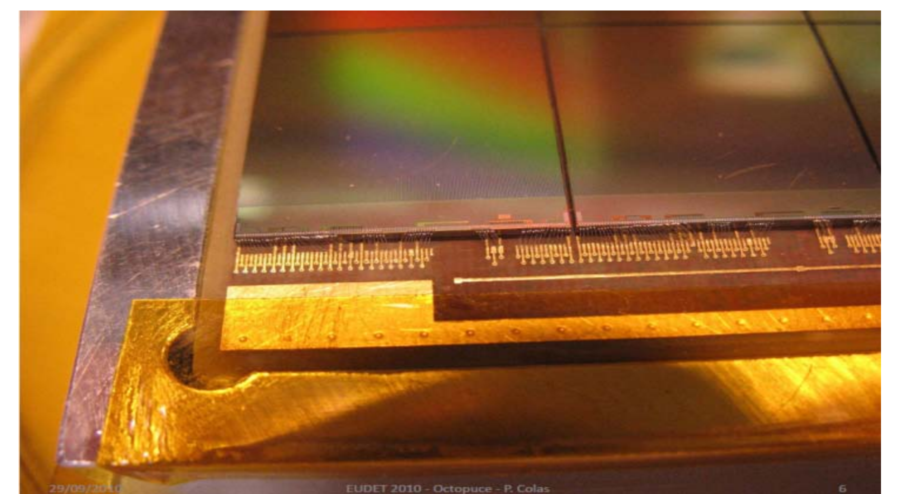
Single-module operation with 5GeV electron beam in B=1T

8 Ingrid TimePix chips: Octapos

TimePix chip
65 000 digital pixels (55 μm x 55 μm) with "single" time and TOT measurement, an Ingrid MicroMEGAS, the resistive Si layer to protect Timepix. Capability to detect single electron. Only one hit for a cell.







- TimePix1 (CMOS 250nm) is not designed to be power-pulsed.
- TimePix3 (CMOS 130nm) will have a power pulsing strategy. (submit: 2012)

Summary

- Technologies for realization of the advanced endplate are being prepared.
- 16ch S-ALTRO demonstrator chips were fabricated and their characterization is being performed. Depending on the results, final S-ALTRO strategy will be discussed.
- Test of CO_2 cooling and power pulsing is going to be performed using advanced endplate test board at KEK in 2011.
- Some semi-advanced endplate plans are presented.