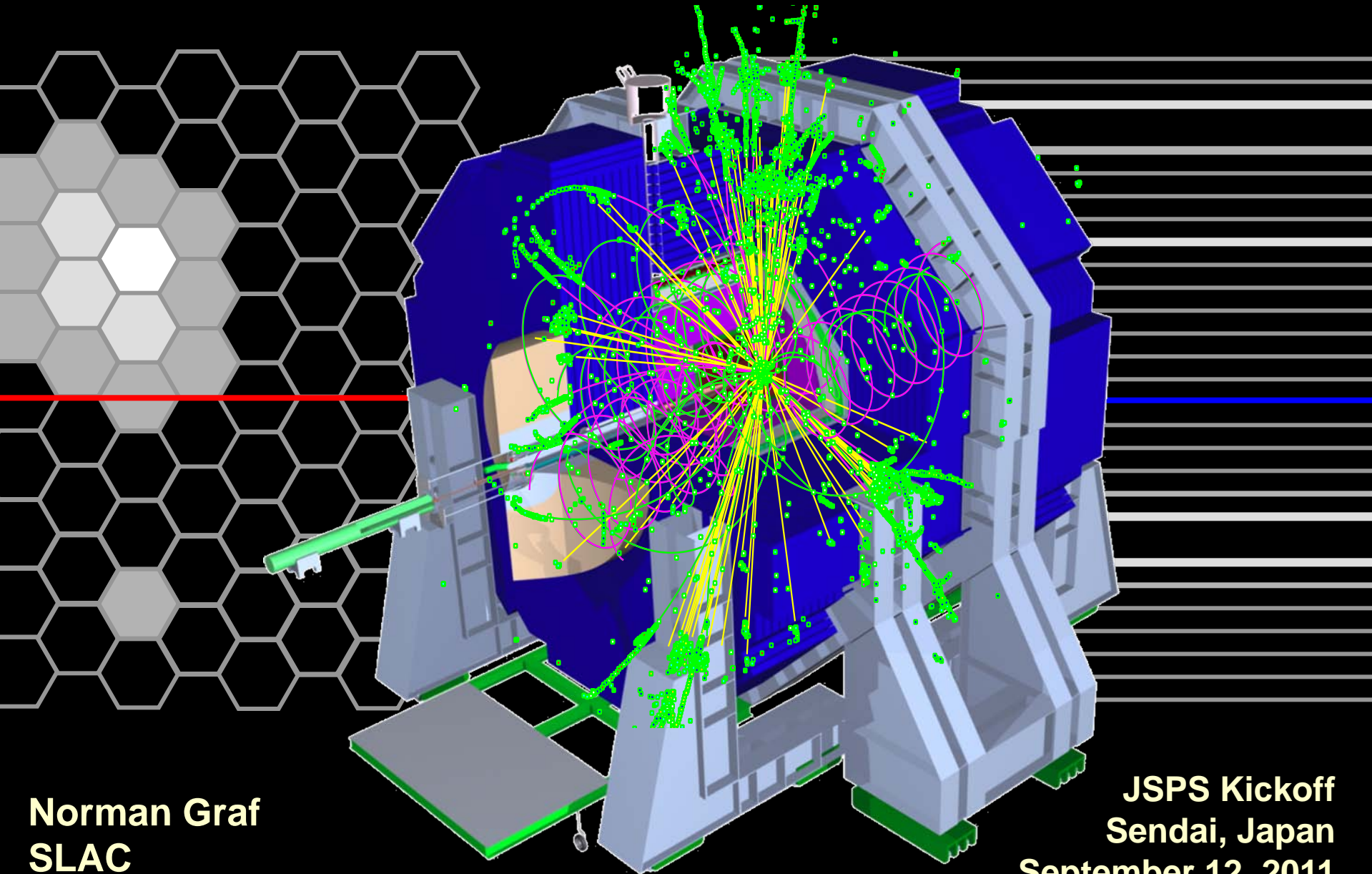


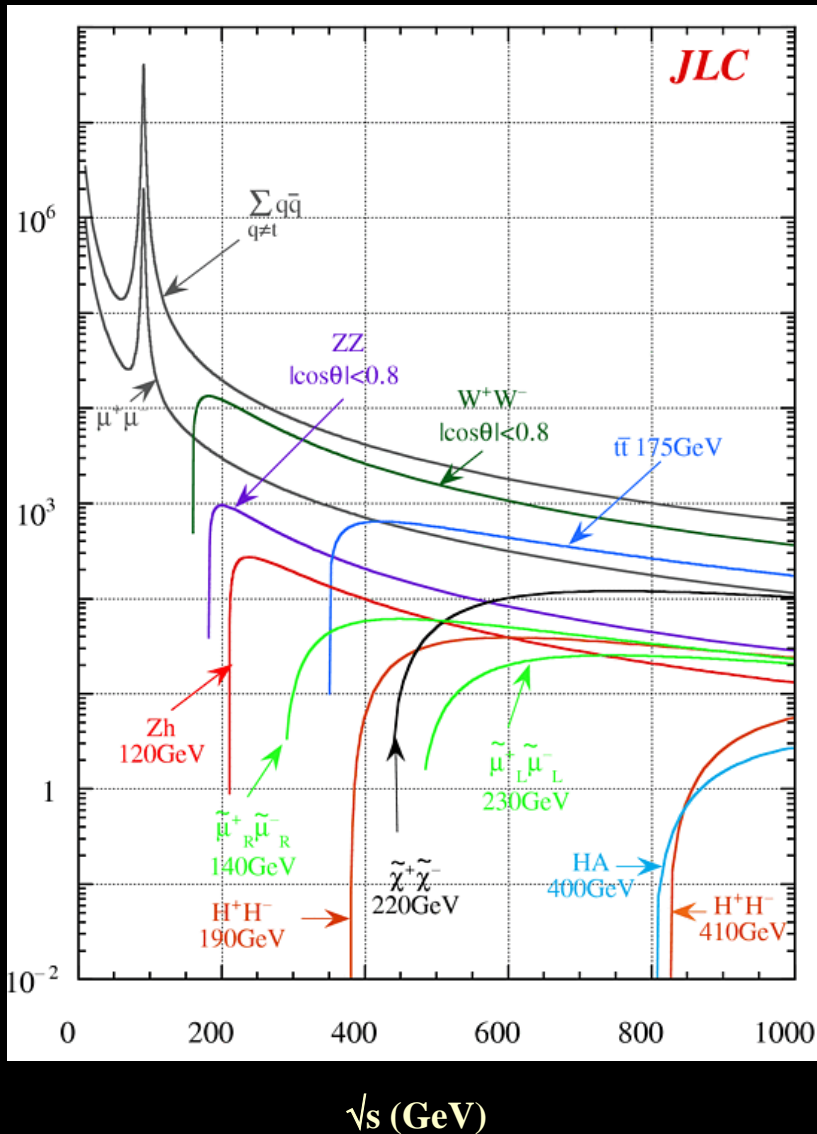
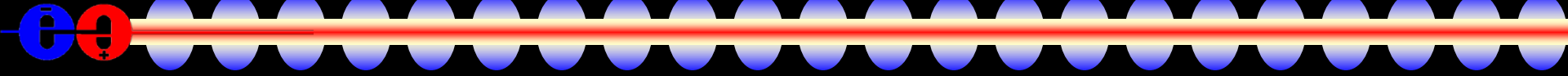
# The Silicon Detector Concept



**Norman Graf**  
**SLAC**

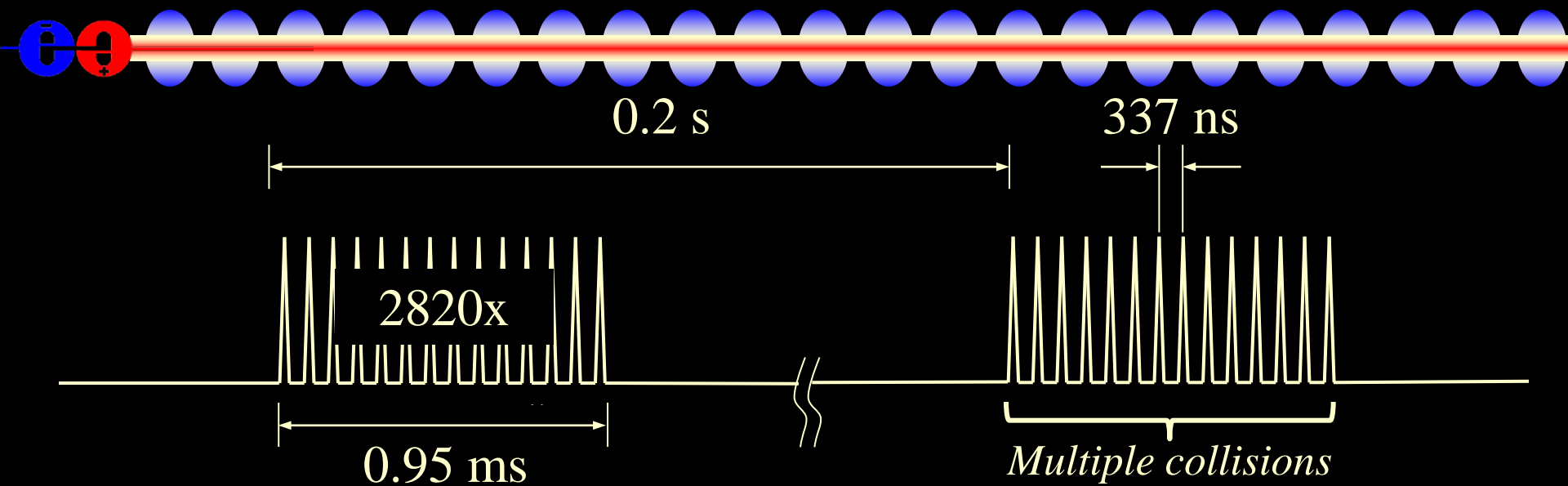
**JSPS Kickoff**  
**Sendai, Japan**  
**September 12, 2011**

# Linear Collider Environment



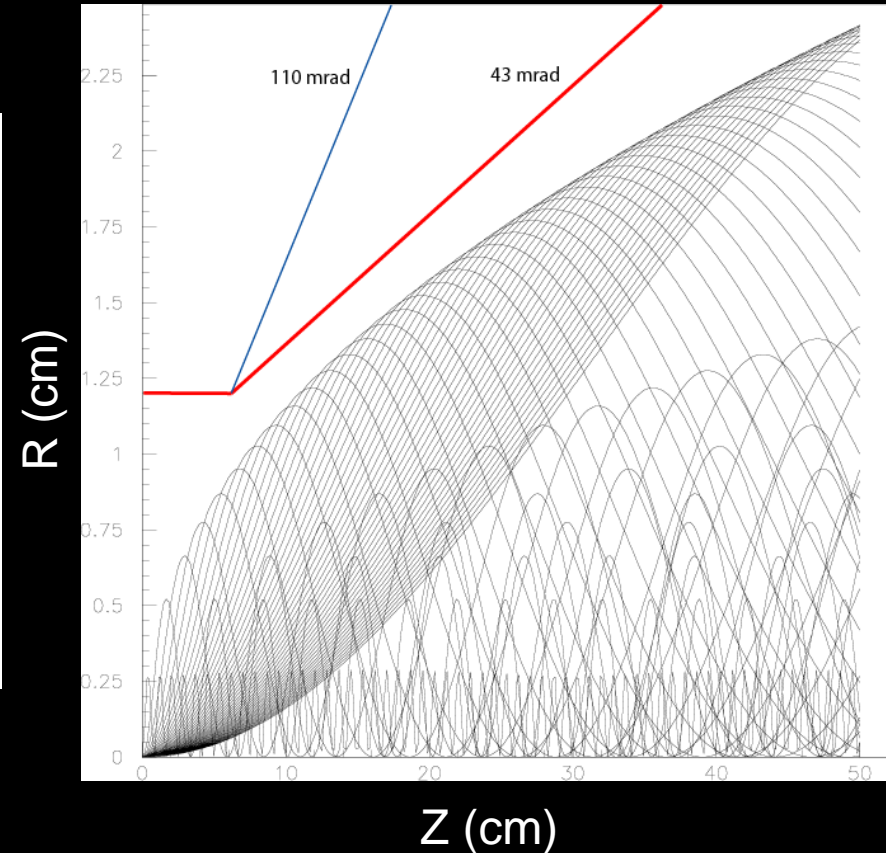
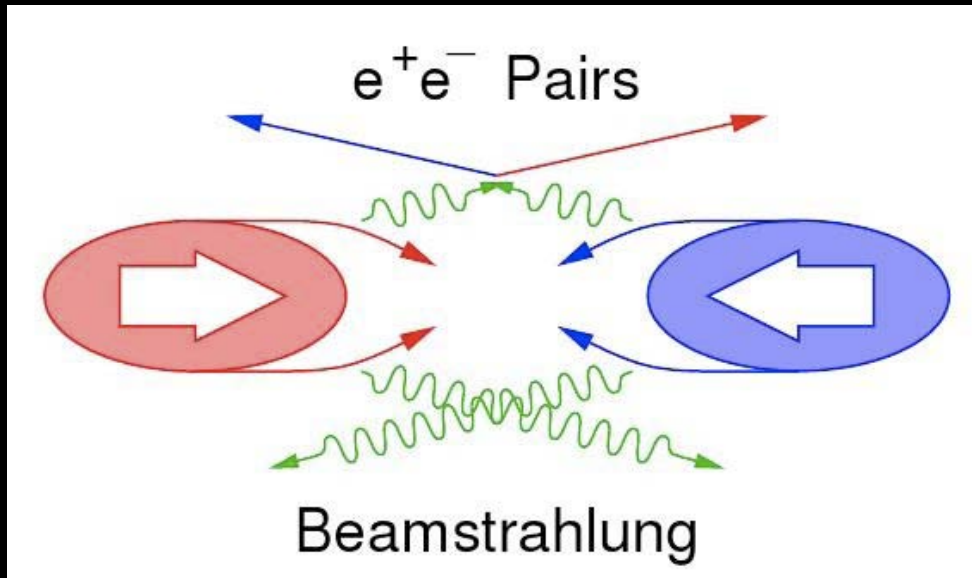
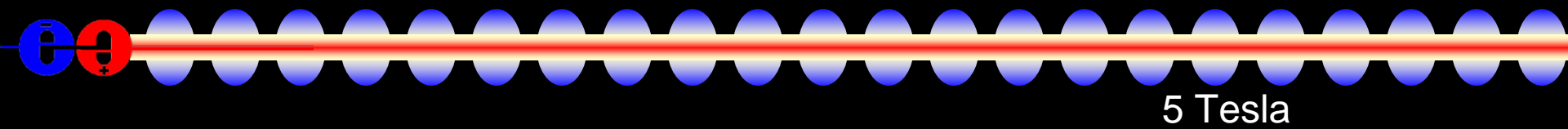
- Detectors designed to exploit physics discovery potential of  $e^+e^-$  collisions at  $\sqrt{s} \sim 0.5 - 1\text{TeV}$ .
- Perform precision measurements of complex final states with well-defined initial state:
  - Tunable energy
  - Momentum constraints
  - Known quantum numbers
    - $e^-, e^+$  polarization
  - Very small interaction region
- “Democracy” of processes and lower cross sections, plus precision measurements, require sensitivity to all decay channels.
  - W/Z separation in hadronic decays
  - jet flavor tagging

# ILC Beam Structure



- Beam structure allows for power pulsing
  - reduce power between bunch “trains”
  - reduces cooling needs
- Beam structure requires bunch disambiguation
  - multiple readouts during train
  - time-stamping of subdetector hits

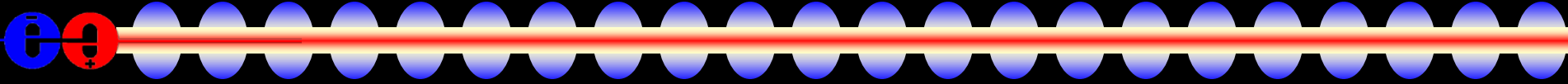
# ILC Beam



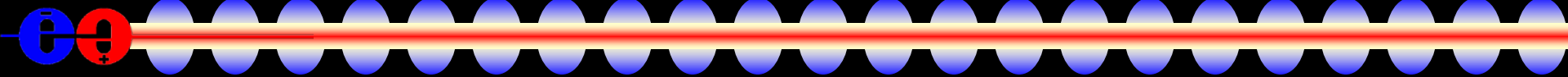
“Pinch” of beams increases luminosity, but disruption creates pairs via beamstrahlung.

High field required to stay clear of “cone of death”.

# Detector Requirements

- 
- Precision invariant mass resolution
    - Higgs recoil measurement for  $Z \rightarrow e^+e^-$ ,  $\mu^+\mu^-$
    - Fully reconstruct hadronic final states for W/Z ID & separation
  - Tag quark flavor with high efficiency and purity.
    - top quark Yukawa coupling ( 8 jets, 4 b), higgs self-coupling
  - Excellent missing energy/mass sensitivity.
    - SUSY LSP
  - Require:
    - Excellent vertexing capabilities:
      - Inner radius close to beampipe, high precision, time resolved  $\sigma_{r\phi} \approx \sigma_{rz} \approx 5 \oplus 10/(p\sin^{3/2}\theta)$
    - Exceptional momentum resolution:
      - High magnetic field, low-mass precision tracker  $\sigma(1/p_T) = 5 \times 10^{-5} (GeV^{-1})$
    - Precision calorimetry:
      - “Particle Flow”, imaging sampling calorimeter  $\sigma_{Ejet} / Ejet \approx 3\%$
    - Hermeticity:
      - Minimal supports, on-detector readout.  $\Omega = 4\pi$
  - Affordable!  $\rightarrow$  cost-constrained optimized design

# *The Silicon Detector Concept*



- **Detector is the best fully integrated system**
  - Not a collection of “best” subdetectors.
  - Use “Particle Flow Algorithm” as primary design guide.
  - Tightly integrated simulation / reconstruction / analysis effort provides physics performance metric.
  - Tightly integrated parametric cost model provides cost as function of performance.
- Si/W EM Calorimeter: highly segmented, dense, good E resolution
- Minimizing size (cost) of ECAL → space constraints on tracking system (R)
- Recover momentum resolution ( $\sim BR^2$ ) with central magnetic field of 5 T.
- Use 5 layer barrel + endcap pixel vertex detector close to beam.
- Si  $\mu$ -strips in 5 layer tracker for excellent  $\delta p/p$ , pattern recognition, and input charged track trajectories for calorimeter cluster association (PFA).
- Compact Hadron Calorimeter to stay within affordable, buildable coil.
  - dense absorber, excellent segmentation, small readout gap necessary
- Instrumented magnetic flux return serves as muon system, tail-catcher for penetrating showers, self-shielding detector.
- Tag timing of tracking, EM Calorimeter, for background reduction by track/bunch association.

# Tracking Detectors

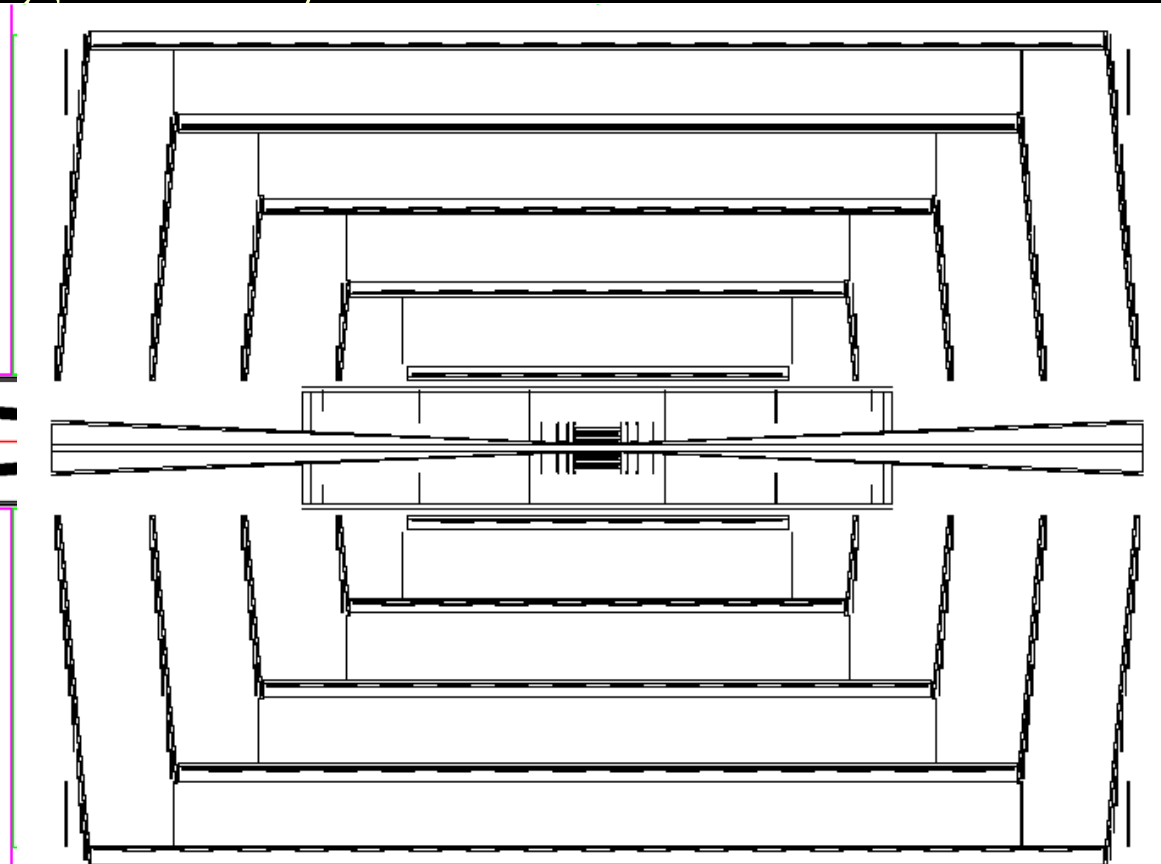
- Although mechanically and technologically distinct, the vertex detector and outer tracker are being designed as an integrated system.

## **Vertex:**

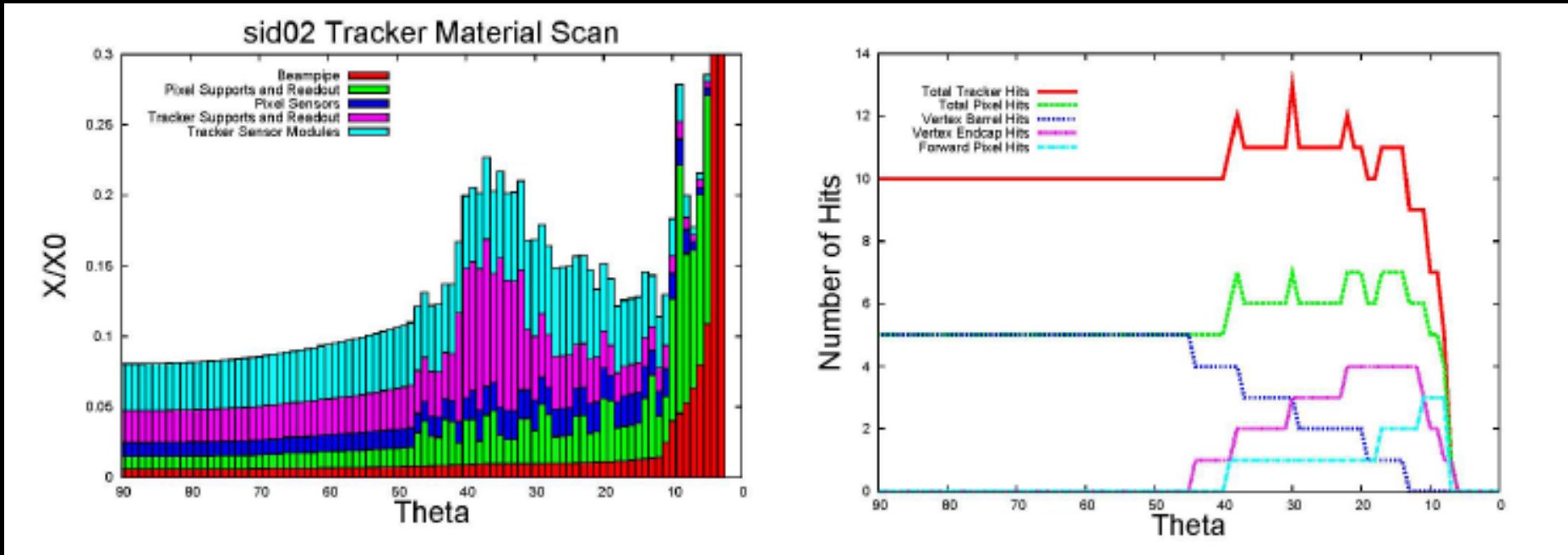
5 barrel + 7 disk  
inner pixel detector

## **Tracker:**

5 barrel (axial strip)  
4 disk (stereo strips)



# Tracking Detectors

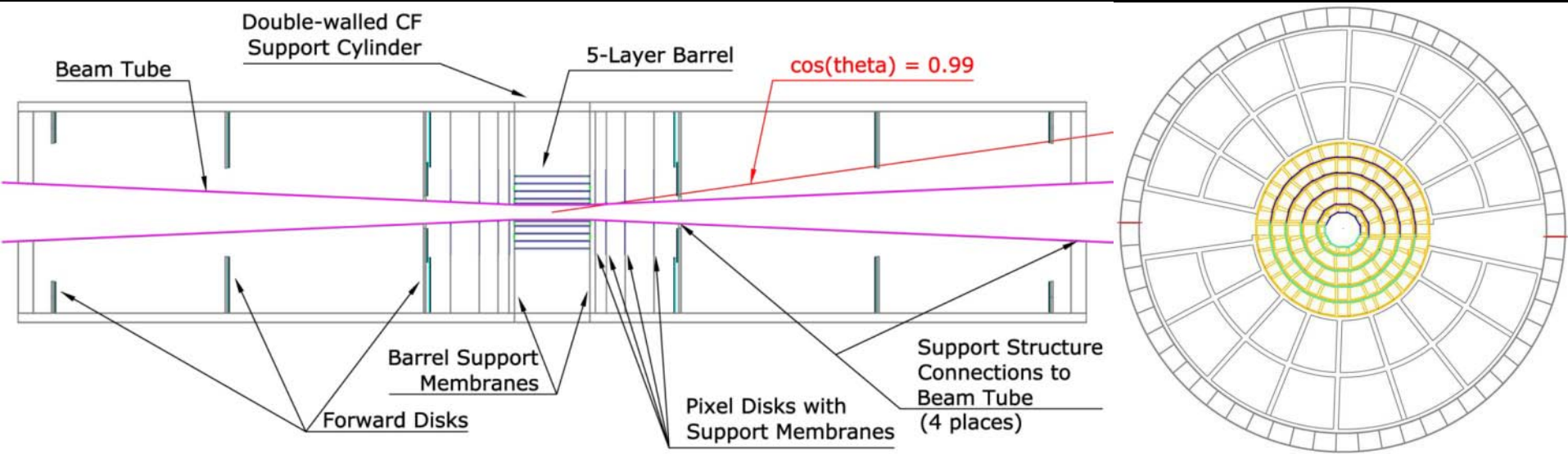


- Material budget  $X/X_0 < 0.2$  throughout the tracking volume.
- Uniform coverage of a minimum of 10 hits per track down to small angles.



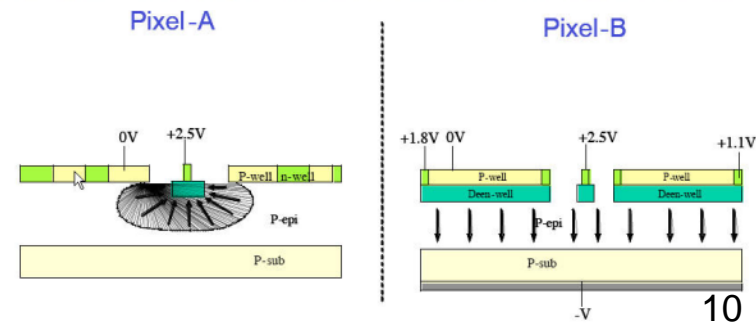
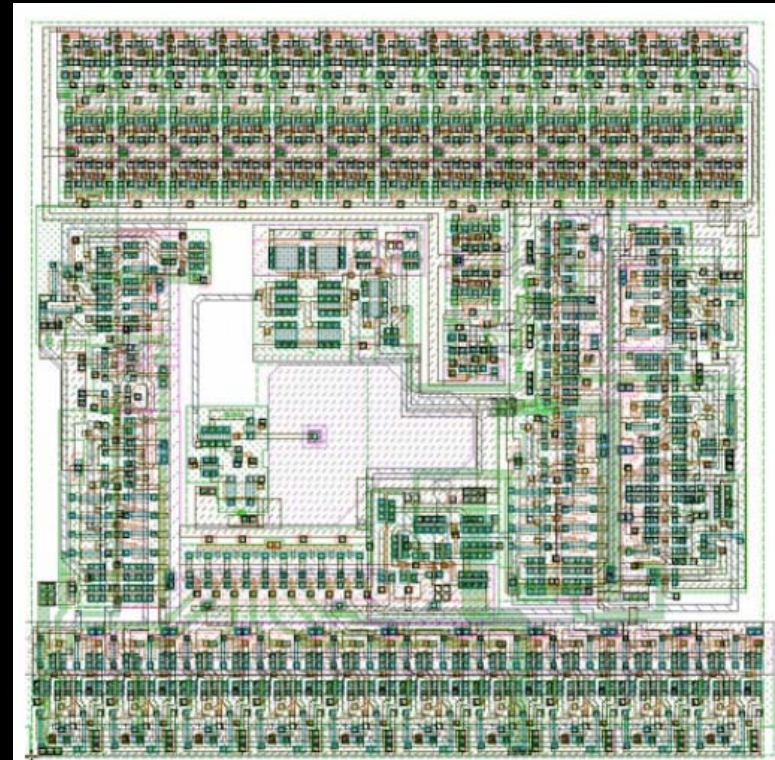
# Pixel System

- **Baseline vertex detector:**
  - **Central: 5-layer barrel, sensors glued on edges to form cylinders**
  - **End cap: two 4-plane end disk assemblies and three additional disks per end for extended coverage**
- **All elements supported indirectly from the beam tube via double-walled, carbon fiber laminate half-cylinder**
- **Gas cooled, power pulsed, low mass**
- **Sensor technology to be determined**



# Chronopixel

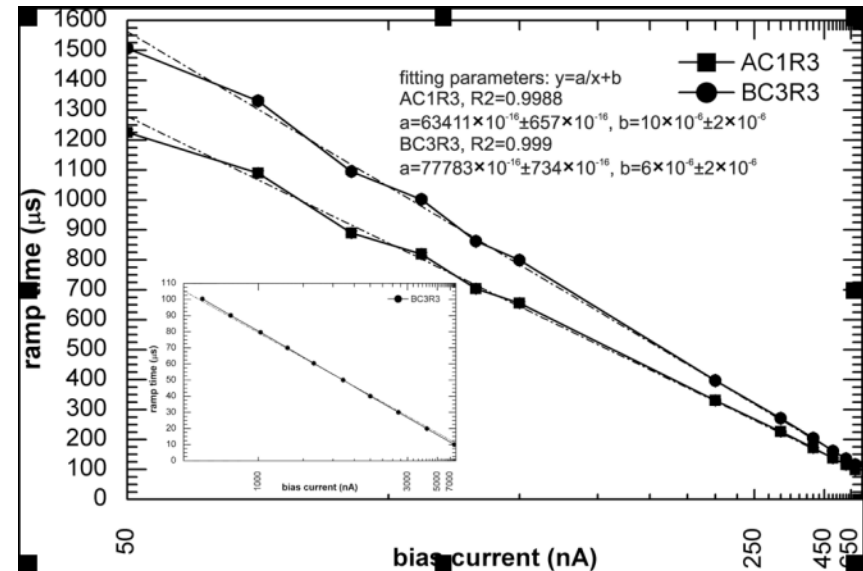
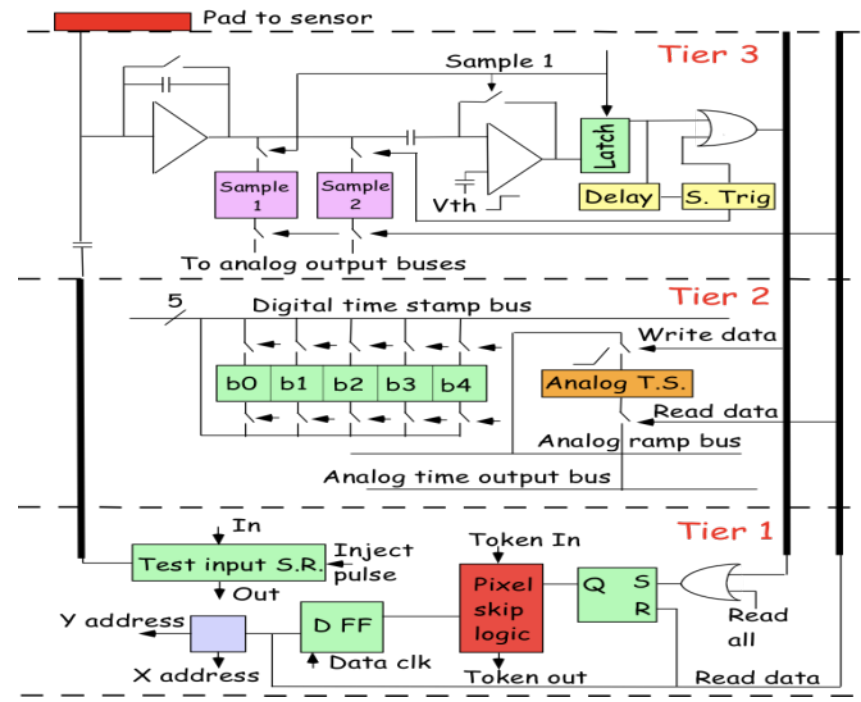
- Chronopixel design provides for single bunch-crossing time stamping
  - When signal exceeds threshold, time stamp provided by 14 bit bus is recorded into pixel memory, and memory pointer is advanced
  - Comparator threshold adjusted for all pixels
- Current design
  - 50x50  $\mu\text{m}^2$  pixels
  - Two pixel architectures
    - Regular p/n-well design (A)
    - Deep n-well design (B)
- Tests show general concept works
  - Good sensitivity ( $\mu\text{V}/e^-$ ) as designed
  - Sensors timestamp max. recording speed (7.27 MHz) is adequate
  - Noise figure meets specifications
  - Analog power pulsing OK



# 3D Vertex Chip – VIP and SOI R&D

VIP is designed to fit time stamping, sparse scan, adc in small pixel

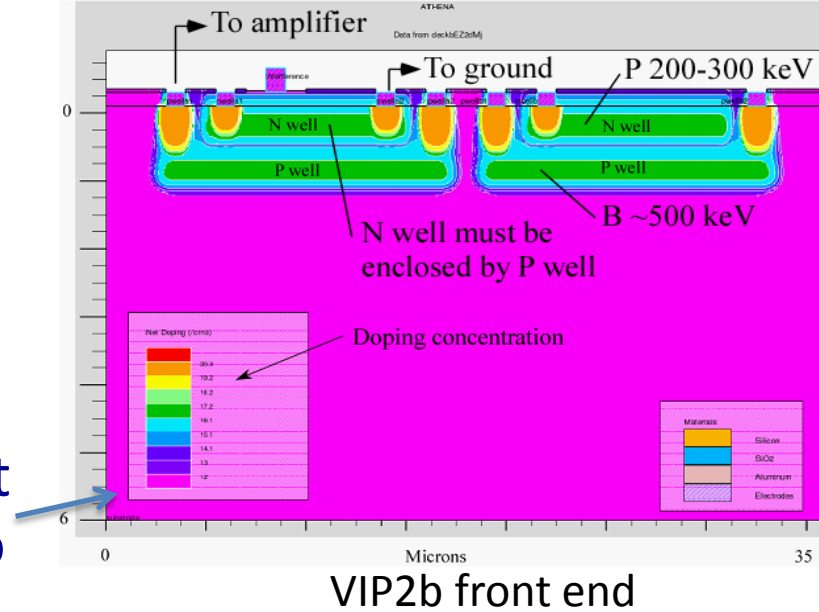
- First two generations – three tiers in 0.18  $\mu\text{m}$  MIT-LL process
- Last generation – VIP2b two tiers in 0.13  $\mu\text{m}$  Global Foundries. 24  $\mu\text{m}$  pixel In final 3D processing – 2D test structures measured



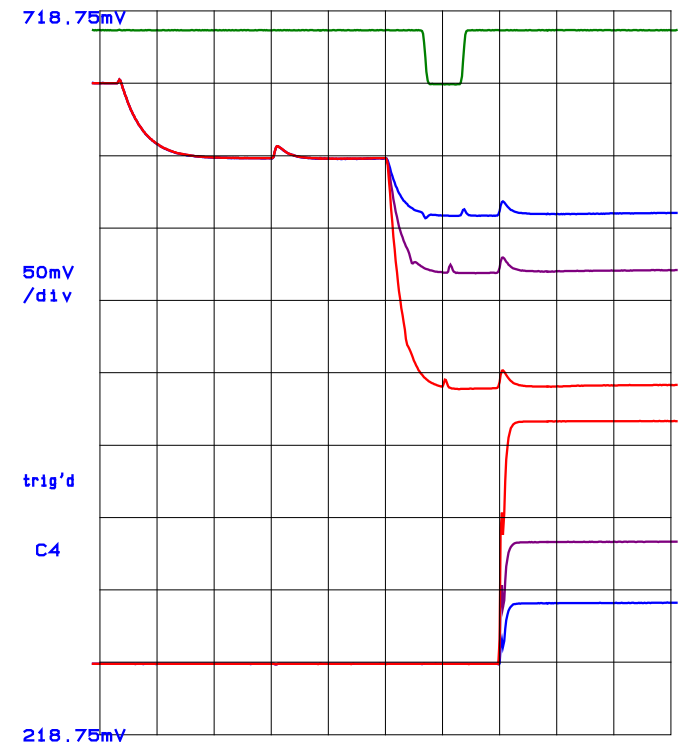
VIP 2a Analog Time Stamp ramp

# 3D/SOI progress and breakthroughs

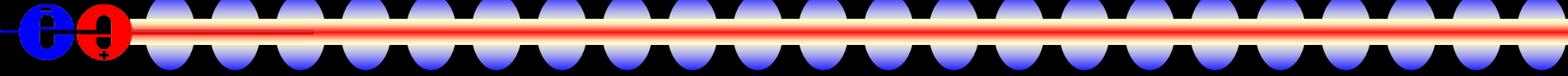
- 3D multiproject chips being tested
- 3D process commercialized
- SOI process developed which is robust against backgate effects and digital to analog coupling.
  - First detector test with electronics integrated with float zone silicon
  - Thinning and laser annealing process demonstrated
- Hope to demonstrate 3D chip/sensor integration this year
- Ready to proceed to full-sized fully functional devices in either SOI or 3D. Both the circuit design and chip/sensor technology has become mature enough for full scale prototypes



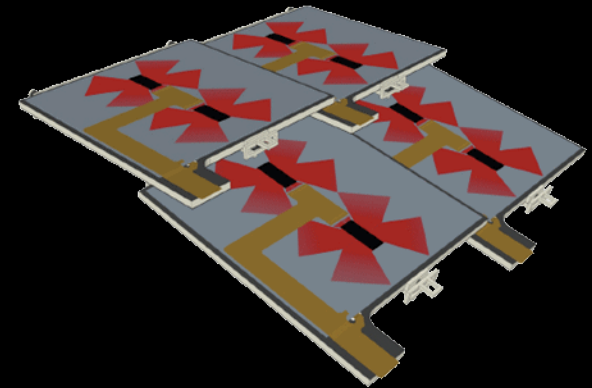
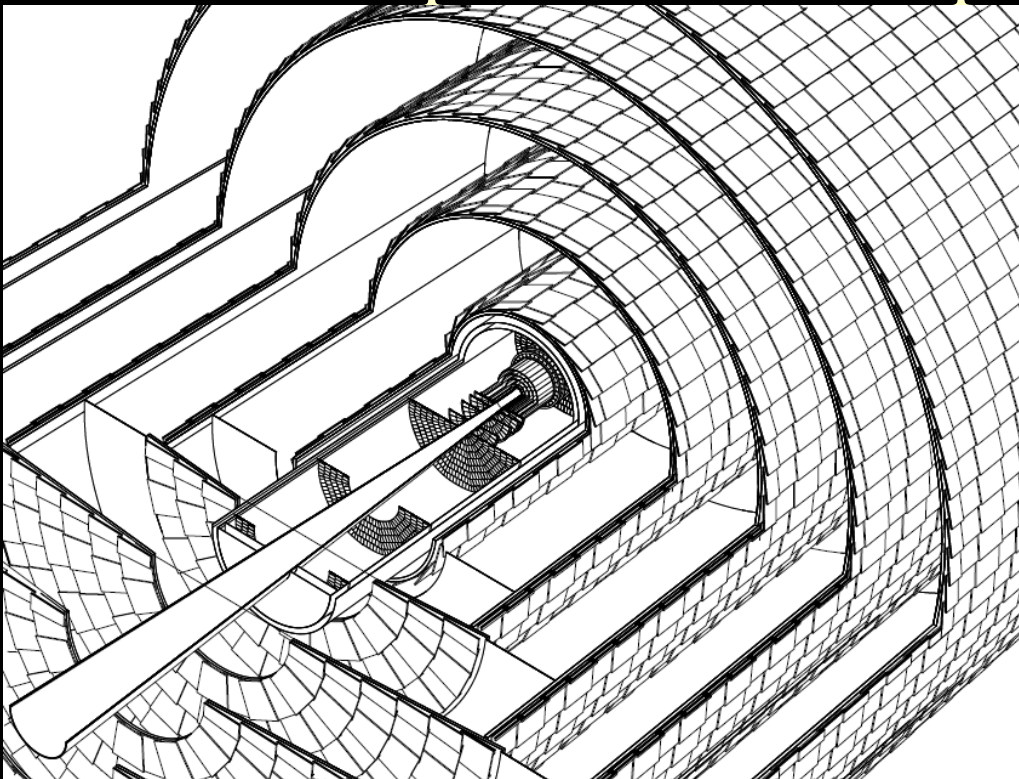
VIP2b front end



# Tracking System

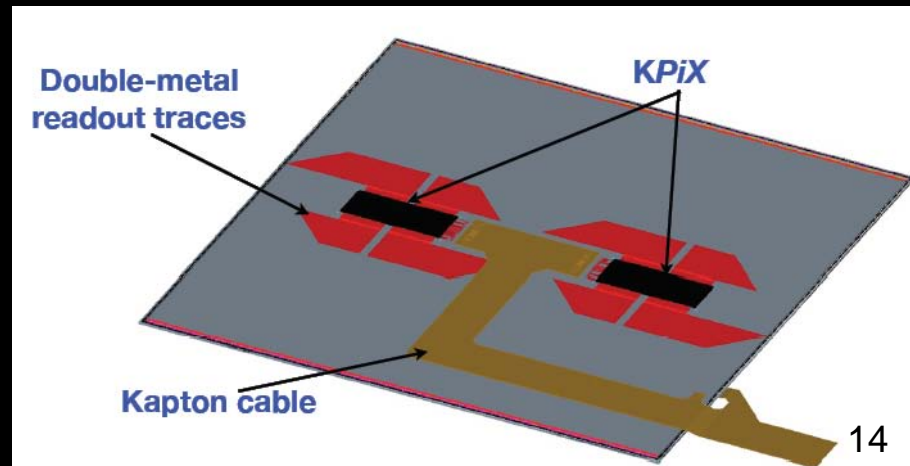
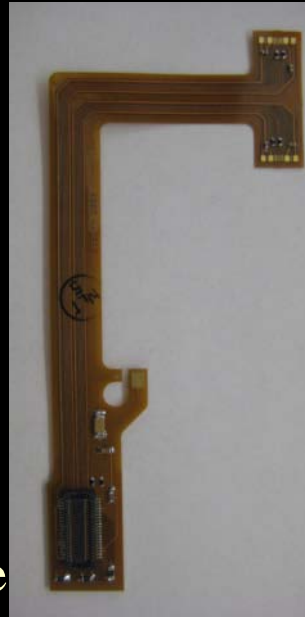


- Barrels composed of carbon-fiber/Rohacell cylinders tiled with overlapping axial readout sensors.
- Dished “disks” tiled with overlapping trapezoidal pairs of sensors to provide stereo r-phi measurements

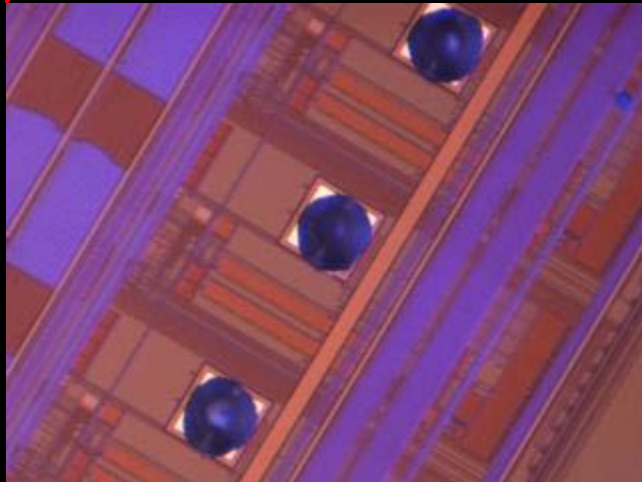
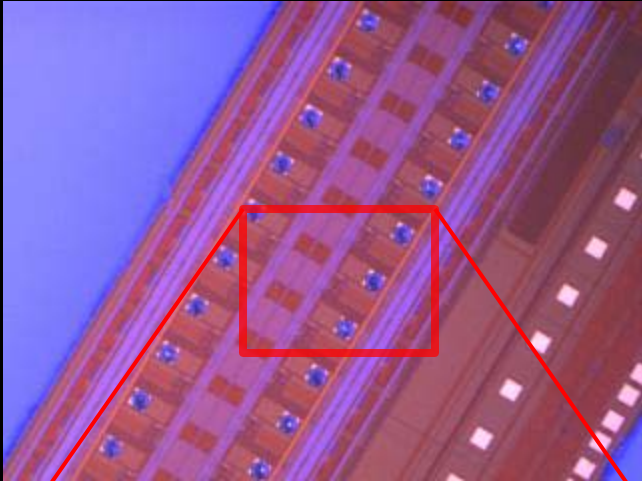


# Sensors and Readout

- Hybrid-less module
- Silicon Sensor
  - 93.5 x 93.5 mm<sup>2</sup> sensor from 6" wafer with 1840 (3679) readout (total) strips
  - Routing of signals through 2<sup>nd</sup> metal layer, optimized for strip geometry
  - Minimize capacitance and balance with trace resistance for S/N goal of 25
  - Power and clock signals also routed over the sensor
- KPiX readout ASIC
- Flexible readout cable

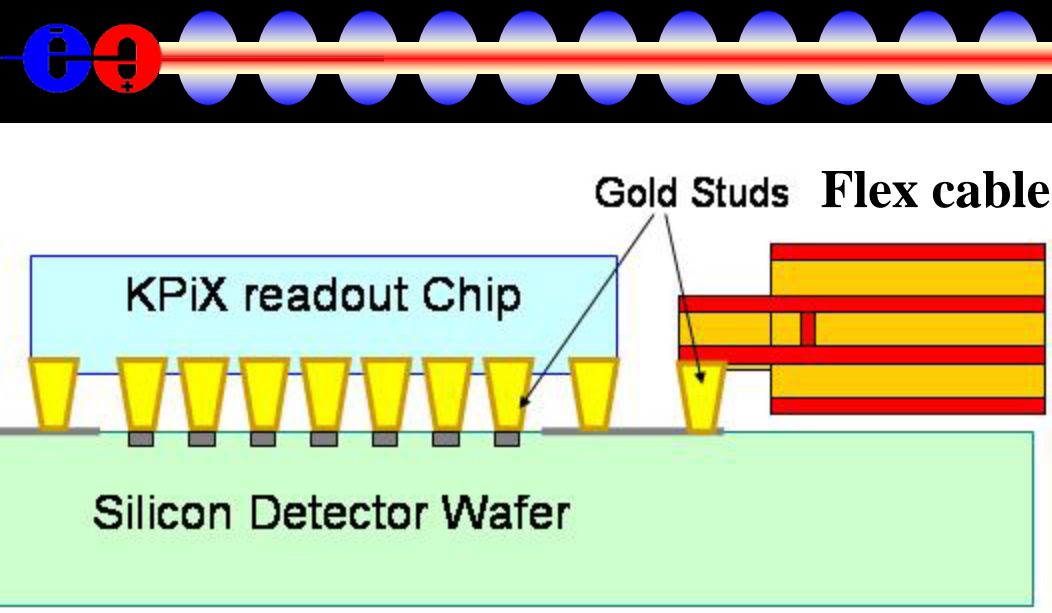


# Gold-Stud Bonding



- Studs are well-formed and centered on the 70x70  $\mu\text{m}$  pads
- Bonding done at UC Davis
- Gold stud attachment using thermo-compression
  - 300-350 C and 150-200 g/bump.
  - Machine limit ~100-200 kg
    - Limits total number of bumps
- Results
  - 160 g/bump ok
  - 100 g/bump insufficient: 4 of 20 bumps were ~open
- Plans:
  - Study systematics with position, uniformity reproducibility

# Readout Cable

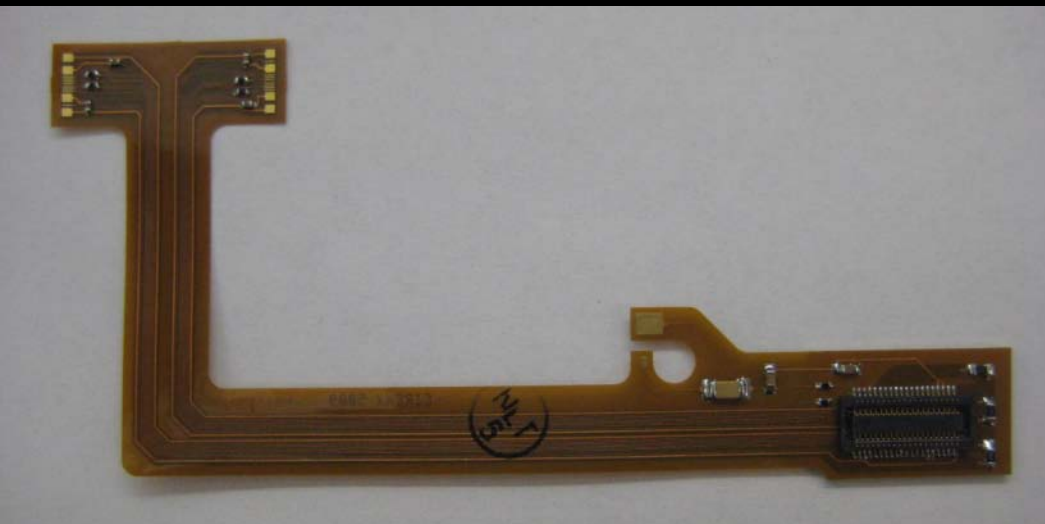


Low-mass readout cables connect tracker modules to the concentrator boards mounted at the ends of each barrel.

- Pigtail, a short cable glued to the module
- Extension, a long cable connecting the Pigtail to the concentrator

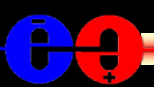
Cables for DM-SiD sensors produced (UNM/Fermilab)

- Being characterized at UNM
- All components in hand to develop full KPIX/DM prototype assembly for performance studies





# Electronics R&D: KPiX



KPiX readout for  
SiD subsystems.

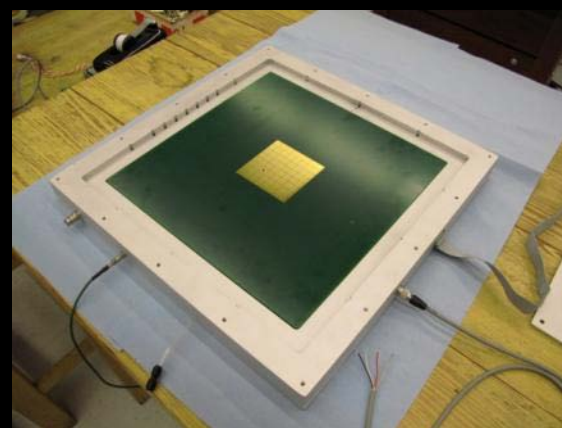
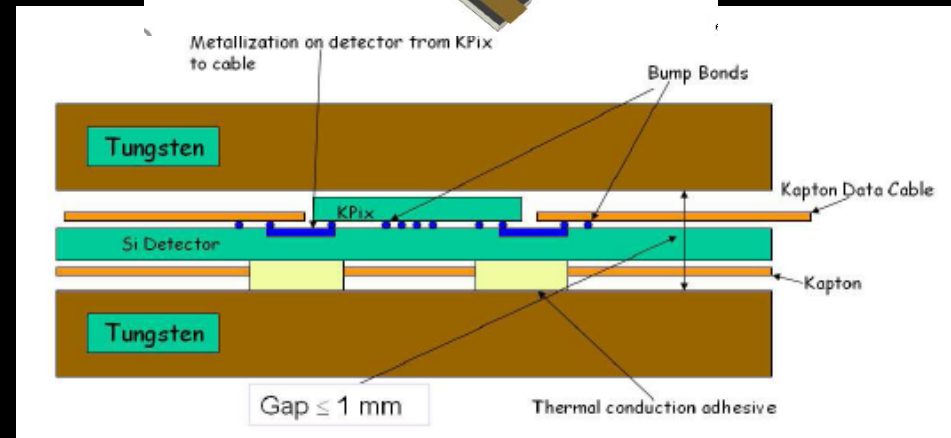
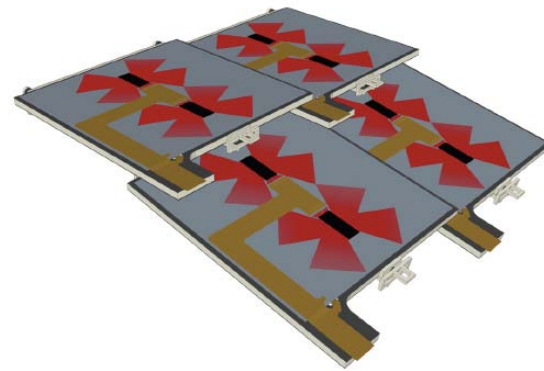
Tracker

ECal

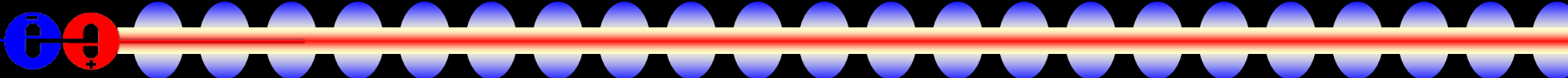
HCal (GEM  
version)

+ working on an  
FCal version

muon RPC

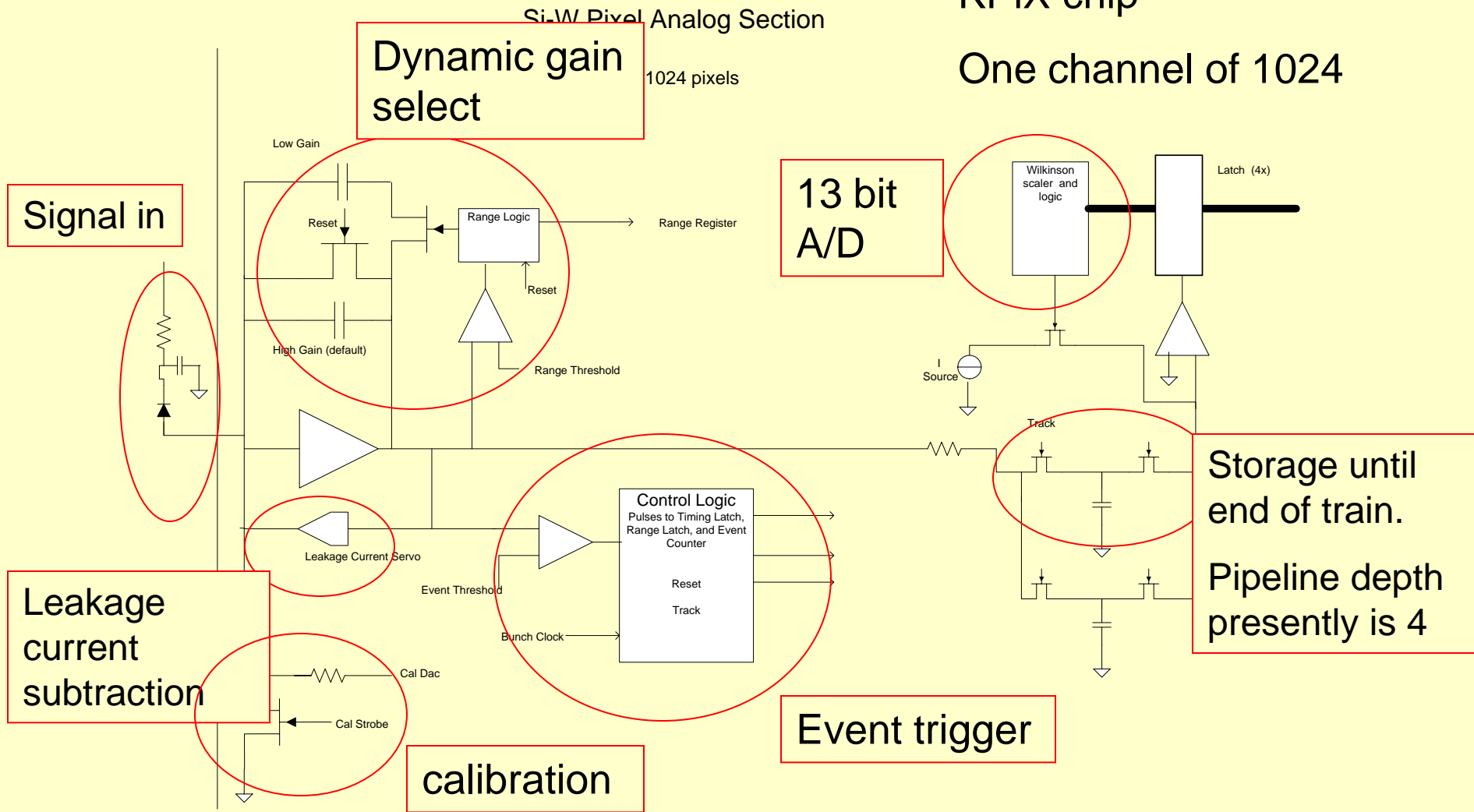


# KPiX Readout

- 
- KPiX is a multi-channel system-on-chip, for self triggered detection and processing of low level charge signals.
  - A digital core controls all operations according to parameters stored during set-up. This allows to match the chip to signals from a variety of sources. A variety of options, selectable by register settings, have been added over several prototype cycles.
  - The only external control signals are system clock, reset and command. Data output is serial.
  - Low average power consumption ( $<20 \mu\text{W}$  per channel) for ILC operation is obtained by powering down between beam spills. Power is reduced by lowering currents by a factor 100 while keeping the supply voltage stable. The current drop is controlled, with a decay time-constant  $\sim 10 \mu\text{s}$ , to limit voltage spikes caused by the cable impedance.
  - The chip is designed to be bump bonded to a Si-sensor, or to a hybrid for large area detectors (RPC's, GEM's). This avoids an extensive signal level cable plant (or headers) for the detector signals, resulting in significant reductions in mass (multiple scattering) and cost.
  - Range- and Noise-Specifications:
    - Peak Signal (Dual Range) 10 pC.
    - Range Switching (selectable)  $\sim 400 \text{ fC}$ .
    - Noise Floor 0.15 fC (1000 electrons).

# KPiX chip

## One channel of 1024



Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch  $n$  and time  $T_0$ .

The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).

The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.

When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)

The Track signal opens the switch isolating the sample capacitor at  $T_0 + 1$  micro s. At this time, the amplitude of the signal at  $T_0$  is held on the Sample Capacitor.

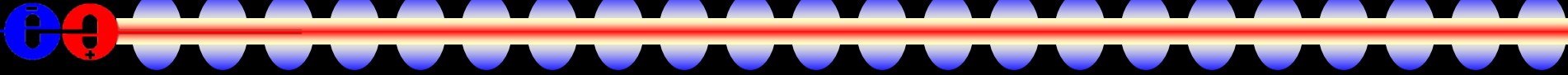
Reset is asserted (synched to the bunch clock). Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)

The system is ready for another signal in ~1.2 microsec.

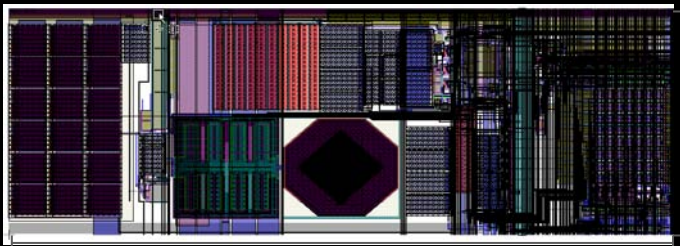
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

# *KPiX Status*

1



- 1024 pixel KPiX now being tested.
- Working on bump bonding KPiX to prototype ECal and tracker detectors.
- Developing 32 KPiX Ethernet interface to replace 3 KPiX USB interface.



# ECAL

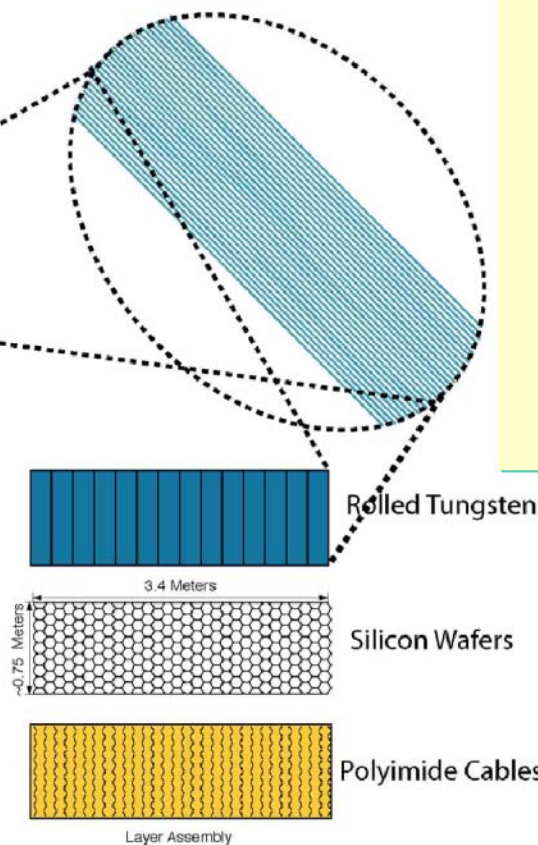


Si-W Calorimeter Concept

ECAL

Inner Tracker

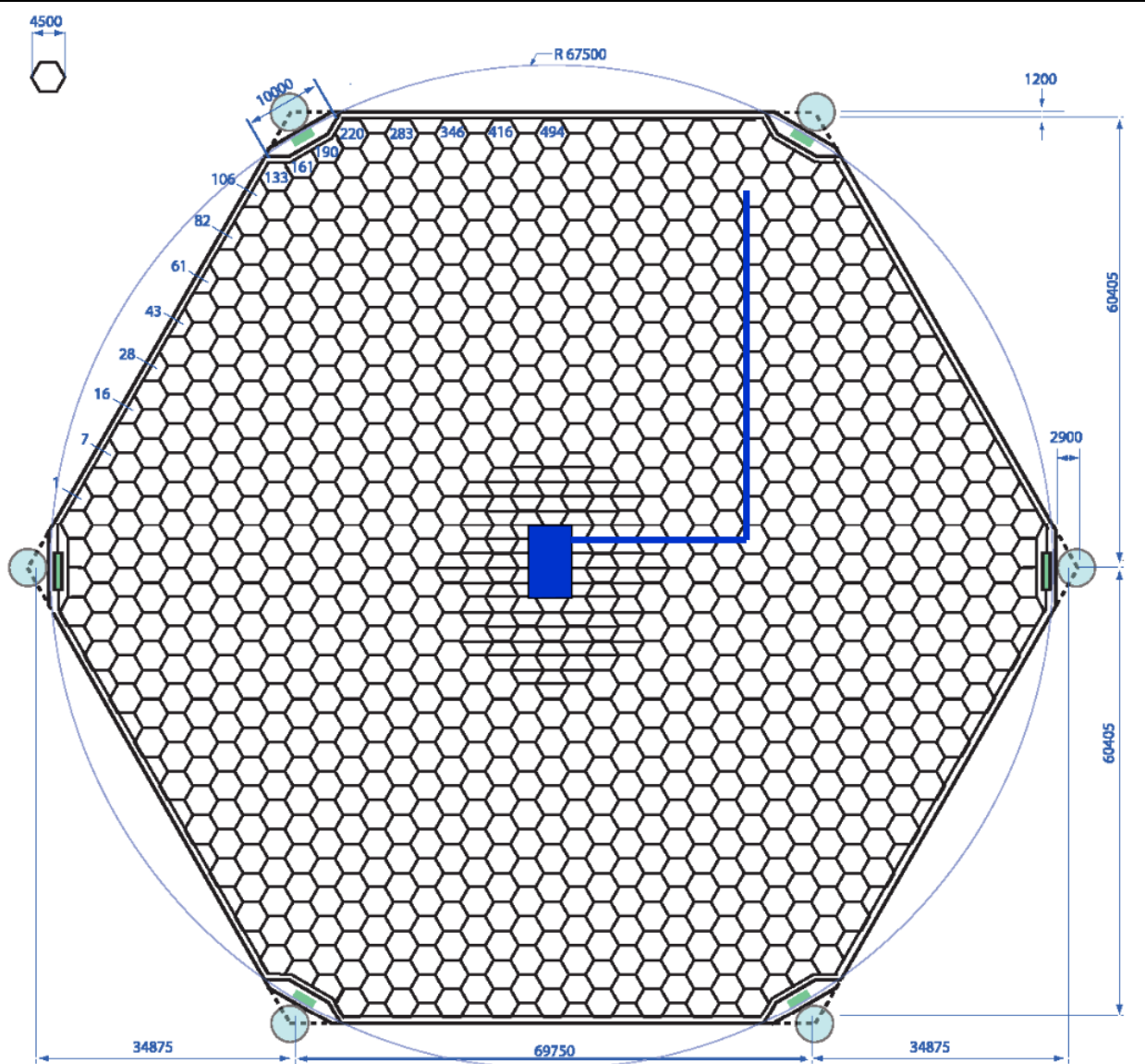
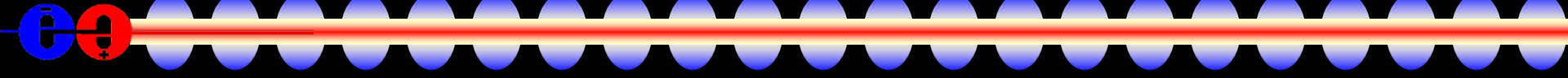
1.25m



Transverse Segmentation  $(3.6\text{mm})^2$   
20 + 10 Longitudinal Samples  
Energy Resolution  $\sim 17\%/E^{1/2}$

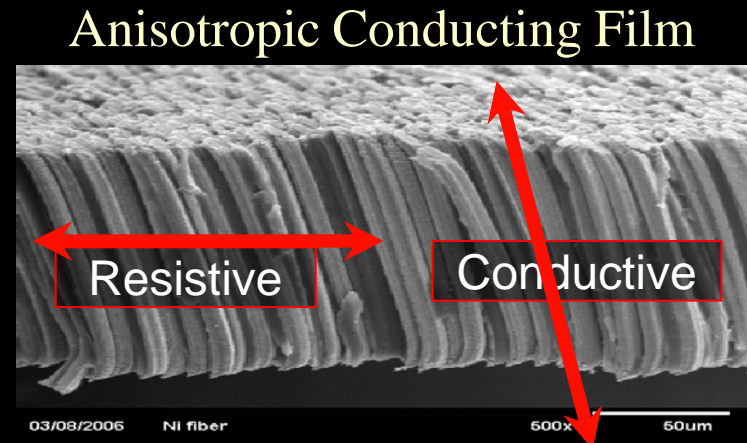
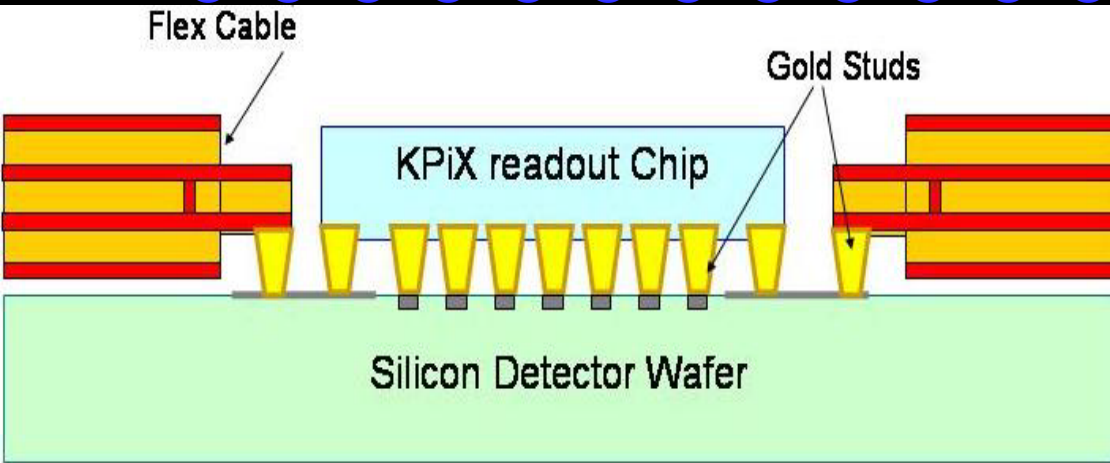
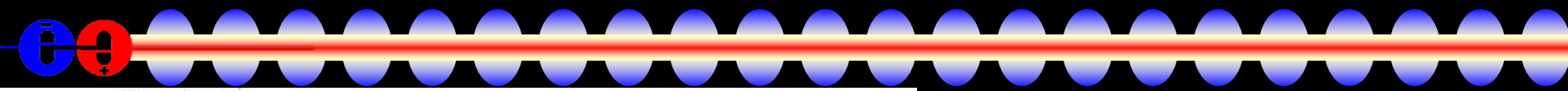
20 layers @  $5/7 X_0$   
10 layers @  $10/7 X_0$   
 $\Rightarrow 17\% / \sqrt{E}$   
 $\sim 1$  mm readout gaps  
 $\Rightarrow 13$  mm effective  
Moliere radius

# Silicon Sensors

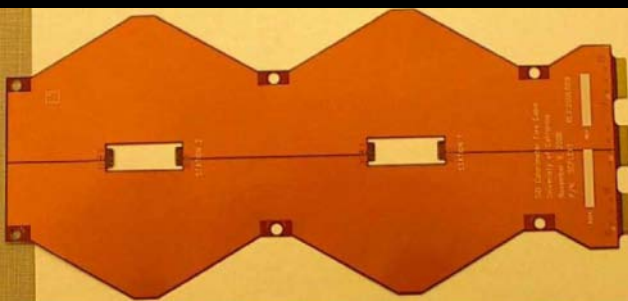


- 6 inch wafer
- 1024  $13 \text{ mm}^2$  pixels
- improved trace layout and split pixels near KPiX to reduce capacitance
- 40 good + 20 NG sensors in hand, Hamamatsu
- KPiX ASIC and sample trace

# Sensor Connection & Cables



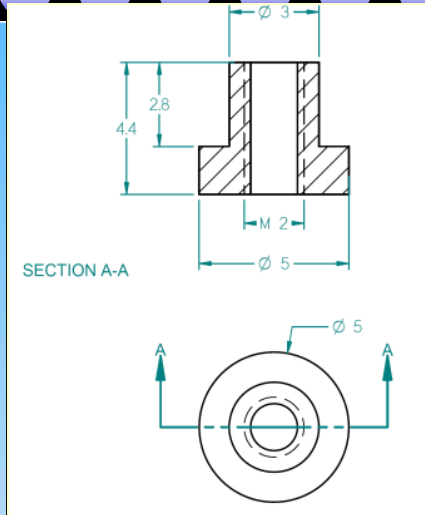
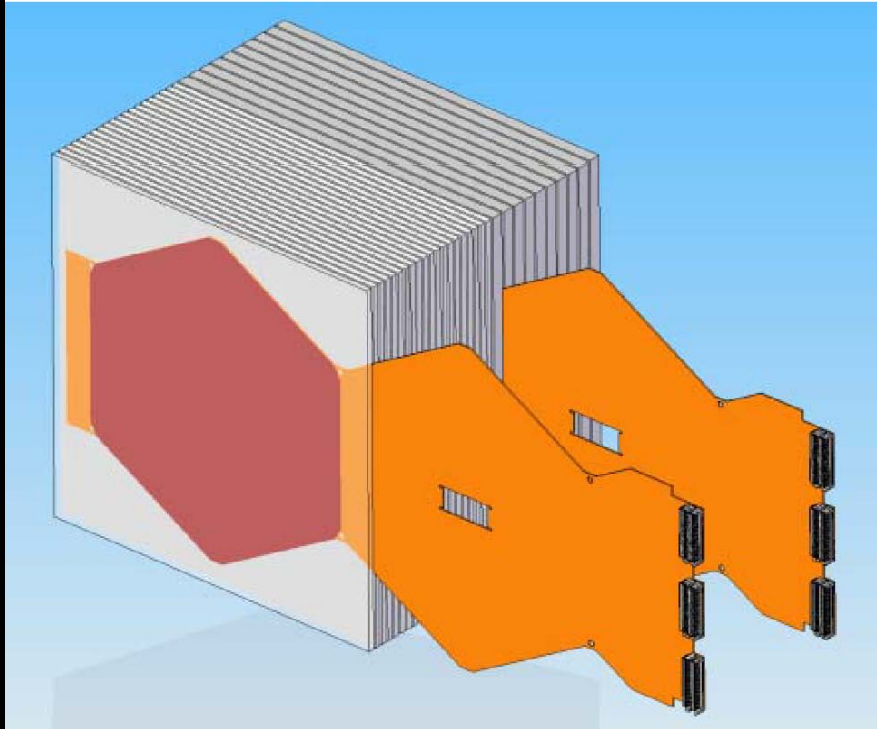
- ACF looks promising for largescale production
- Solder bumps – current default
  - Gold-Stud Thermo-compression bonding crushed the oxide layer resulting in shorts with buried traces.



Short flexcables OK for test stack

- Need to check longer ~1 m cables for SiD.

# ECal Testbeam



spacers

Test one stack with detector-ready components in beam.

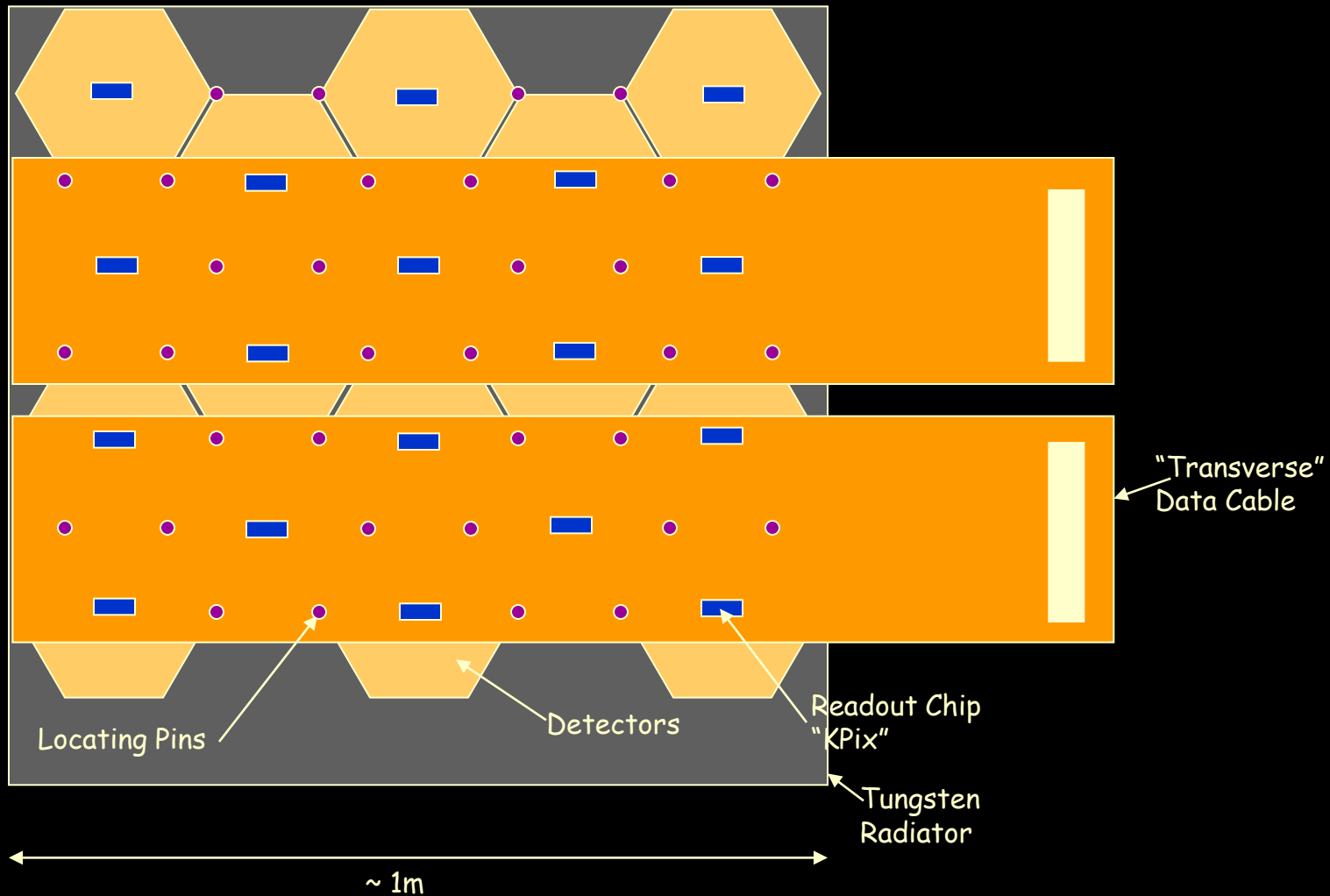


mockup with Lexan plates

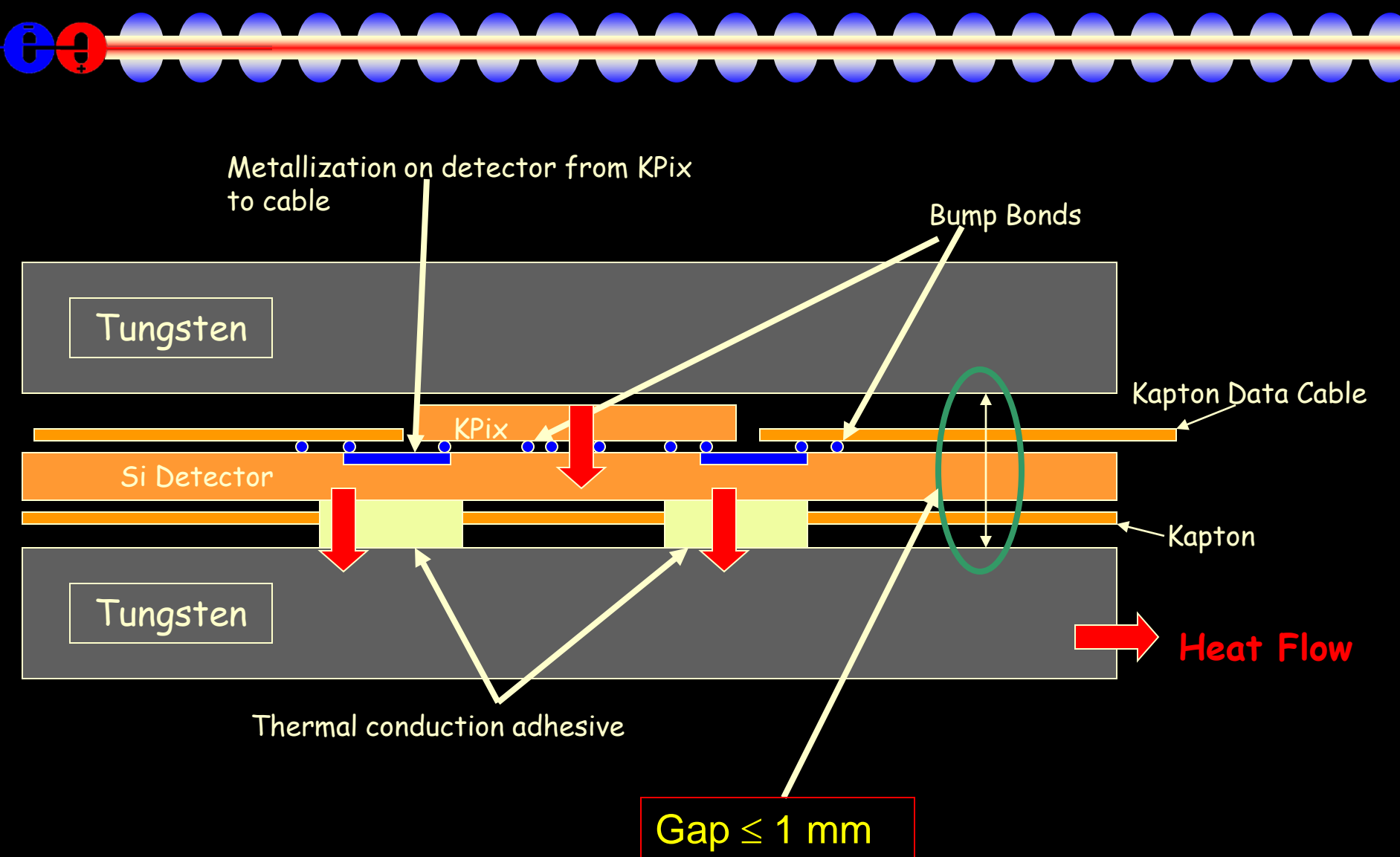




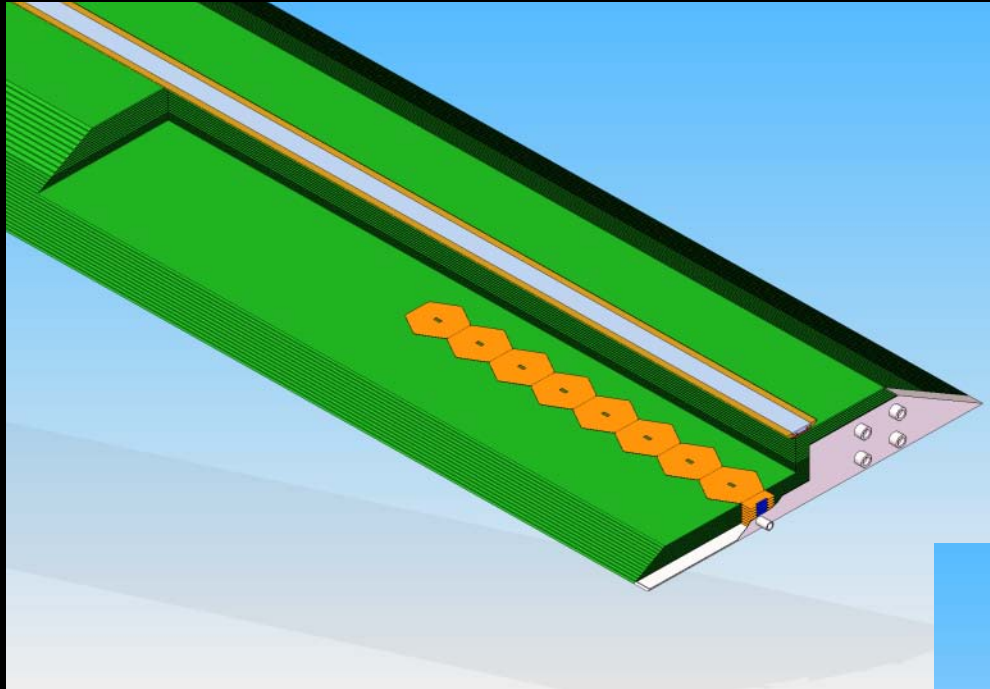
# *ECal Schematic Assembly*



# ECal Schematic Cross Section

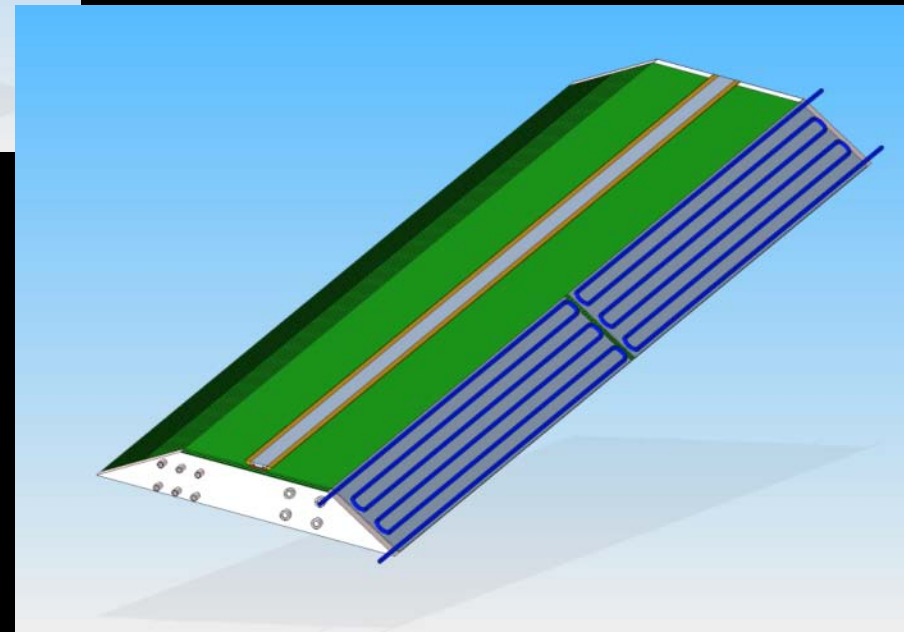


# *ECal Development*

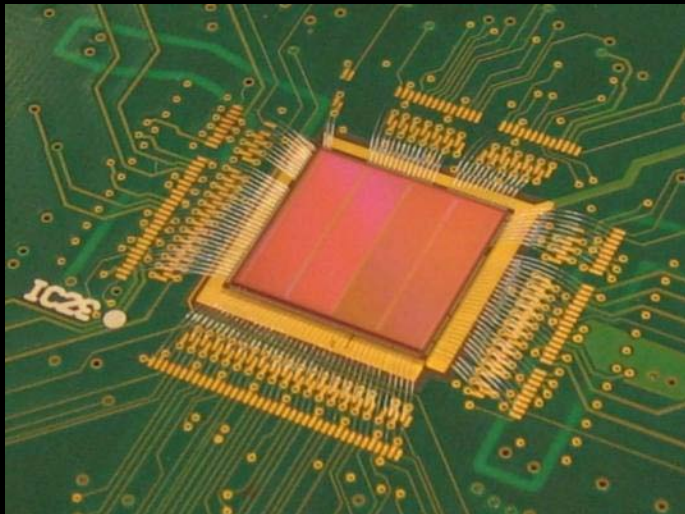
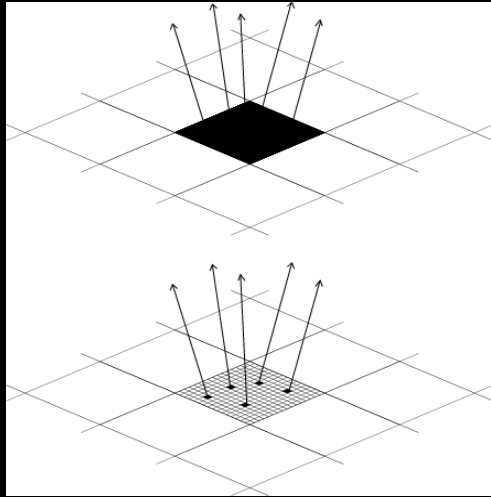


Cutaway view of Ecal module,  
showing readout cable

Heat removed at edges

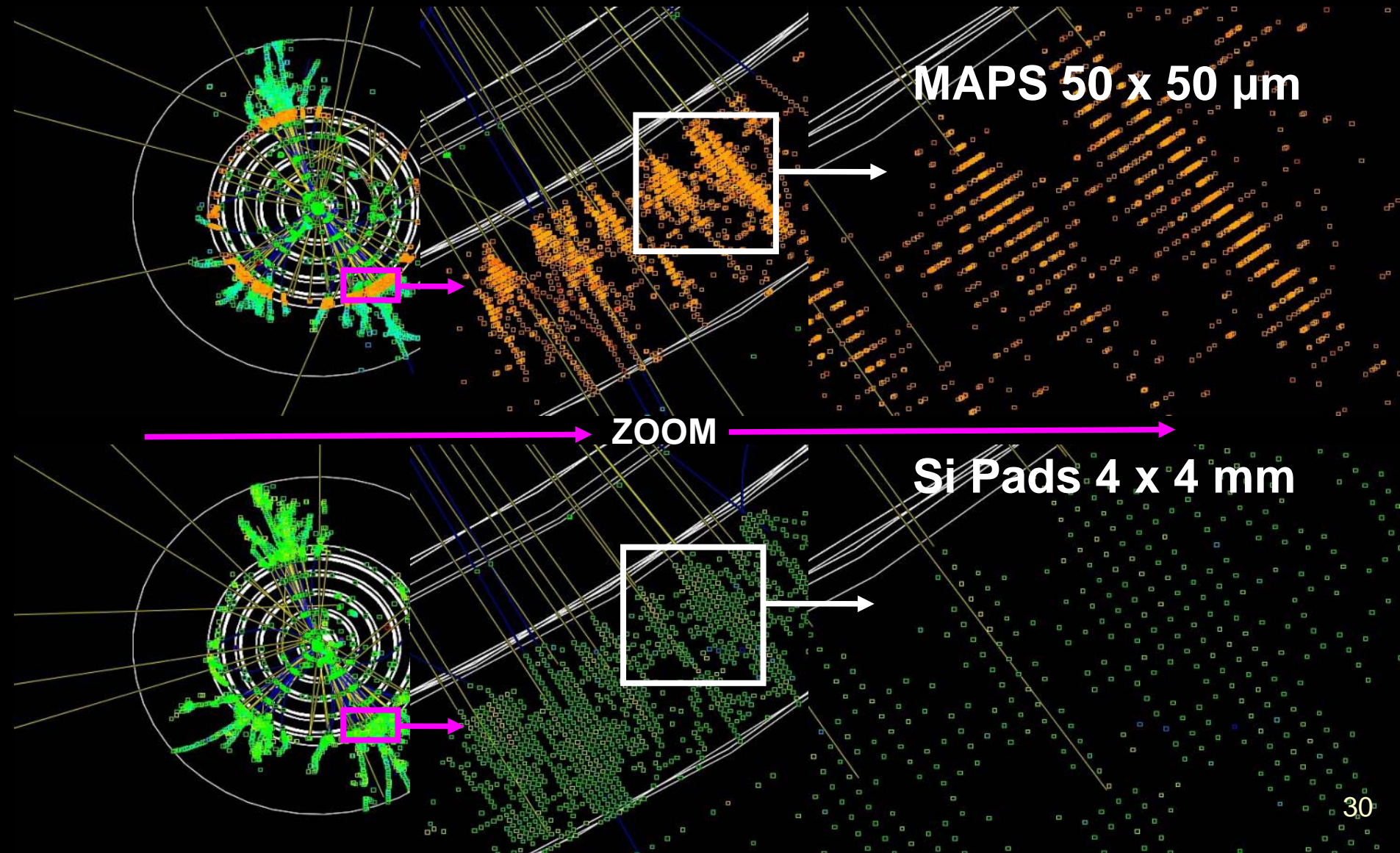
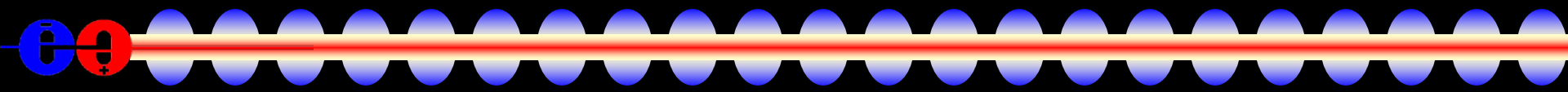


# TeraPixel ECal Option

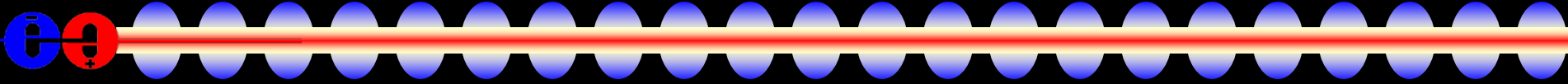


- Digital ECAL
- Operates as a shower particle counter
- Based on MAPS technology
- Deep p-well INMAPS process
- 50 x50 micron pixels
- First generation sensor TPAC1 has been manufactured
- 168x168 pixels, 8.2 million transistors
- Testbeam data with small chip
  - DESY & CERN
- In the process of analyzing

# MAPS Shower Simulations



# *ECal Status*

- 
- Steady technical progress with the R&D
    - 1024-channel KPiX being tested
    - Plan first system tests of the sensor+KPiX (winter 2011).
    - Close to fabricating a test stack for a beam test.
    - Compatible with schedule of SLAC test beam
  - Number of issues to settle for implementation in SiD
    - Finalize the mechanical design for the barrel.
    - System tests: cooling, power delivery, correlated noise, etc.
    - Need a tiling scheme and mech. design for the endcaps

# Digital Hadron Calorimetry: DHCAL

## Role of PFA Hadron calorimeter

- identify energy deposits belonging to neutral hadrons
- measure the energy of neutral hadrons

## Favored HCAL technology

Resistive Plate Chambers (RPCs) with very fine readout

## Development of RPCs for calorimetry

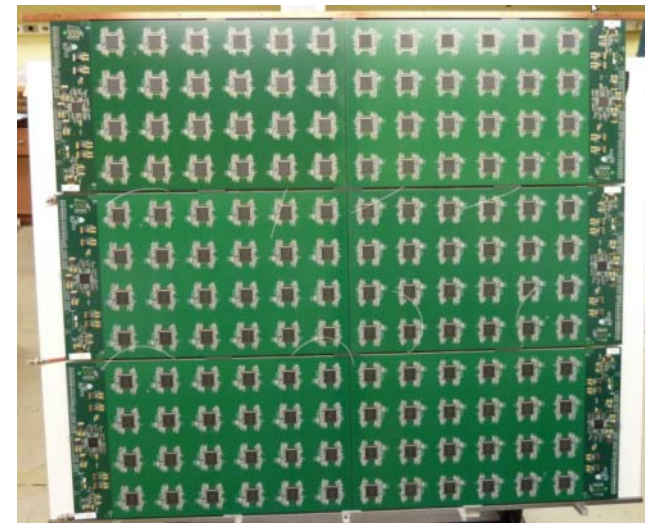
Evaluated various chamber designs  
Detailed measurements with 14-bit ADC and multiple pads  
Results published in NIM paper

## Small scale prototype built and tested in test beam

Up to 10 layers, 20 x 20 cm<sup>2</sup> RPCs with 1 x 1 cm<sup>2</sup> readout pads  
Results published in 5 JINST papers

## Technology for large scale prototype developed

Large RPCs (32 x 96 cm<sup>2</sup>) with minimal edges (very challenging!)  
Digital (=1-bit) readout based on DCAL chip (2 iterations)





# Large scale prototype built

- Produced** ~10,000 DCAL III chips (not a single design fault!!!)  
 205 RPCs  
 337 Readout boards  
 56 cassettes (with protective covers)  
 Low Voltage system (with 384 channels)  
 Gas system (with 28 separate lines)
- Borrowed** High Voltage system (with 64 channels)

**Large effort involving a total of 39 people**

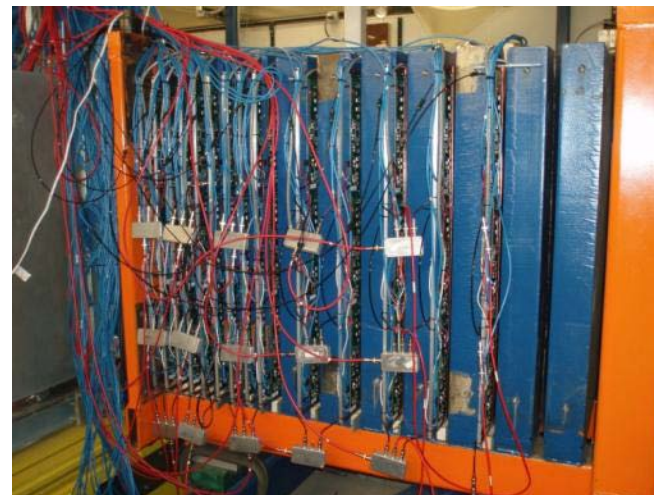
## DCHAL stack

38 layers with 350,000 readout channels  
 Inserted into CALICE AHCAL structure



## TCMT stack

14 layers with 130,000 readout channels  
 Inserted into CALICE TCMT structure



# Testbeam activities

Run period	Date	Configuration	Muon events [10 <sup>6</sup> ]	Secondary beam events [10 <sup>6</sup> ]	Secondary beam momenta [GeV/c]
1	Oct 2010	DHCAL	1.4	1.5	2,4,8,10,12,16, 20,25,32
2	Jan 2011	DHCAL + <b>partial TCMT</b>	1.6	3.6	2,4,6,8,10,60
3	Apr 2011	<b>ECAL</b> + DHCAL + <b>TCMT</b>	3.5	4.8	4,8,12,16,20,25, 32,40,50,60,120
4	Jun 2011	DHCAL + TCMT			32,40,50,60,120
5	Fall 2011	DHCAL with <b>Tungsten</b> + TCMT			4,8,12,16,20,25, 32,40,50,60,120
6	Later	DHCAL <b>w/o absorber</b>			0.50,0.75,1.00, 1.25,1.50,2.00
<b>TOTAL</b>			<b>6.5</b>	<b>+ 9.9</b>	<b>= 16.4M</b>



# Typical pion events at 60 GeV/c

## Note:

These are typical events, not (too) carefully selected

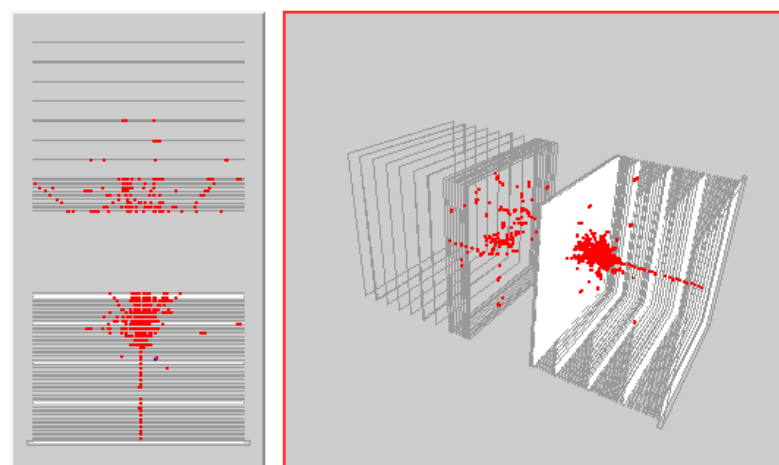
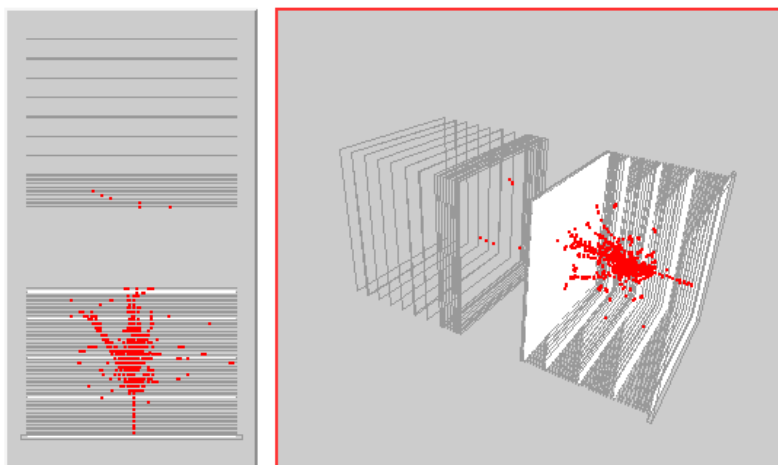
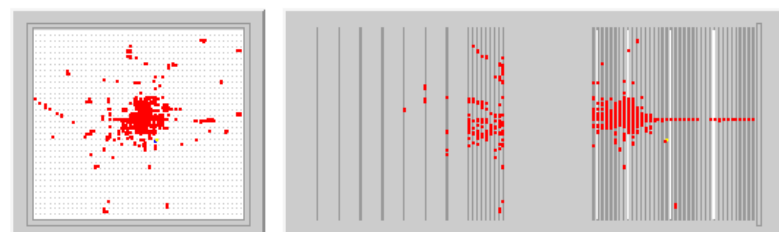
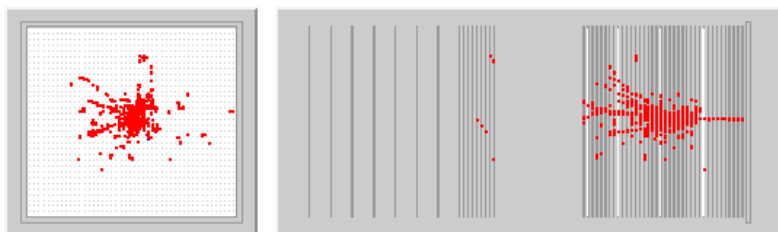
Isolated hits are not noise!

Run 996:0 Event 1055

Time: 6471452  
Hits: 766 Energy: xxx mips

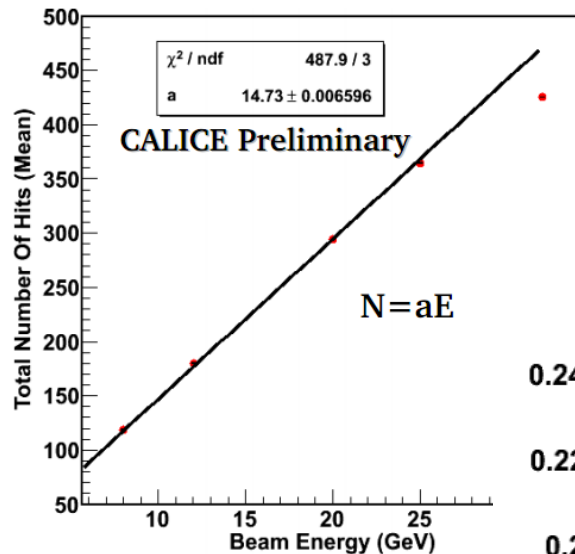
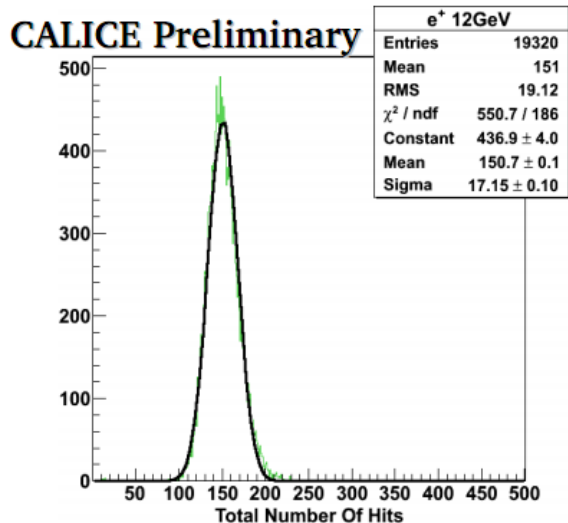
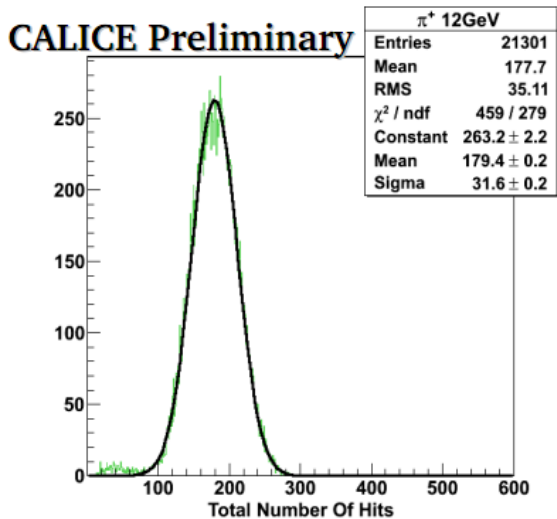
Run 996:0 Event 1076

Time: 8443481  
Hits: 794 Energy: xxx mips



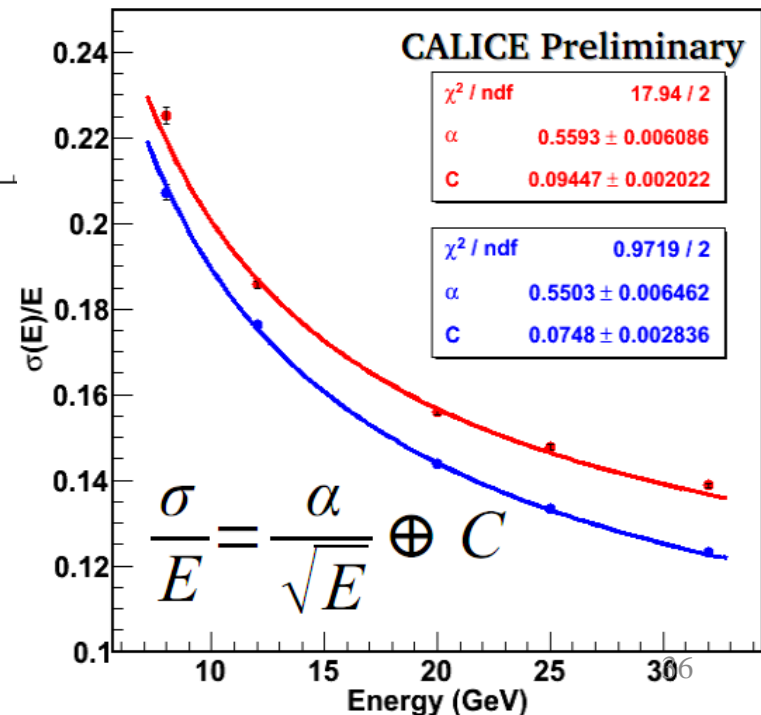
# Results from Analysis of Secondary Beam Events

Example -  $p = 12 \text{ GeV/c}$



Response to pions

32 GeV/c not included in fit  
 Without cut on containment  
 With cut on containment



# Preliminary results from test beam

## Noise rate

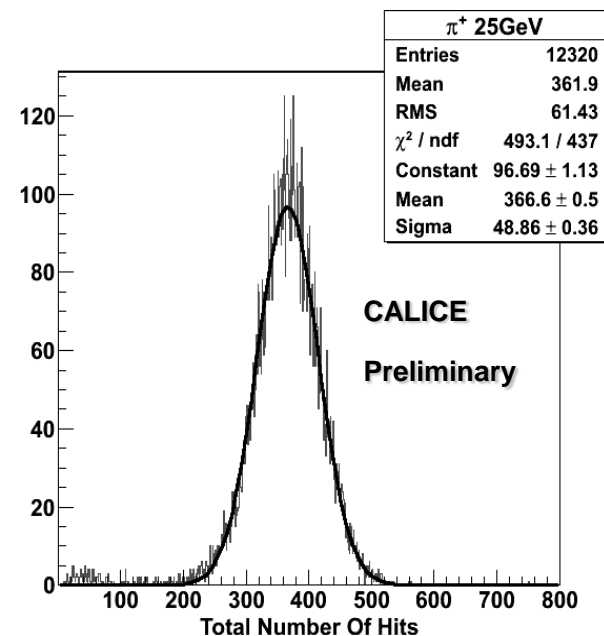
Higher than anticipated, due to elevated temperature  
 Noise rate corresponds to 0.1 Hits/(triggered event) in the DHCAL +TCMT  
 Still ~negligible

## Muon calibration

Many analysis ongoing...  
 Average efficiency = 93.6%, pad multiplicity = 1.56, as expected  
 Alignment of layers, calibration and simulation of response in progress

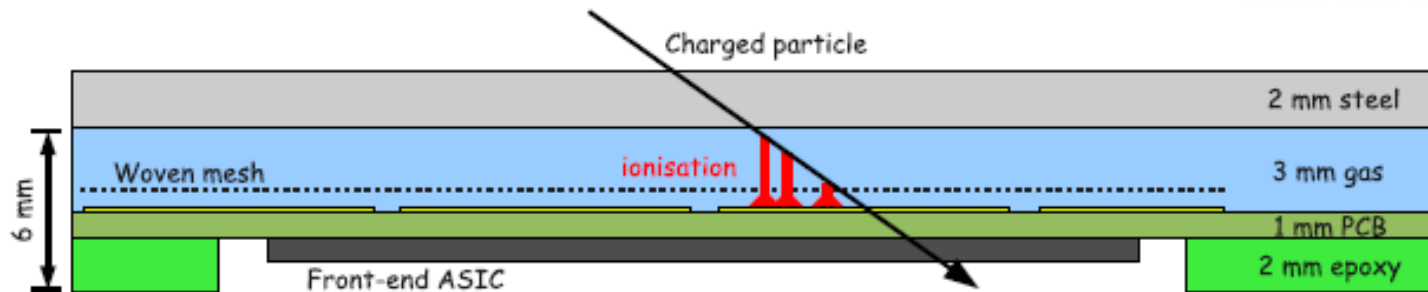
## Positron/pion analyses

Many topics to be covered...  
 Response to both positrons and pions similar to expectation from previous simulation work



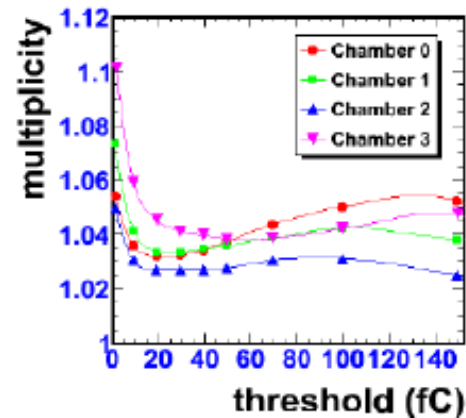
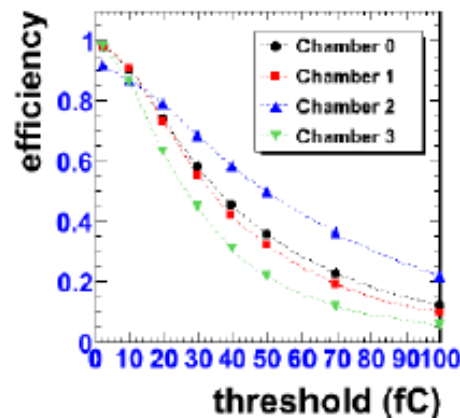
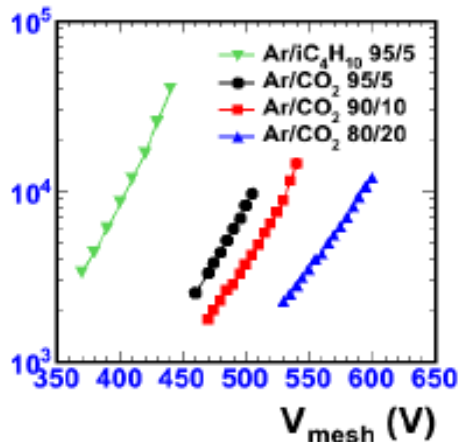
**The concept of a DHCAL with RPCs  
 is close to being validated**

# Micromegas-DHCAL

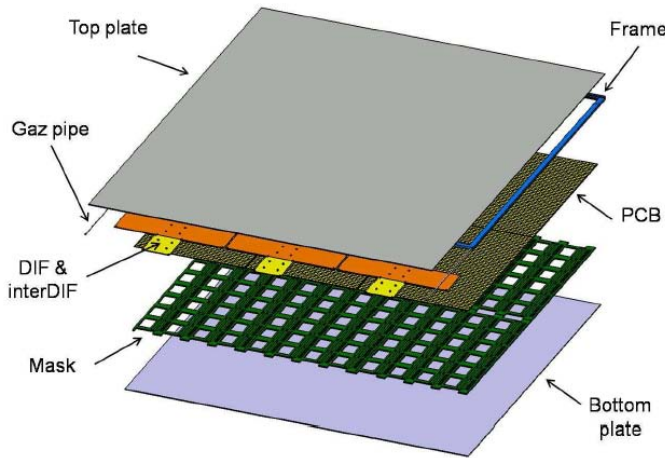


## ■ MICROMEAS for a DHCAL:

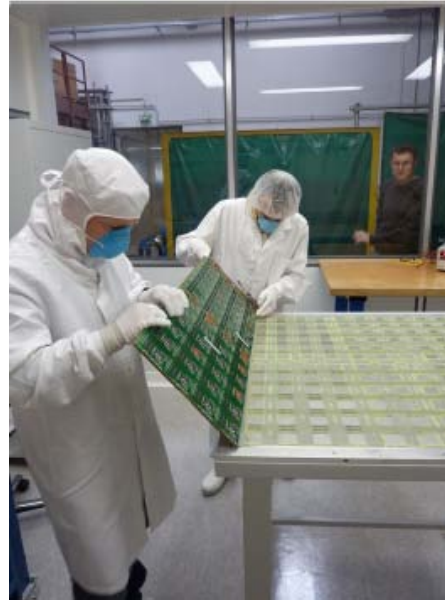
- fast, radiation hard, good aging properties, robust, large area, high gas gain, spark proof, standard gas mixture (Ar,  $iC_4H_{10}$ ,  $CO_2$ )
- small avalanche charge → sensitive front-end electronics



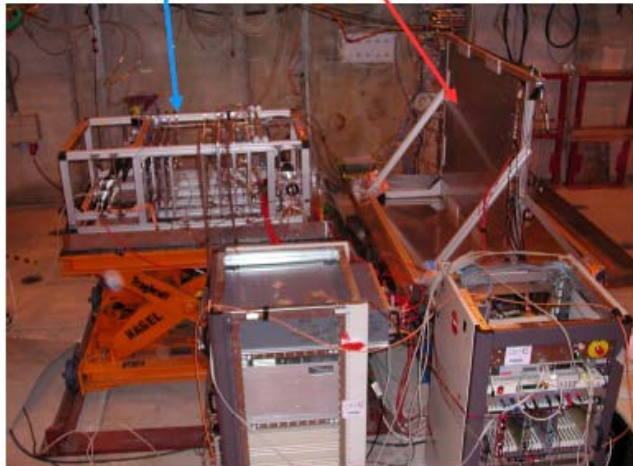
# Micromegas-DHCAL



After 1 week the 1 m<sup>2</sup> is fully assembled!



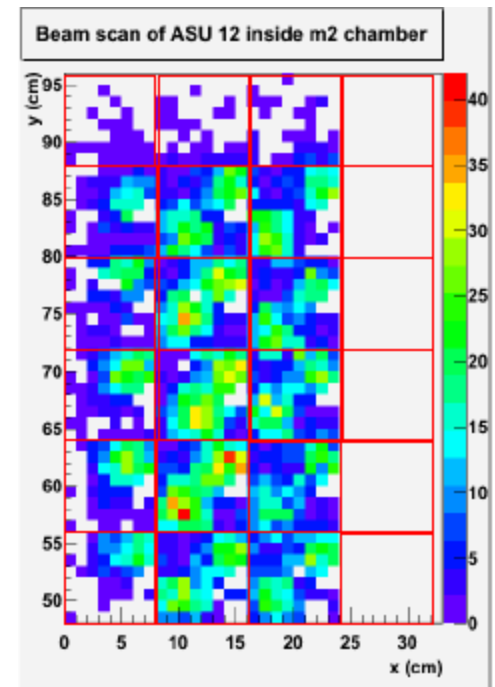
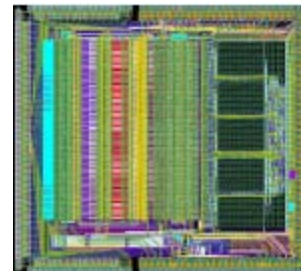
Design for 1m<sup>2</sup>  
Telescope 1m<sup>2</sup> prototype



SPS/H4 beam

- 4 weeks in June/July 2010
- 150 GeV/c muons and pions

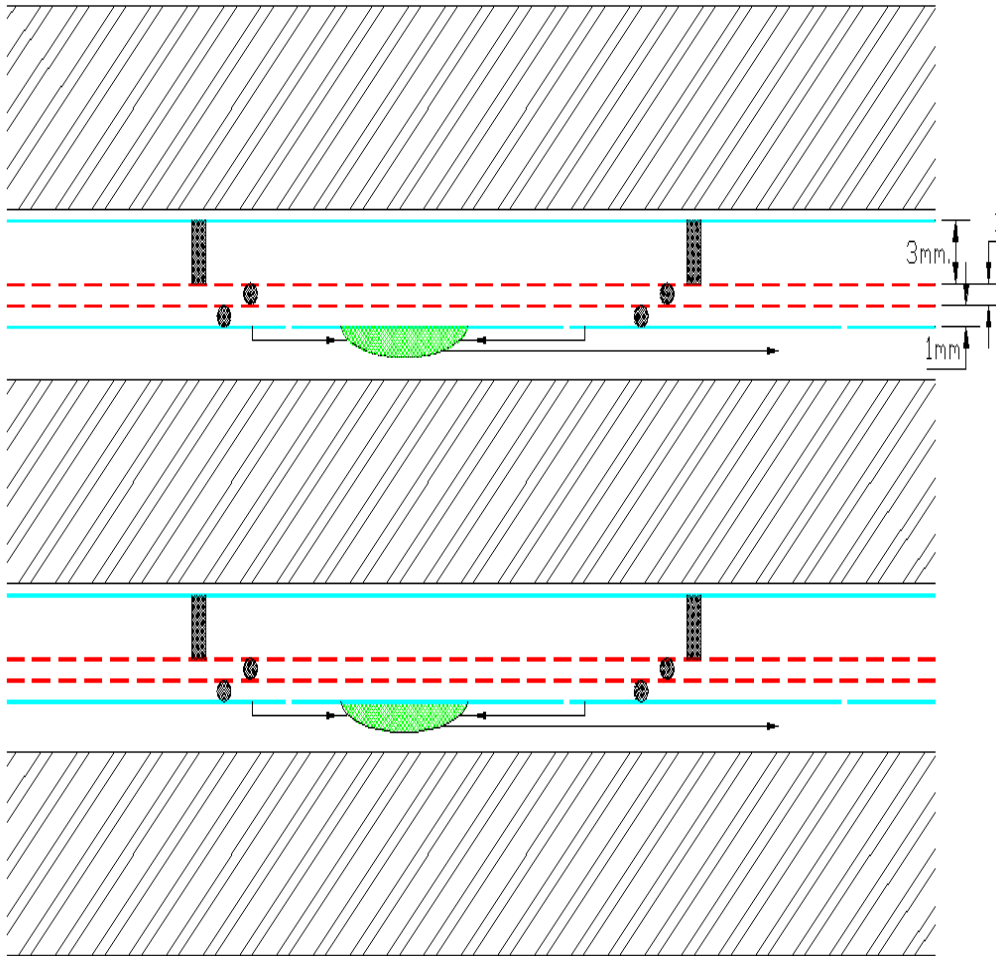
Low efficiency - non-optimal electronics



New readout chip MICROROC  
Development with LAL/OMEGA  
Shaping time matching the detector signal duration

# GEM/DHCAL active layer concept

## GEM-BASED DHCAL CONCEPT



NOT TO SCALE

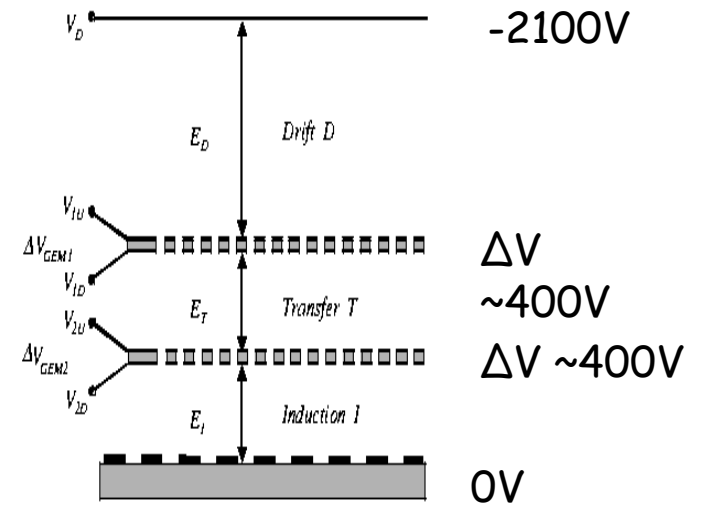
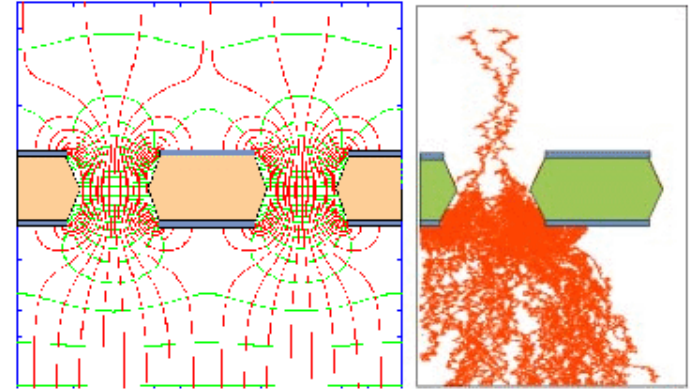
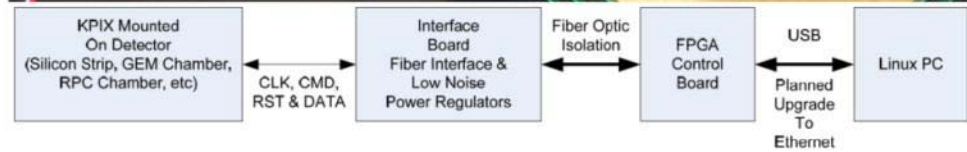
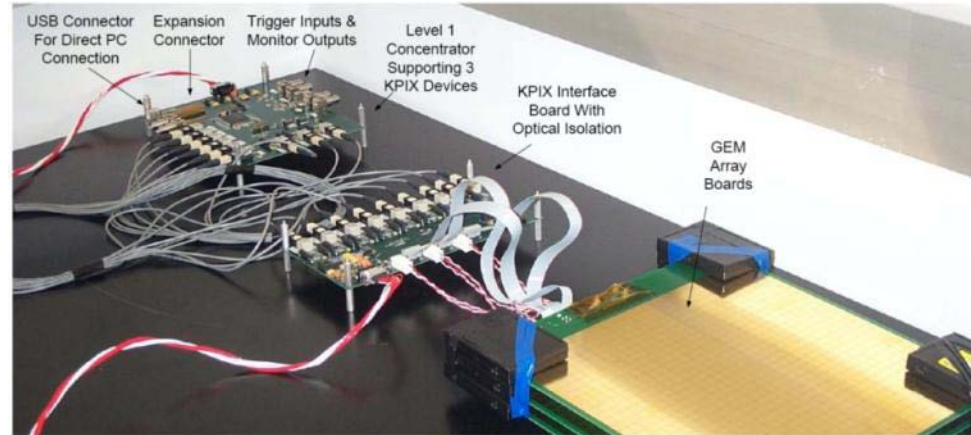
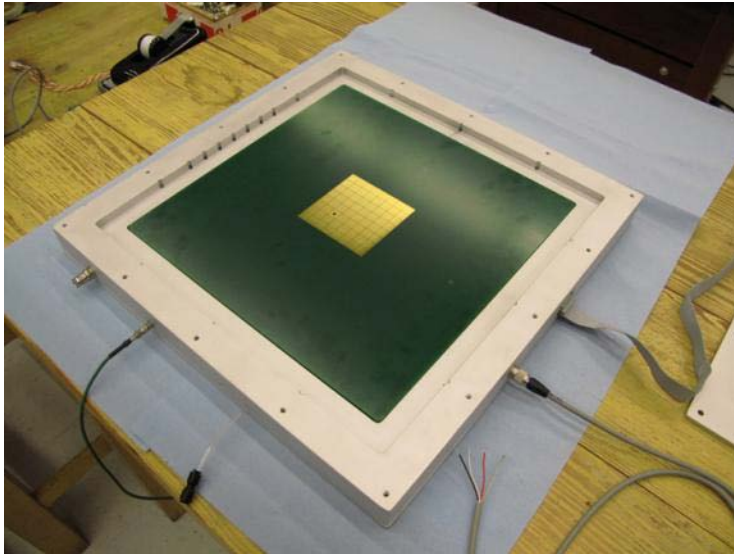


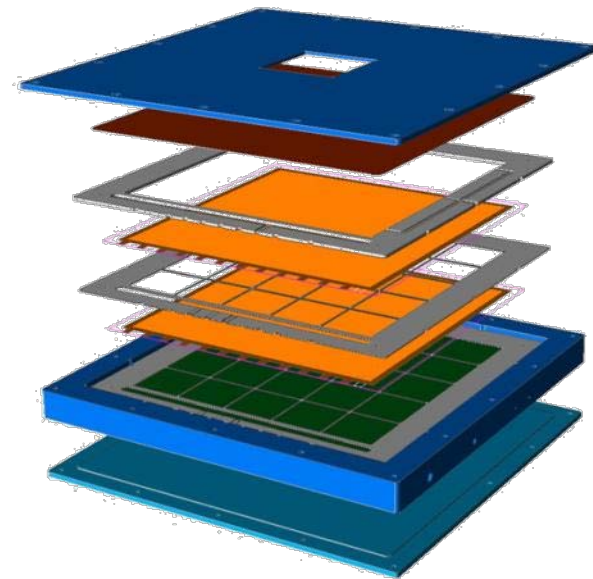
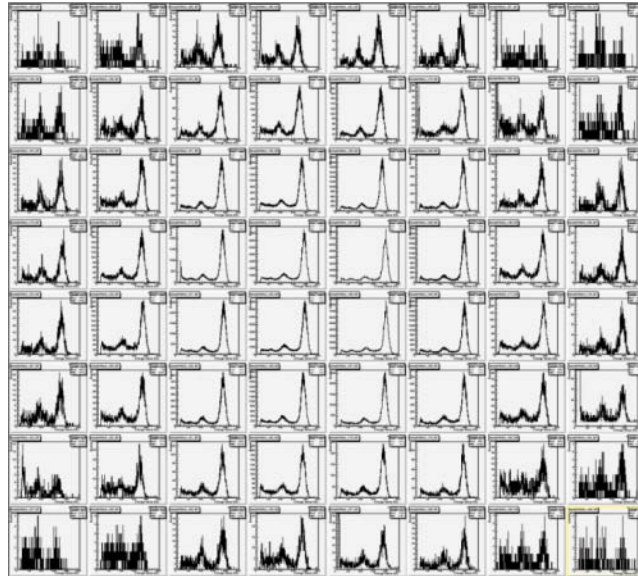
Fig. 1: Schematics of a double-GEM detector.



# SiD GEM-DHCAL

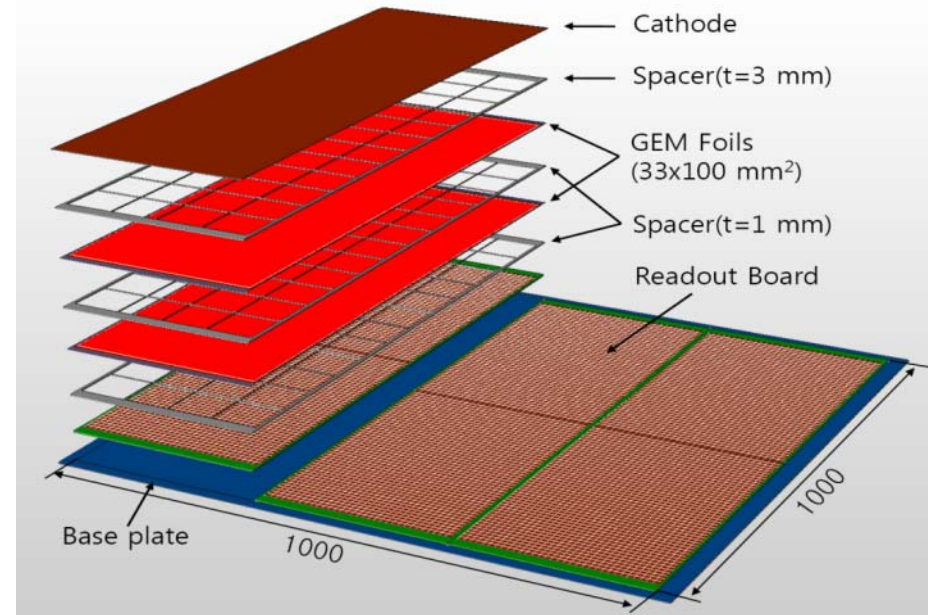


30cm x 30cm  
GEM-DHCAL  
prototype



# UTA's 100cm x 100cm Digital Hadron Calorimeter Plane

First 5 of 33cmx100cm GEM foils delivered early July, 2010



**Phase II** → 33cm x 100cm unit chamber characterization

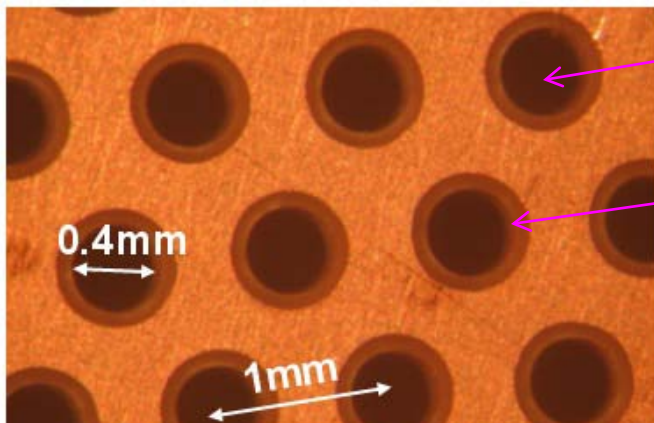
Early 2011 at MTBF: Using available KPix chips and DCAL chips

**Phase III** → 100cm x 100cm plane GEM DHCAL performances in the CALICE stack

Early 2011 - Late 2011 at Fermilab's MTBF or CERN

Five 100cm x 100cm planes inserted into existing CALICE calorimeter stack and run with either Si/W or Sci/W ECALs, and RPC planes in the remaining HCAL

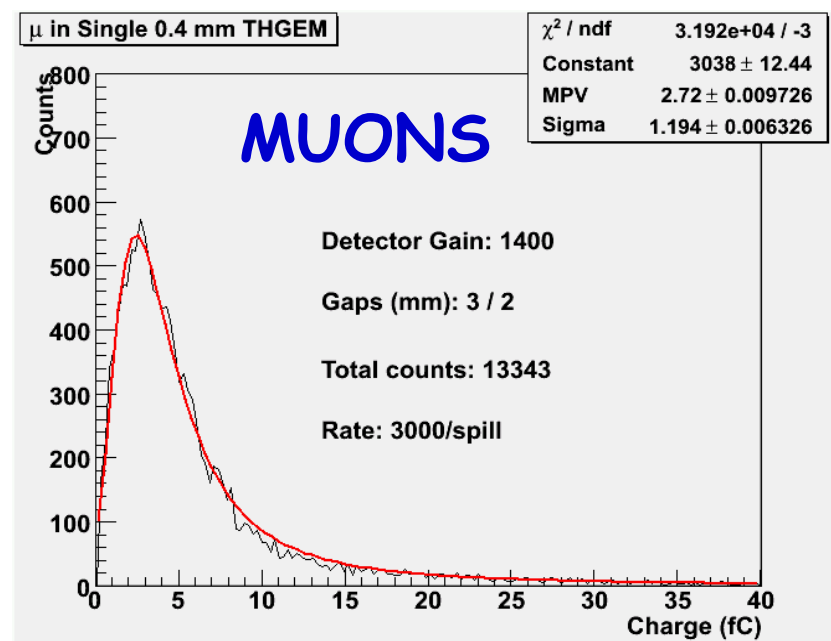
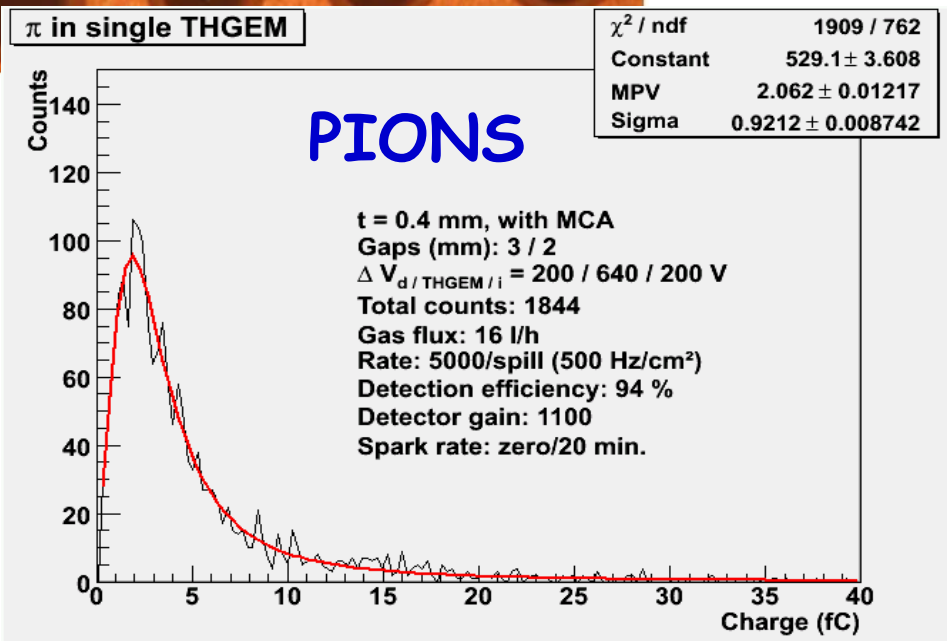
# SiD thick-GEM-DHICAL



drilled

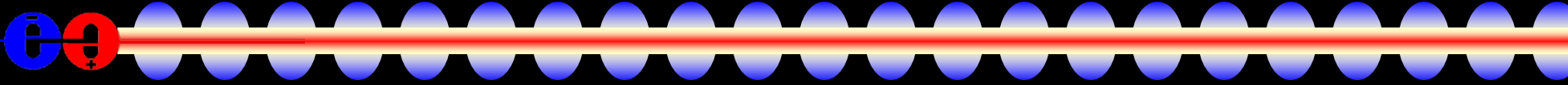
etched

- PCB Based GEM → Cost effective
- 0.5 - 1mm thick PCBs
- Drilled 0.4mm holes with 1mm pitch
- Expected to have higher gain per GEM
- 10cmx10cm tested, up to 30cmx30cm produced

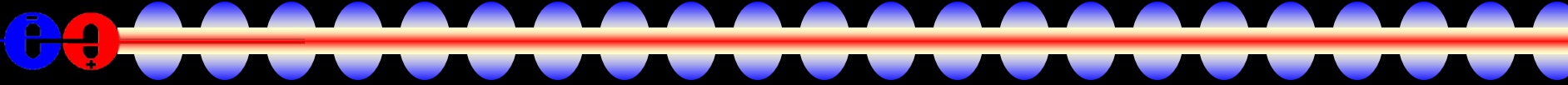


Measured very low discharge rates even with pions

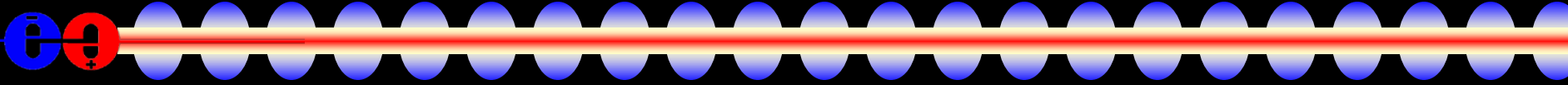
# *HCal Next Steps*

- 
- RPC option: continue with testing the 1m<sup>3</sup> stack. Calorimeter will be exposed to muons and pions and positrons of various energies. The response and energy resolution will be measured together with characteristics of hadronic showers, for Particle Flow Algorithms. R&D for Technical Prototype.
  - GEM option will test its 1m<sup>2</sup> layers as part of the CALICE hadron calorimeter prototype, and will design and build a complete, integrated layer with minimal thickness and full services. Thick GEM prototypes will also be assembled and tested as large sections of thick GEMs become available. Gas studies for thick GEMs will also continue.

# *HCal Next Steps*

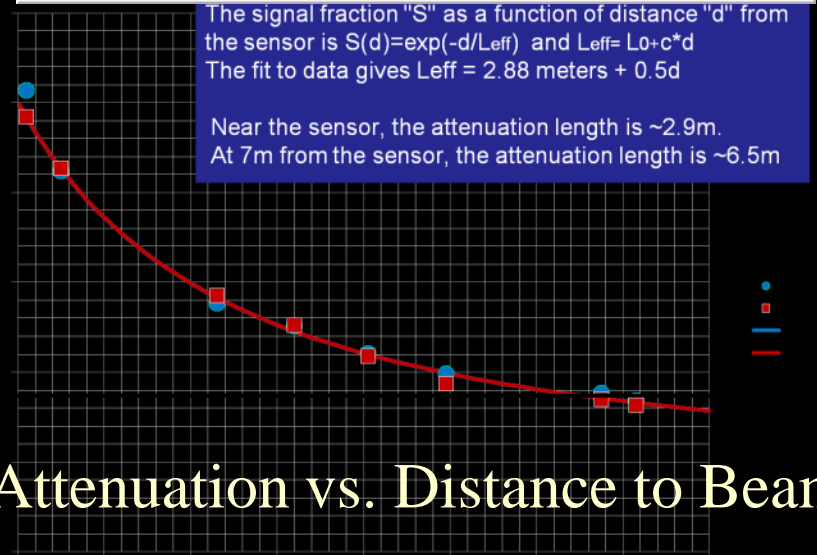
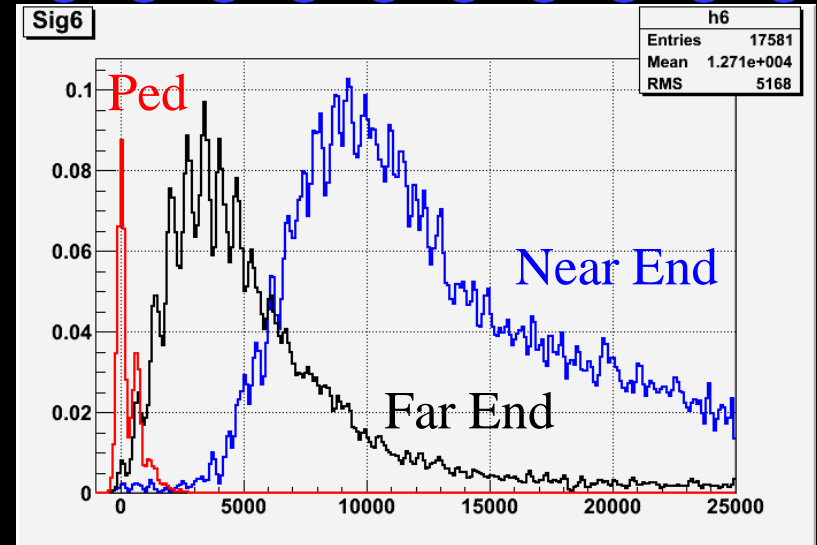
- 
- Micromegas option : Test of the  $1\text{m}^2$  chamber in the W-structure with AHCAL CERN PS T9. Objective: – First comparison between  $1\text{cm}^2$  pad Micromegas and  $3\text{cm}^2$  scintillating tile layers
  - Scintillator/SiPM option\* : insertion of the integrated readout layer planes fabricated with the CALICE/EUDET electronics into the CALICE absorber stack. Followed by the commissioning and exposure of this prototype to a test beam.
  - Homogeneous dual-readout calorimetry\* : development of suitable crystals, photodetectors, and associated readout electronics, all in preparation for a demonstration of linearity and energy resolution for hadrons in a test beam, while developing a conceptual design for inclusion of this technology into SiD.

# *Muon System RPC Studies*

- 
- Babar Forward Endcap RPCs
    - H. Band, U. Wisconsin
  - Similar construction to Atlas/CMS RPCs
  - Wide range of rates/current accumulated over ~ 6 years
  - Good overall efficiency but clear signs of aging
  - RPC readout with KPix
  - BESIII/Daya Bay RPCs
    - C. Lu Princeton U.
  - No linseed oil
  - Accelerated aging studies
    - with  $^{60}\text{Co}$
    - Sizable efficiency losses
    - Damage from to HF produced in gas
    - Testing linseed oil impregnated Bakelite
    - Developing thin Bakelite for possible use in HCAL

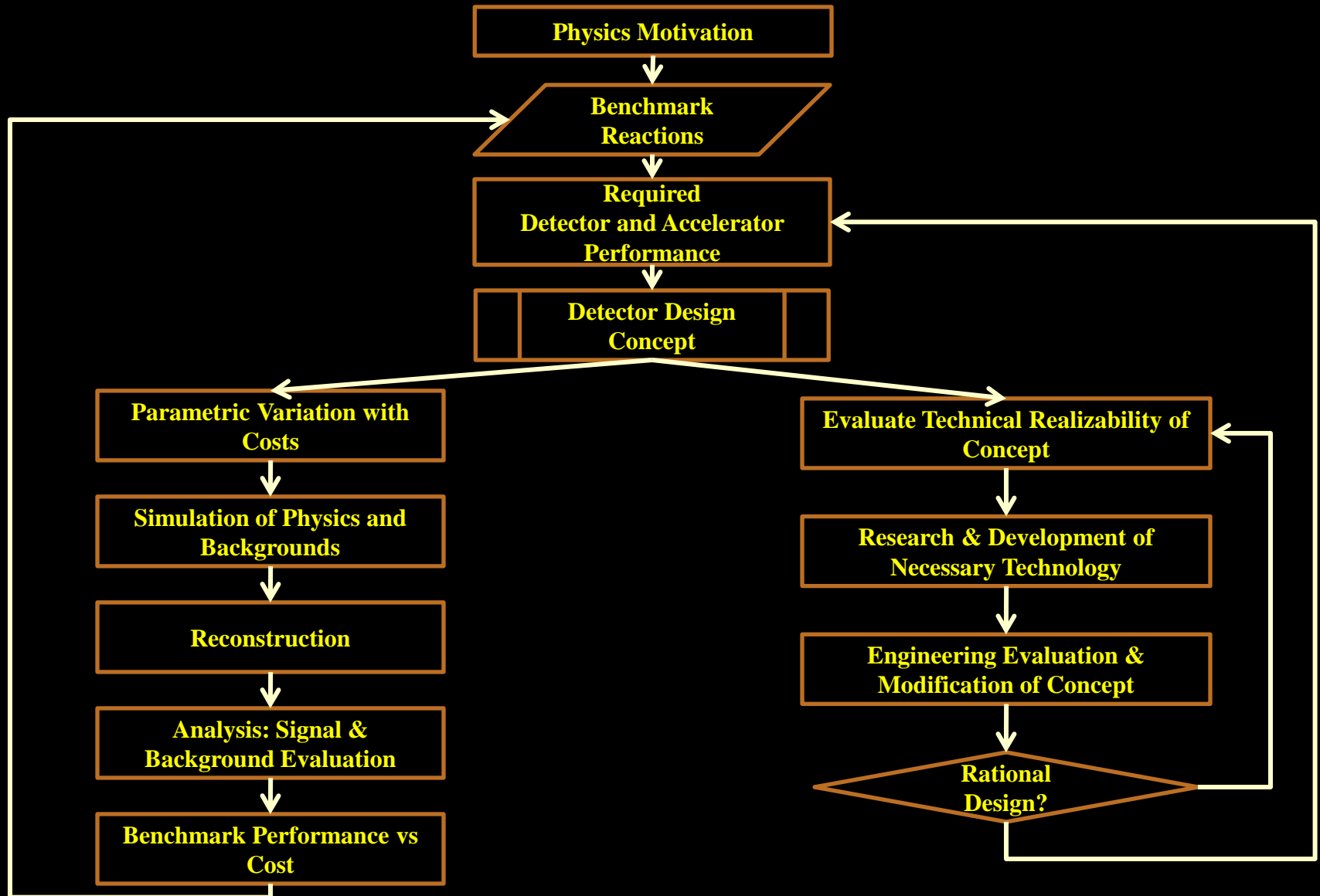
# Muon System Scintillators

- Alternative baseline
- Double scintillator strip, read out with SiPM with integrated wave form digitizer (212 MHz)
- T-995 Beam Tests at Fermilab MTBF
- SiPM making huge progress



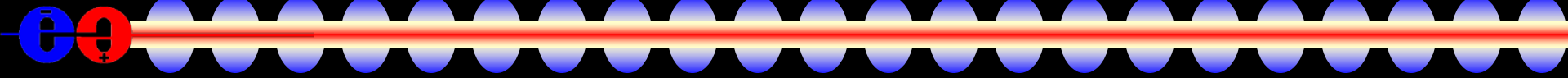
Attenuation vs. Distance to Beam

# Detector Development Process



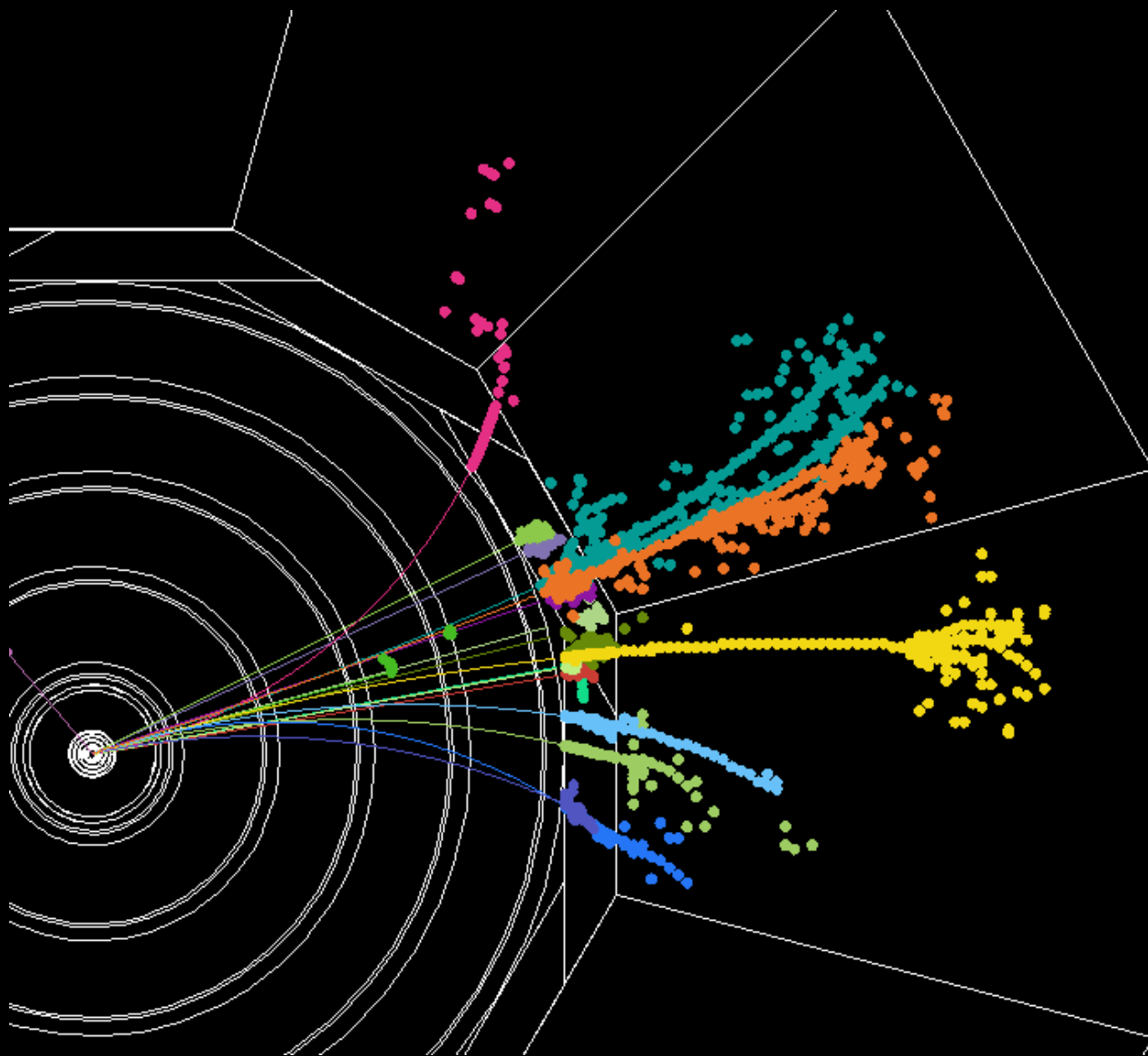
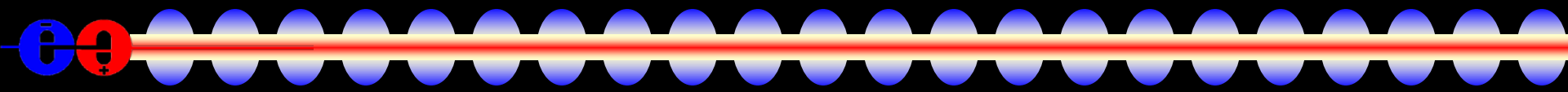


# Simulation & Reconstruction



- **SLIC provides full detector simulation in Geant4**
  - runtime detector description in XML
  - stdhep input
  - standard LCIO output
- **org.lcsim reconstruction/analysis suite**
  - Java-based reconstruction & analysis framework
  - full, *ab initio* signal digitization, track finding & fitting, calorimeter cluster finding and association (PFA)
  - LCIO provides access to global LC code base
    - flavor-tagging via LCFI
    - PFA via Pandora
  - AIDA histogramming and fitting
  - WIRED 3-D event display

# Reconstruction



# *The Silicon Detector Concept*

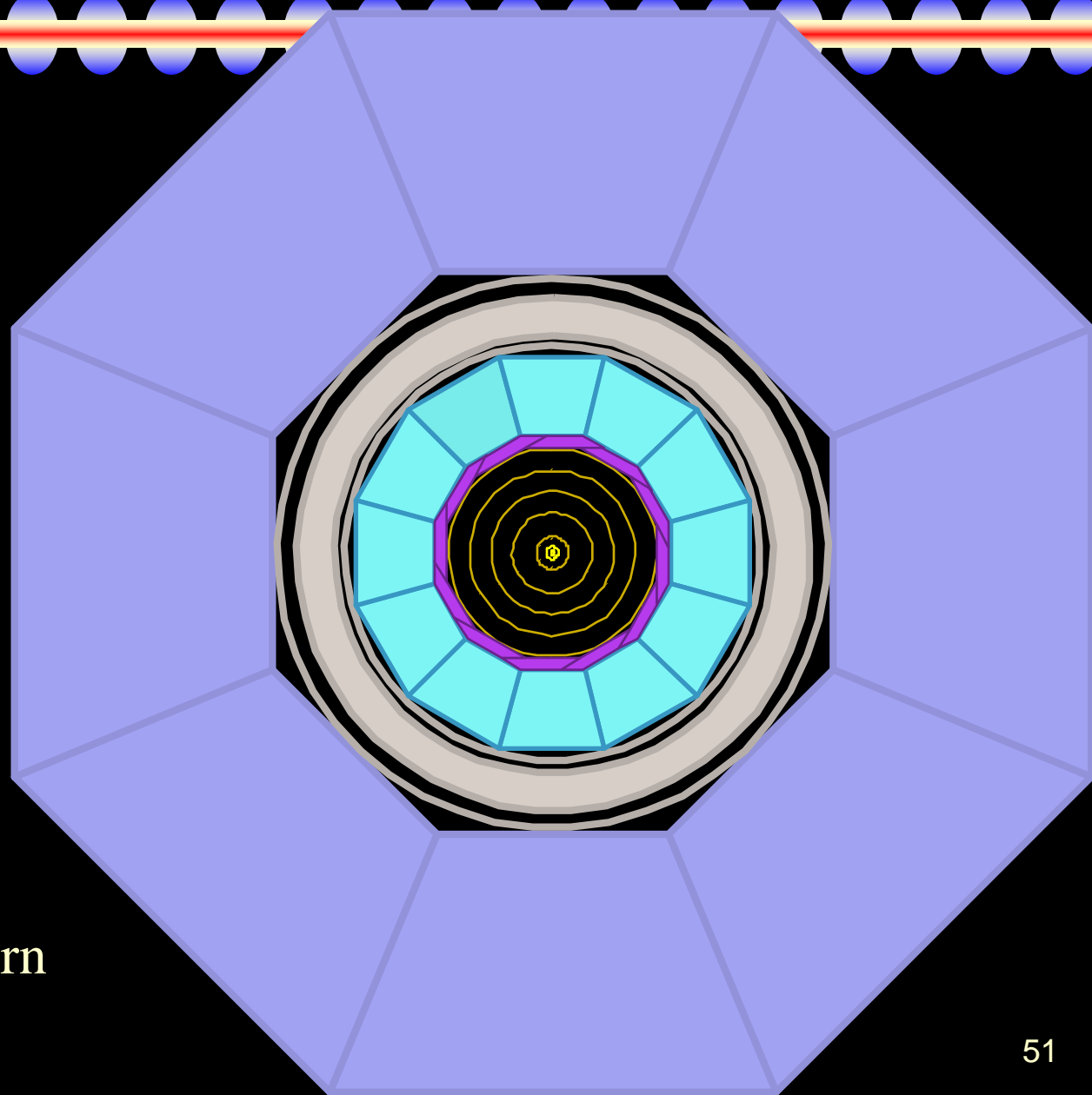
Integrated tracker

Si/W ECal

Steel / RPC HCal

5T Solenoid

Self-shielding  
instrumented flux return  
Muon System



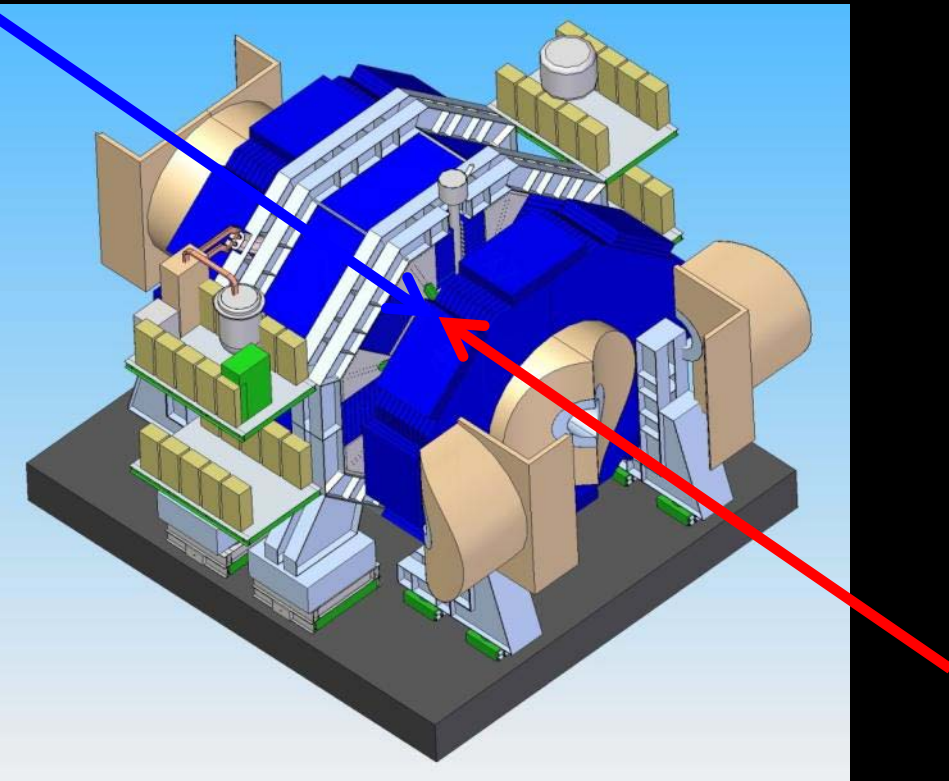
# The Silicon Detector Concept



# Installation & Push-Pull

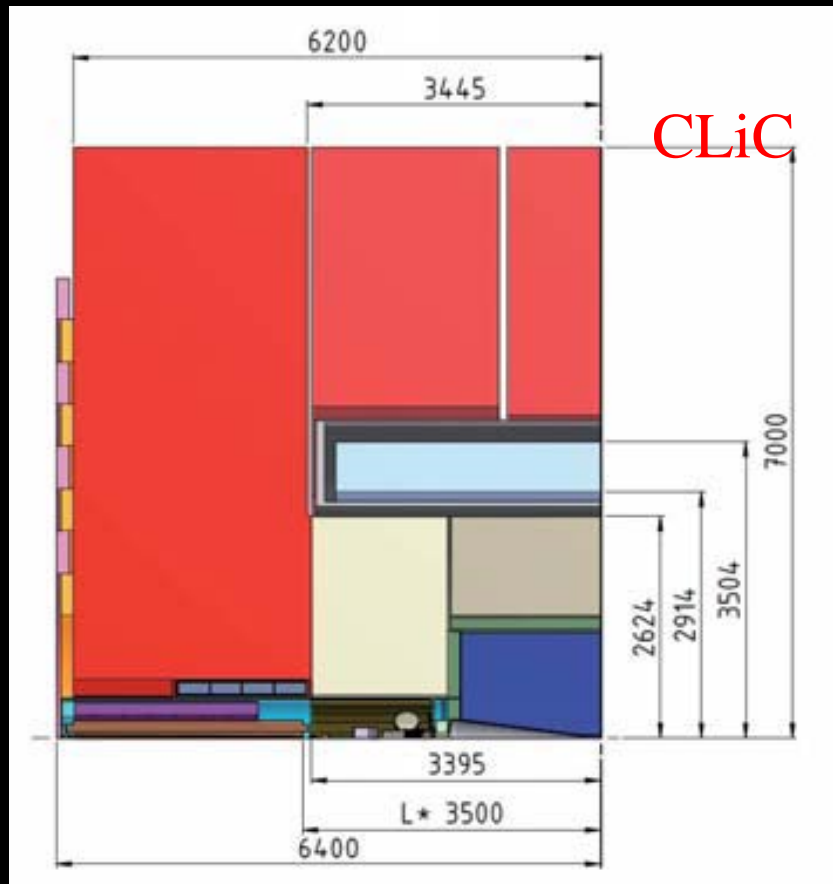


- ILC & CLiC envision two detectors sharing a common interaction region.
  - Luminosity sharing is accomplished via “push-pull” with detectors on movable platforms.
- SiD is studying functional requirements for the interaction region, associated access shafts, and significant surface facilities for a deep vertical access site; and is beginning studies for a horizontal access site.

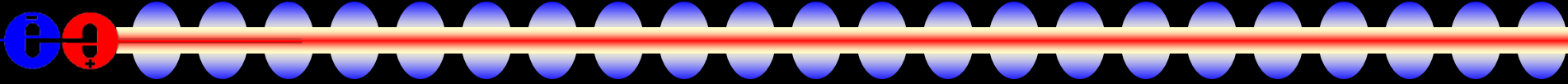


# SiD @ CLiC

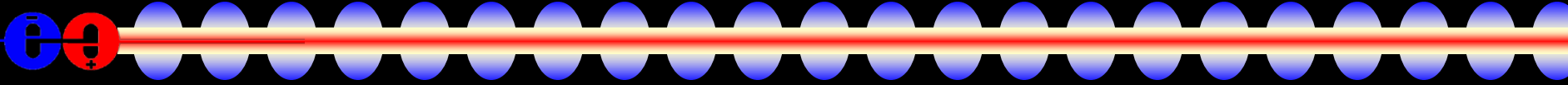
- Conceived for the NLC, optimized for the ILC, but also adapted for CLiC.



# *The Path to 2012*

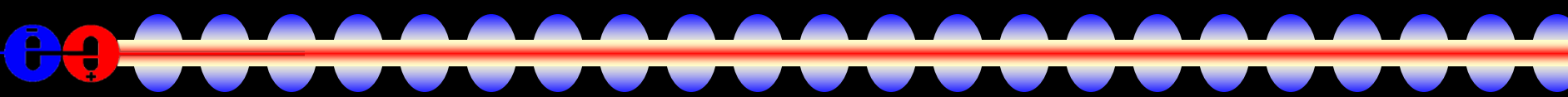
- 
- Focus and goal for SiD is the Detailed Baseline Design of the detector for 2012.
  - The ILC Letter Of Intent exercise was a significant milestone. Since then we have continued R&D for all subsystems.
  - Ongoing work in all subsystems, but each on its own timeline – aiming for convergence by 2012, but it is clear that R&D will continue beyond this point.
  - Apologies to all excellent efforts not mentioned.
  - Developing more realistic detector description – folding in increasing realism in subsystem elements.
  - Mutually beneficial cooperation and collaboration with CLiC detector group on SiD’.

# *Strategy for future Lepton Collider Physics/Detector Studies*

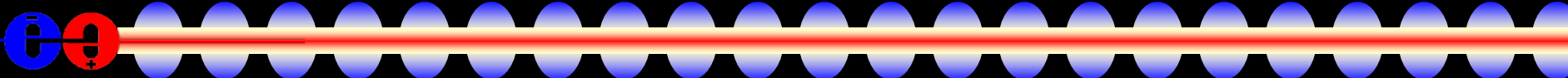
- 
- Five HEP labs presented DOE HEP with a “White Paper on US Strategy for Physics and Detectors at Future Lepton Colliders” at the HEP Electron Program review in 2010
    - Urged support for continued studies of the physics and detectors at lepton colliders, suggesting what studies were appropriate, and proposing in general terms how to proceed
  - They noted that the desired energy reach is still uncertain, and listed several candidate machines at different stages of development, ILC (mature), CLIC (evolving), and the Muon Collider (MuC) (nascent) with different energy capabilities.
  - They also noted that an even-handed comparison of these different options would educate the whole HEP community and prepare it for a rational choice in the future Snowmass 2013 clearly represents such an opportunity



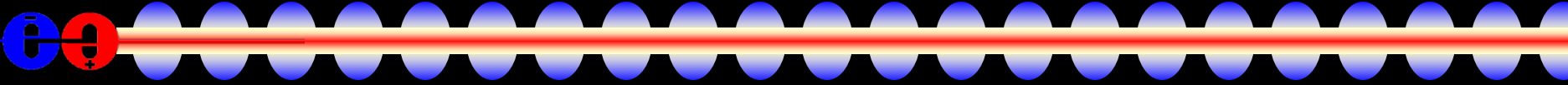
# *Lepton Collider Framework Proposal*

- 
- Goal: Establish the physics capability for energy frontier lepton colliders
  - LCFP will coordinate studies needed to reach that goal
    - Define and compare the physics potential for Lepton Colliders with a common benchmarks and simulation tools
    - Evaluate machine backgrounds and their impact on physics capabilities
    - Provide feedback to the machine designs
    - Support developing detector concepts for Lepton Colliders
    - Provide a common simulation framework
    - Establish a list of critical R&D required
    - Coordinate Lepton Collider related detector R&D as part of a national generic R&D program

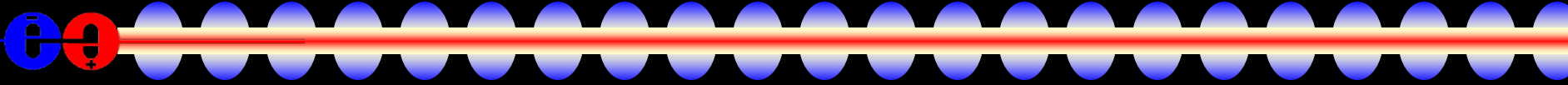
# 2012 and Beyond

- 
- LCDRD developed in response to current University Detector R&D Program (SiD/Oregon) funding ending at end of 2011. Continuation and extension.
    - Support all Lepton Colliders: ILC, CLIC, MuC
    - Support detector concept development
    - Identify R&D critical for concepts and initiate it
    - Finish up ILC R&D, start CLIC R&D, identify needed MuC R&D
    - Support the lcsim simulation infrastructure for detector studies .
  - SLAC submitted (after internal review) consortium proposal combining 14 individual proposals on March 18, 2011.
    - After DOE establishes funding level for Consortium, Review Board will set funding levels consistent with DOE guidelines
    - Annual reviews and solicitations of new proposals; annual reports to DOE.
  - Need a common simulation framework to support physics and detector studies
    - SLAC & Fermilab will submit a joint proposal to DOE to enhance LCSim physics and detector response capabilities and provide community support

# The way forward

- 
- Open-ended detector R&D is, however, in the long-term not sustainable.
    - Need a project to provide the stimulus for integrated system design and a timeline for construction.
    - The biggest disadvantage for a continued viable detector R&D program is the fact that there is no construction timeline for the ILC, CLiC, or MuC.
  - SiD presents a viable, credible concept which could be quickly (for HEP) realized.
    - [SiD meeting at SLAC, Dec. 14-16, 2011.](#)
  - Waiting on LHC discoveries...

# *Make No Little Plans*



Make no little plans. They have no magic to stir men's blood and probably themselves will not be realized. Make big plans; aim high in hope and work, remembering that a noble, logical diagram once recorded will never die, but long after we are gone will be a living thing, asserting itself with ever-growing insistency. Remember that our sons and grandsons are going to do things that would stagger us. Let your watchword be order and your beacon beauty. Think big.

*Daniel Burnham*