TPC in A JSPS Grant in Aid (Tokubetsu suishin)

TPC requirements in ILC

What we had proposed and what we obtained

1 Module(detail -> Yonamine's talk)

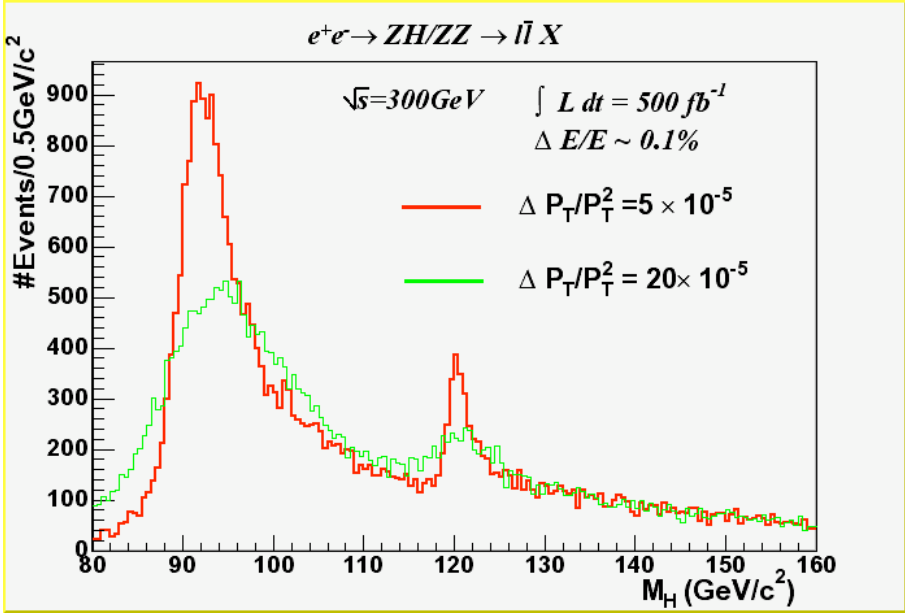
2 Gate,

3 Adv.EndPlate(detail -> Fusayau's talk)

What we will do

schedule

Requirements to TPC from ILC



Good momentum resolution for high Pt tracks

Missing mass resolution @ Higgs shtrahlung

$\sigma/P_T \sim 5 \times 10^{-5} P_T$ (with VTX)

$1 \times 10^{-4} P_T$ (TPC only)

100um spatial resolution

over large volume(200hits)

calibration system under

non-uniform field

high $\omega\tau$ gas in strong B field

Good tracking efficiency for PFA

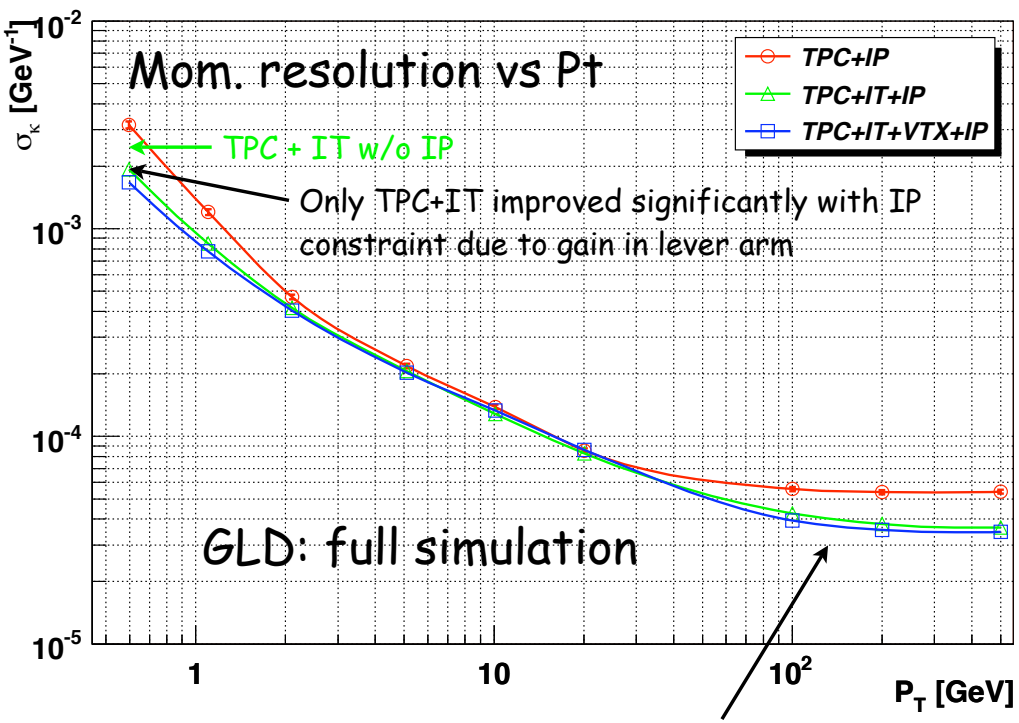
2 track separation

robust tracking system

dead region

many/fine pitch readout

maximize sensitive area



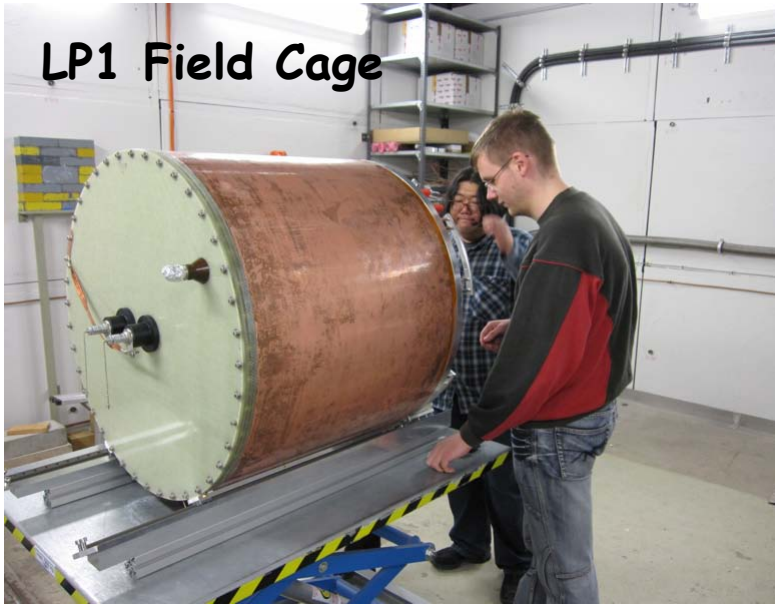
Low material budget for outer detector

thin Field Cage honey comb base cylinder(DESY)

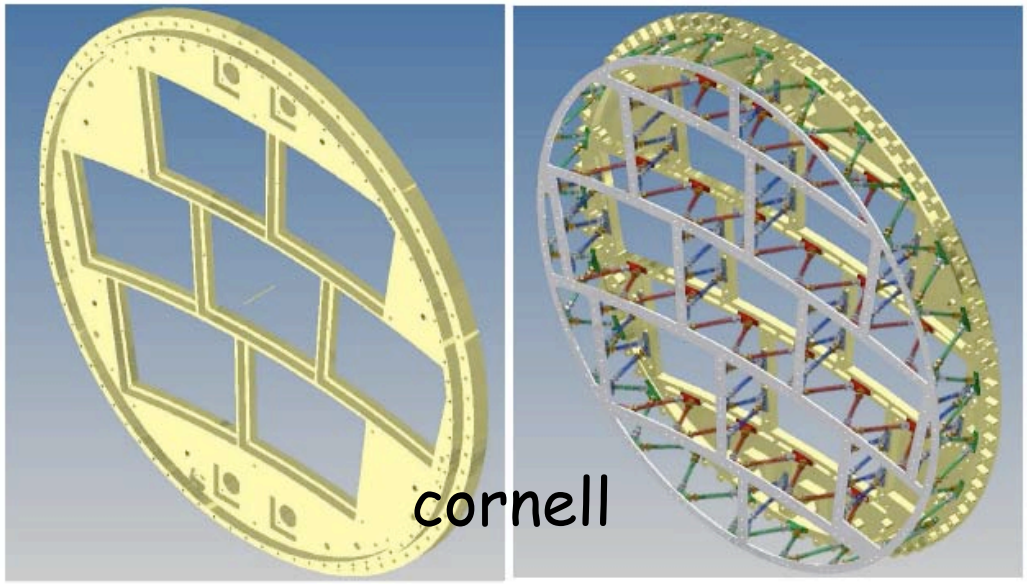
light End Plate space frame (Cornell)

compact readout system w/ cooling

ASIC + 2PCO2



LP1 endplate



Middle size module structure

~25x17 cm2

easy to handle

Durable to Background

low Z material

less Hydrogen for neutron bkg

fast drift gas

shut ion back-flow

CF4 quencher instead of CnHm

Gate device

R&D is organized under LC-TPC collaboration

Phase 1

"proof of principle" phase
study/demonstrate performance
using small test chamber

Phase 2

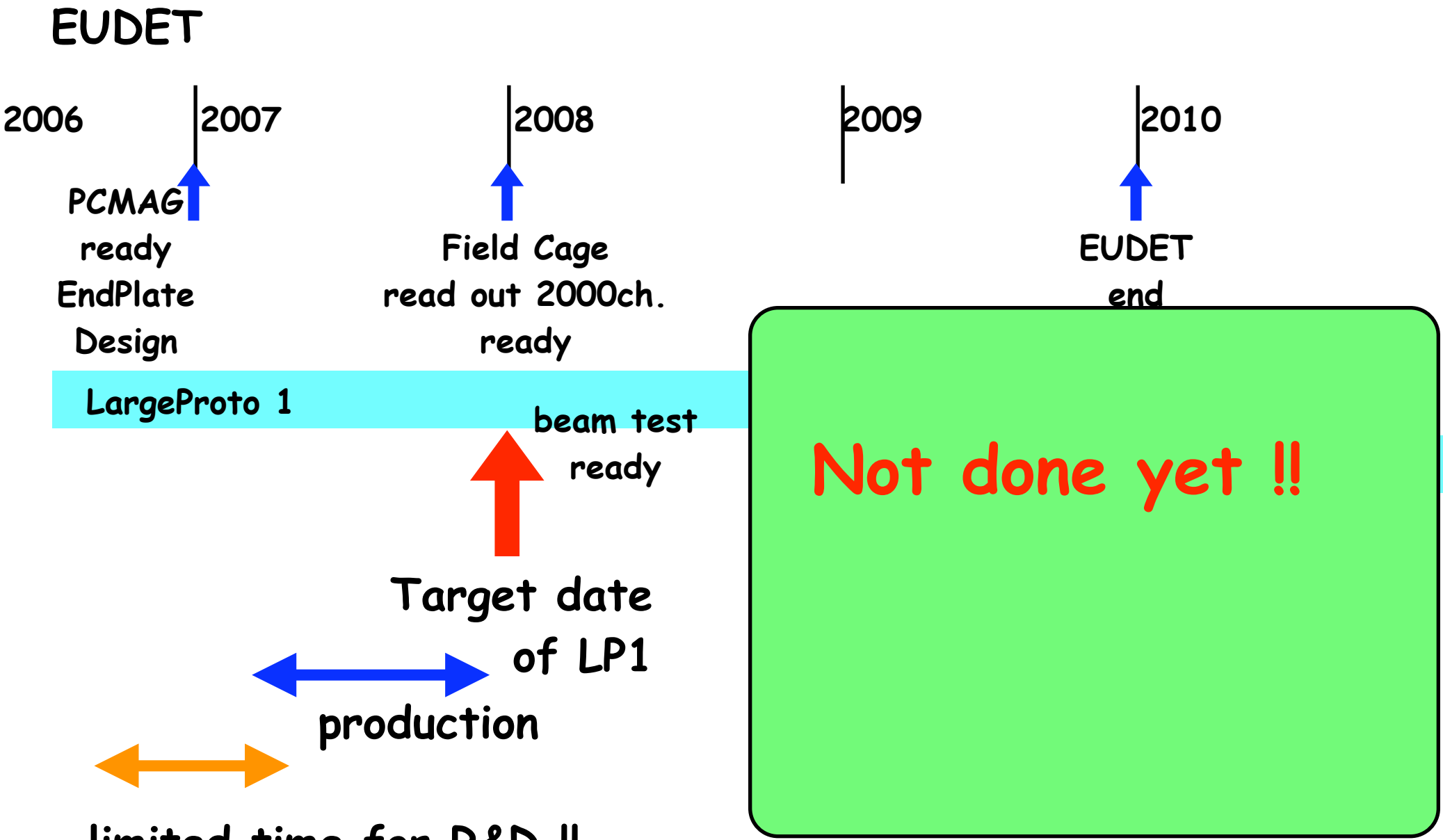
"consolidation" phase
demonstrate performance with
realistic
"large" size prototype

Phase 3

"design" phase
design real TPC for ILC exp.

Large Prototype test
using common FC/EP
test facility (EUDET@DESY)

Our schedule@2006



Concept of Asian GEM module LP1

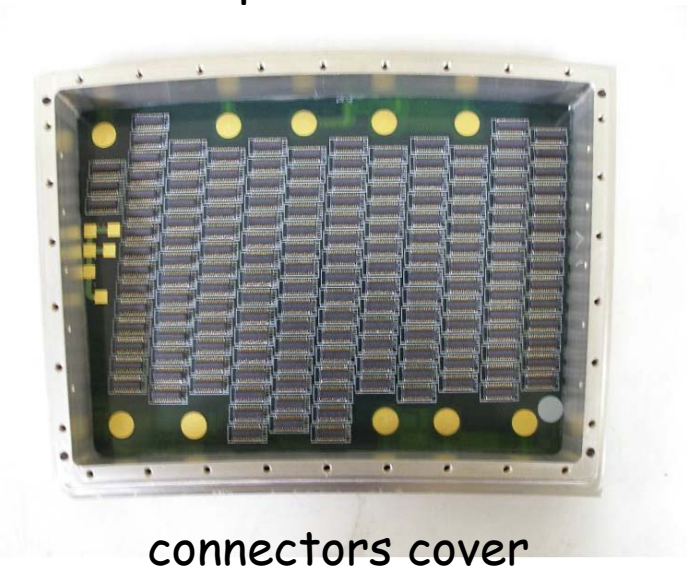
Pad plane (w/ Tsinghua U.)

pad pitch ~1.1mm

pad height ~5.5mm

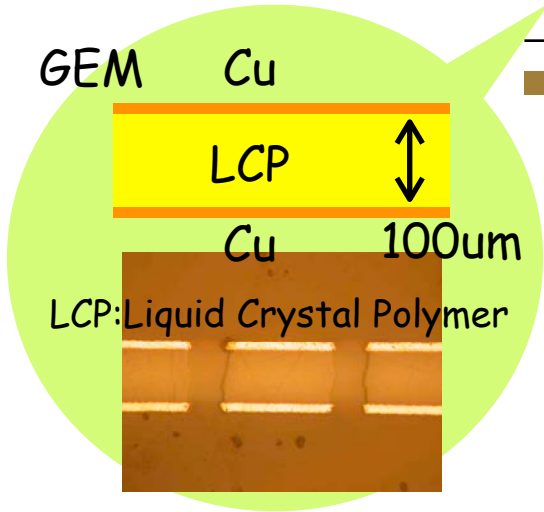
by ~300um diff.@amp.GEM

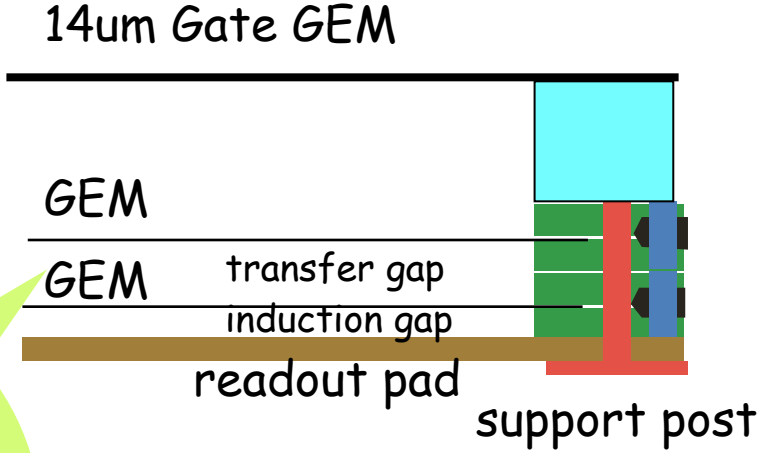
~5000 pads/module



connectors cover

most of the area in backside

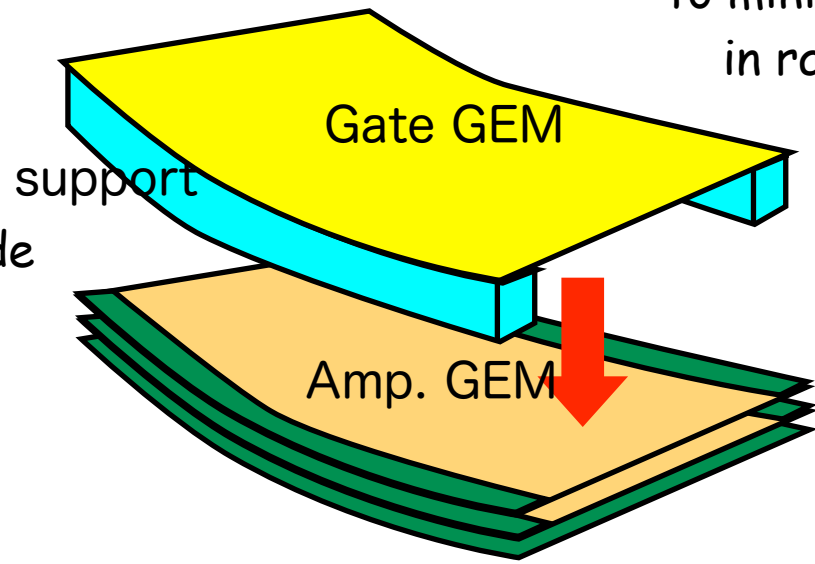




Amp. structure

Double 100um thick GEM

GEM stretched by support post
to minimize dead(support) area
in radial direction



GEM gate

14um thick GEM

Difficulties we had met

GEM Gate did not work as we had expected

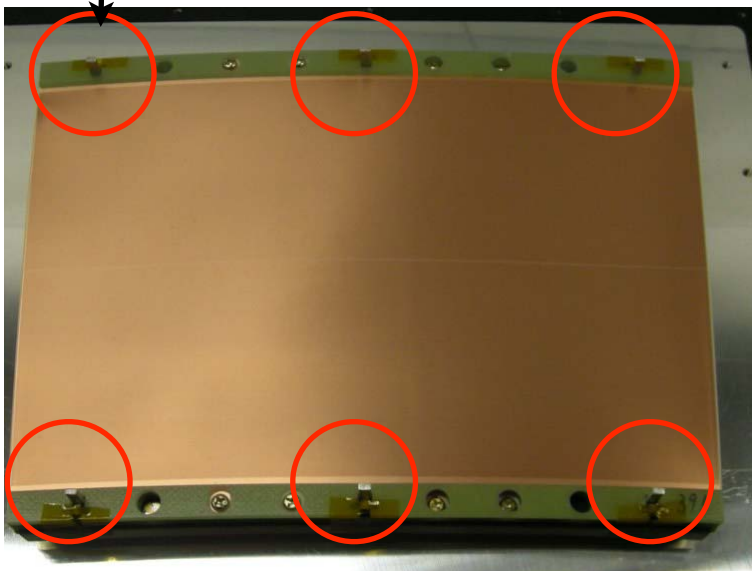
electron transmission is below 50% with std. technique.

thin(14um) GEM is easily expand @ stretching -> size control is not easy
touch to neighbor module

Metal Post introduced large field distortion.

Al post was used instead of the super engineering plastic(PEEK) due to COST!!

without GATE, metal post face to drift region and deteriorate E field
ExB make large distortion to track signal



Module installation test with EP2

HV leaks/unstable GEM operation

complex electrode connection in limited space
- connection is ensured by screw
- small washer is necessary for mechanical tolerance

mechanical precision of module
- fabrication of GEM structures ; too much

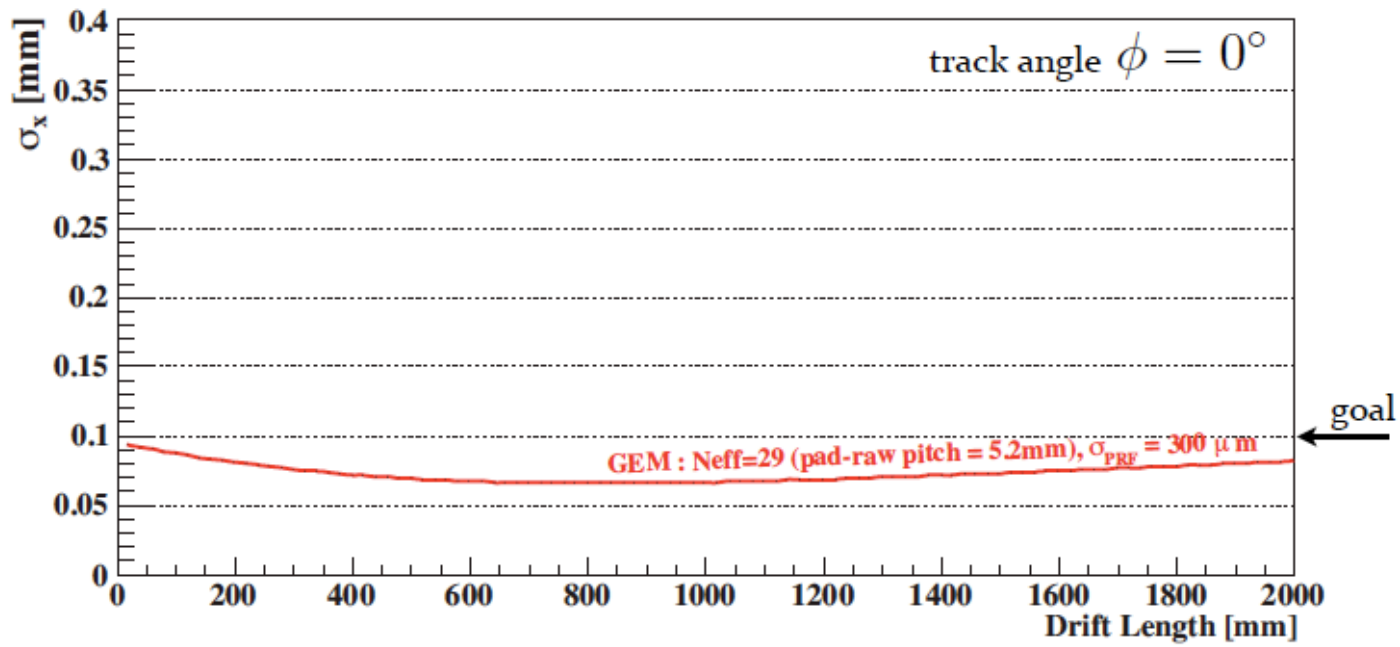
GEM segmentation
- Optimal size of GEM seems to be less than 100cm2
  - our 2 segment GEM has ~150cm2; a little bit larger
- Optimal operation HV condition is not examined

Many problems happen but they can be fixed by matured engineering / technical improvement

Expected resolution @ILD TPC based on beam test result

Ryo Yonamine will talk module test results on Sep.13

Extrapolation of point resolution to the ILD-TPC

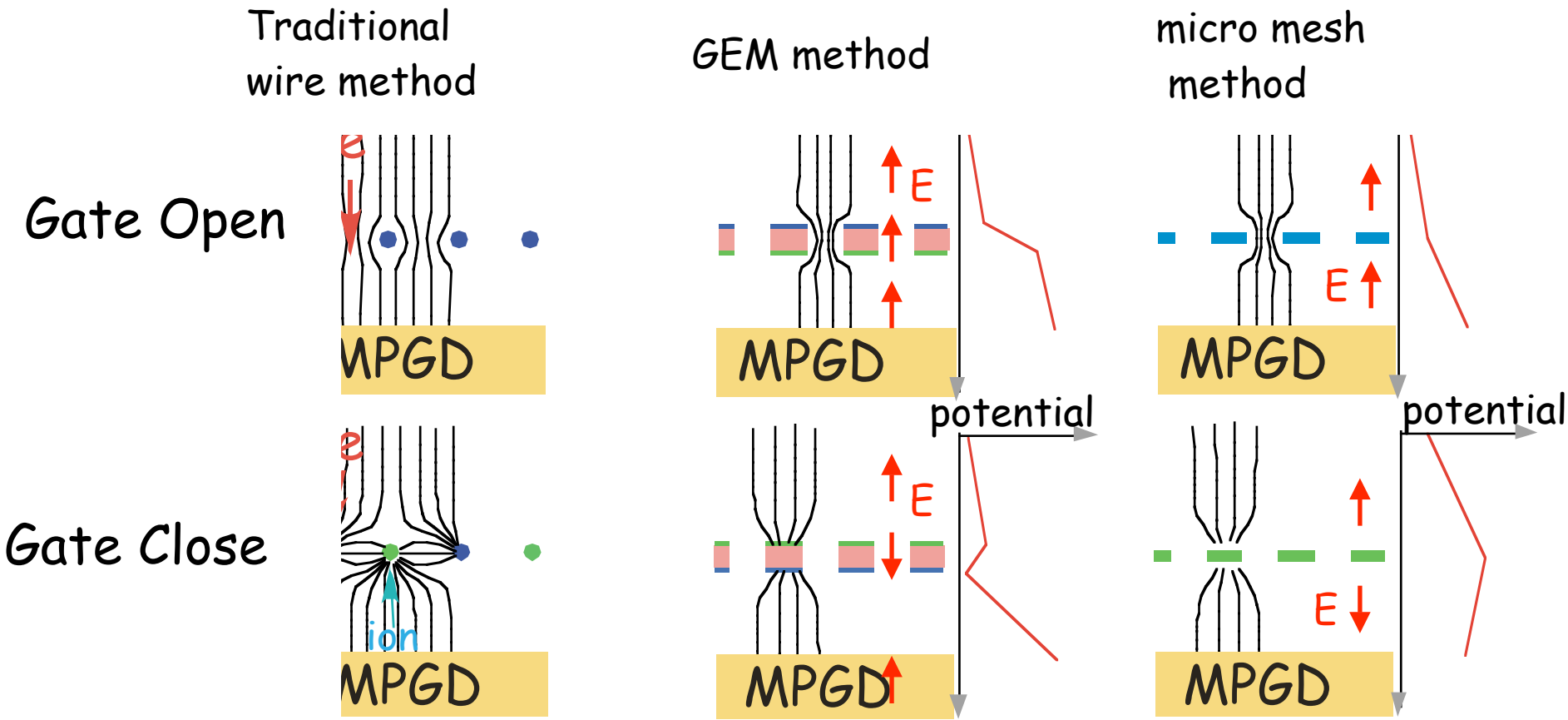


Double GEM seems to satisfy the requirement for the ILD-TPC performance in terms of point resolution.

2011年9月9日金曜日

Gate is another issue

We can imagine 3 methods easily.



Wire :

wire spacing would be large enough
not to deteriorate resolution by ExB
wire spacing ~O(1 mm)
need stiff structure to stretch wires
Local change of E field around wires

GEM :

Electron transmission is in question
collection/extraction efficeincy
hole pitch ~O(100um)
need structure to hold GEM
No change of E field @ drift region

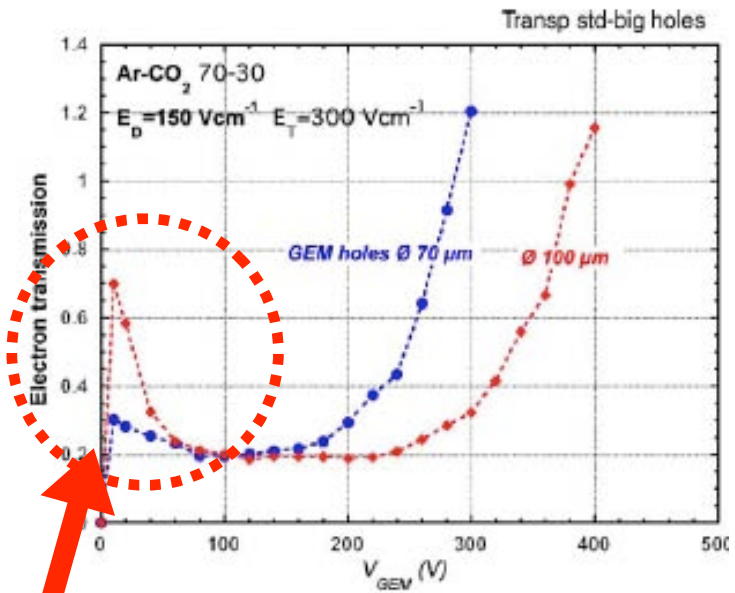
Micro mesh :

need thin mesh
for higher transmission
mesh pitch ~O(50um)

Larger change of E field
@ drift region

Electron transmission @ Gate

F.Sauli, L.Ropelewski,P.Everaerts NIM A560(2006)269-277

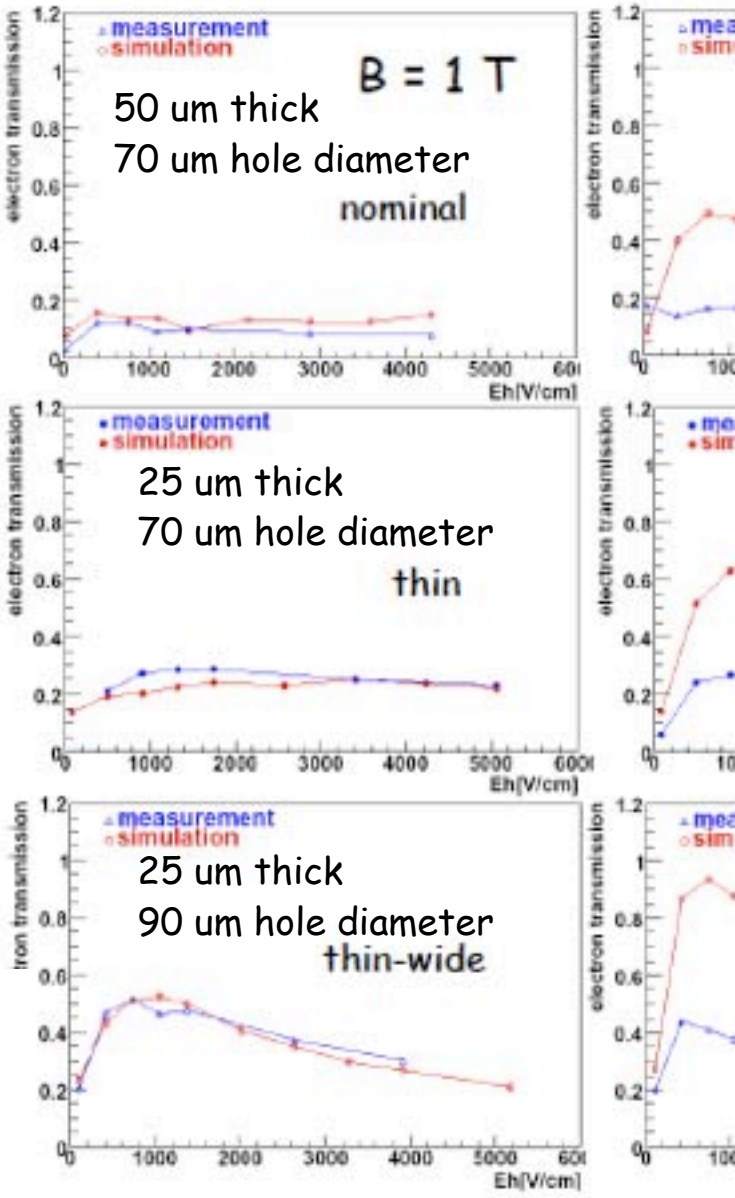


. 6. Comparison of electron transmission for two GEM foils: standar
0 µm holes at 140 µm pitch) and large (100 µm holes at 140 µm pitch)
as filling A–CO_2 70–30.

High elec. transmission @ low VGEM

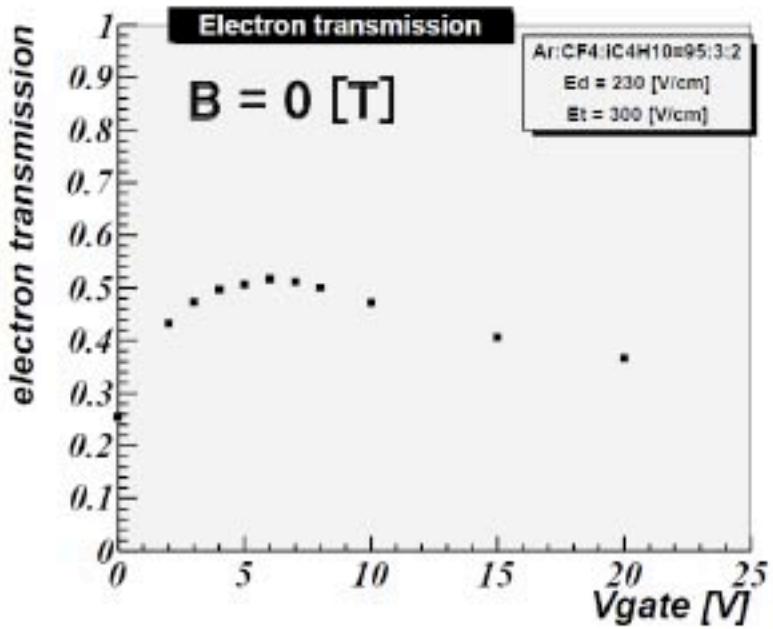
Hint to use GEM as Gate

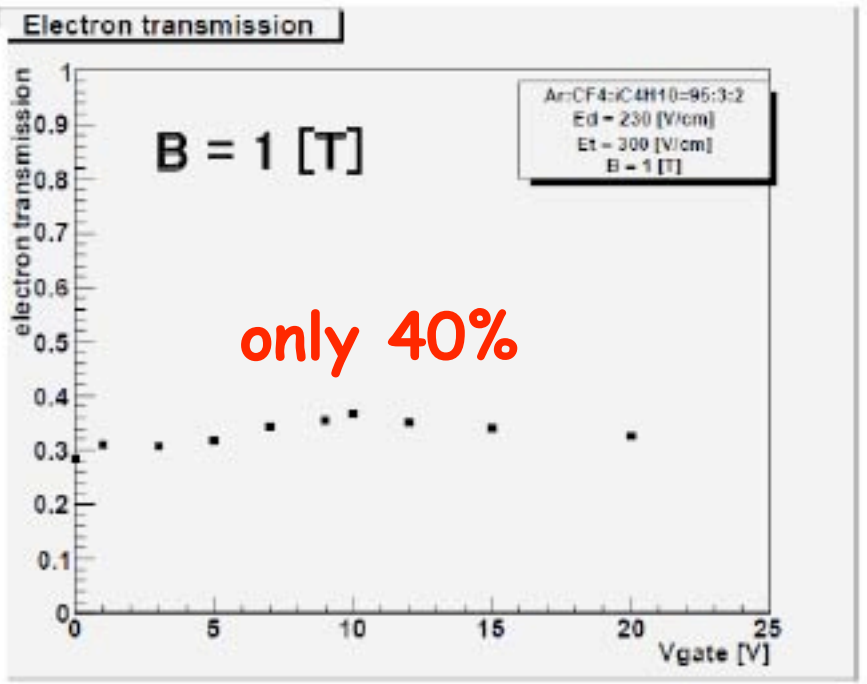
But it not happen to high $\omega\tau$ gas



More difficult for T2K gas real condition even with 14um thick GEM

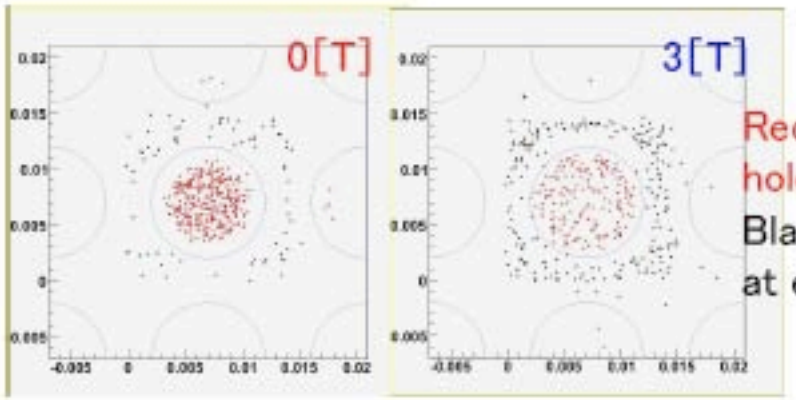
E_D = 230 [V/cm]
E_T = 300 [V/cm]





- B field dependency

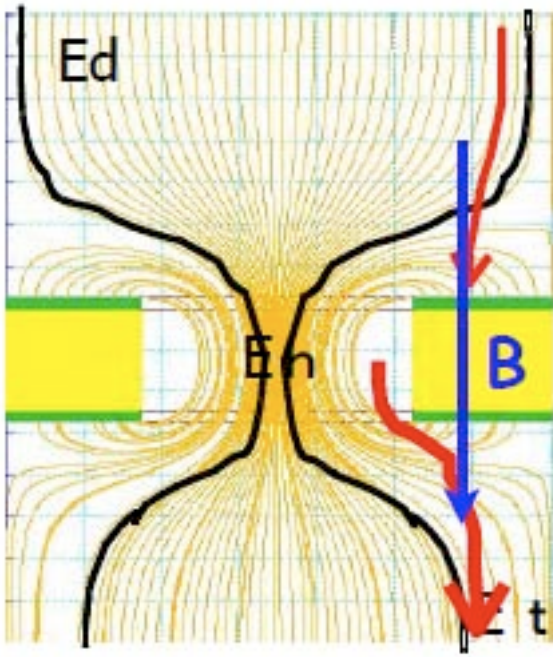
High B field ⇒ Electrons move along B field due to lorentz angle,
# of electrons into the hole decreases



Red : into the hole
Black: arrived at electrode

GEM Gate device

Wire gate would work if we make it properly.
does this fit to LP1 module structure ?



Let us think more about a feasibility of GEM Gate

What limits electron transmission of GEM ?

Aperture seems to be the most important under high B
Our 14um thick GEM has 35% of aperture
and obs. trs. was ~0.5 @1T.

hole pitch 140um
hole diam. 90um

Standard GEM production technique would not provide
sufficient electron transmission (~80%or more)

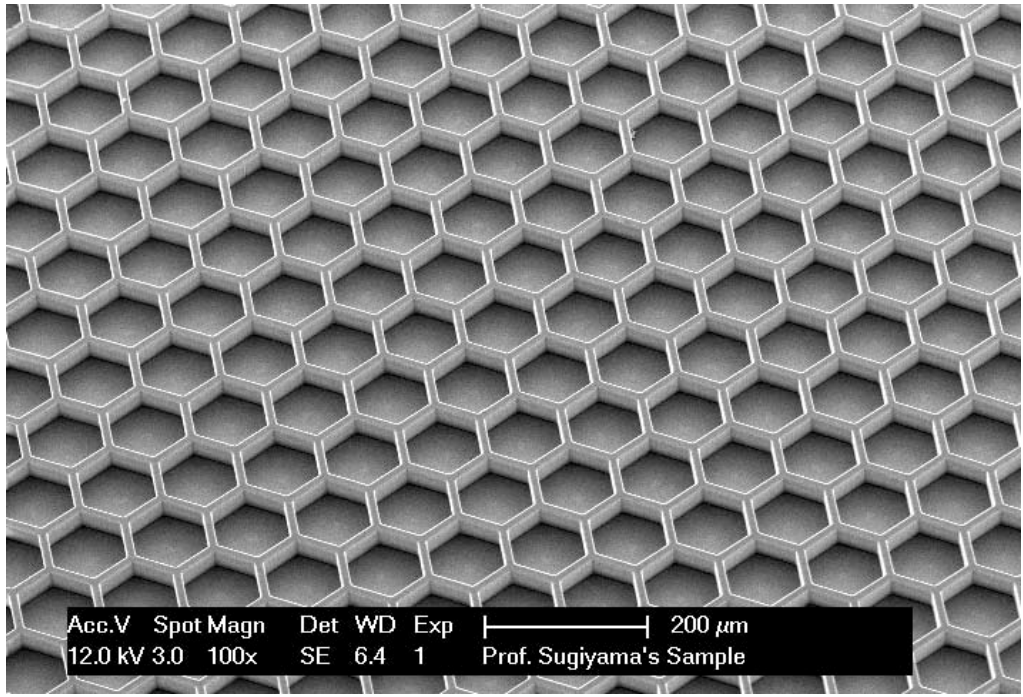
we need 10um thick wall in 100um pitch

passive process (etching) cannot control 10um

Photo lithography technique may be able to handle

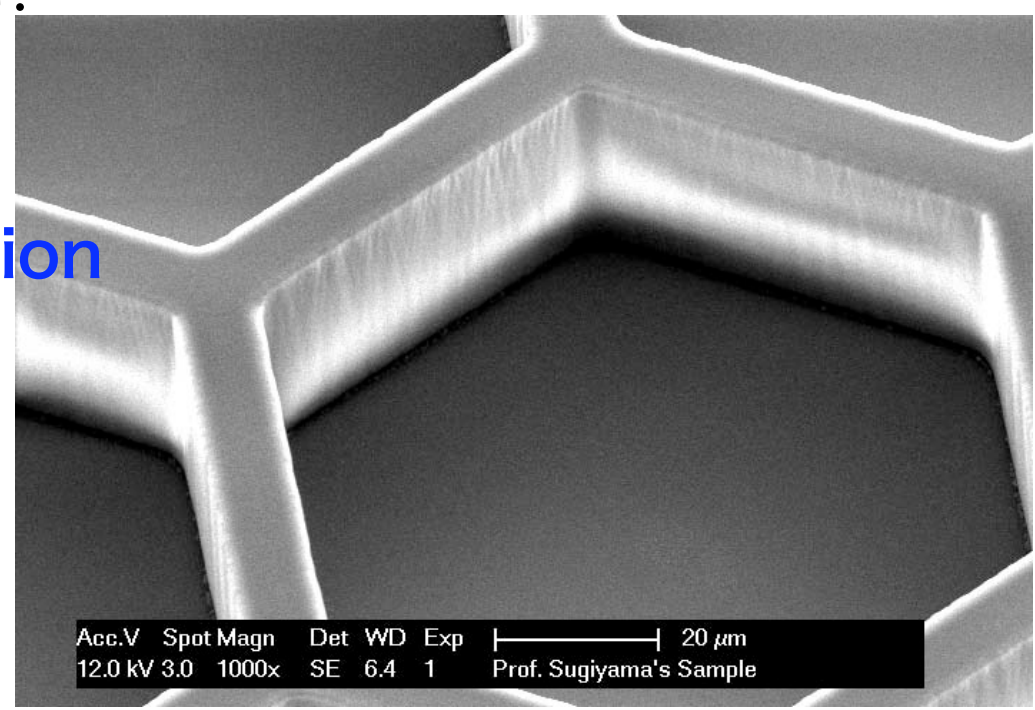
SU8 sample

photoresist structure
on Si wefare



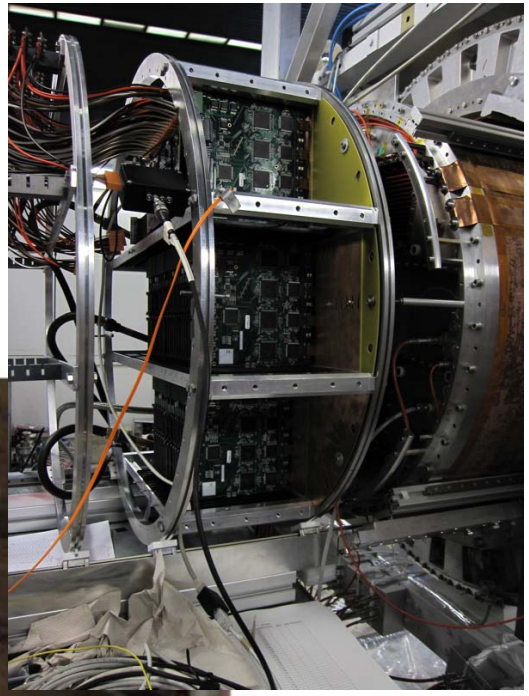
we are trying to construct
metal layer but not get result yet.

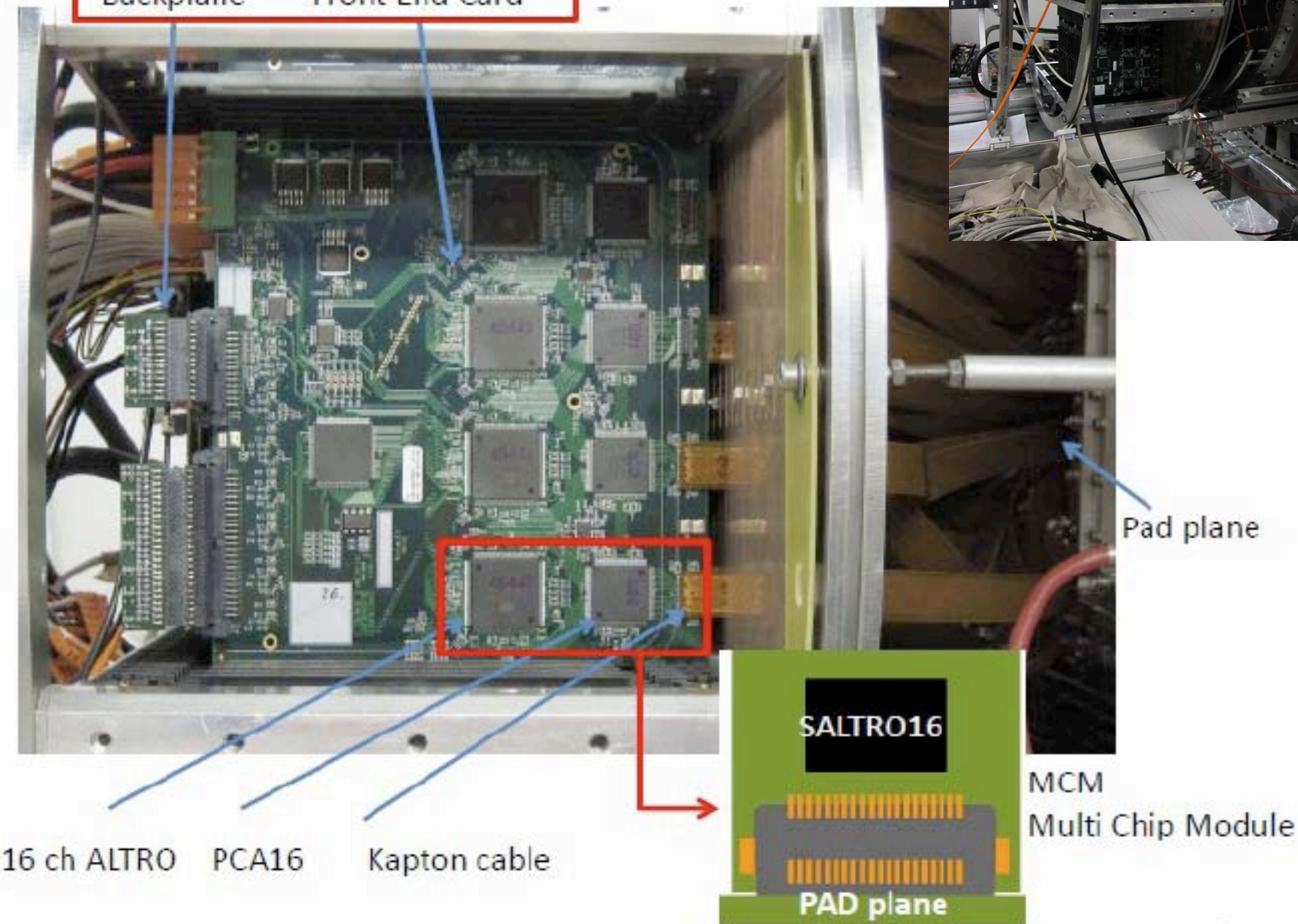
Keep wire gate as fall back option
but we hope to make new one



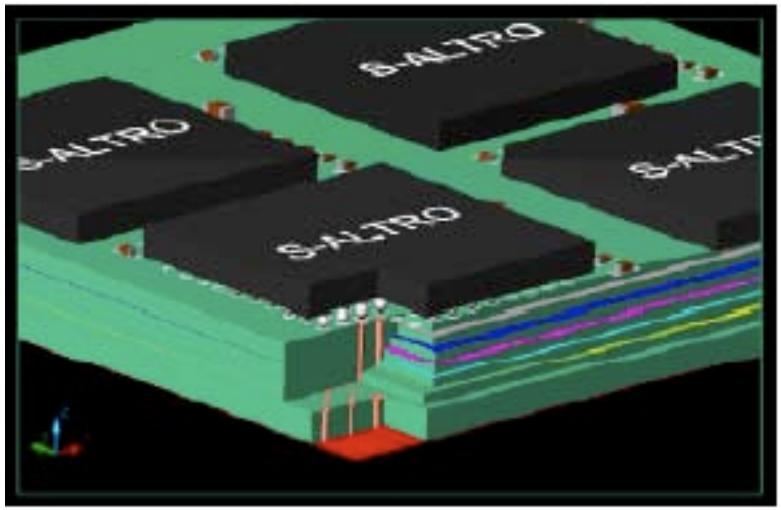
Integration of PCB+RO electronics
= Advanced Endplate

reduction of size/material





FEC -> 1chip s-Altro



Original S-Altro contains 64 ch in a chip.
Bare chips are directly mounted on PCB surface(Flip chip:bump bonding)

Power consumption ~ 20kW/m2
Cooling of PCB/chip is important issue.
Power pulsing is necessary.

need verification

R&D of sAltro64

S-Altro16 has been developed as prototype and characterization is on-going.
Power consumption will be reconsidered (esp. for ADC)

R&D of PCB

Analog/digital mixed board
Cooling test using dummy module is on-going by 2 pahse CO2

AEP related talk is given by Fusayasu tomorow

Difficulties of AEP

sAltro64	sAltro16 was made
	4 times more channels
chip/mount	circuit check of bare chip
	bonding yield
	module production yield
cooling@test	possible? how?

pre-AEP before full AEP

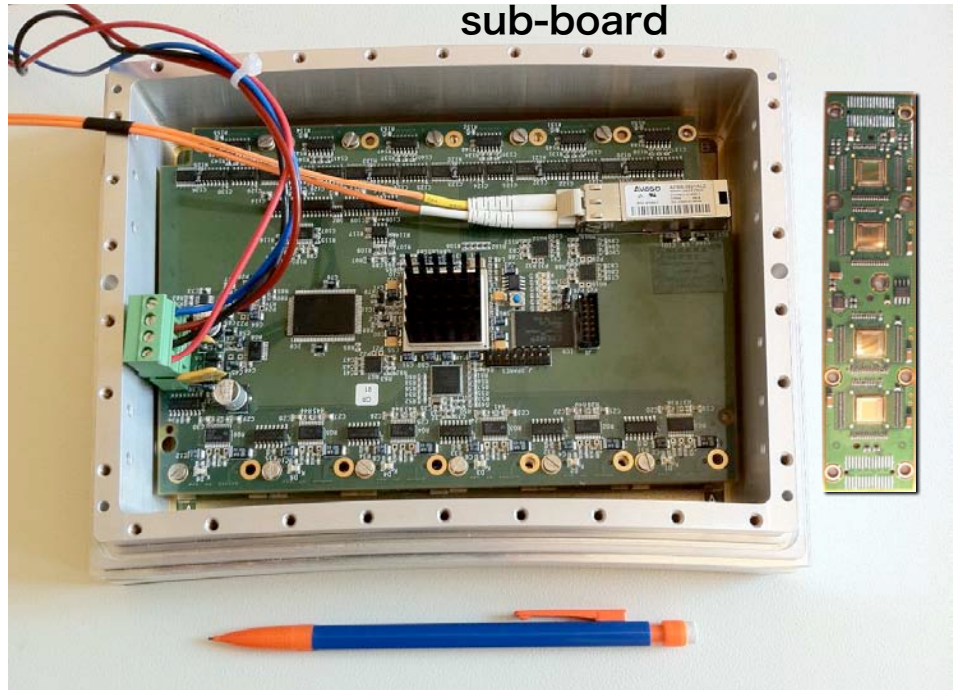
chip mounted on sub-board / not directly on PCB

- increase yield of sub-board
- easy replacement

but

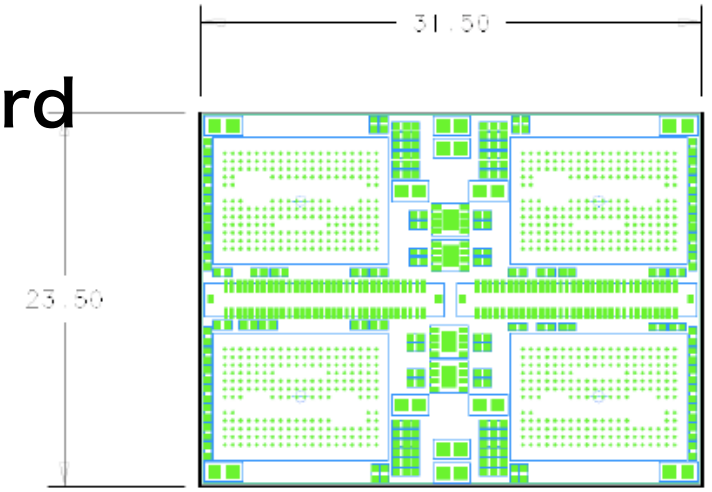
- increase material
- increase # connectors
  - mechanical precision
- complex cooling
- enough density??

Micromegas module using AFTER electronics sub-board



LUND sAltro16 card

The FEC-MCM for SALTRO16



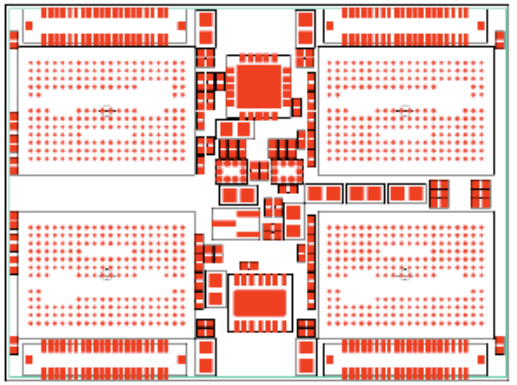
Connector to readout and LV
Should be reduced to minimum

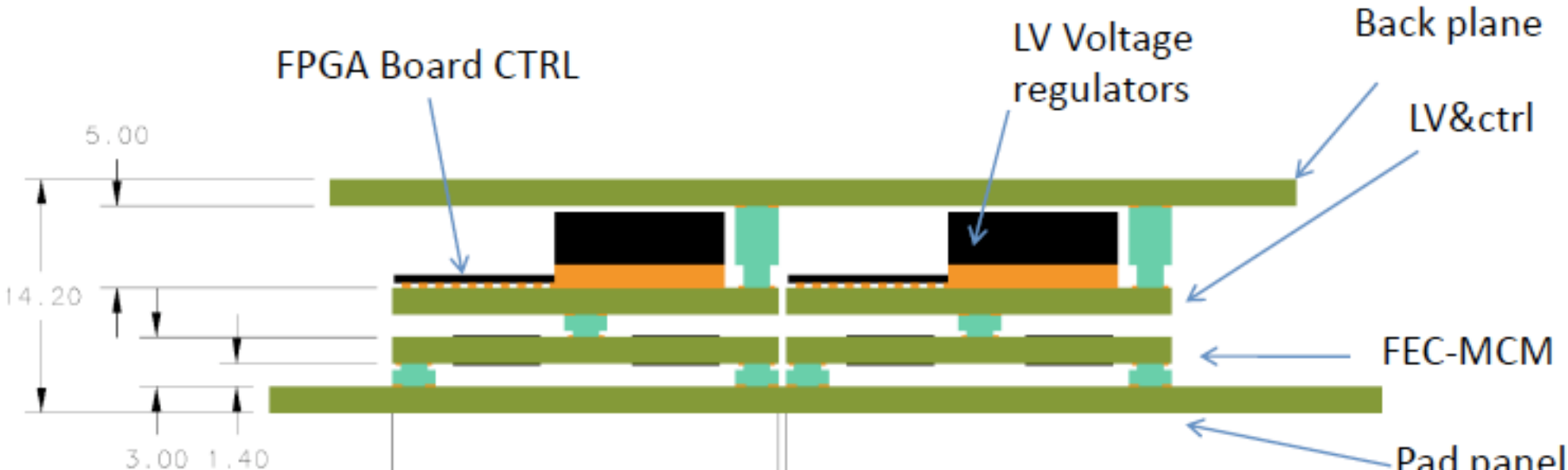
Top side

Below side

No room for boardcontroller and circuitry for
Readout. Place on separate card.

Connectors to pads





What we will do for Next　　for Completion of "Phase2"

We keep the stretch method to minimize radial dead space
but we don't use the unremovable "post"
new structure is necessary

New Pad Plane

same pad pitch/height
fit to sAltro16 sub board

New Amplification structure

New stretch mechanism
New GEM design : segmentation/HV line
HV connection

common design
with 3GEM(DESY)
(MicroMegas ?)
if possible

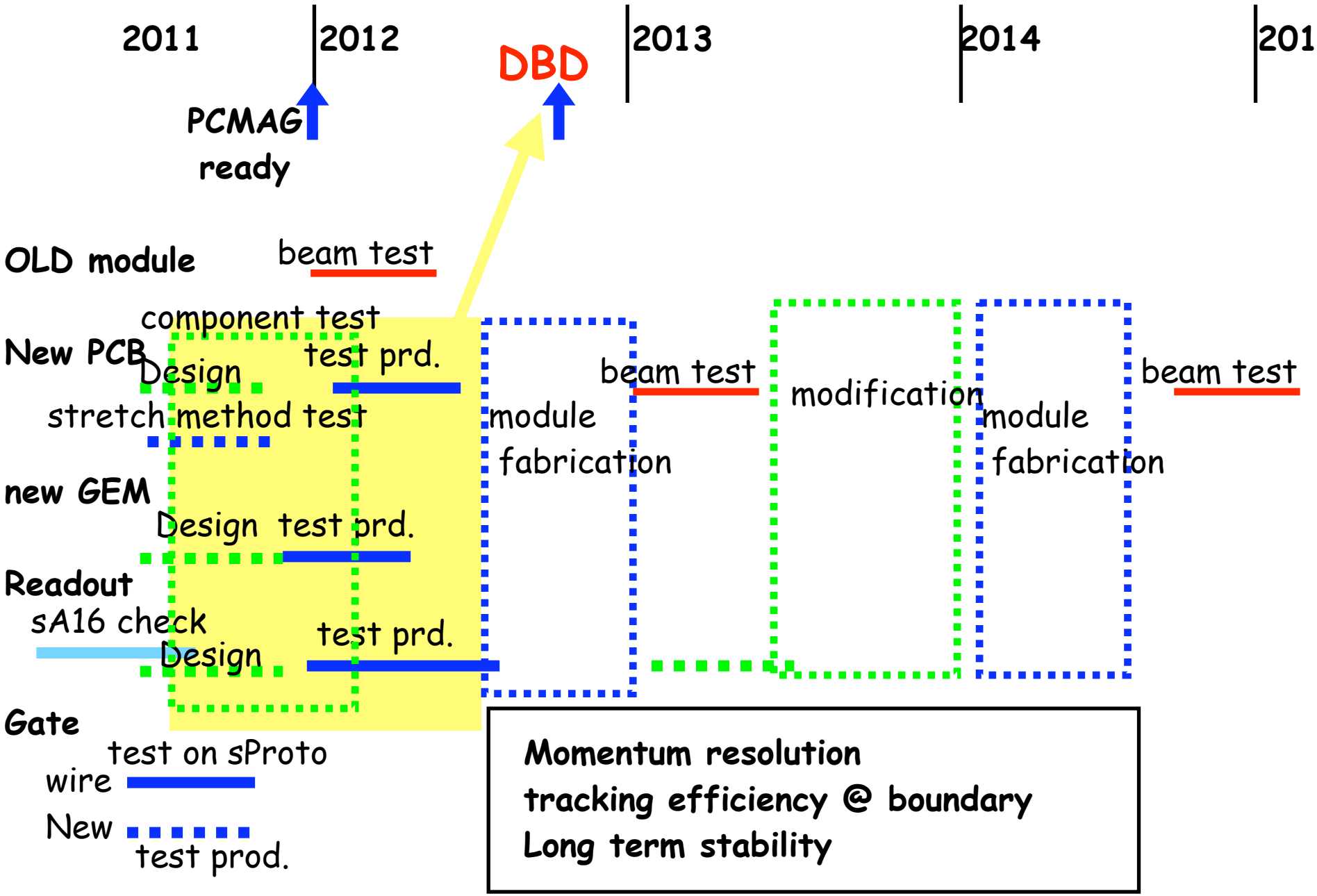
New RO scheme

sAltro sub board + control board

test box

simulate LP1 environment / multi module?

Schedule


2011
2012
2013
2014
2015
DBD
PCMAG
ready
OLD module
beam test
component test
New PCB
Design
test prd.
stretch method test
module
fabrication
beam test
modification
module
fabrication
beam test
new GEM
Design
test prd.
Readout
sA16 check
Design
test prd.
Gate
test on sProto
wire
New
test prod.
Momentum resolution
tracking efficiency @ boundary
Long term stability