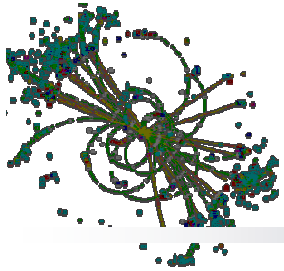
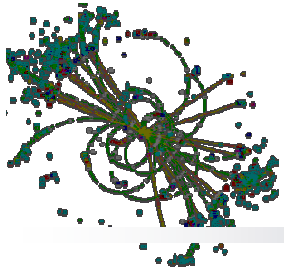


Status of the Chronopixel Project

N. B. Sinev
University of Oregon, Eugene

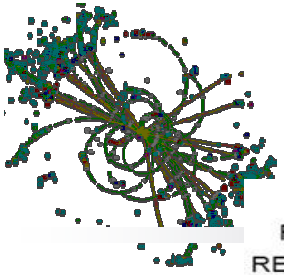
In collaboration with J.E.Brau, D.M.Strom (University of Oregon, Eugene, OR), C.Baltay, H.Neal, D.Rabinovitz (Yale University, New Haven, CT), Thomas Senko (SRI International –Sarnoff)

EE work is contracted to Sarnoff Corporation

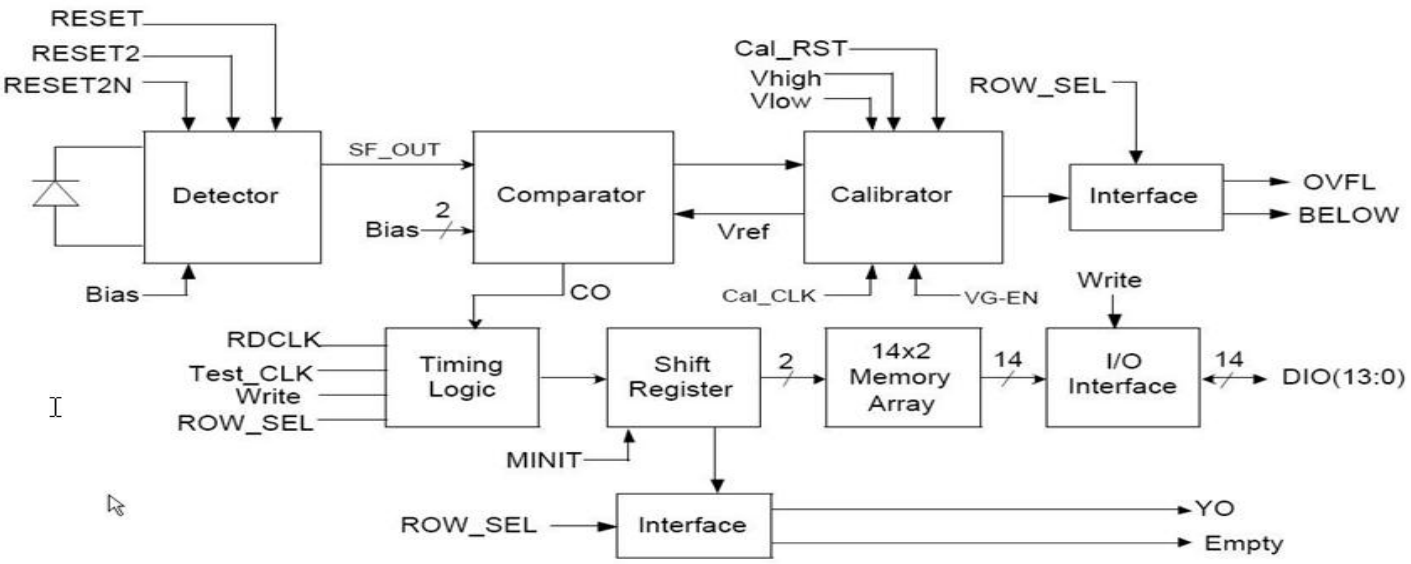


Outline of the talk

- First prototype design
- First prototype test results
- Timeline
- Design of the next prototype
- Some simulations of expected parameters
- Conclusions



First prototype design



- Monolithic CMOS pixel detector design with time stamping capability was developed in collaboration with Sarnoff company.
- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.
- If another particle hits the same pixel during the same bunch train, second memory cell is used for this event time stamp.
- During readout, which happens between bunch trains, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.
- Comparator offsets of individual pixels are determined in the calibration cycle, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.
- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.

Sensor design

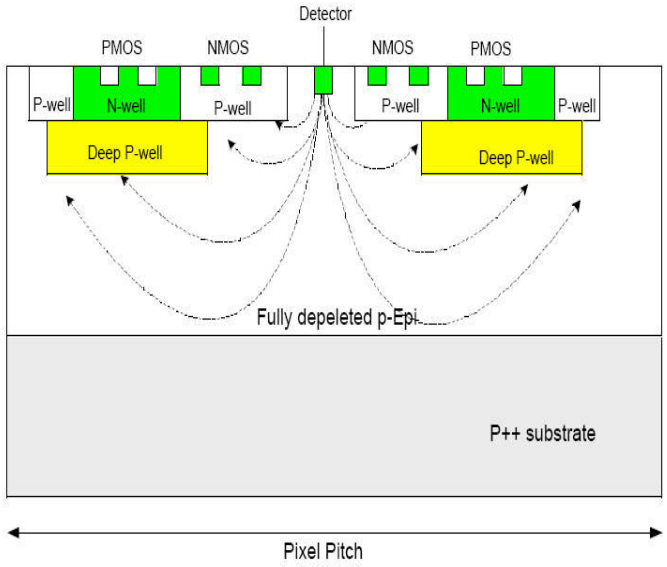


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

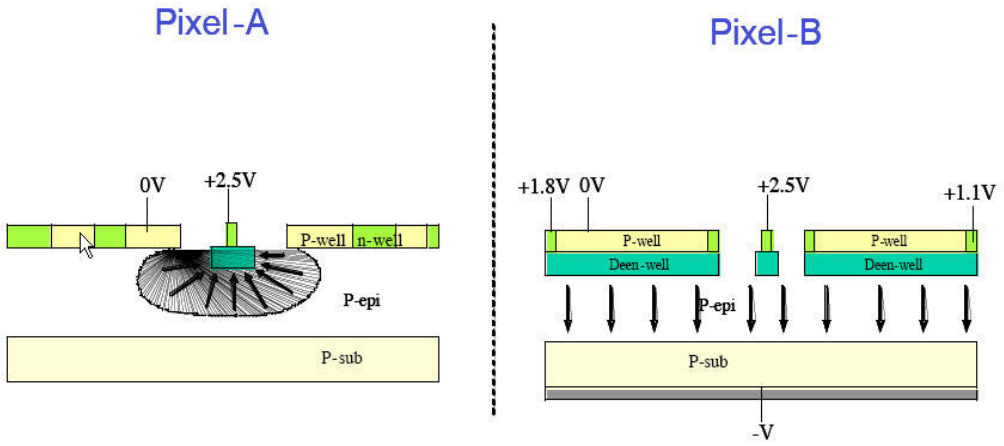
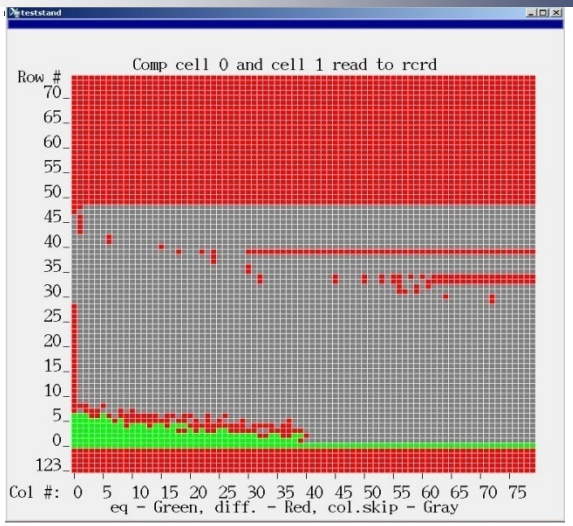


Figure 6.3 Comparison of the vertical cross section views of two pixels

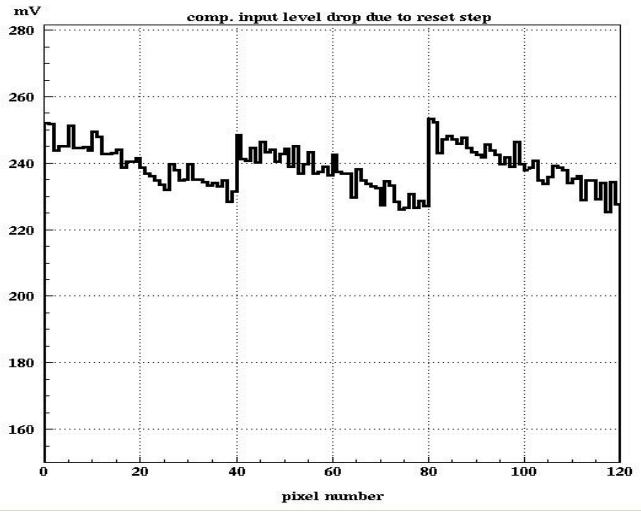
Ultimate design, as was envisioned **Two sensor options in the fabricated chips**

- **TSMC process does not allow for creation of deep P-wells. Moreover, the test chronopixel devices were fabricated using low resistivity (~ 10 ohm*cm) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs deep n-well, encapsulating all p-wells in the NMOS gates. This allow application of negative (up to -10 V) bias on substrate.**

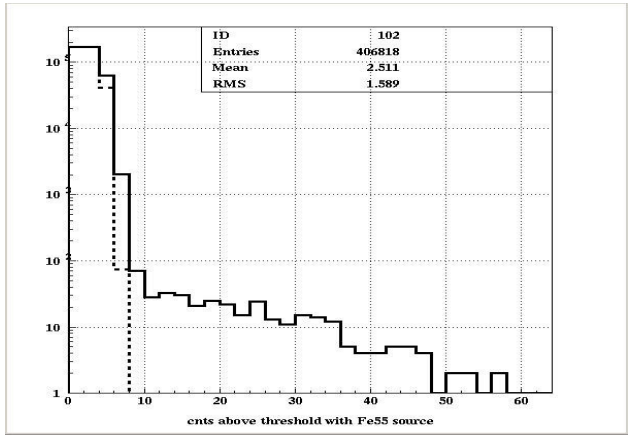
First prototype test results



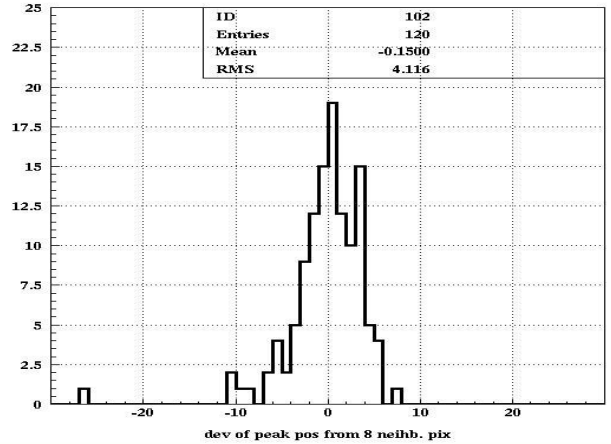
Correctly working pixels are shown in green



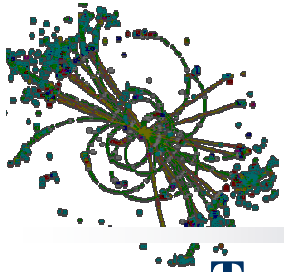
Change of power supply V depending value along rows



Signal from Fe55 distribution (dotted – without source)



Distribution of comparator offsets

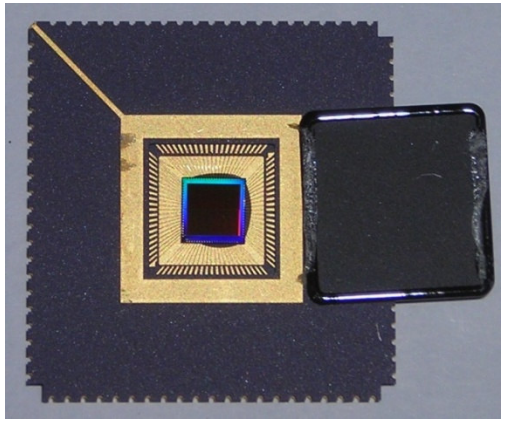


Conclusions from tests

- Tests of the first chronopixel prototypes are now completed.
- Tests show that general concept is working.
- Mistake was made in the power distribution net on the chip, which led to only small portion of it is operational.
- Calibration circuit works as expected in test pixels, but for unknown reason does not work in pixels array.
- Noise figure with "soft reset" is within specifications (0.86 mV/35.7μV/e = 24 e, specification is 25 e).
- Comparator offsets spread 24.6 mV expressed in input charge (690 e) is 2.7 times larger required (250 e). Reduction of sensor capacitance (increasing sensitivity) may help in bringing it within specs.
- Sensors leakage currents ($1.8 \cdot 10^{-8} A/cm^2$) is not a problem.
- Sensors timestamp maximum recording speed (7.27 MHz) is exceeding required 3.3 MHz.
- No problems with pulsing analog power.

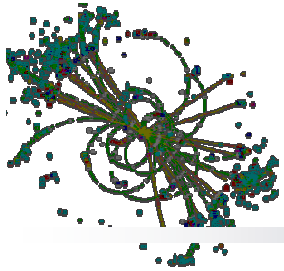
Timeline

- **January, 2007**
  - Completed design – Chronopixel 1
    - **2 buffers, with calibration**
- **May 2008**
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Low resistivity (~10 ohm*cm) silicon
- **October 2008**
  - Design of test boards started at SLAC
- **June 2009**
  - Test boards fabrication. FPGA code development started.
- **August 2009**
  - Debugging and calibration of test boards
- **September 2009**
  - Chronopixel chip tests started
- **March 2010**
  - Tests completed, report written
- **May – August 2010**
  - Discussions on the second prototype design, principal features of the prototype 2 defined, solution to the main problems found



First prototype

- **September 2010**
  - contract with Sarnoff for developing of second prototype signed.
- **October 2010 – August 2011**
  - Sarnoff works stalled
- **September 2011**
  - Sarnoff resumed work.
- **December 2011**
  - Prototype 2 design completed.
- **February 2012**
  - Tape out for TSMC shuttle run 02.25.2011



New prototype

- We have discussed with SARNOFF engineers the design of the next prototype. In addition to fixing found problems, we would like to test new approach, suggested by SARNOFF – build all electronics inside pixels only from NMOS transistors. It can allow us to have 100% charge collection without use of deep P-well technology, which is expensive and rare (or at least is non-standard). To reduce all NMOS logics power consumption, dynamic power scheme was proposed by SARNOFF.
- We have signed contract with Sarnoff for the next prototype design in September 2010, and hope to be able to submit it for manufacturing to TSMC in February of 2012.
- In September of 2011 Sarnoff suggested to build next prototype on 90 nm technology, which will allow to reduce pixel size to 25μ x 25μ
- Simultaneously with production of next prototype, test stand will be modified.

Prototype 2 design

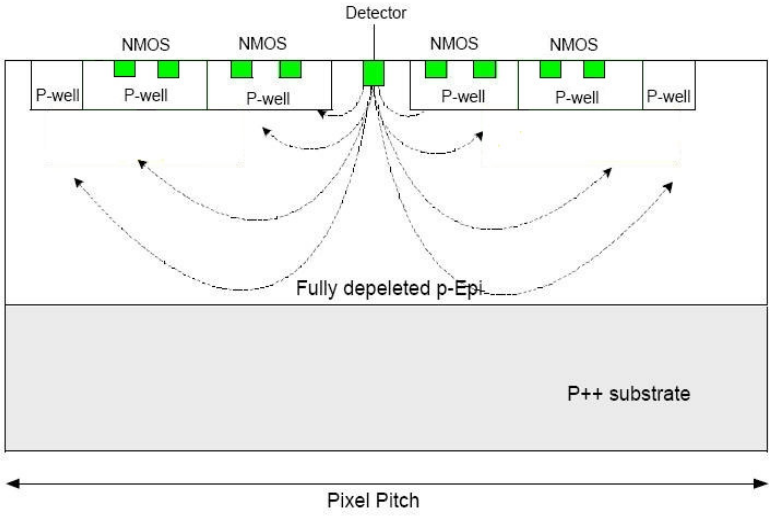
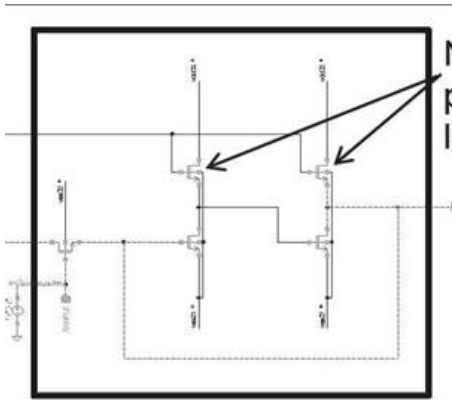


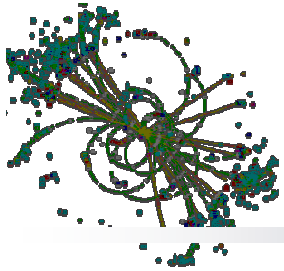
Figure 11.1 Proposed pixel architecture



NMOS Latch is refreshed periodically by clocked NMOS load

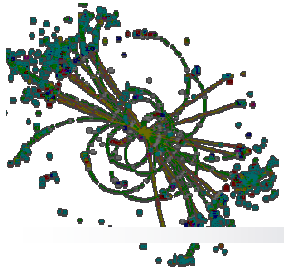
Clocked Dynamic NMOS Latch is a very efficient memory element. NMOS inverters and NOR gates can also be clocked to save on static power consumption.

Proposed dynamic latch has, however , technical problem in achieving very low power consumption. The problem is in the fact, that nmos loads can't have very low current in conducting state – lower practical limit is 3-5µA. This necessitate in the use of very short (few nanoseconds) refreshing pulses to keep power within specified limit. However, we found solution to this problem, which allows to reduce current to required value without need for short pulses.



More problems with 90nm design

- Because of shorter channels and lower voltage, it is very difficult to build comparator with large gain using only nmos transistors.
- So, we decided to allow use of pmos transistors inside pixels, but minimize their use only to comparators.
- It will reduce charge collection efficiency by the factor 1- S_{pm}/S_{se} where S_{se} is sensor electrode area and S_{pm} is the area of all pmos transistors in the pixel. We can expect the S_{pm} to be around 5 μ^2 and we want to reduce S_{se} from about 100 μ^2 as it was in the first prototype to something like 25 μ^2 . It should reduce noise level, which is proportional to squire root of capacitance (if it expressed in the units of charge). Expressed in units of signal amplitude kTC noise is increasing with reduced capacitance as inverse of squire root of its value, but sensitivity grows linear with 1/C.
- So, we can expect our charge collection efficiency be about 80%.
- However, we need to add width of depleted layer to electrode areas. It will reduce area ratio and reduce charge collection efficiency
- Next slides show final prototype 2 design and simulation of it's performance



Prototype 2 design completed

SRI International
SARNOFF

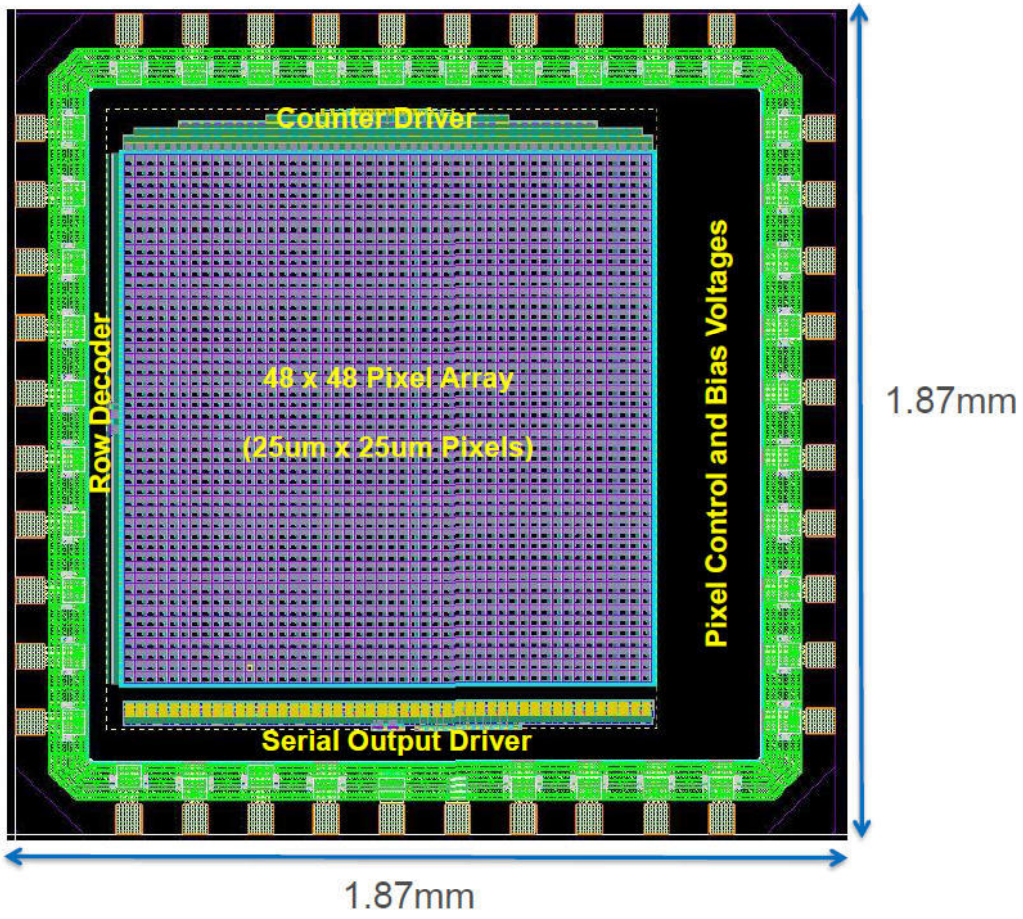
Chronopixel 2 Features

- TSMC 90nm CMOS Process
- 1.2 volt thin oxide MOSFET
- 2.5 volt thick oxide MOSFET
- 1.87mm x 1.87mm chip
- 40 pads (10 each side)
- 40 pin DIP package
- 25um x 25um pixel
- 48 x 48 pixel array
- Deep NWELL detector
- Analog hit detection
- Analog offset calibration
- Two 12 bit counter registers
- Mostly NMOS logic

Chip layout

SRI International
SARNOFF

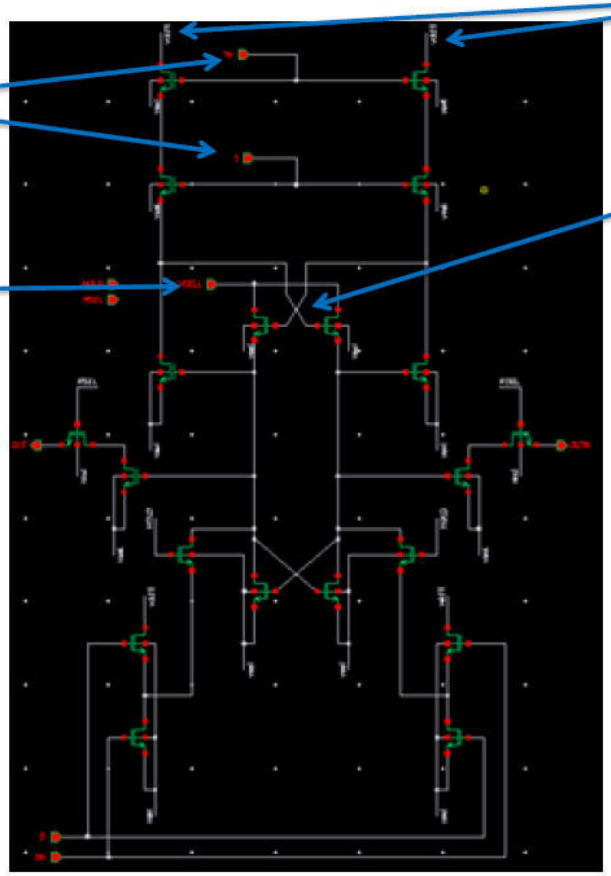
Chronopixel 2 Test Chip Layout



Final memory cell design

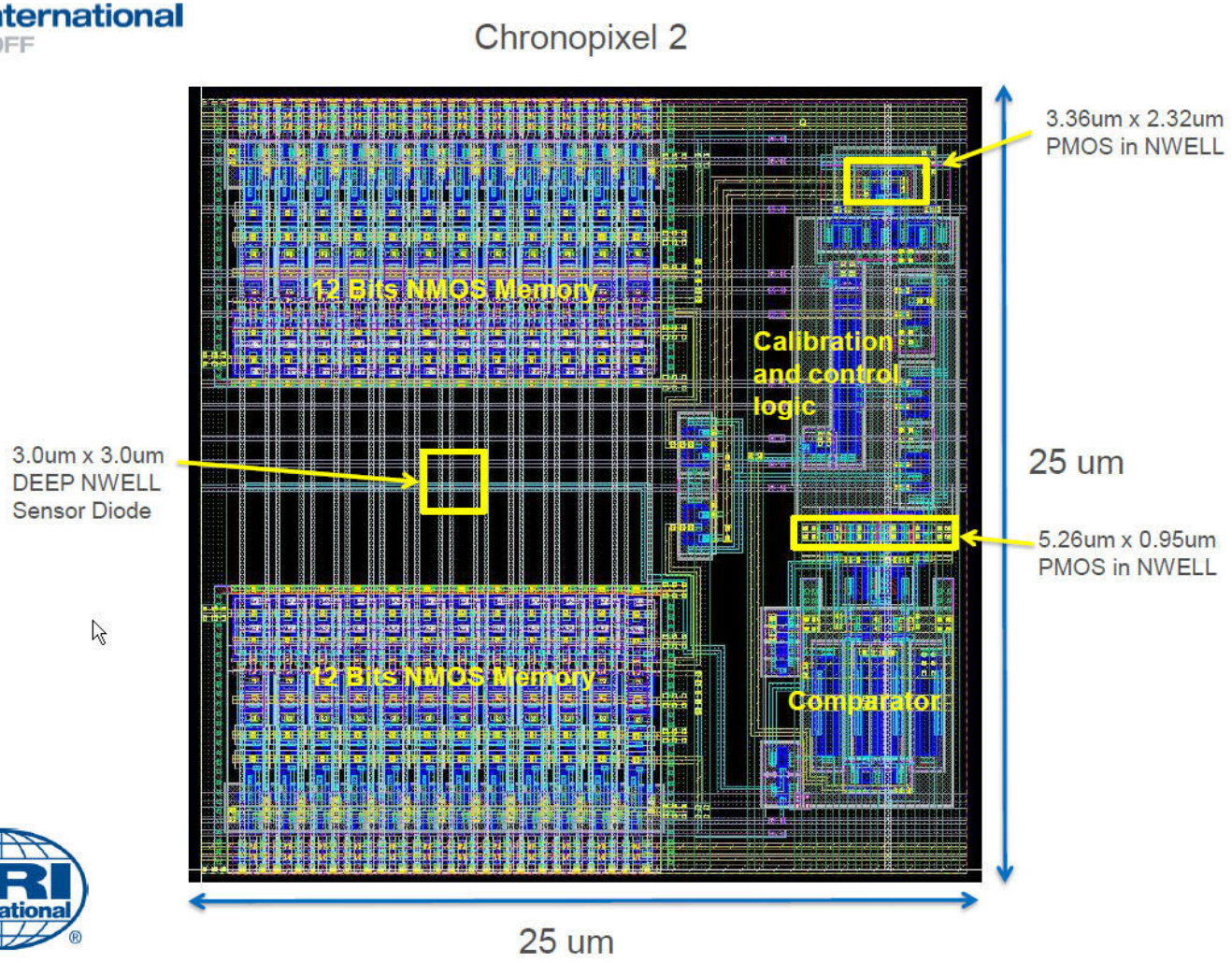
SRI International
SARNOFF

Thin Oxide NMOS Memory Cell



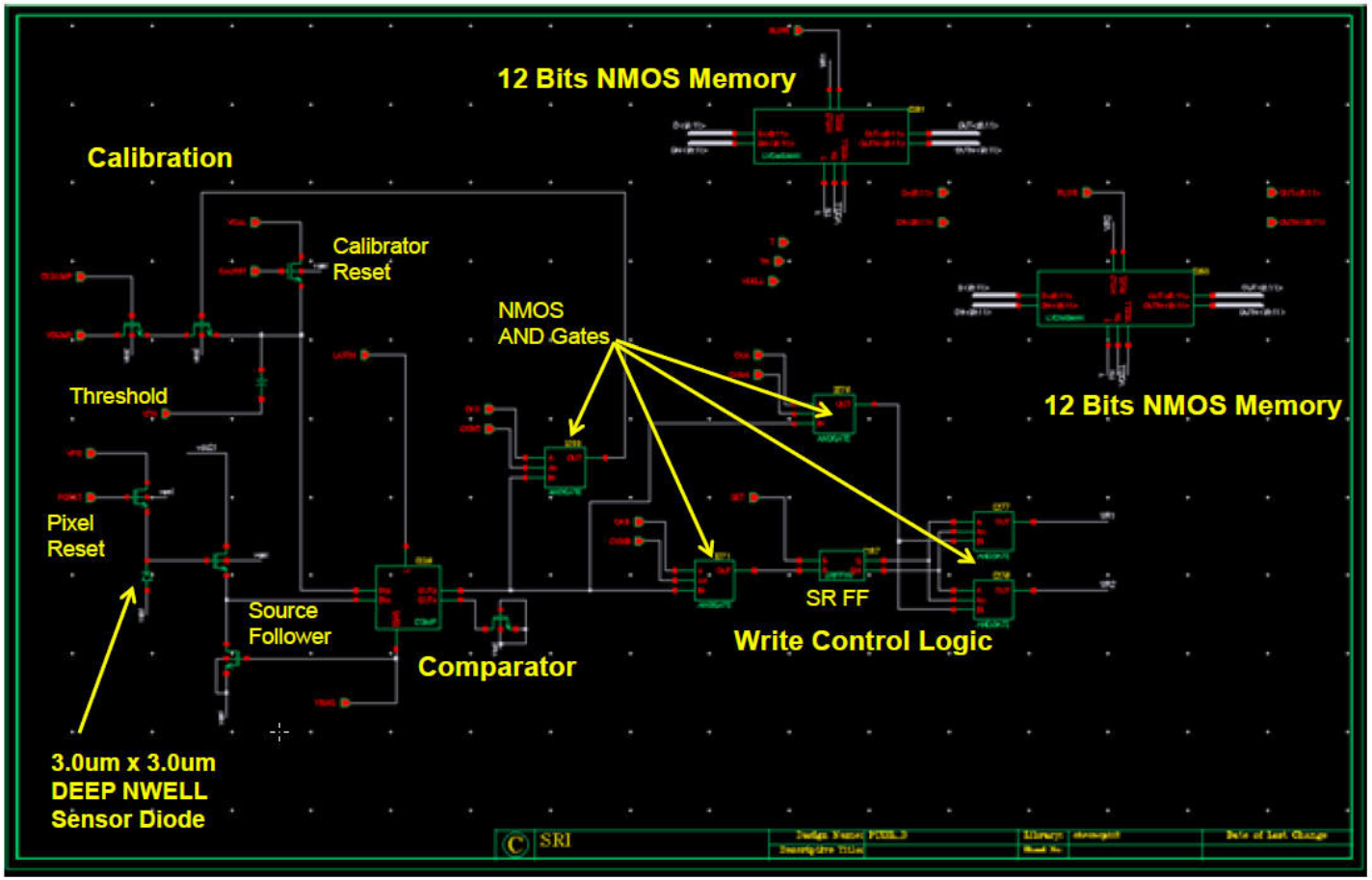
Prototype 2 pixel layout

SRI International
SARNOFF

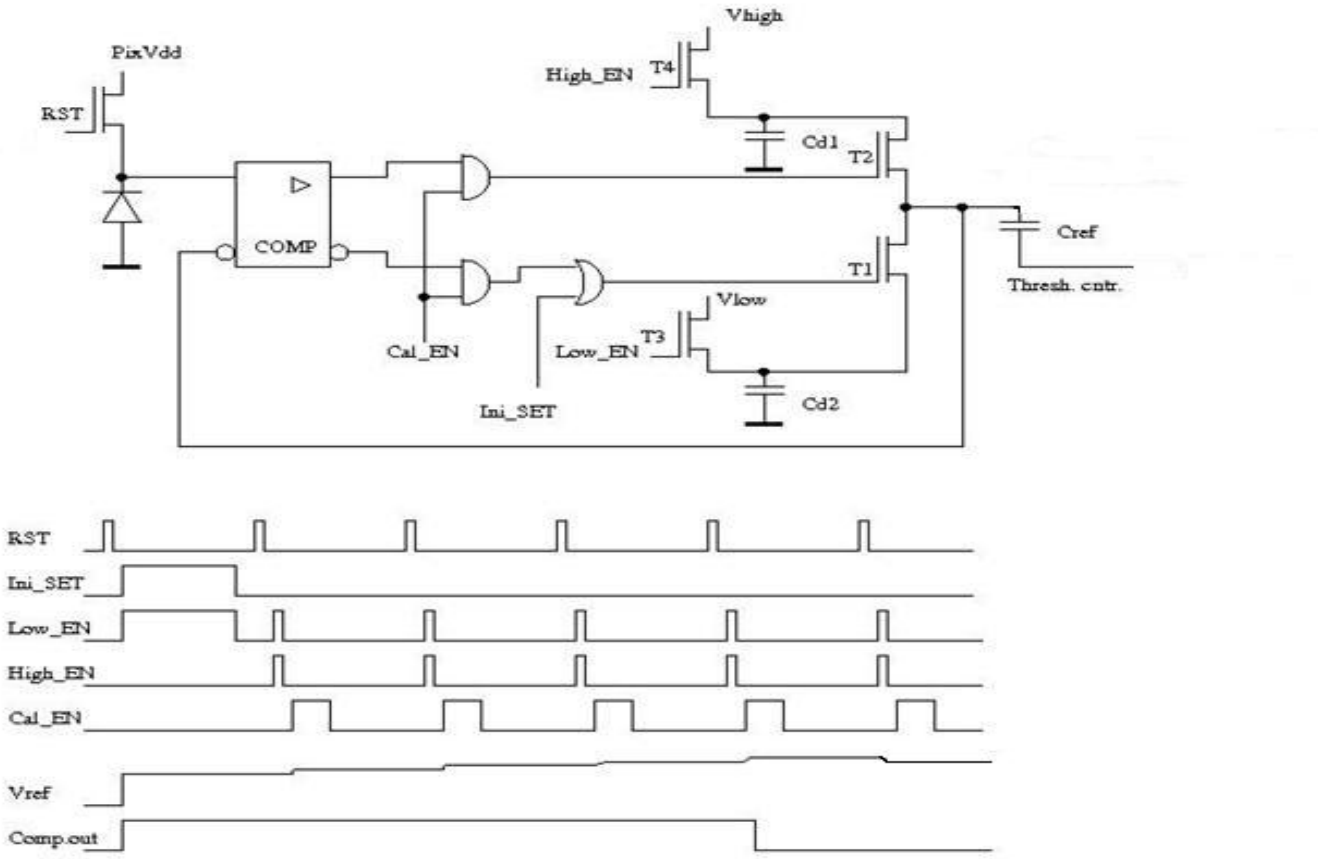


Final Pixel design

Pixel Schematic



New analog comparator offset calibration - idea

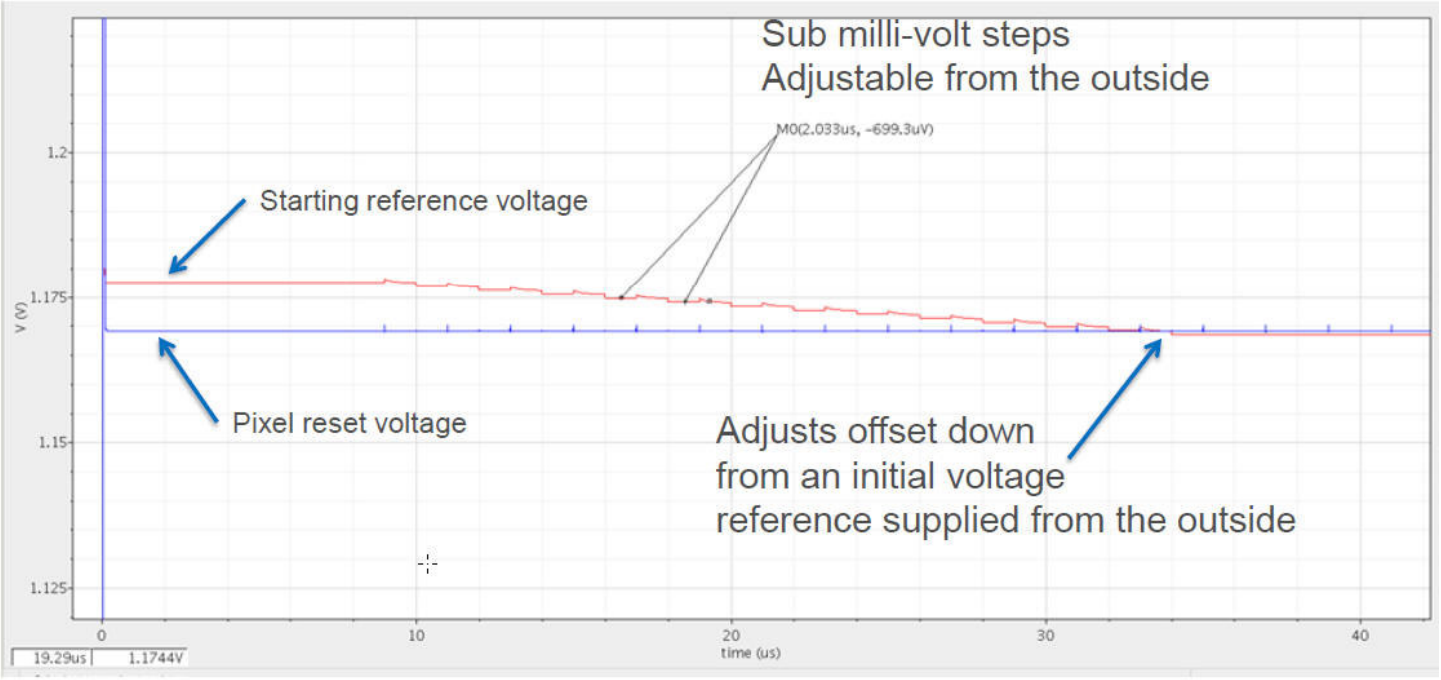


- **Next idea was to replace calibration circuit from digital where offset is kept as a state of calibration register with analog circuit in which offset is kept as a voltage on a capacitor.**

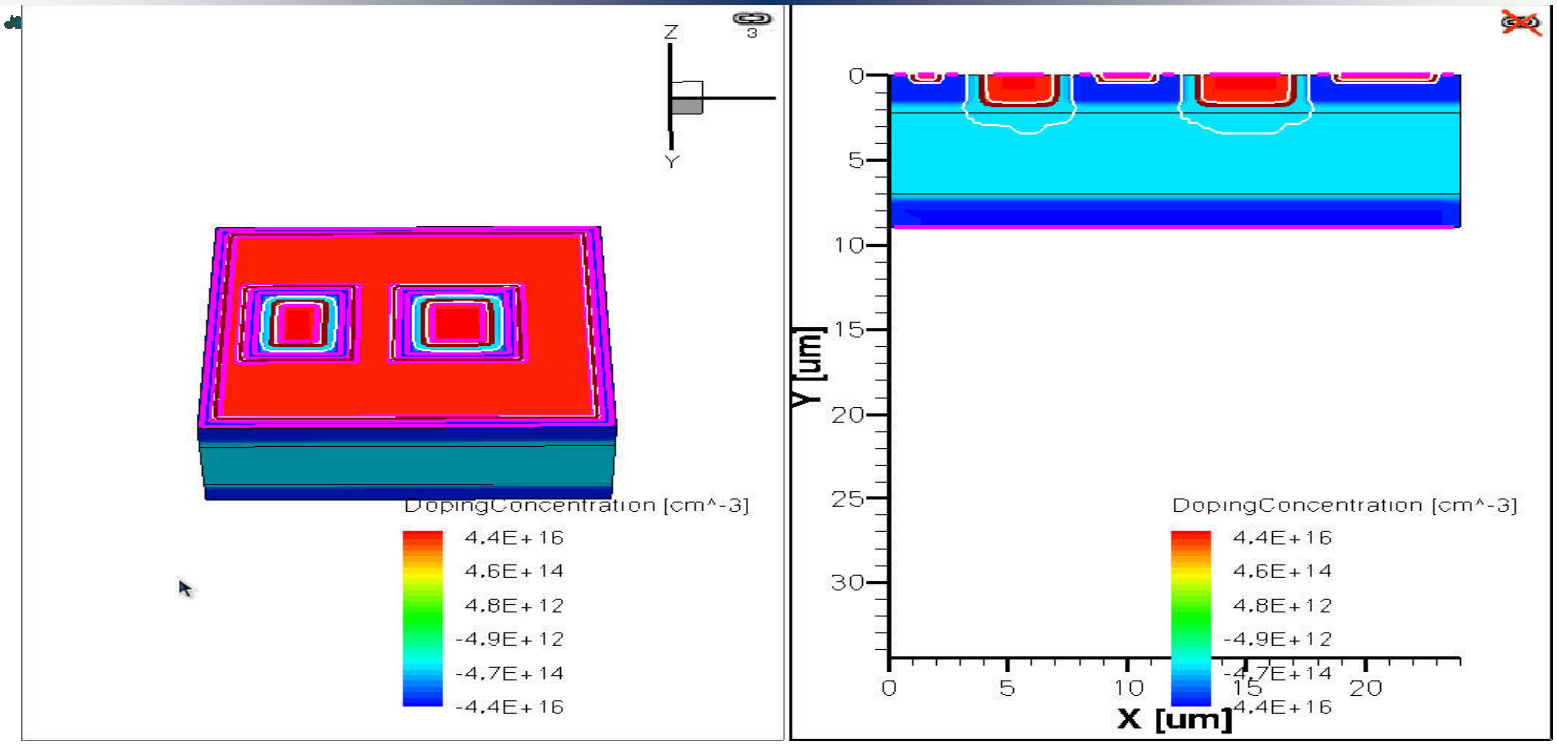
Real design calibration SPICE simulation

SRI International
SARNOFF

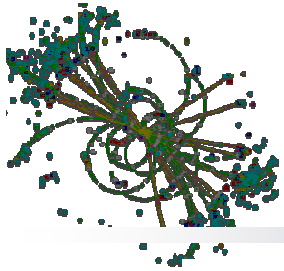
Comparator Offset Calibration



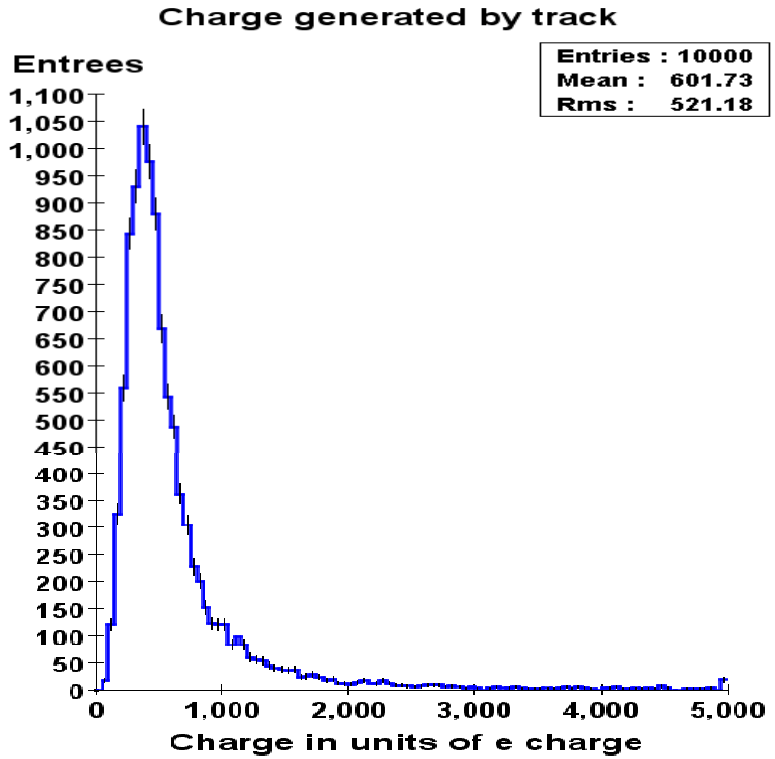
Prototype 2 simulations

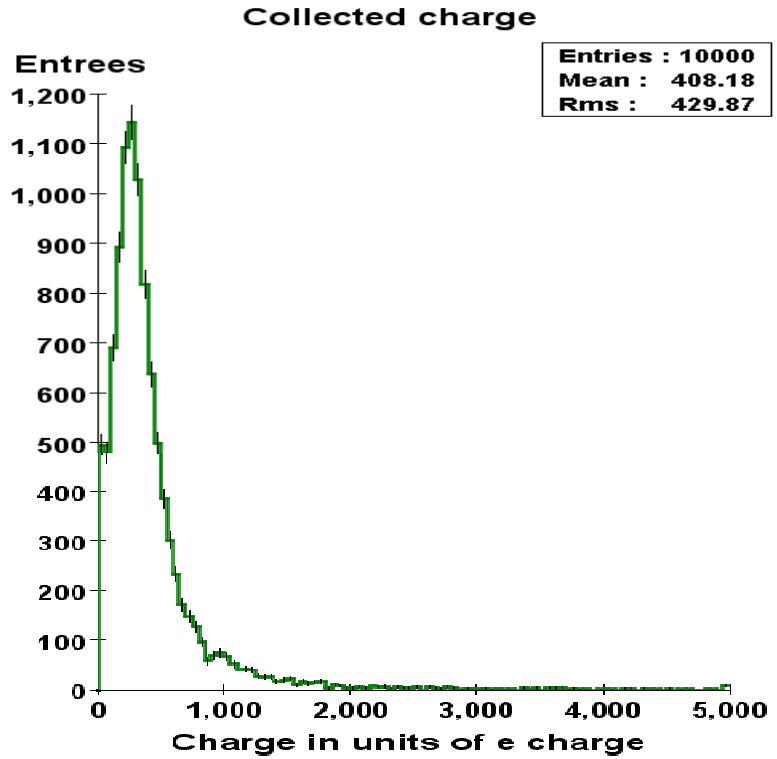


Here you can see simplified pixel model I used to simulate charge collection.
Large red squire in the center – signal collecting electrode, small red squire at the left – area taken by pmos transistors, the rest of the red on left picture shows n-wells of electronics , which are sitting on the top of p++ doped areas. White line outlines depleted region. I simulated larger charge collecting electrode (16 μ^2 instead of 9 μ^2) because we can increase it and I think it will be better. Area of PMOS transistors corresponds to final layout (shown on slide 14).



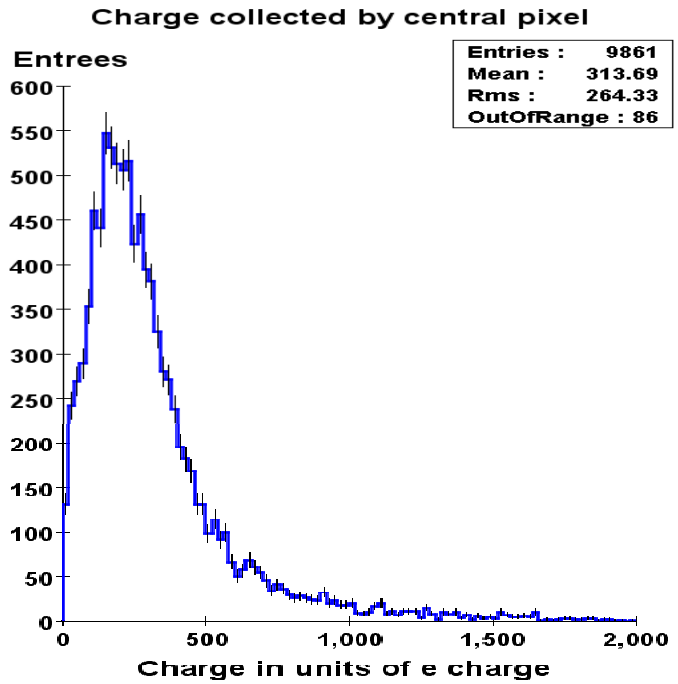
Prototype 2 simulations – charge collection

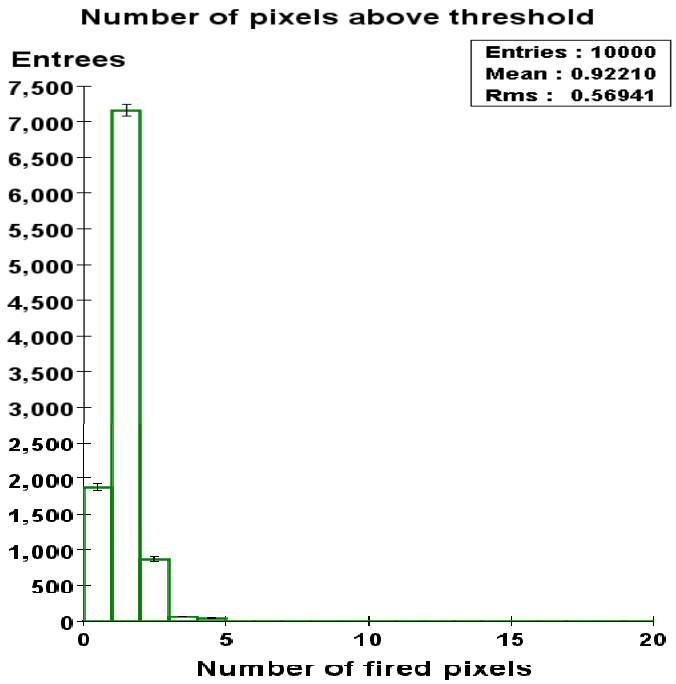




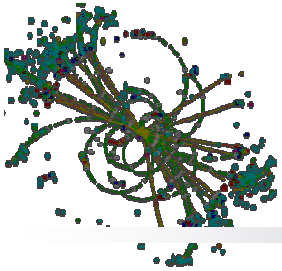
Here are results of charge collection simulation.
On the left is the distribution of number of electron-hole pairs, generated by track in the pixel (generated charge). On the left - amount of collected by all nearby pixels charge. From the numbers charge collection efficiency is 67.8 %

Prototype 2 simulations mip efficiency

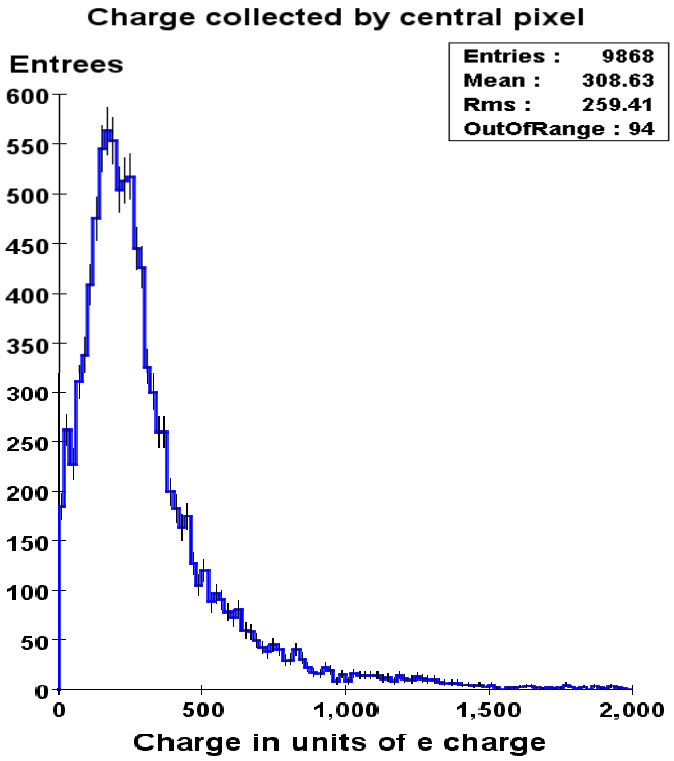


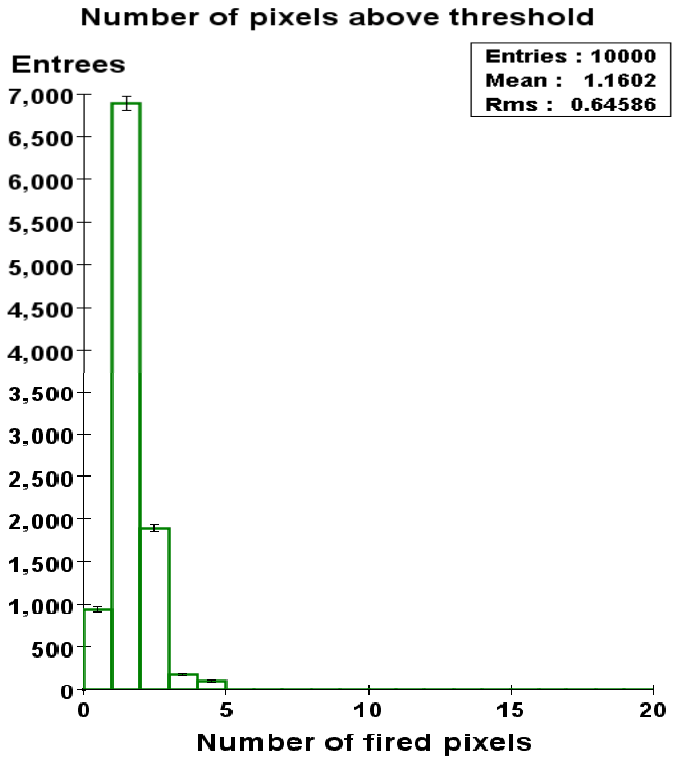


Here are results of mip track registration efficiency simulation.
On the left is the distribution of number of amount of charge, collected in the central pixel in cluster. On the right - number of fired pixels when track passes the sensor with pixel threshold 125 e, which is 5 sigma of noise if its level is 25 e. Number of events with 0 fired pixels is about 18%, so track registration efficiency is 82%.
If we will achieve noise level 15 e we can set lower pixel threshold – see next slide.

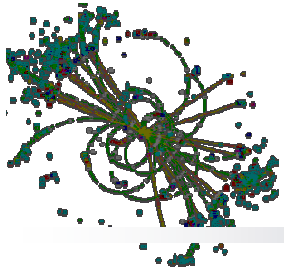


Prototype 2 simulations - continue





The same as on previous slide, but with noise level 15 e (pixel threshold 75 e).
Number of events with 0 fired pixels is about 9%, so track registration efficiency is 91%.



Conclusions

- Simulations show, that second prototype could achieve almost acceptable for final device parameters.
- Expected pixel size 25 x 25 microns is close to what we want.
- One of the important questions – will the new calibration technique work?
- Moving to 65 nm technology is straight forward, no significant development needed and it will lead to 18 x 18 μ pixel size.
- If second prototype tests will confirm our simulation, we may get close to our specification sensor even with standard TSMC process! And if we would like better spatial resolution, we will need only to increase epi layer thickness, which should not be a problem .
- We will need to optimize charge collection electrode size to maximum signal/noise ratio. Probably we can make prototype 2 with 2-3 variations of charge collecting electrode dimensions and compare performance.
- We expect starting prototype 2 tests in the summer of 2012.