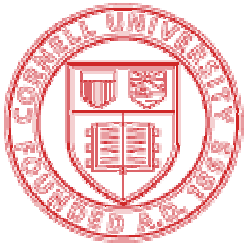
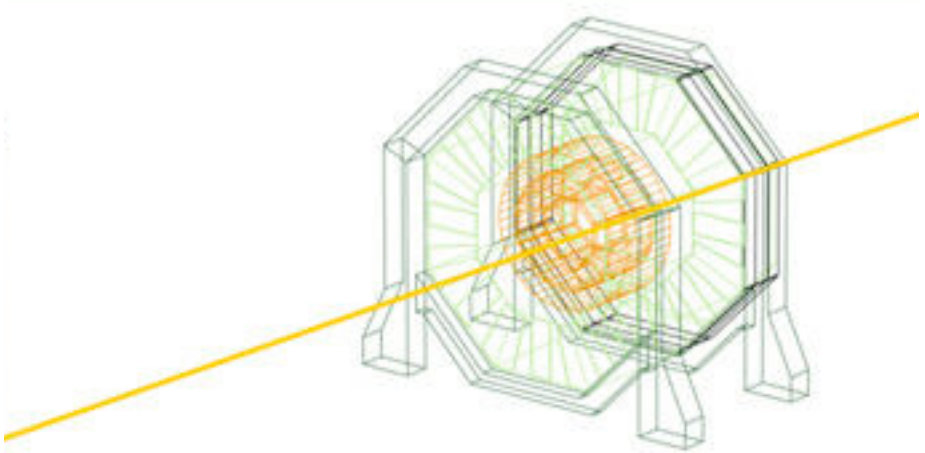


Cornell University
Floyd R. Newman Laboratory for
Elementary-Particle Physics



# 3D Sensors

Julia Thom-Levy
Cornell University

SiD Detector Workshop, SLAC

Dec.14th, 2011

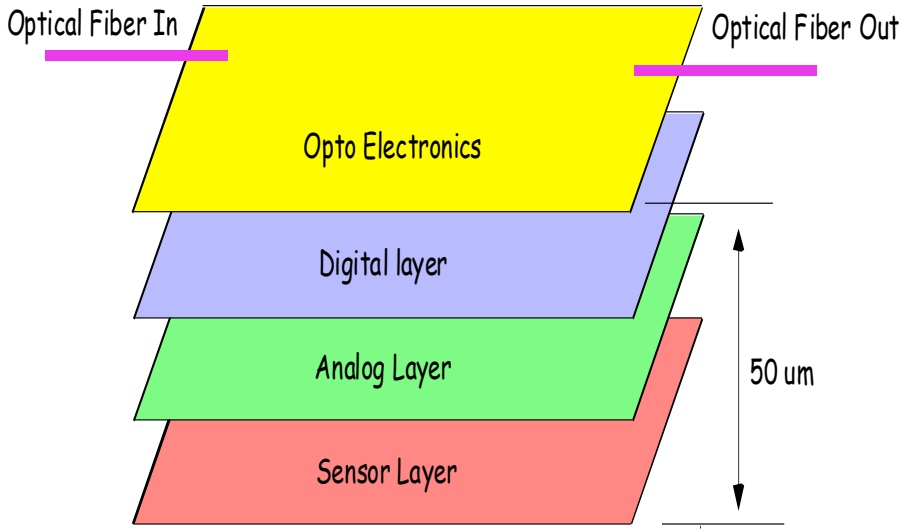
# Outline

1. Vertically integrated circuit technology (3D-IC)
   - Reminder: TSVs, thinning, bonding,…
   - Status of 3D-IC designs completed by FNAL

2. Toward larger area fully active modules
   - Active edge sensors as part of a 3D assembly
   - Initial work on active edge sensor simulations
   - tiles for the SiD forward disks

# 3D-IC technology

2 or more layers (“tiers”) of active semiconductor devices that have been thinned, bonded and vertically interconnected to form a monolithic circuit




Designer's Dream

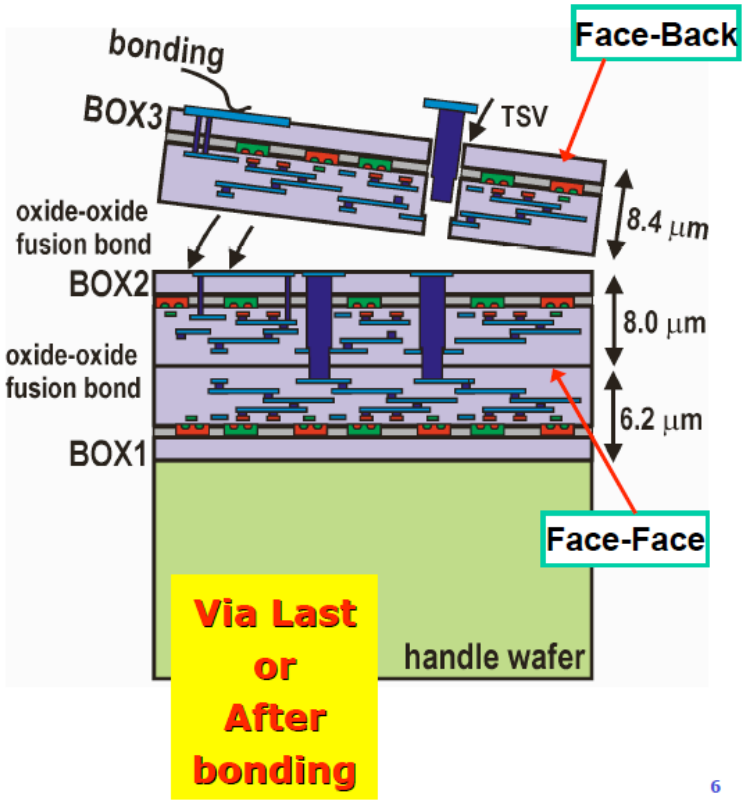
# 3D-IC technology

- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O  pads (less dead area)
  - Technology of each layer can be separately optimized
  - Reduce interconnect power and crosstalk
  - Can increase complexity- more transistors per $cm^2$
  - Process now accessible commercially

- excellent technology to match the tight requirements of high pixel resolution, low power, and low mass for SiD vertex detector

# Emerging key technologies

- Through-Silicon-Via etching (TSV) and metallization
- Wafer thinning (<25μm)
- Precision alignment (<1μm)
- (fusion) bonding of thinned wafers to form a monolithic unit

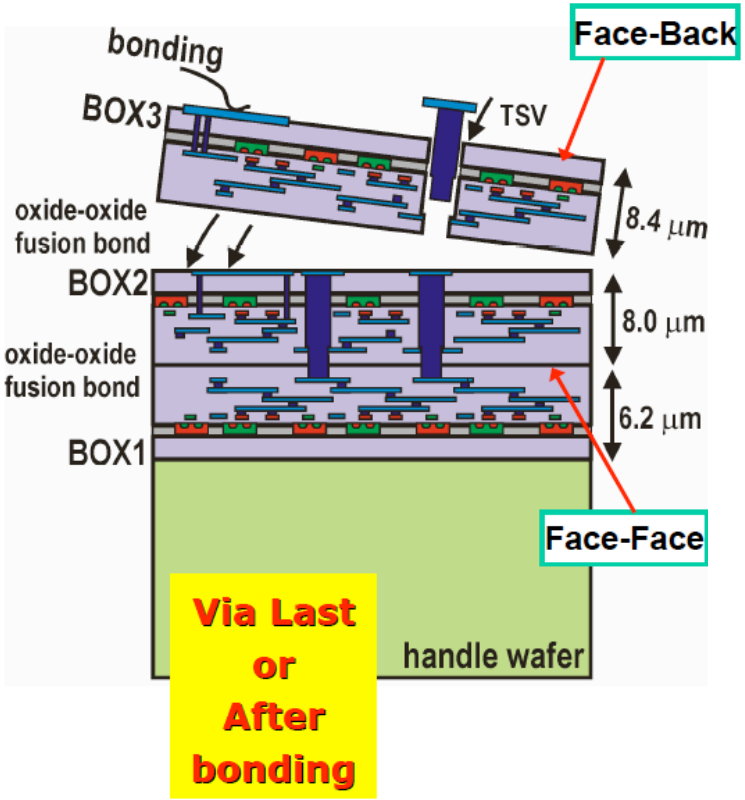


# 3D circuits for HEP at FNAL

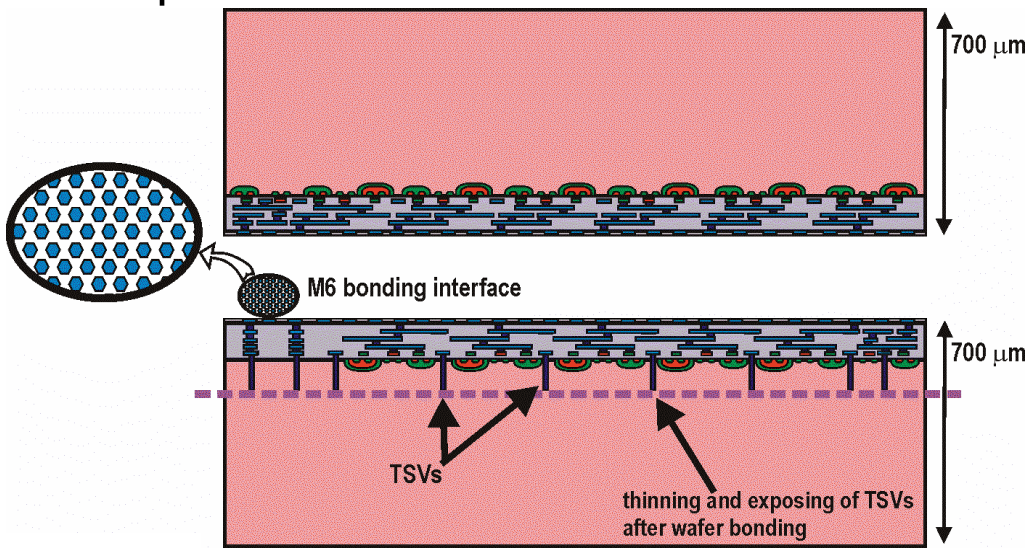
- 2006: FNAL participates in 2 multi-project-wafer runs (MPW), organized by MIT-LL and submitted the VIP (vertically integrated pixel) chip, driven by ILC specs for vertex pixels. Proof of 3D principle
  - MIT-LL: 3 tier fully depleted SOI process
  - Tiers communicate through TSV's
- In 2009, FNAL initiated and organized the first 3D-IC MPW for HEP and related fields
  - Standard CMOS foundry process (0.13 μm), wafers fabricated by Global Foundries
  - 3D processing and stacking done by Tezzaron (IL)
- FNAL contribution to the MPW:
  - VICTR chip (vertically integrated CMS tracker for sLHC)
  - VIP2b (ILC pixels, 8-bit digital time stamp)
  - VIPIC (x-ray spectroscopy)

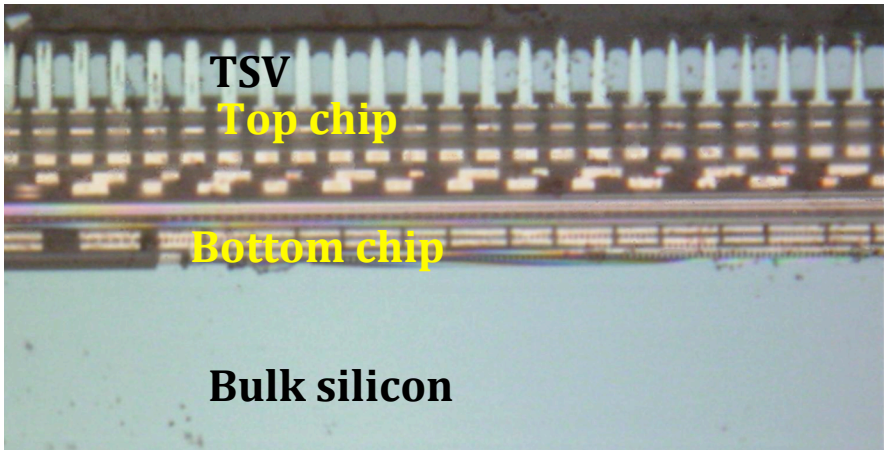
# 3D demonstrator chips

VIP1 and VIP2a chips using MIT-LL process



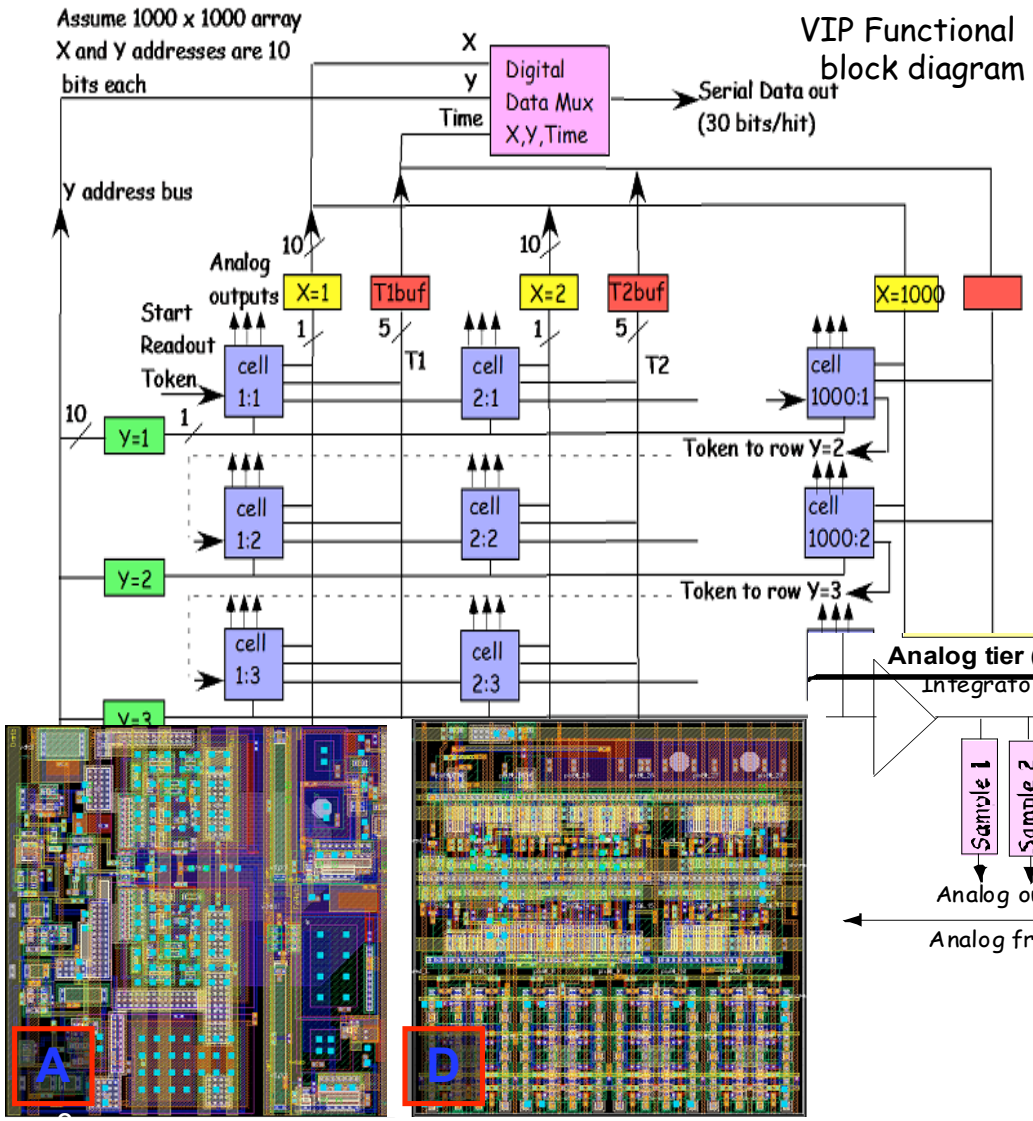

VIP2b uses standard CMOS foundry process:

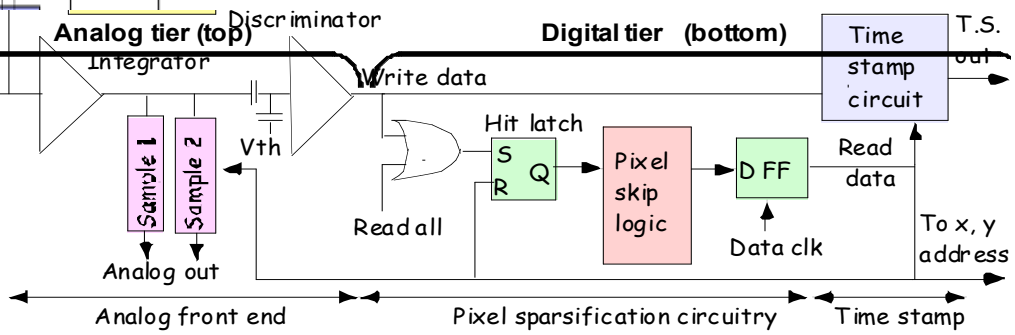


# The VIP2b design

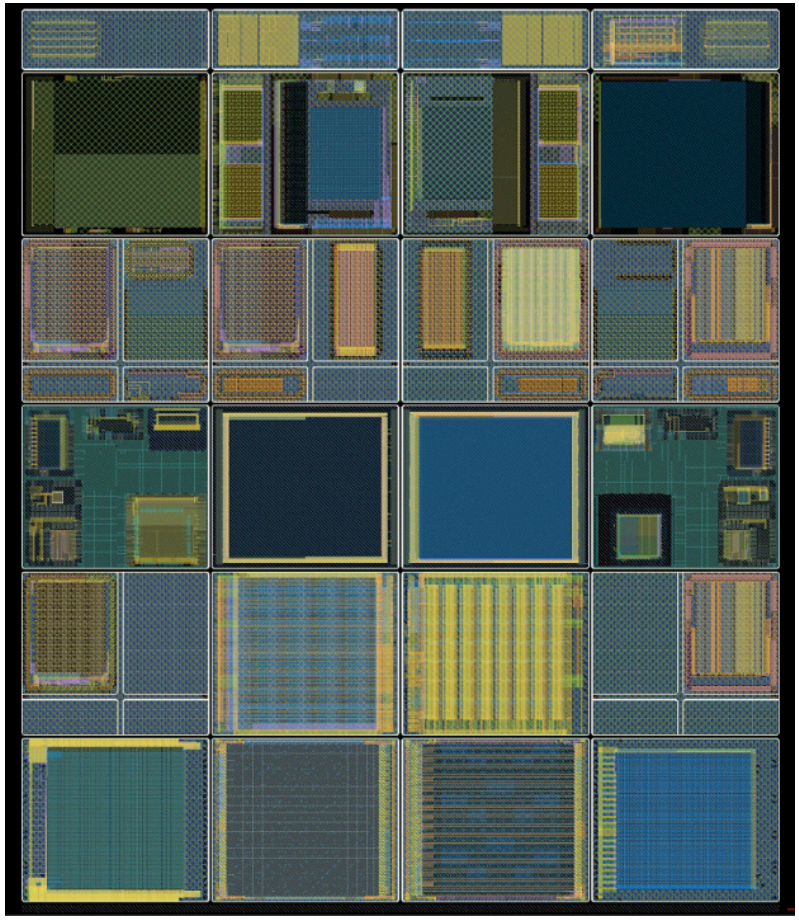
**Design migrated from MIT-LL to Tezzaron 3tier->2tier**




- How it works:
- 192 × 192 array of 24x24 $\mu m^2$ pixels
- 8 bit digital time stamp ($\Delta t$=3.9 $\mu s$)
- Readout between ILC bunch trains of sparsified data
- Sparsification - token passing scheme
- Single stage signal integrating front-end with 2 S/H circuits for analog signal output with CDS
- Analog information available for improved resolution
- Separate test input for every pixel cell
- Serial output bus
- Polarity switch for collection of $e^-$ or $h^+$

First chips from the 3D multiproject run were received in September 2011:



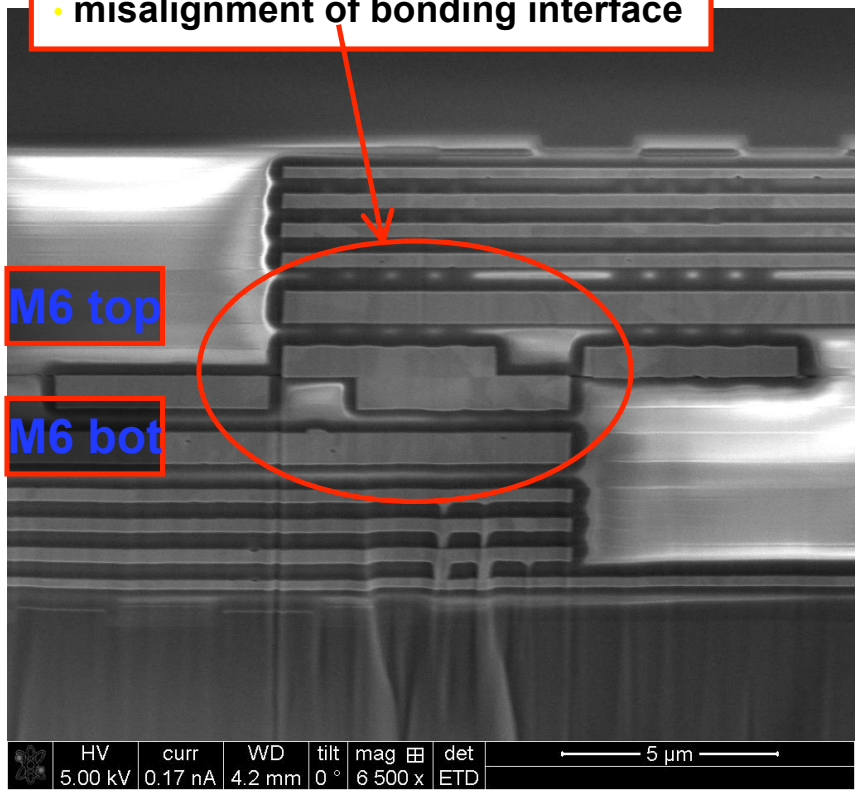
3D Multiproject Reticule


- **Wafer was back-thinned, and back Al pads were deposited, then singulated and distributed**

# Testing of stacked devices: first results

Some 3D circuits performed properly, but problems with pixel interconnects. Cause: substantial misalignment of top and bottom layers

More wafers expected to arrive with the problem fixed

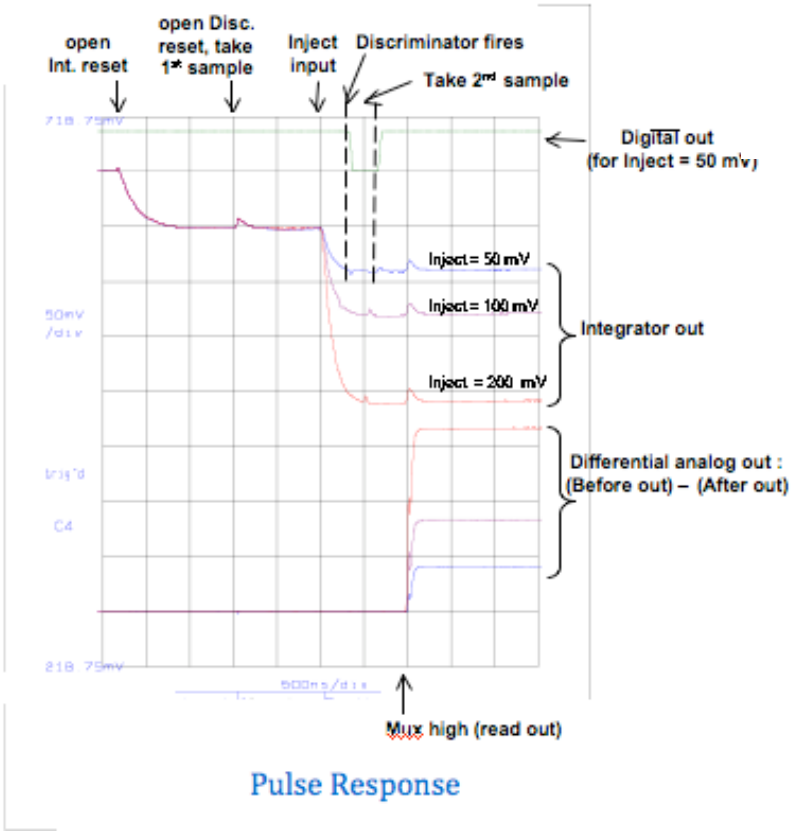



SEM picture courtesy of P. Siddons BNL

Additional 12 wafers started at Global Foundries at Tezzaron expense – due in January 2012.

# VIP2b (analog) test results

## Pulse Response




Pulse Response

## Noise

| Csel | Cin added | Cin + Cinstray | Noise at Inv. Out (mV) | Noise at Inv. Out (e) | Noise at Int. Out (mV) | Noise at Int. Out (e) |
|---|---|---|---|---|---|---|
| 111 | 0 | 12.5 fF | 2.26 mV | 16 e | 0.74 mV | 19 e |
| 110 | 4 fF | 17 fF | 2.58 | 18 | 0.79 | 20 |
| 101 | 8 | 21.5 | 2.84 | 20 | 0.82 | 21 |
| 100 | 12 | 26 | 3.11 | 22 | 0.87 | 22 |
| 011 | 16 | 30.5 | 3.38 | 24 | 0.93 | 23 |
| 000 | 28 | 44 | 4.09 | 29 | 1.04 | 26 |

Bandwidth not very sensitive to Cin

Bandwidth varies with Cin

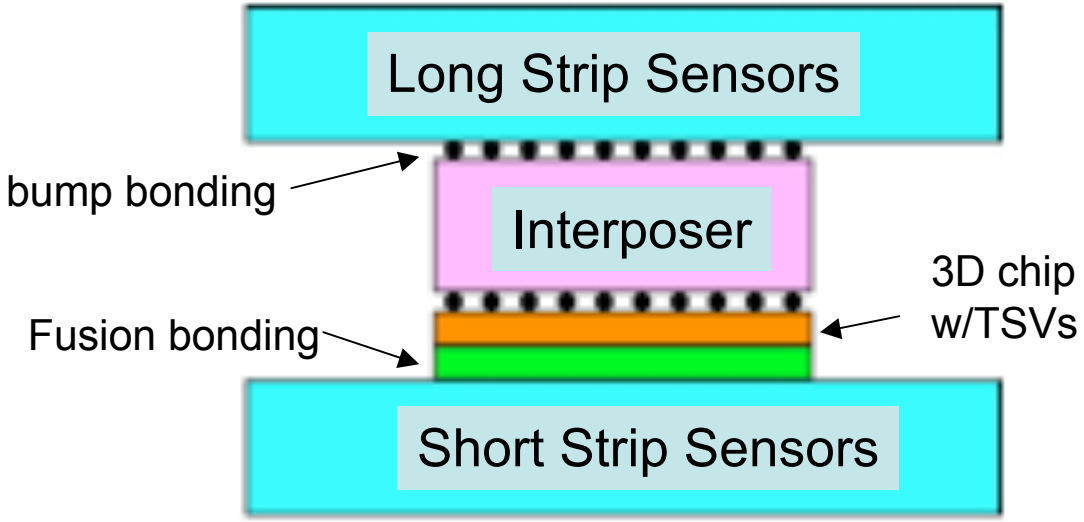
Reasonable pulse response and low noise on VIP2b (analog)

# VICTR (Vertically Integrated CMS Tracker) chip

2 tier 3D device with readout and coincidence circuit. Will be bonded to strip sensor planes, separated by 1mm thick “interposer” that transports signals through vias

• locally collects hits from 2 sensors, finds hit pairs with $p_t$>2GeV for trigger decision on the detector

• transfers data to vector forming circuit, which rejects track vectors with low pt to reduce data rate before transferring data off the detector



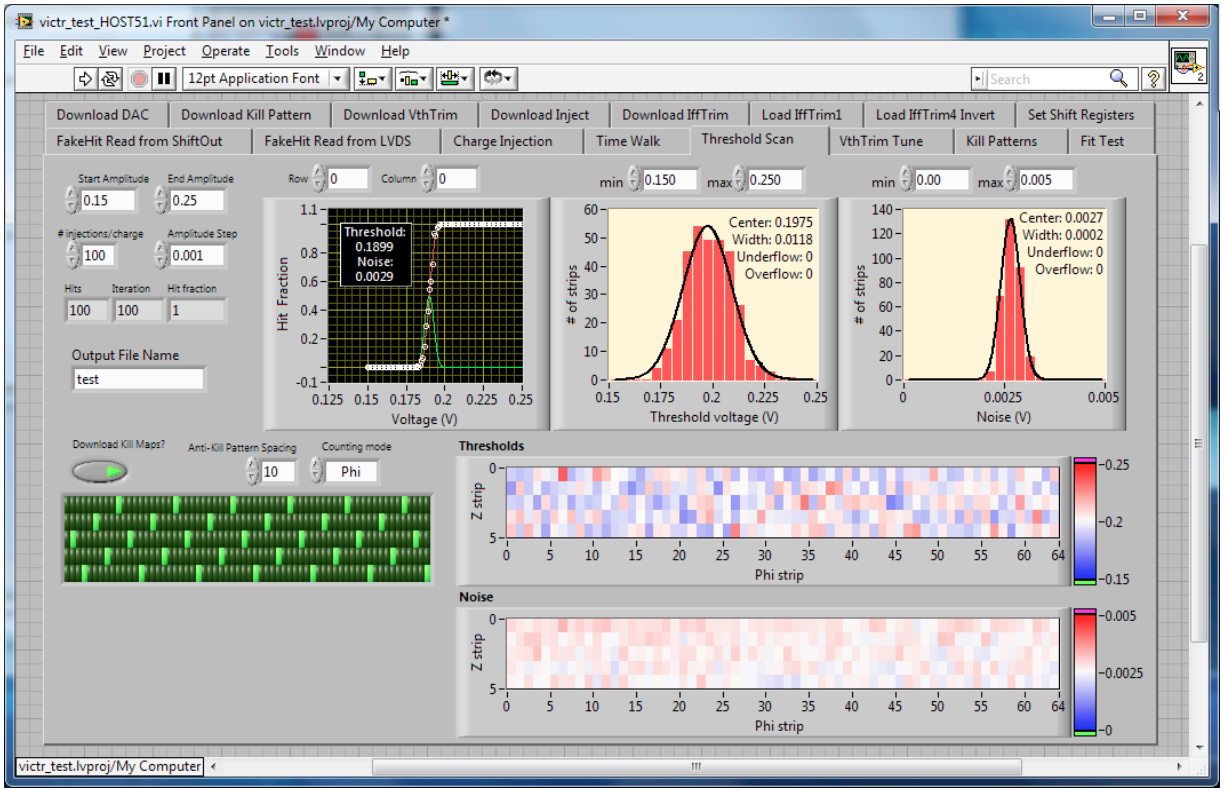
# VICTR testing: first results

We have been able to test most of the VICTR chip

- The two tiers of the VICTR chip could be tested individually only, but chip seems to work well
- Expect that full chip will be OK

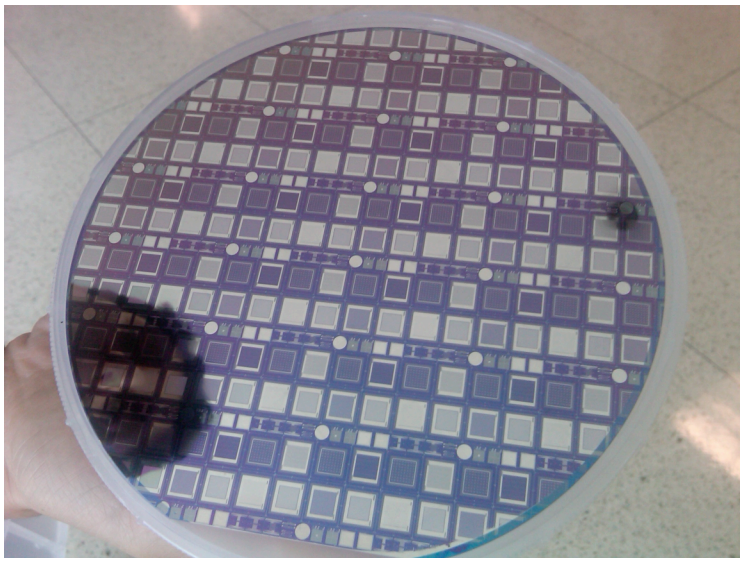
Testing the VICTR chip: time walk measurements, threshold scans and tuning, investigating crosstalk, etc

Labview FPGA Test system at FNAL and Cornell



# bonding to sensors

- Next: bond radiation sensors to the 3D-IC chips
  - VICTR (sCMS track trigger): 2 sensors, “phi” and “z” tiers
  - VIP2b (ILC pixels): array of 192 x 192 pixels, pitch: 24 $\mu m^2$
- Sensors were fabricated at BNL, following rules of special wafer bonding process
  - tested, look good
- Bonding technique: oxide-to-oxide direct bonding, (“DBI”), process developed by Ziptronix



**BNL Sensor Wafer**

# Summary Part 1

- Active program of 3D-IC applied to HEP
  - FNAL pioneered 3D-IC application for HEP
- Design and assembly of 3D devices is challenging, but
  - demonstrator chips work well
  - current problems with misalignment are being worked out
  - other (more difficult) parts of processing fully proven: back-grinding down to TSVs' tips, deposition and patterning of back Al, etc
- Commercial Si brokers have made 3D chips available
  - Significant step towards making this technique viable for detector applications

# The next step: larger area modules

- Size of 3D devices I've talked about so far is determined by reticule size
  - Sub-micron CMOS electronics dictates ~2x3 cm
- If we want to bond to a larger area sensor there is a very serious issue of yield (i.e. many small chips bonded to large sensor)
  - Smaller sensors are problematic because saw edges cause leakage currents- active area constrained to distance from the edge 2-3 times the thickness, causing dead area
- How to make larger area fully active modules?

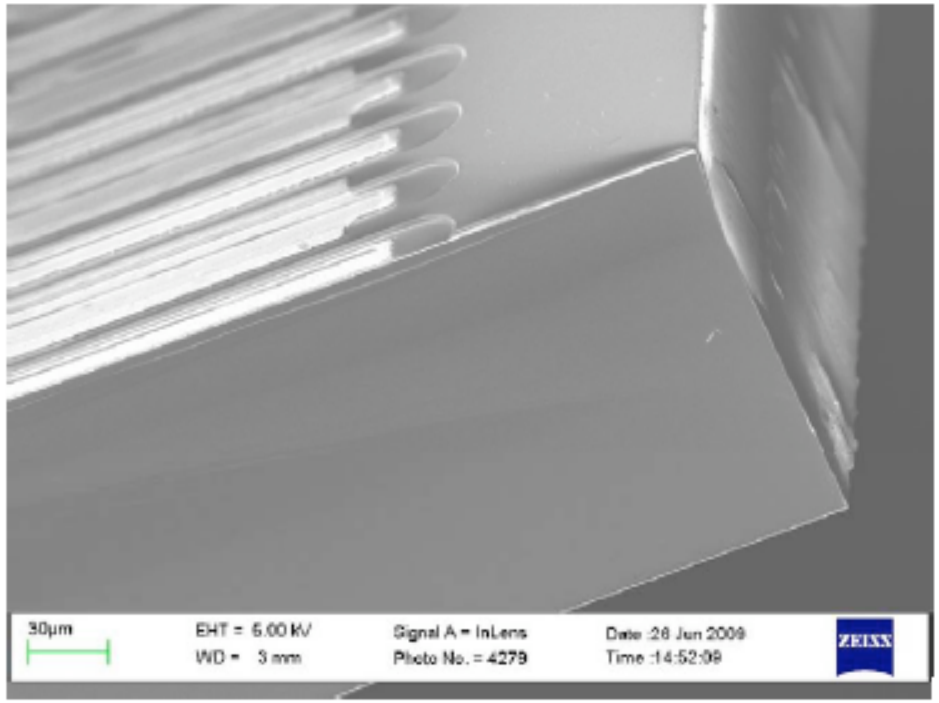
➔ active edge sensors

# Active Edge Sensors

- Active edge technology was developed as part of 3D detector R&D and uses the same deep etching and implantation technologies

- Ion etching can produce an “atomically smooth” edge – small leakage and sensitive to within a few microns of the edge (compare to 3x thickness of conventional sensors due to leakage currents)

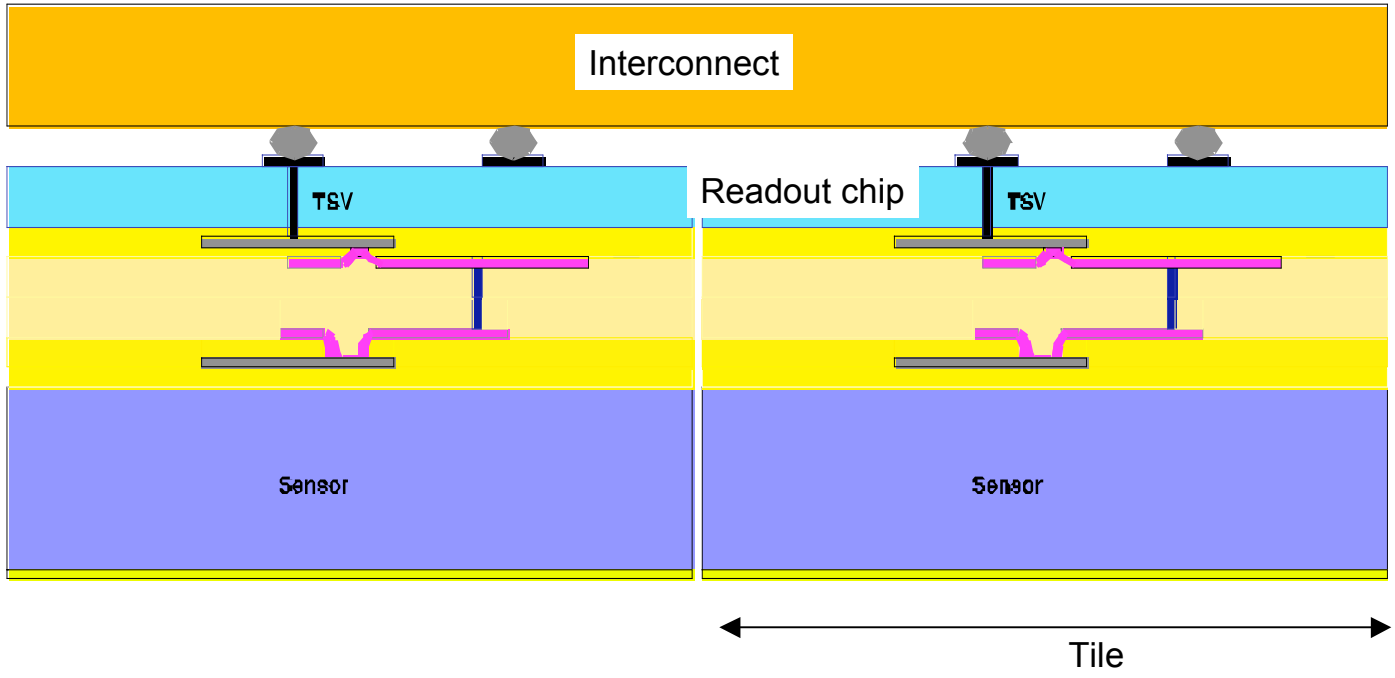
*Eraenen, Kalliopuska et al,NIM A 607 (2009) 85-88,*




VTT (Tech.Research Center, Finland) has demonstrated devices mounted on silicon-on-insulator substrates which allows processing thin sensors

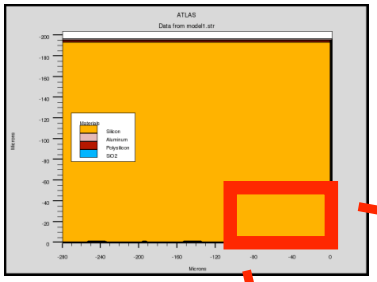
# An integrated sensor ROIC structure

Idea: oxide bond edgeless sensors with 3D readout chips to provide integrated sensor/readout tiles that can be tested before assembly into a module (➔yield)

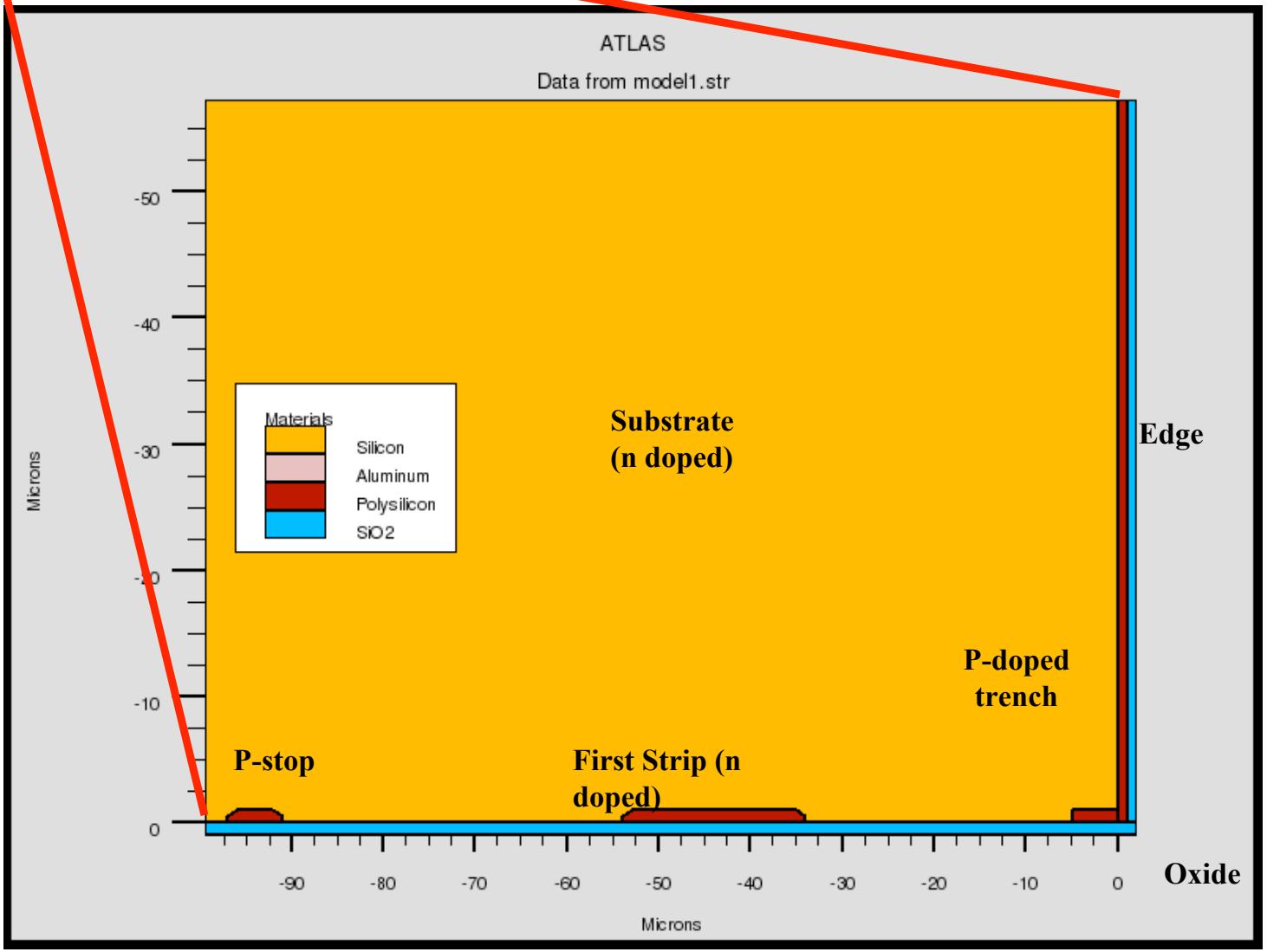


# An integrated sensor ROIC structure

- FNAL has an order with VTT to fabricate active edge sensors and an order with Ziptronix for oxide bonding
  - First step: use these with 3D test wafers to demonstrate the concept of fully active tiled arrays which could achieve high yields and small dead areas
- starting p-on-n sensor design phase.
- our group at Cornell is doing simulation work to support the sensor design phase:
  - investigate leakage current, breakdown voltage, interstrip resistance and other electrical properties of the sensor
  - how do they depend on the placement of p-stops, strip pitch, etc



Started with microstrip detector detailed in
*NIM A 607 (2009) 85-88*

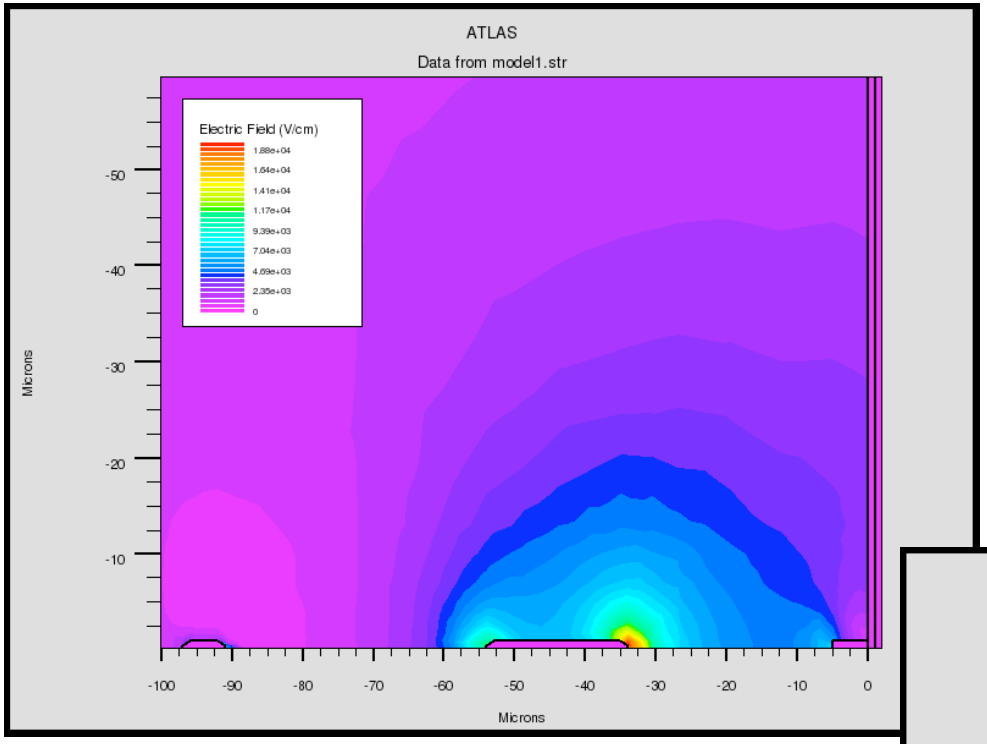


# The Simulation

SILVACO

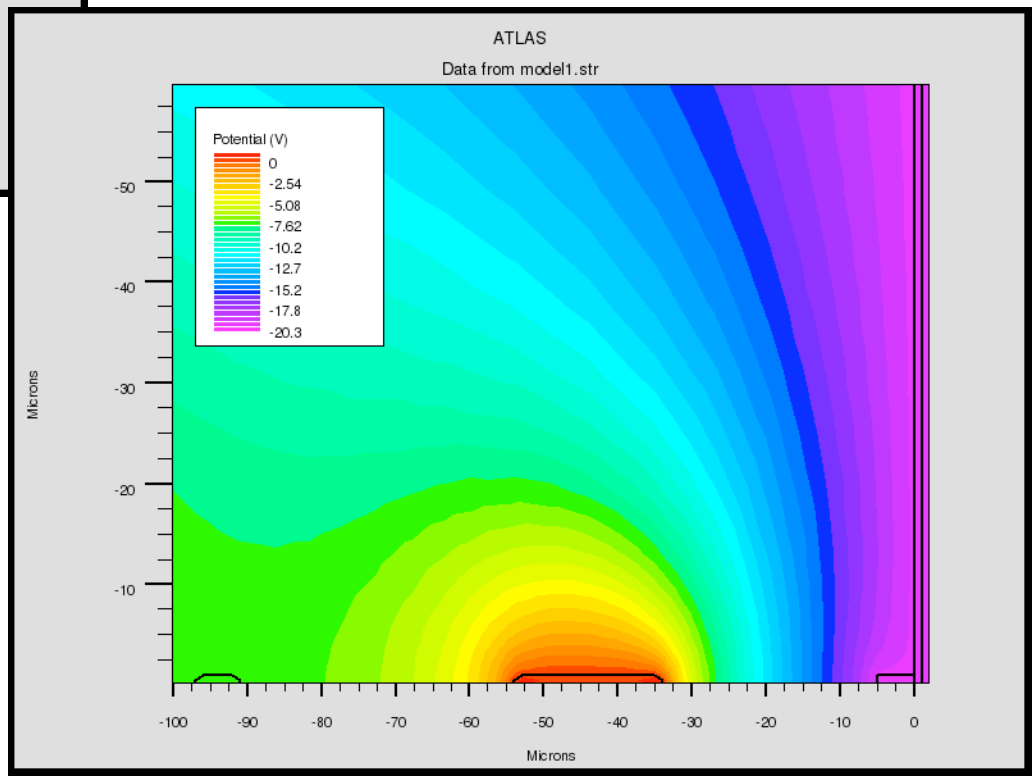
- Commercial Silvaco software, a process and device simulation, places a negative voltage on the base of the wafer and solves Maxwell's equations along with a charge conservation equation on a grid of points to approximate the true solution.
- The solution includes information on voltage, electric field, electron and hole density, current density, etc for each grid point
- The simulated volume is 197 μm (wafer thickness) by 280 μm (including the first three strips) by 100 μm

# Electric field, Potential



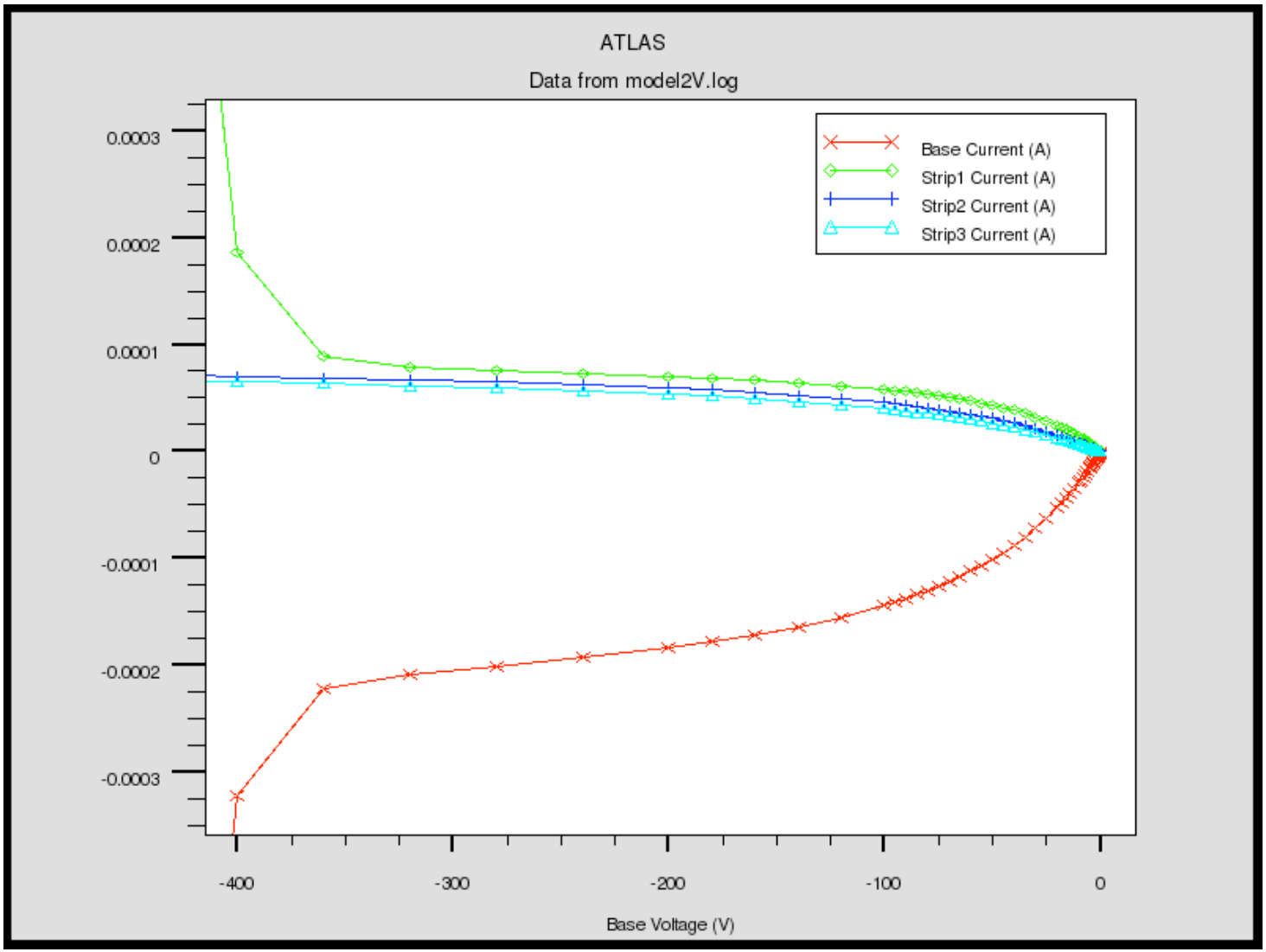

E field (0-10kV/cm)

Potential (0-20V)



# IV curves

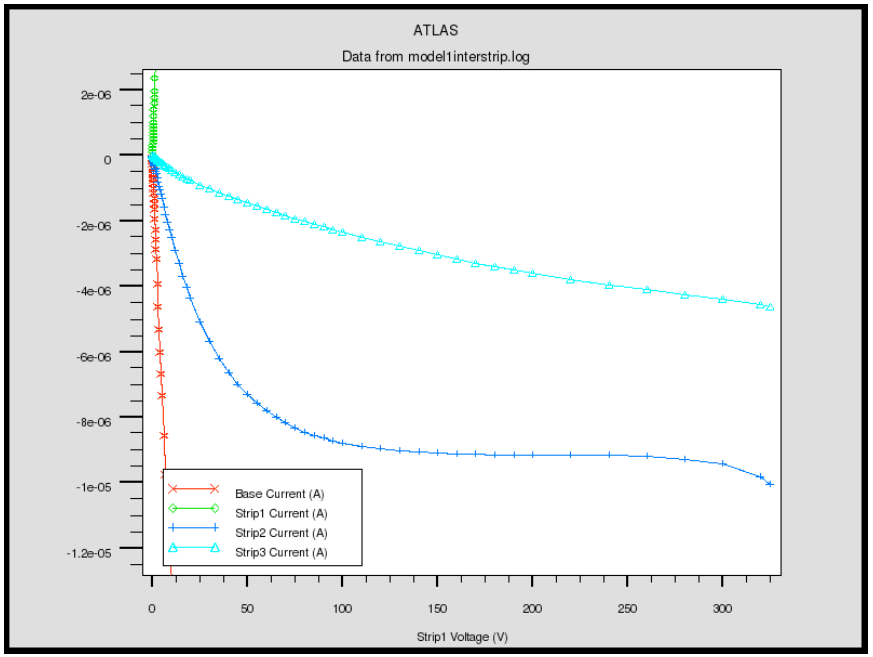
Initial studies show that breakdown voltage does not vary much if we change edge distance and p-stop placement by 10's of microns



# More about simulation work

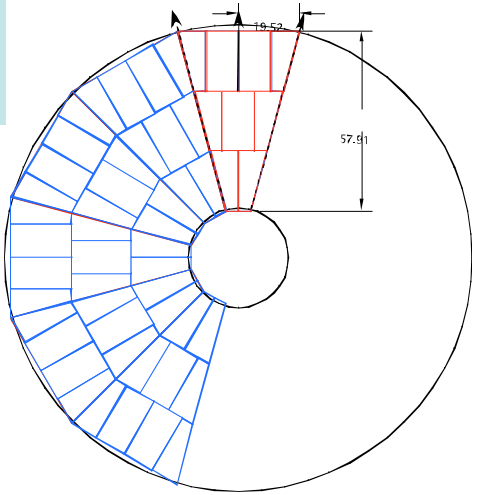
- Also investigating of interstrip resistance and leakage currents
  - Important to correctly model the device in 3 dimensions- still working on it.
- Once a realistic simulation is established, can use it to guide design of sensor.

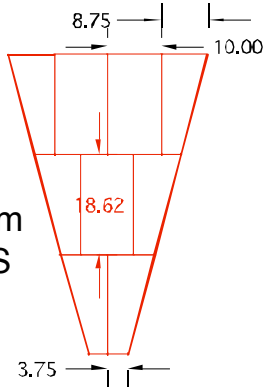
Apply voltage on first strip to determine interstrip resistance: compare to experimental values.



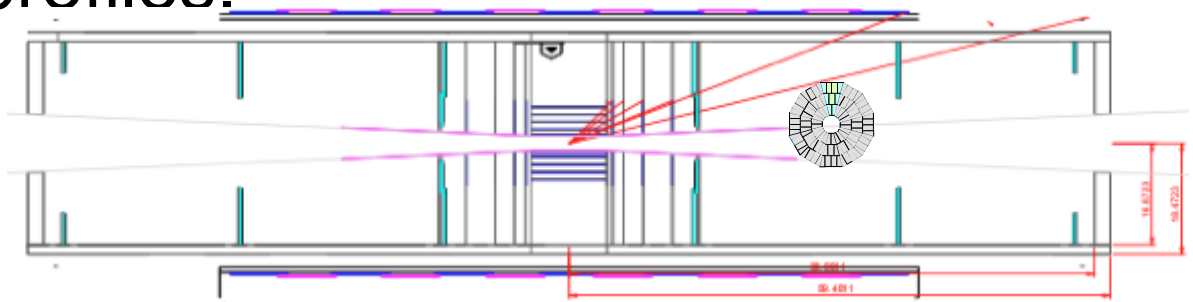
# Forward Disks

- Forward disks for SiD are a good example of how tiles can be used. Two or three types of tiles can be used to form a wedge – wedges are then assembled to form disks.
- Active edge trenches can be any shape – generate needed chip profiles.






Example of a disk formed from 2 types of CMOS or 3D sensors



# Summary Part 2

- Active program of 3D-IC applied to HEP
  - FNAL pioneered 3D-IC application for HEP
- Design and assembly of 3D devices is challenging, but demonstrator chips successful overall
- Plans for bonding to edgeless sensors, design and simulations underway
- Forward  disks at SiD are a good example of how integrated sensor/readout tiles can be used to form suitable dead-space less active pixel detectors.

# Backup Material

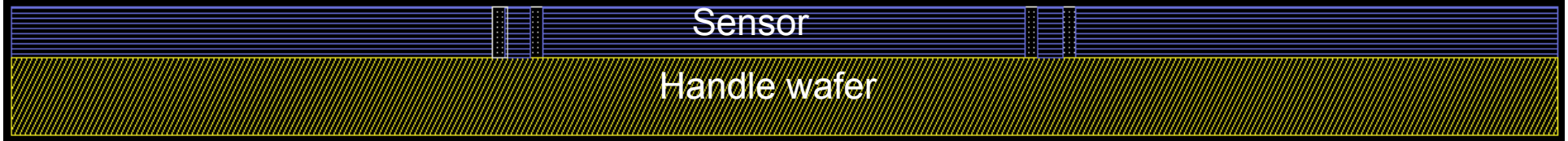
# Fabrication Flow

Start with separate readout and sensor wafers

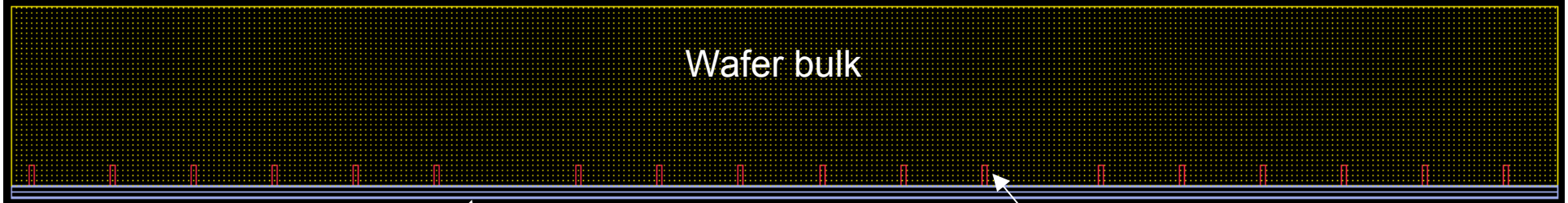
Trenches

Active edge Sensor wafer

Form trenches in SOI sensor wafer

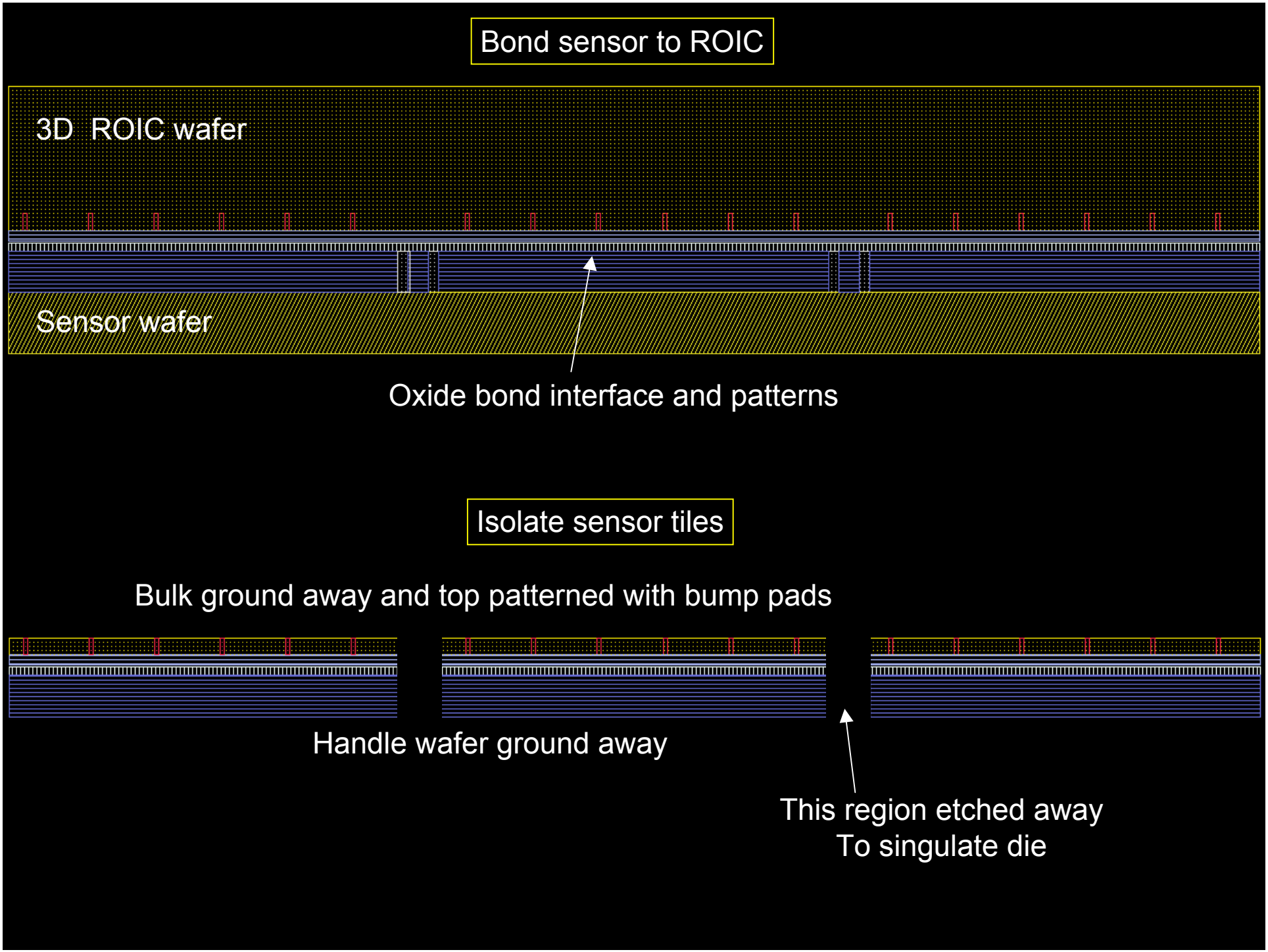



3D ROIC wafer



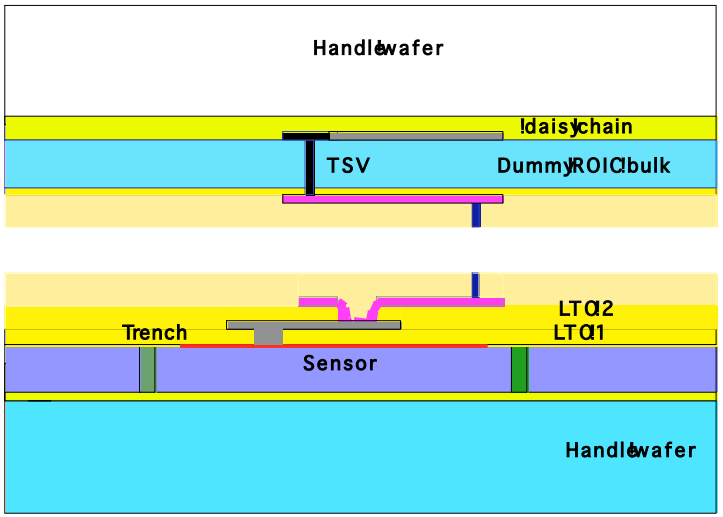

Circuitry

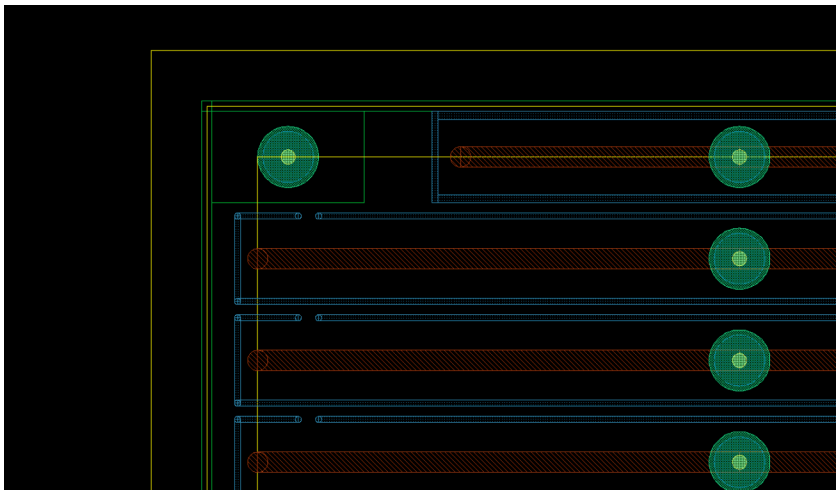
Through silicon vias


Bond sensor to ROIC
3D ROIC wafer
Sensor wafer
Oxide bond interface and patterns
Isolate sensor tiles
Bulk ground away and top patterned with bump pads
Handle wafer ground away
This region etched away
To singulate die

# Active Edge Sensors

- We have an order with VTT to fabricate active edge sensors and an order with Ziptronix for oxide bonding
- These would be used with 3D test wafers to demonstrate the concept of fully active tiled arrays which could achieve high yields and small dead areas
- Starting p-on-n sensor design phase.
- Cornell is doing simulation work to support the design phase

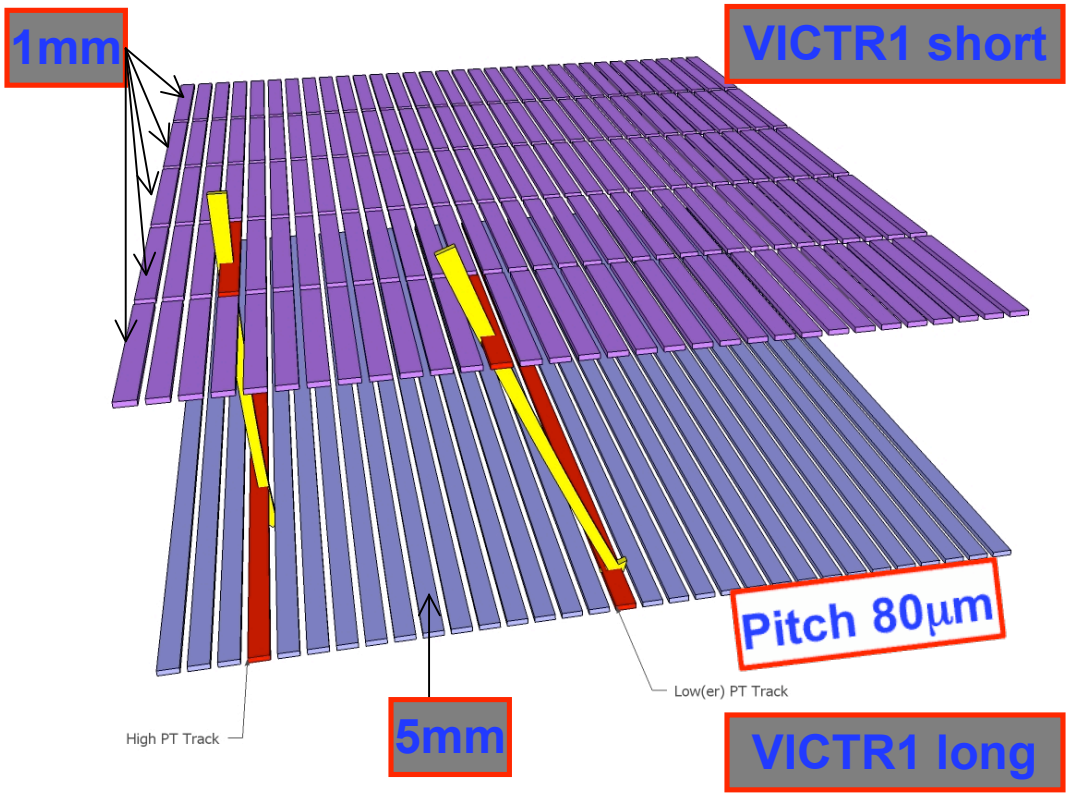


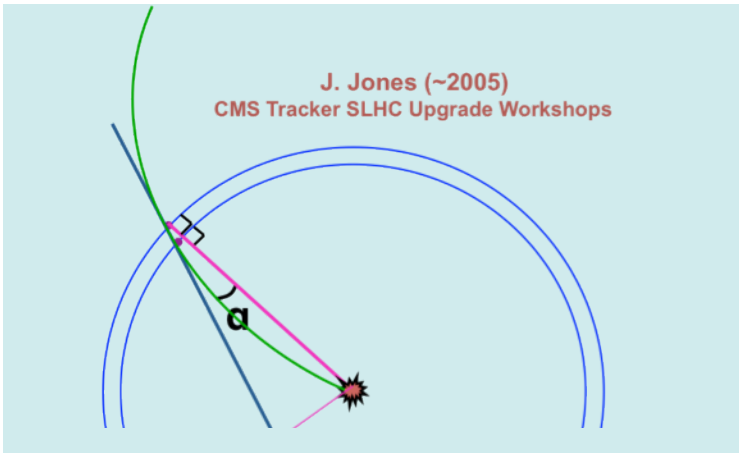



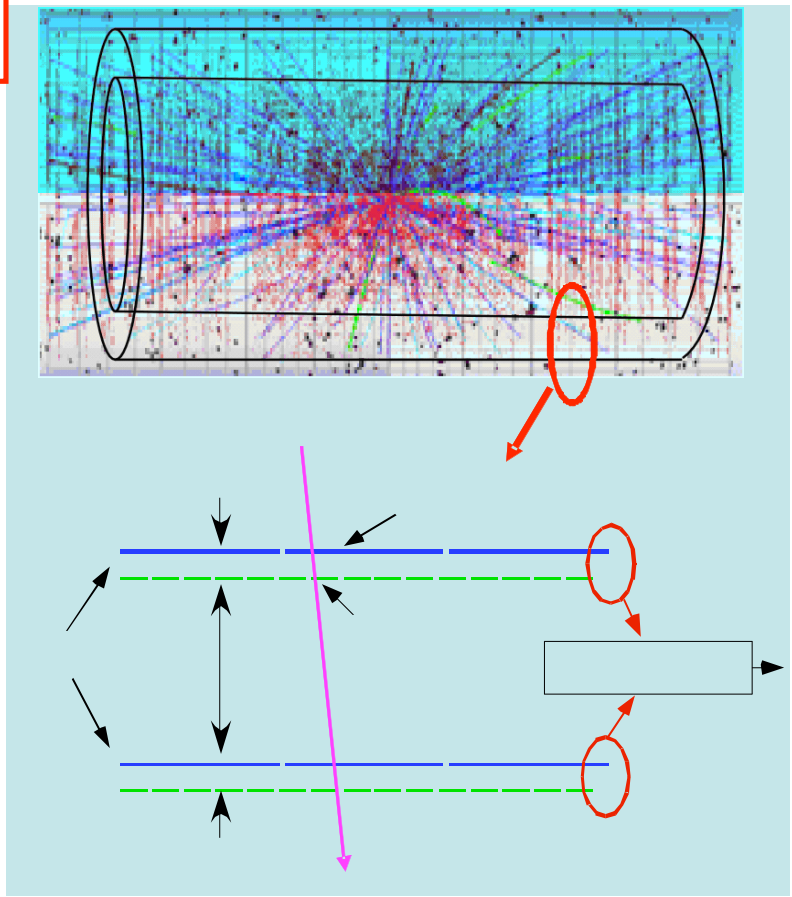
# Fermilab MPW: VICTR

- Vertically Integrated CMS Tracker
- VICTR is response to need of much higher selectivity for trigger at HL LHC

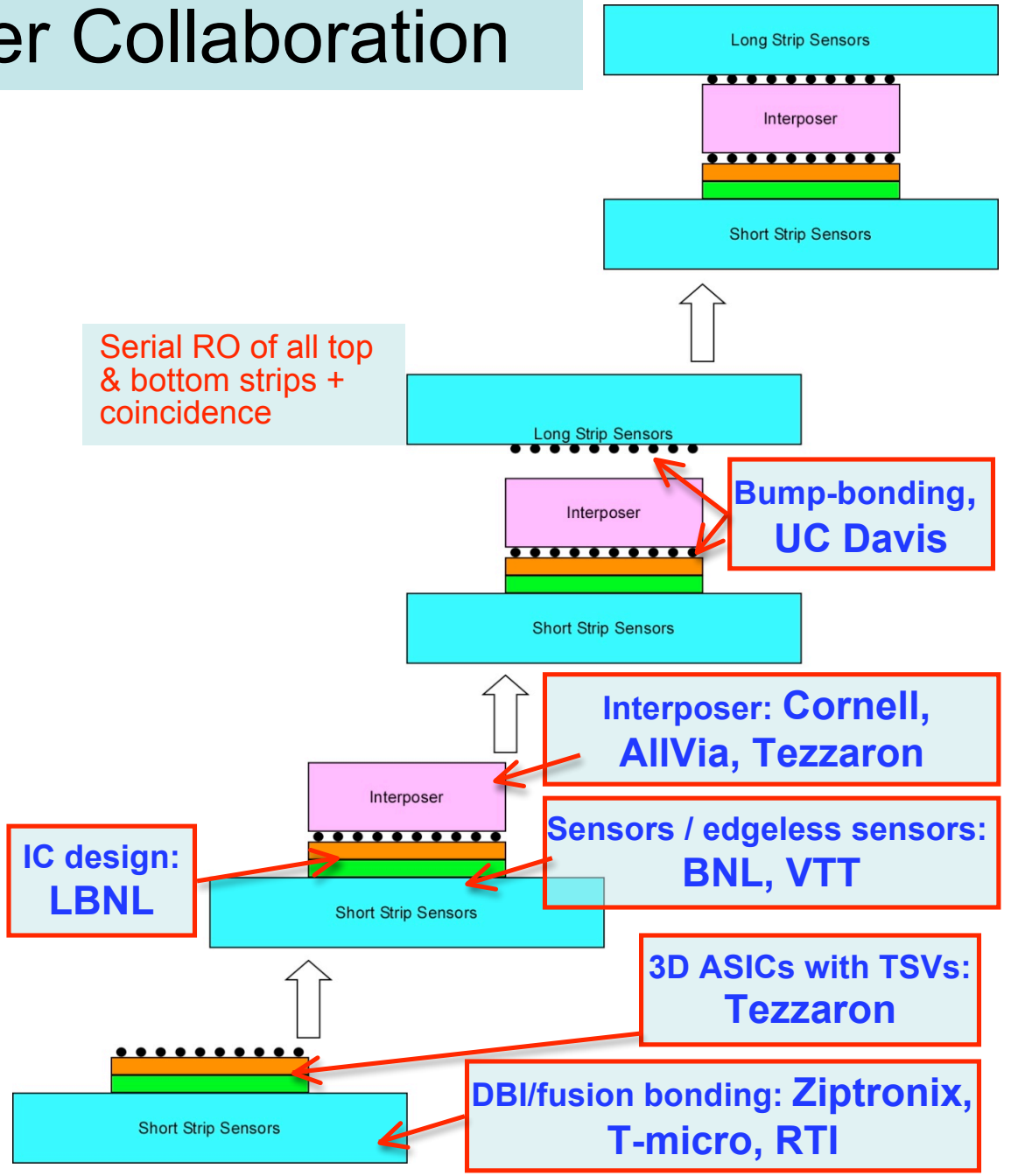
**Proposed idea: to discriminate on tracks of $p_T$ exceeding threshold (bent of track in B-field)**



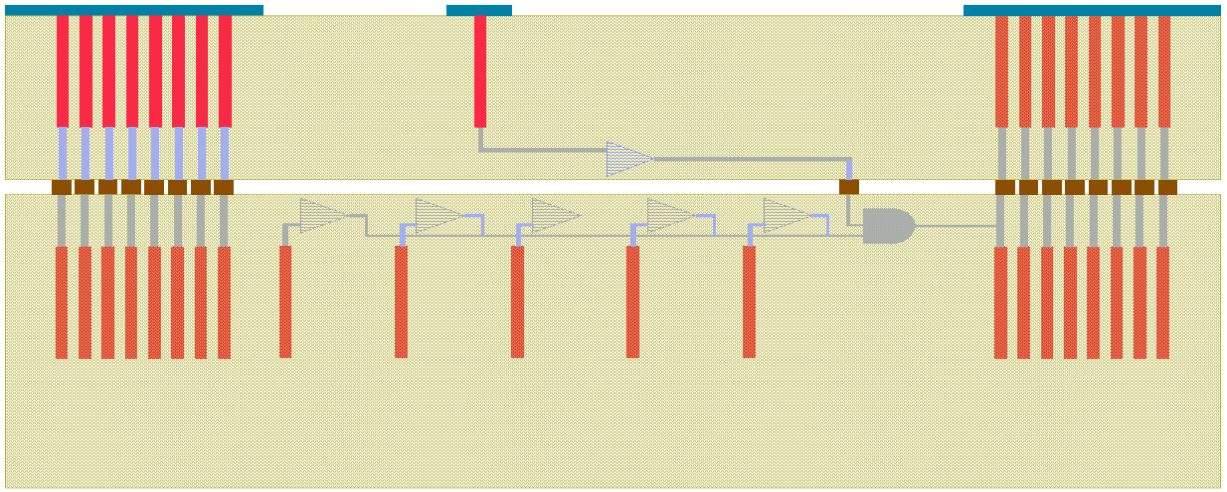
# Track Trigger Collaboration

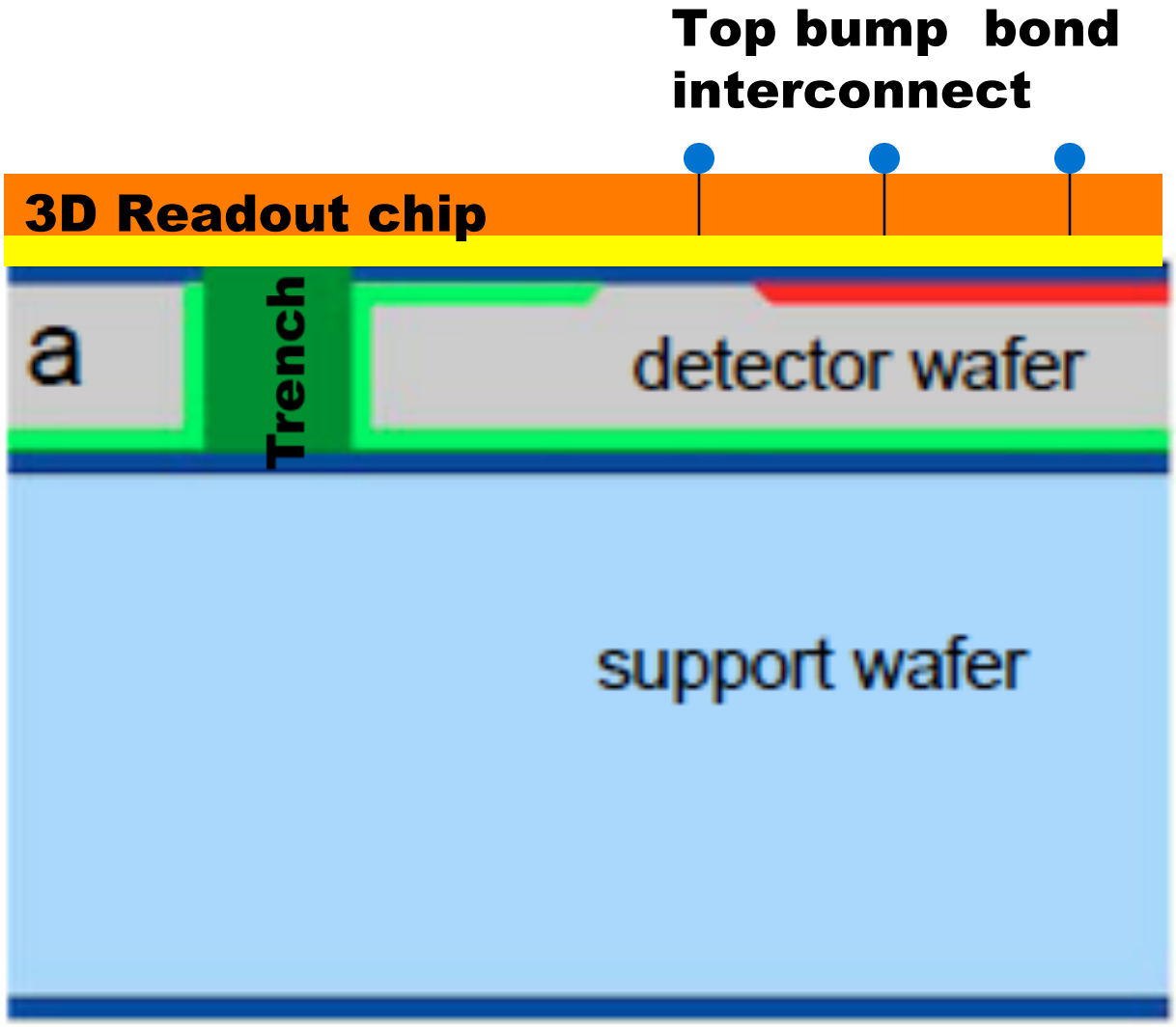


Top Chip

Circuit layers

Bottom Chip

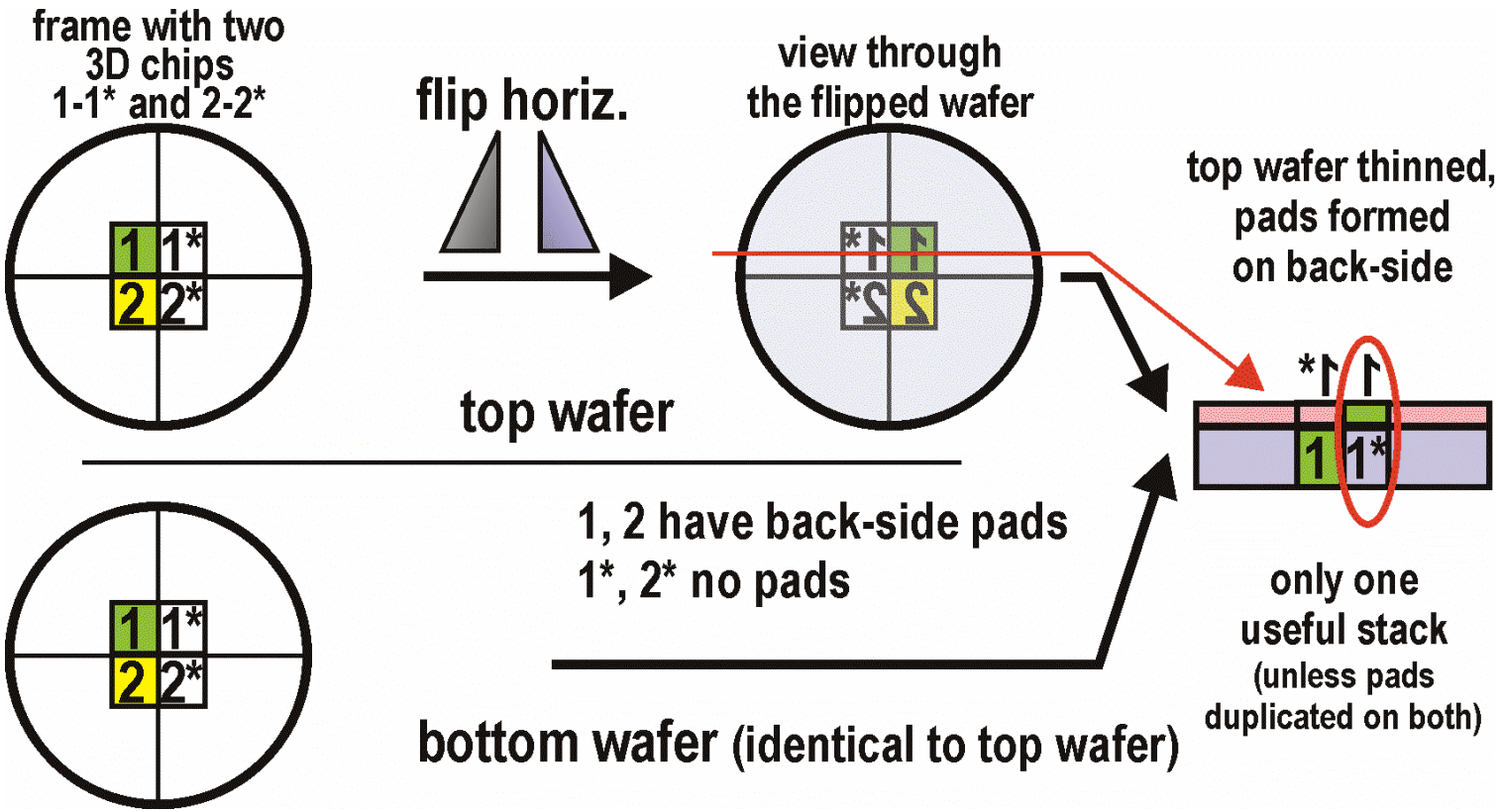



Top bump bond interconnect
3D Readout chip
a
Trench
detector wafer
support wafer

(VTT)

# FNAL's 3D MPW approach

Single mask, top and bottom chips on the same reticule:



# VICTR (Vertically Integrated CMS Tracker) chip