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Developments of Readout ASIC for FPCCD vertex detector

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I would like to present the resent developments of the readout ASIC for FPCCD vertex detector at ILC. Using Fine Pixel CCD(FPCCD) for the vertex detector is one of the attractive options for realizing ILC's physics. FPCCD uses a pixel size of 5×5um2 , which enables high position resolution. However also causes the total number of read out pixels to become extremely large (20,000x128pix/ch). These total number of pixels must be readout in the inter beam-beam time(200ms). This poses strict constraints on the readout system concerning speed, noise level and power consumption. I will report on the results of the resent developed readout system as well as the status of the new developing readout system and how they meet these demands.

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