Towards a technological prototype of the SiW Ecal

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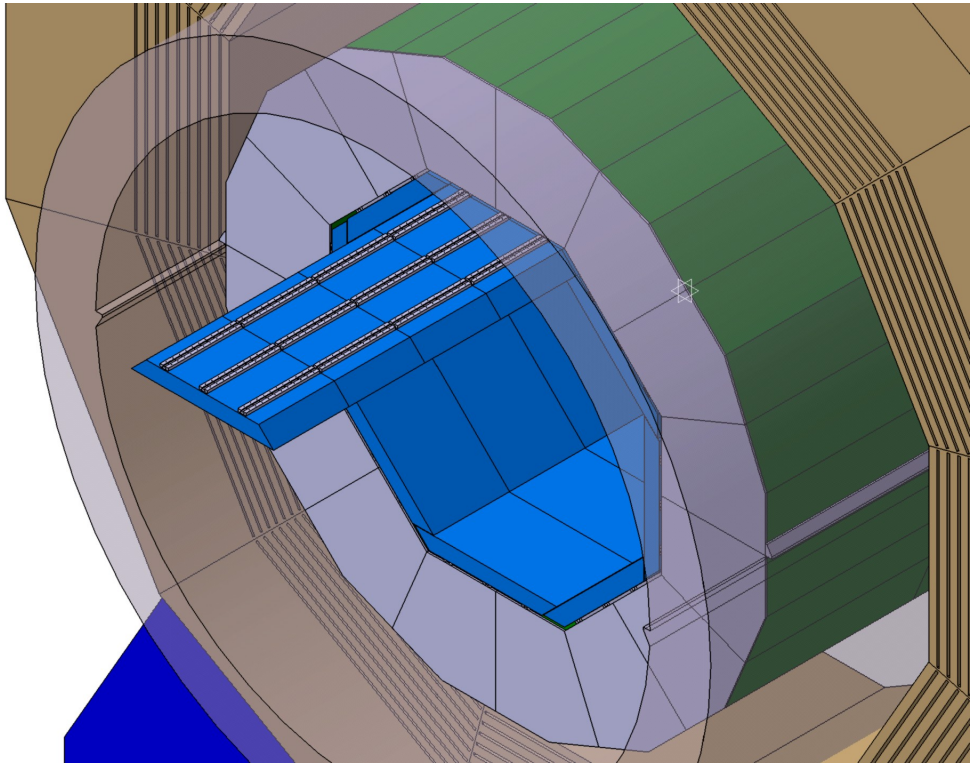
LAL Orsay

KILC Daegu/Korea September 2011

SiW Ecal - Basics

The SiW Ecal in the ILD Detector



Basic requirements

- Extreme high granularity

- Compact and hermetic

Basic choices

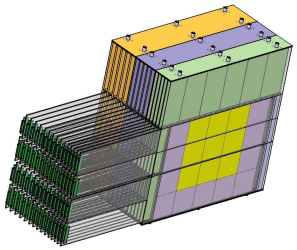
- Tungsten as absorber material
  - X_0=3.5mm, R_M=9mm, λ_I=96mm
  - Narrow showers
  - Assures compact design

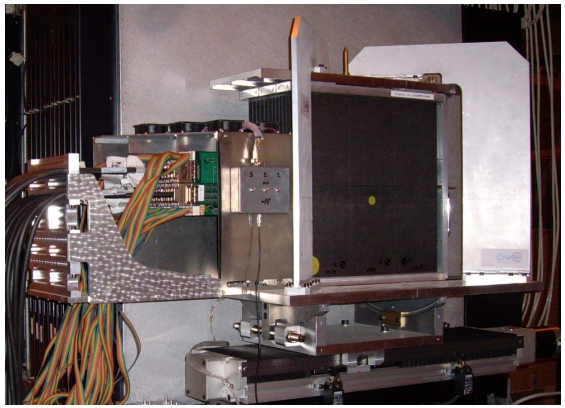
- Silicon as active material
  - Support compact design
  - Allows for pixelisation
  - Large signal/noise ratio

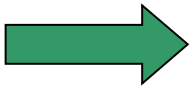
SiW Ecal designed as particle flow calorimeter

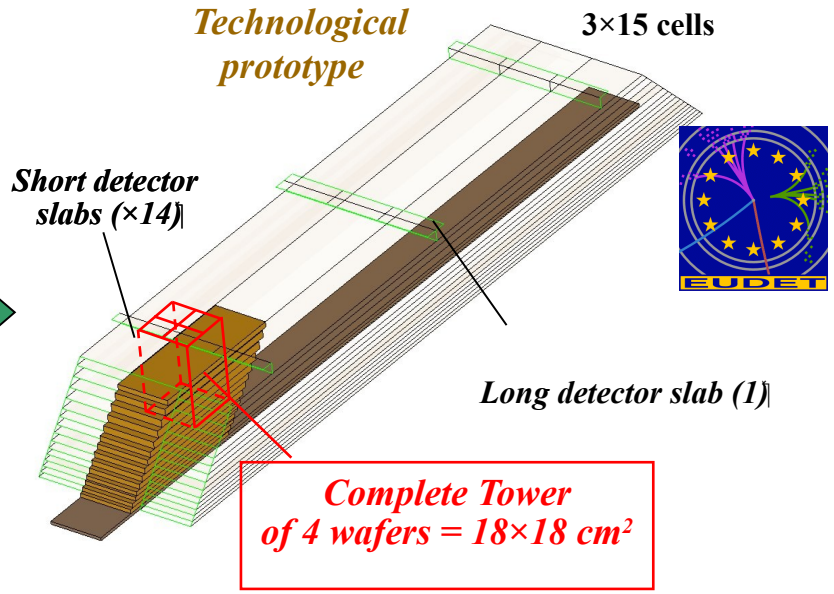
Technological prototype

Technical solutions for the/a final detector





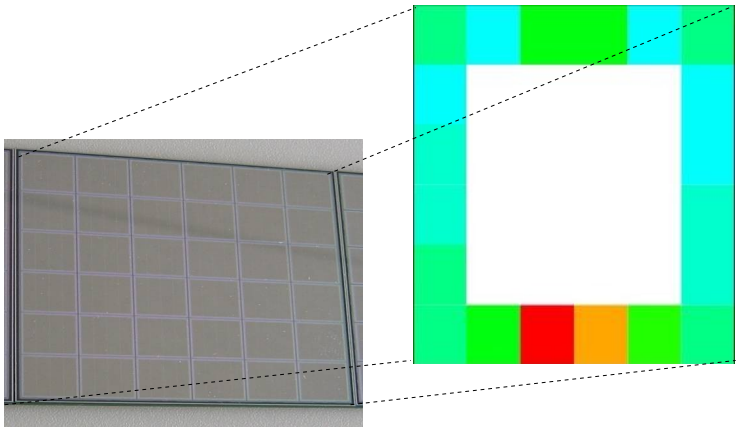




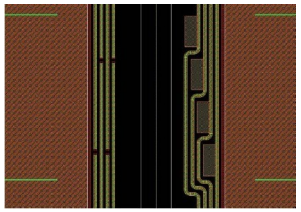
- Realistic dimensions
- Integrated front end electronics
- Small power consumption
  Power pulsed electronics
- Construction, beam tests 2010 - ...

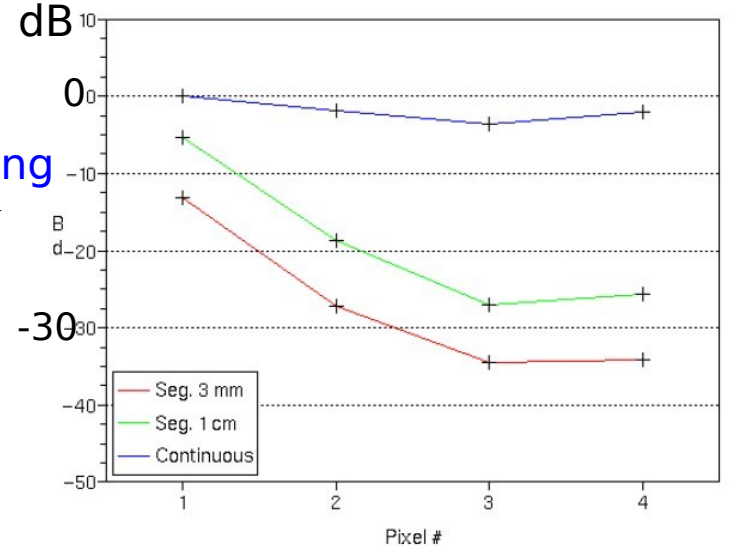
R&D for silicon wafers

Square pattern in wafer response



Segmented guardring



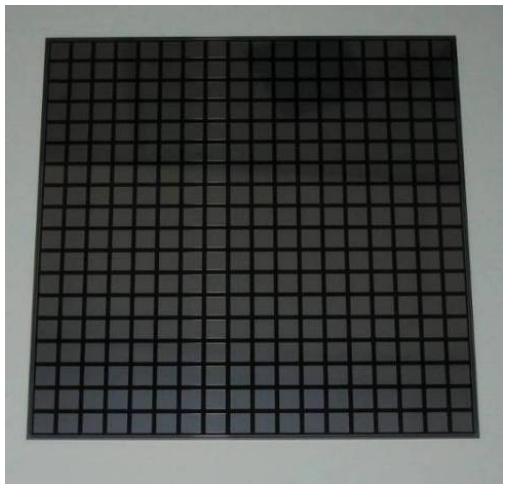


Xtalk continous guardring <-> Pixel

Attenuation of Xtalk

Beyond the physics prototype

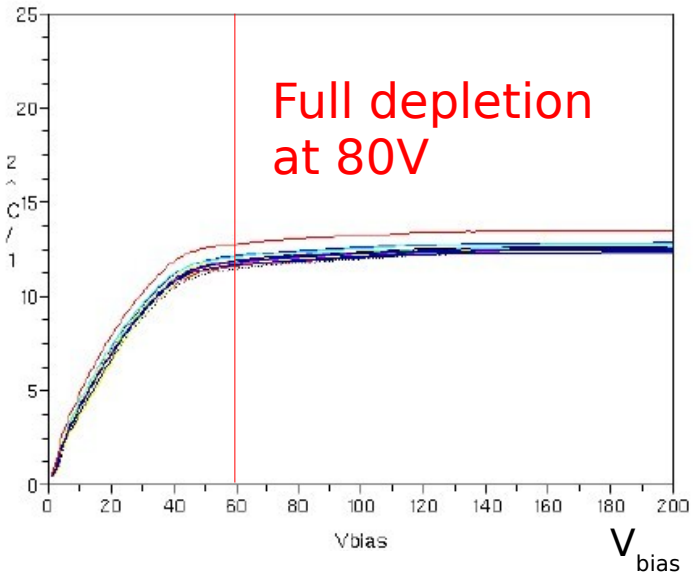
Wafers with smaller pixels



5x5 mm² pixels
~optimal “ILD width”

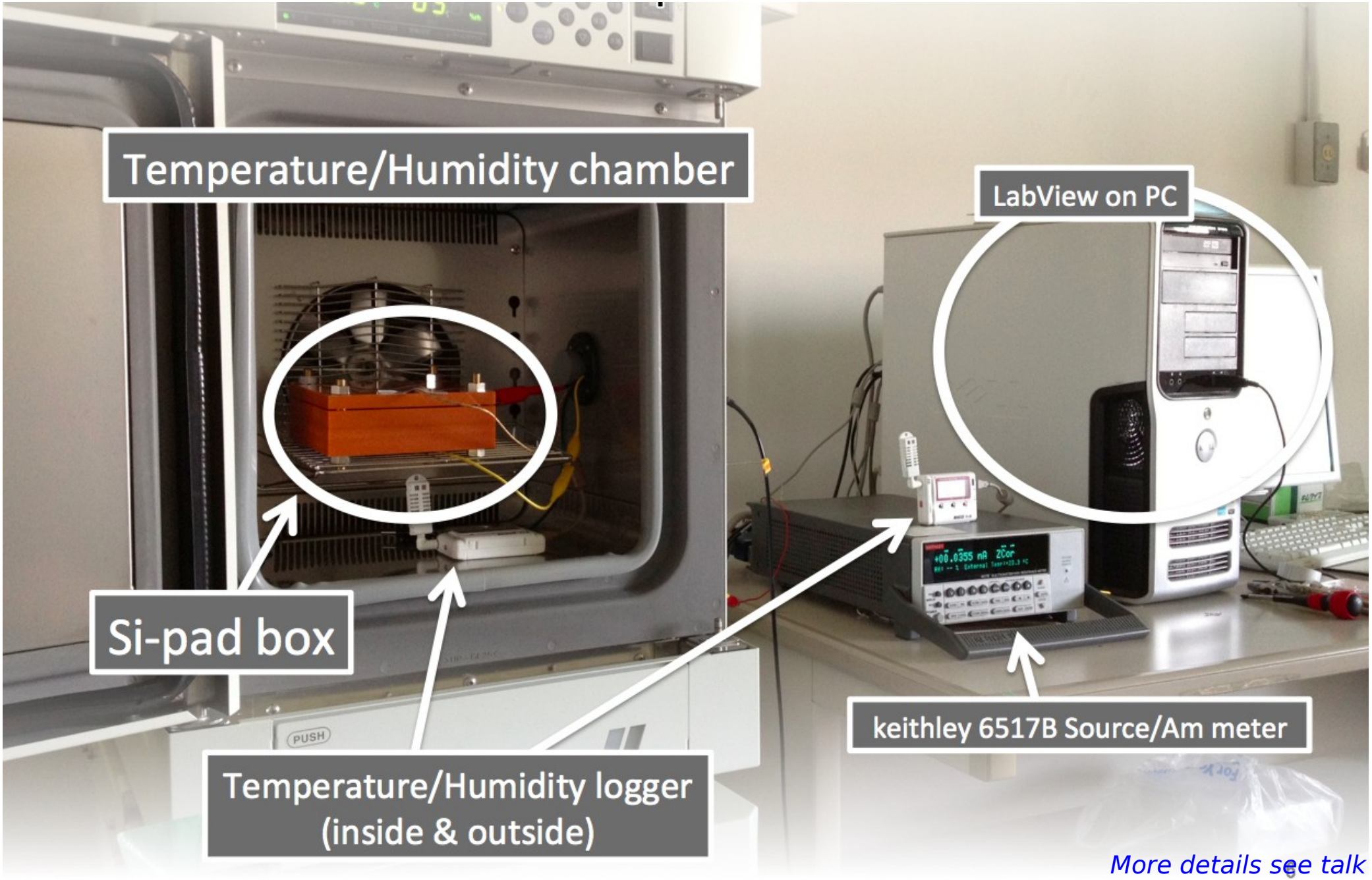
Thickness: 325 µm

Characterisation



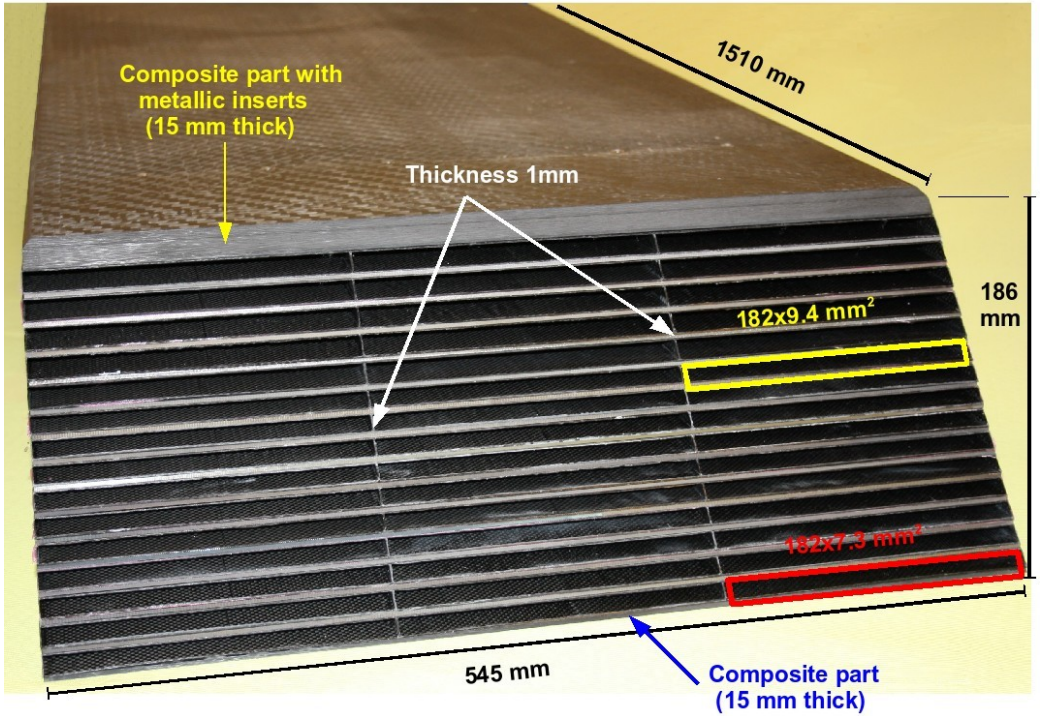
Breakdown
at ~500 V

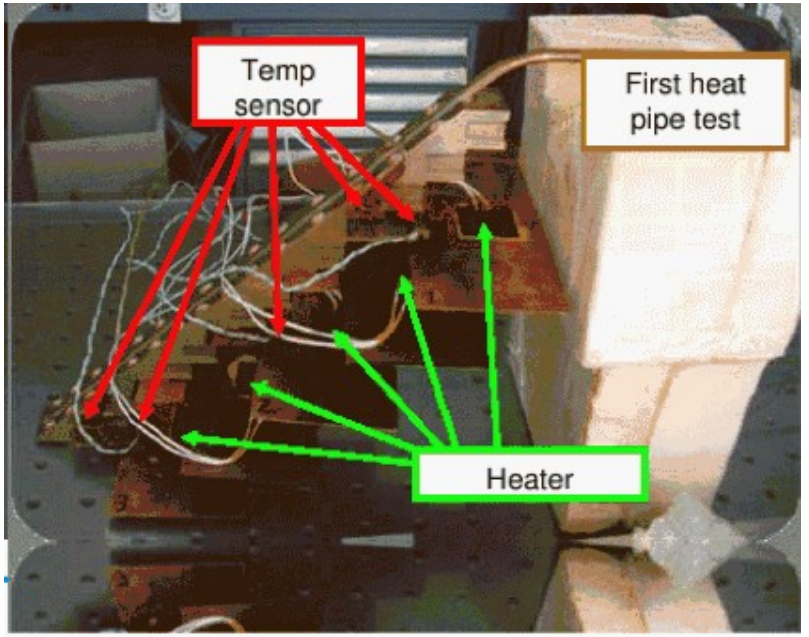
R&D on Si wafers at Kyushu

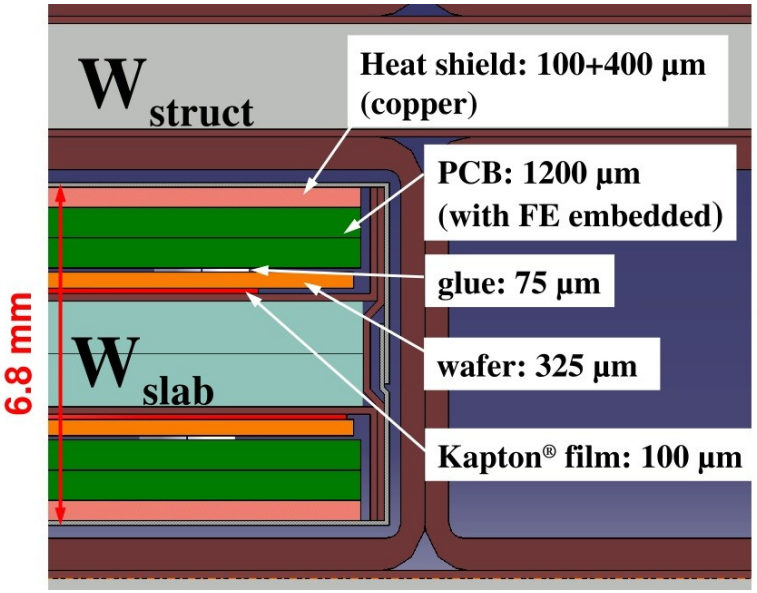


More details see talk by Kou Oishi

Technological Prototype – Design





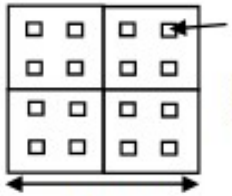


- ⇨ Gaps (slab integration) : 500 µm
- ⇨ Heat Shield: 500 µm
- ⇨ PCB : **~1200 µm**
- ⇨ Thickness of Glue : 100 µm
- ⇨ Thickness of SiWafer : 325 µm
- ⇨ Kapton® film HV : 100 µm
- ⇨ Thickness of W : 2100/4200 µm (± 80 µm)

Thermal studies

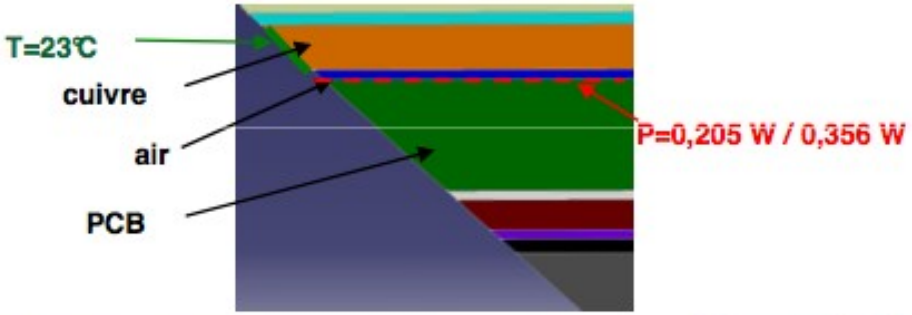
Inlet

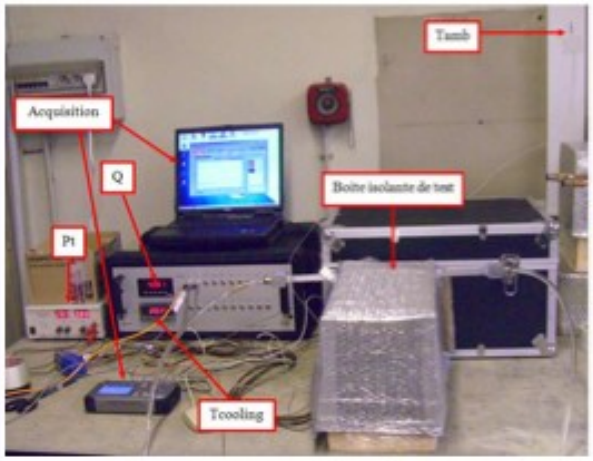
Power on PCB = 0,205 W / 0,356 W



Barrel : (1,6.10-3*16)/180*1445=0,205 W
EndCap : (1,6.10-3*16)/180*2500=0,356W

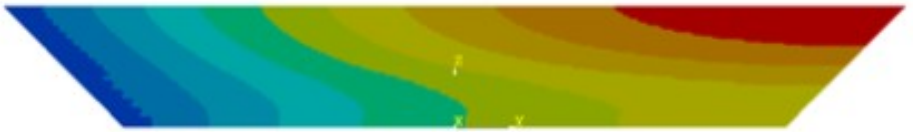
Boundary condition T = 23 ℃ beginning of the copper plate
Air between copper plate and pcb is in the model





Results

Barrel : (1.5m)



ΔT = 2,2℃

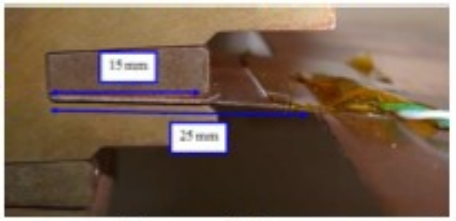
End Cap : (2.5m)

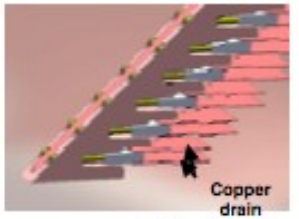
ΔT = 6℃

Conclusion

Low T°gradient -> cooling system suitable
Cooling front –end (front of slab sufficient)

Confirmation: **25 mm** free opening in DIF for extraction of cooling system



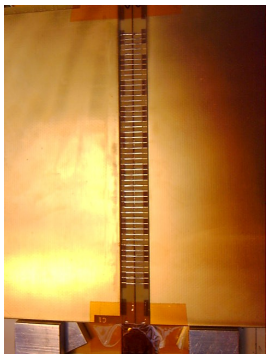


Copper plate / heat exchanger link

Ecal detector layer - Principle

A layer is composed of several short ASUs:

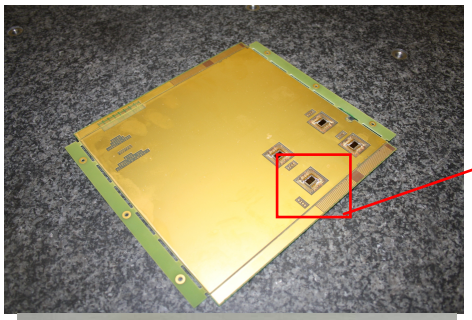
- A.S.U. : Active Sensors Units



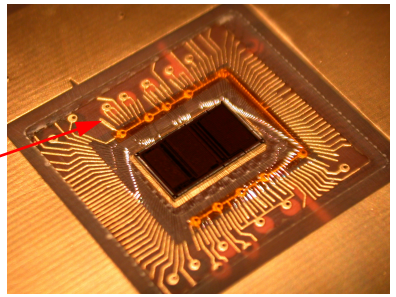
Interconnection work (see later)

Dedicated mechanical 'scaffolding' will be constructed

Chip+PCB+SiWafer =ASU



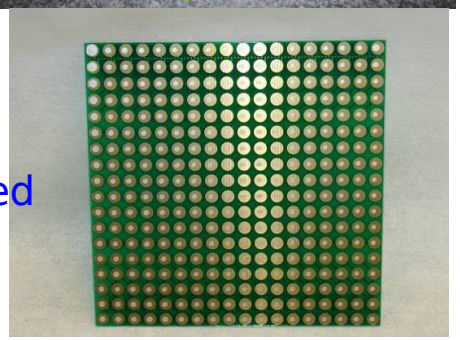
Bonding realised by CERN



Chip embedded

PCB is glued onto SiWafers

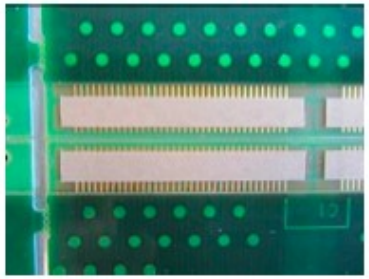
Gluing robot about to be commissioned



Length of layer:

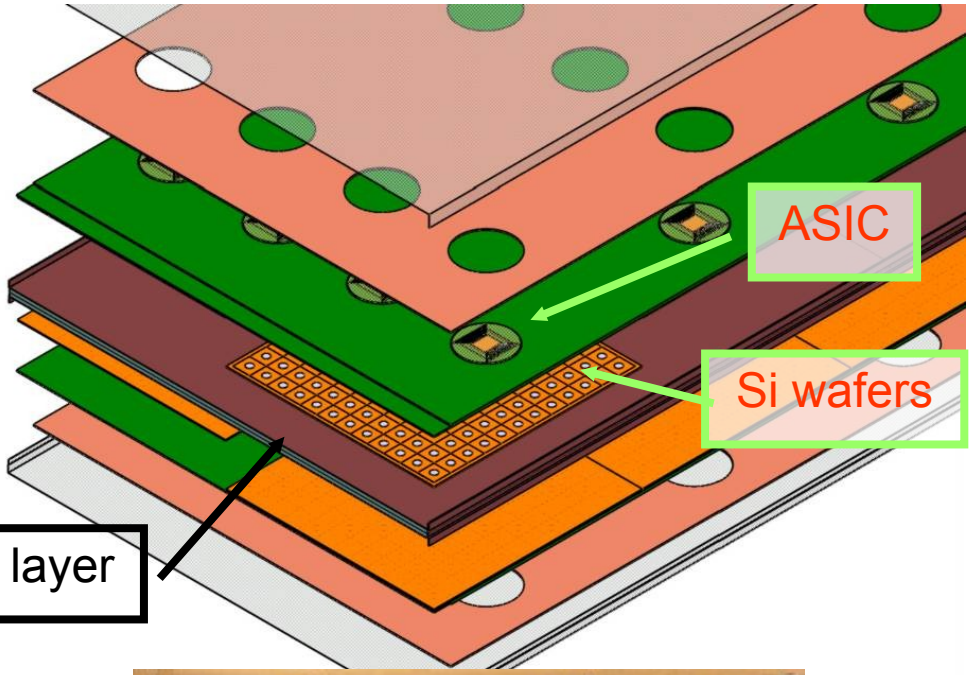
1.5m for barrel
2.5m for endcaps

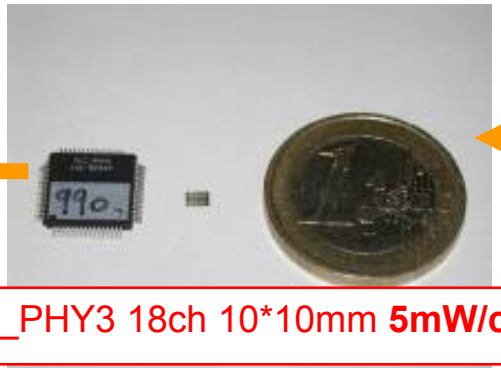
Comprehensive study of interconnection techniques

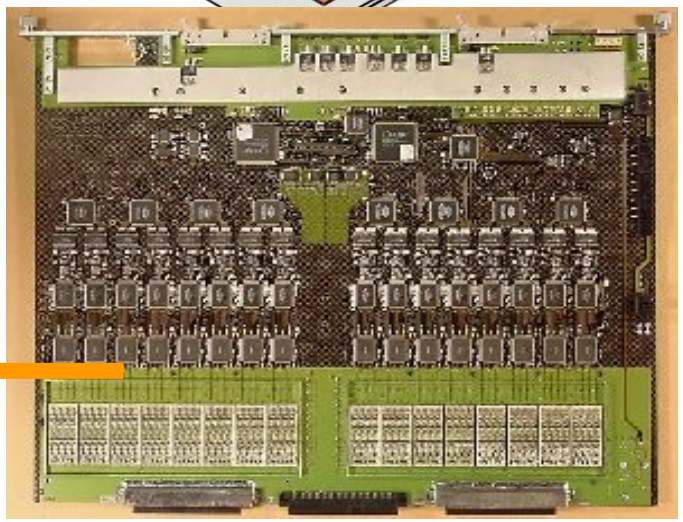
Technology	Advantages	Disadvantages
N°1 Solder 	-Proven technology -Possible to repair -~3 euros/connector	-Difficult procedure -Too much heat for the glue of wafers -Cannot be industrialized
N°2 ACF 	-Easy to install -Easy to remove -Easy to industrialize	-Needs to have a perfect planarity -Needs to have a thermode ~15Keuros -10mA maximum per wire -~30 euros/connector -Too much pressure =mechanical stress for the wafers
N°3 Spécial Kapton 	-Easy to install -Good reliability -Possible to repair -Easy to industrialize -Good strength -~4 euros/connector	-I don't know yet

Front end electronics

- Requirements to electronics
  - Large dynamic range (~2500 MIPS)
  - **Front end electronics embedded**
  - Autotrigger at ½ MIP
  - On chip zero suppression
  - **Ultra low power («25µW/ch)**
  - 10^8 channels
  - Compactness







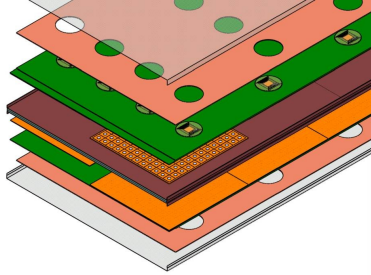
ILC : **25µW/ch**

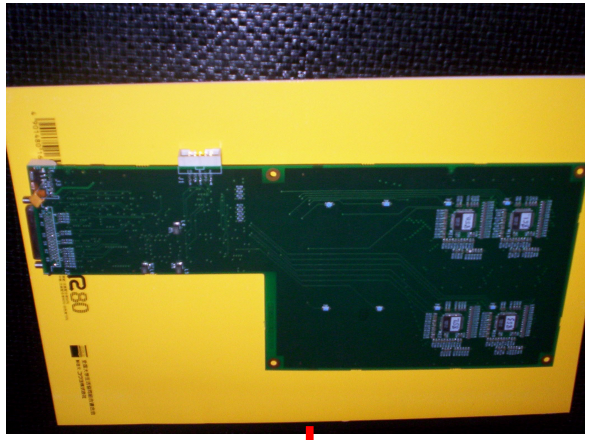
FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**

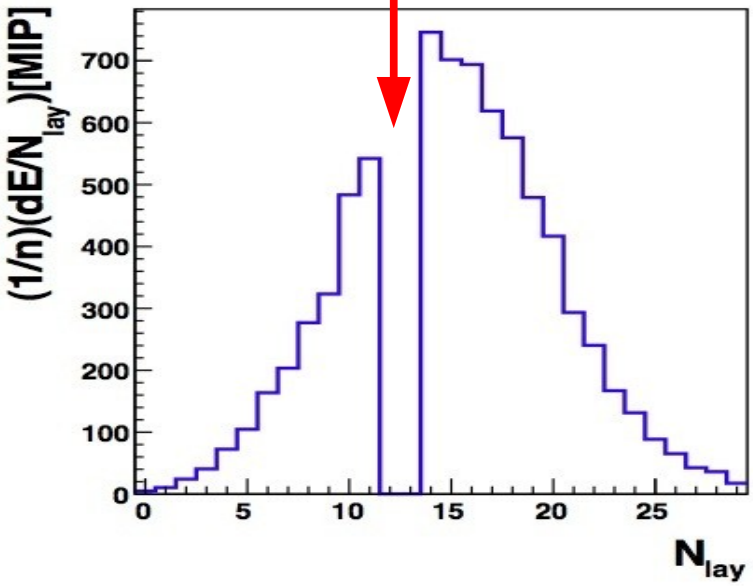
Embedded electronics - Parasitic effects?

Exposure of front end electronics to electromagnetic showers



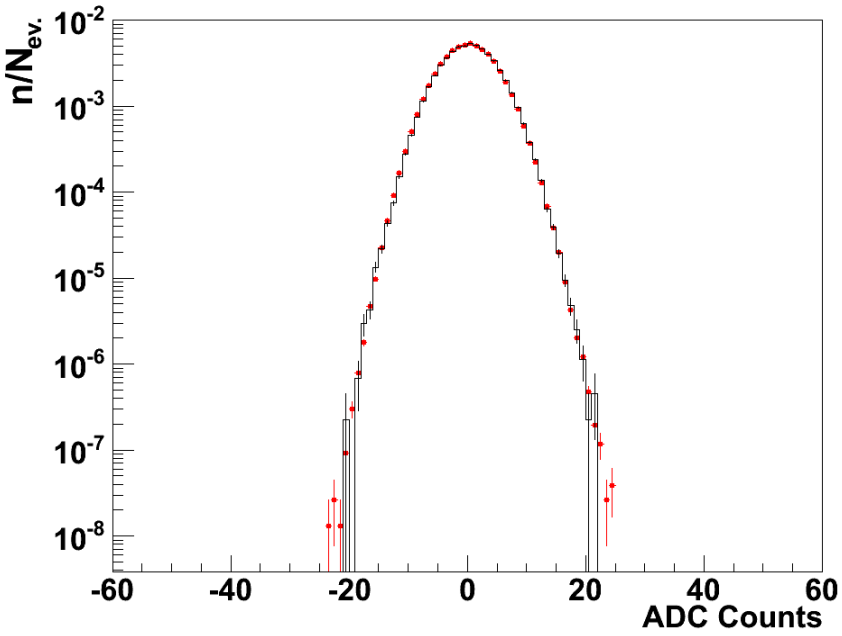


Chips placed in shower maximum
of 70-90 GeV elm. showers



Possible Effects: Transient effects
Single event upsets

Comparison: Beam events
(Interleaved) Pedestal events

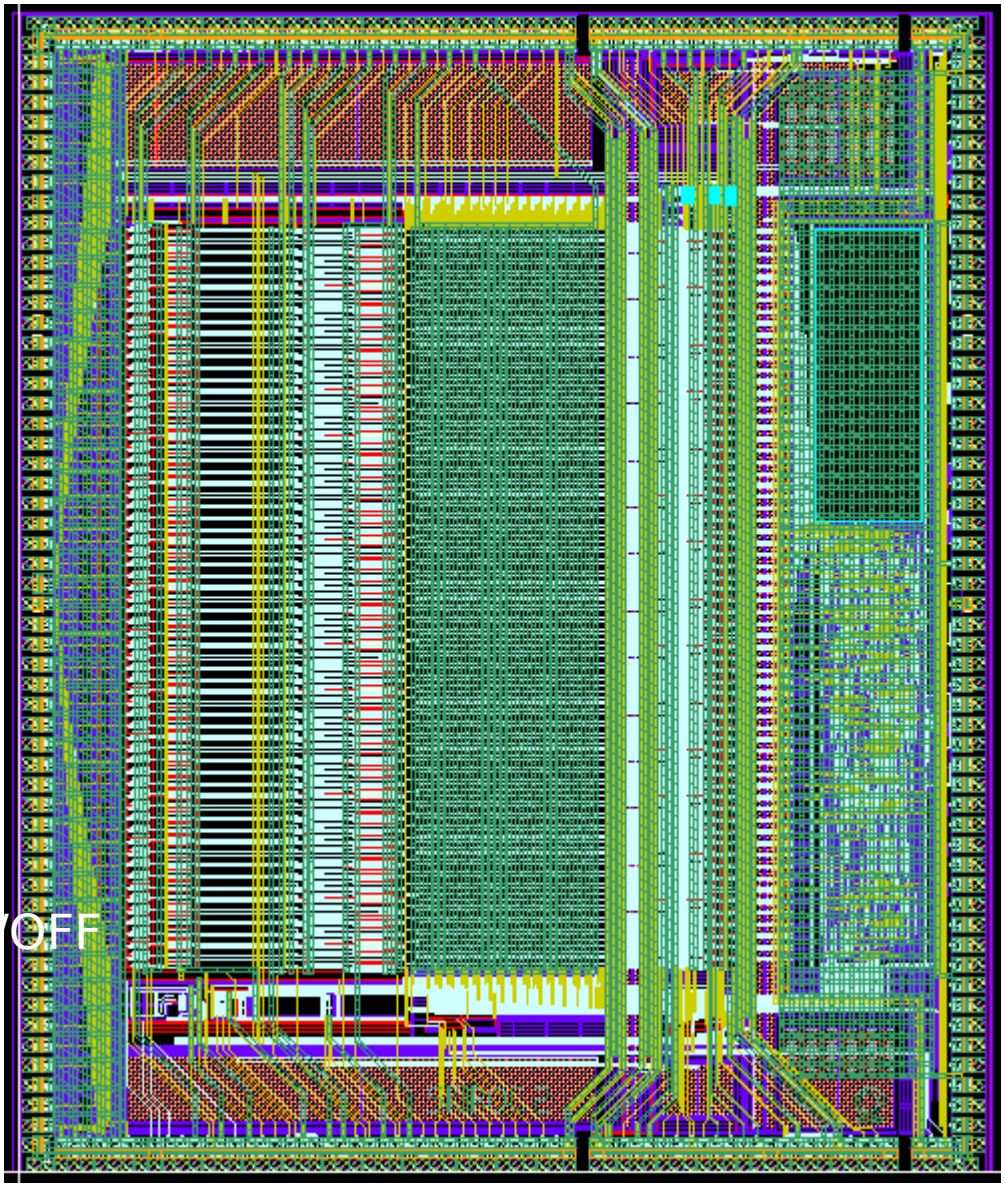


- No sizable influence on noise spectra by beam exposure
  ΔMean < 0.01% of MIP ΔRMS < 0.01% of MIP
- No hit above 1 MIP observed
  => Upper Limit on rate of faked MIPs: ~7×10^{-7}

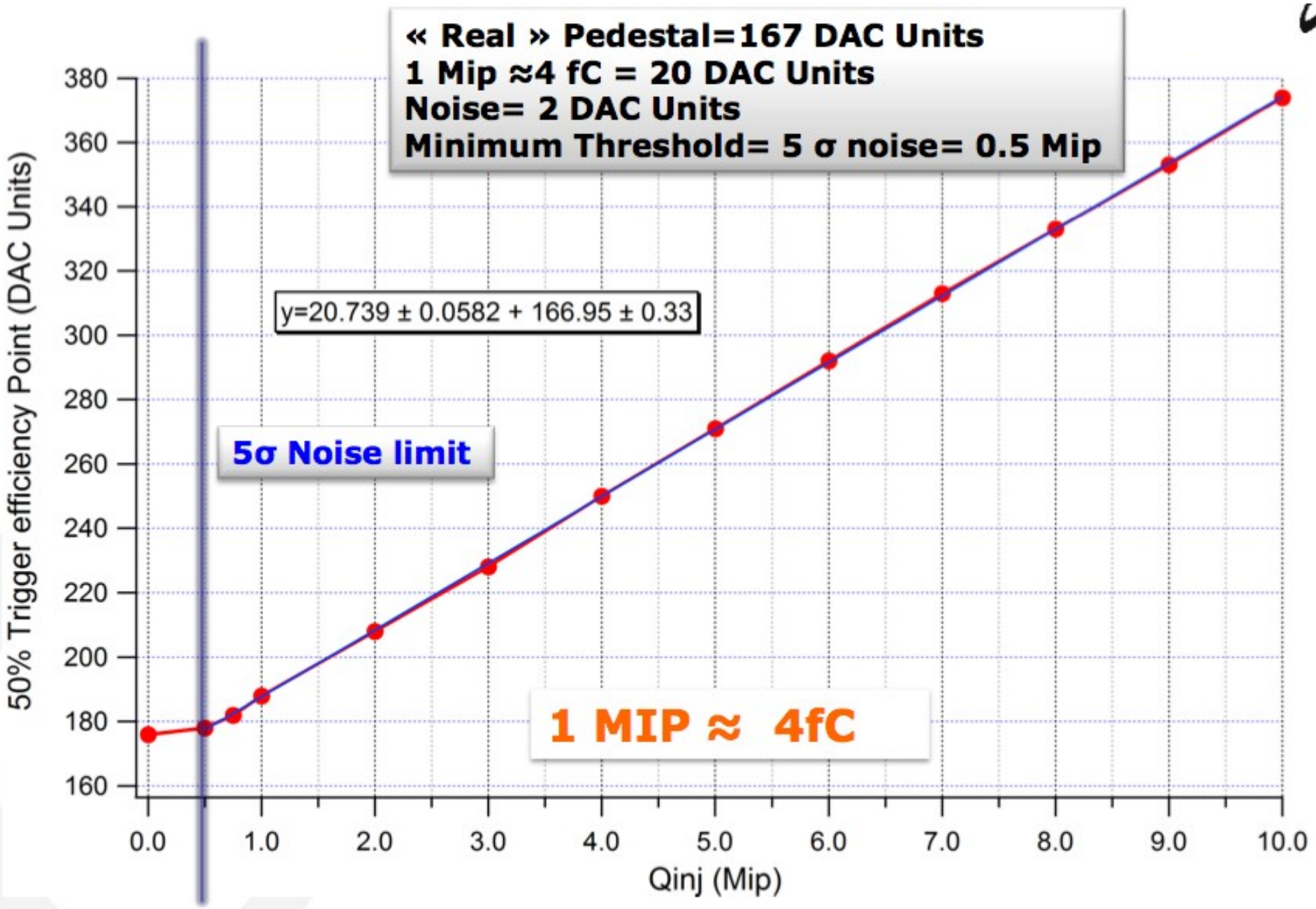
NIM A 654 (2011) 97

The Ecal ASIC - SKIROC

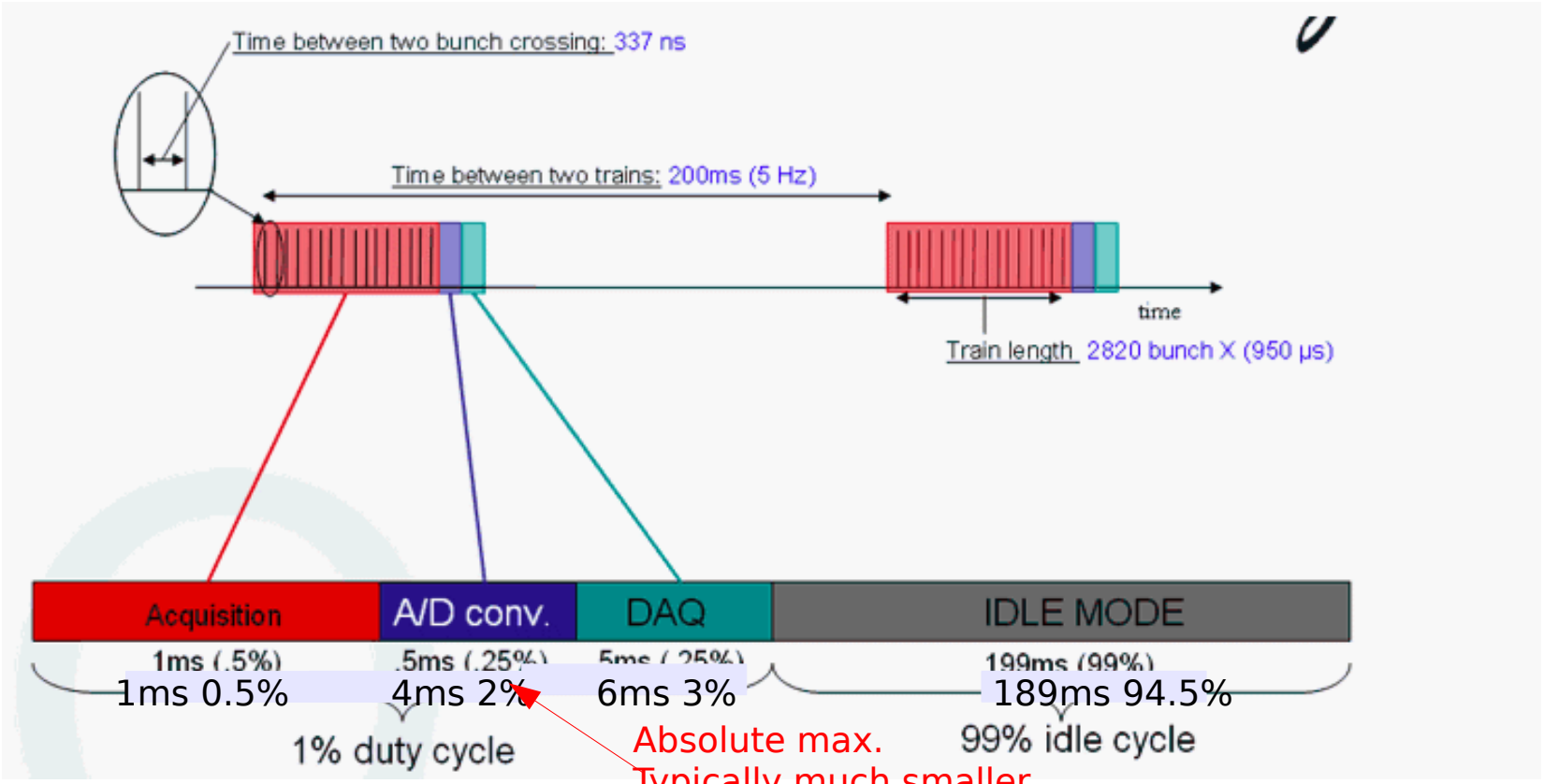
- 64 Channels
- Vss split :
  - Inputs
  - Analogue part
  - Mixed part
  - Digital part
- 250 pads
  - 3 NC
  - 17 for test purpose only
- Enhanced Power control
  - Full power pulsing capability
  - Each stage can be forced ON / OFF
- Die size
  - 7229 µm x 8650 µm



Example for SKIROC characterisation – Trigger efficiency



Power pulsing (better power gating)



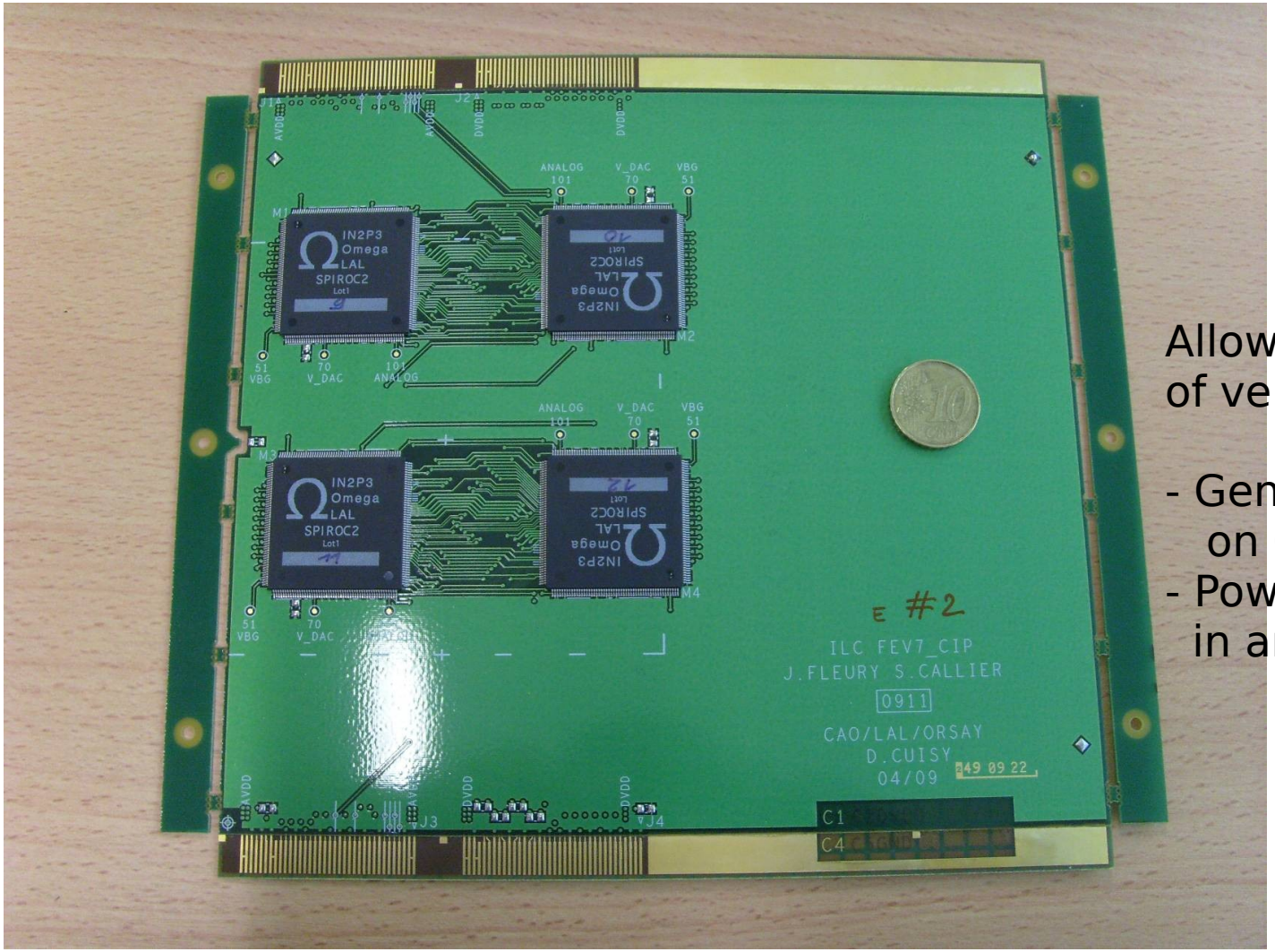
- Electronics switched on during 1ms of ILC bunch train and immediate data acquisition

- **Bias currents** shut down between bunch trains

- Mastering of technology is essential for operation of ILC detectors
  Measurements for SKIROC chip 1.7 mW <=> 27 uW/ch
  Test with SKIROC chip started in lab last week, stay tuned
  m3 of SDCHAL power pulsed with similar chip

R&D for PCBs

PCBs with 'conservative' technology FEV_CIP (Chip in Package)

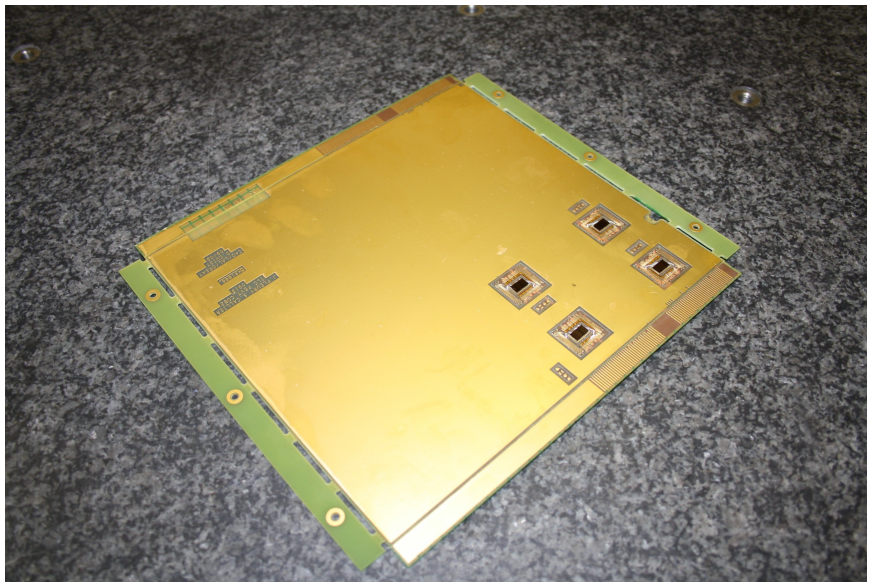


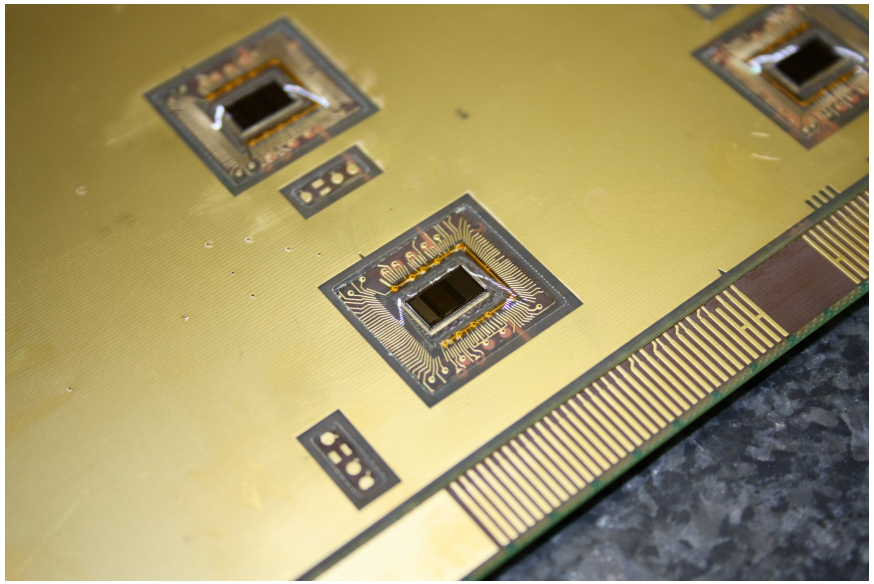
Allows us to realise a number of very useful tests

- General functionality of ASU on Cosmic bench and in beam
- Power pulsing in and outside of magnetic field

Stepwise approach to address R&D challenges

The next step FEV8 with COB – Chip on board





- Circuits wire bonded inside cavities

- Ultra thin

  9 layer board with max. 1.2mm thickness

- Ultra flat

  Deviation from total flatness max. 0.5mm

  Compare with industrial standard ~3mm

- Circuits need to be encapsulated withresine

  Non trivial to realise

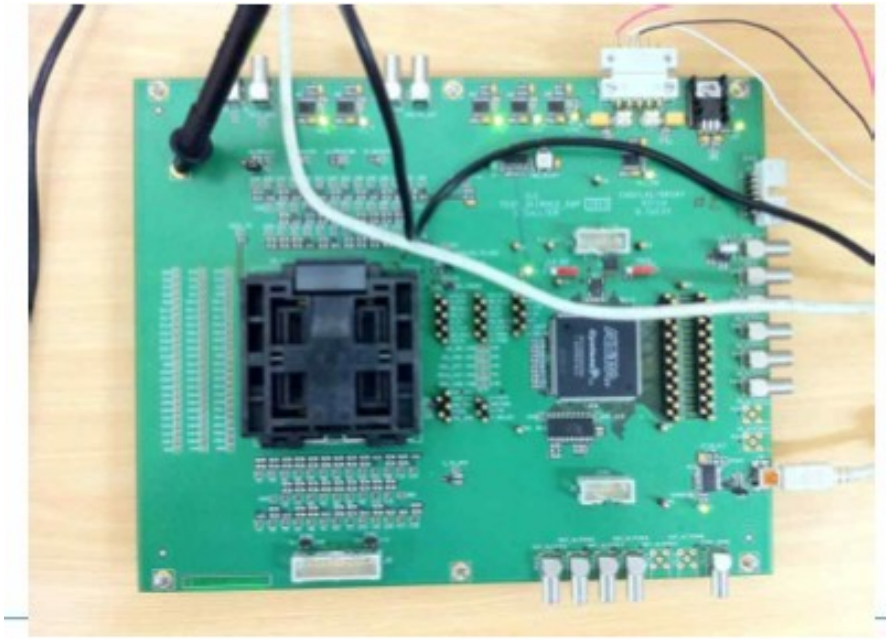
  Home made solution and idustrial solution at hand

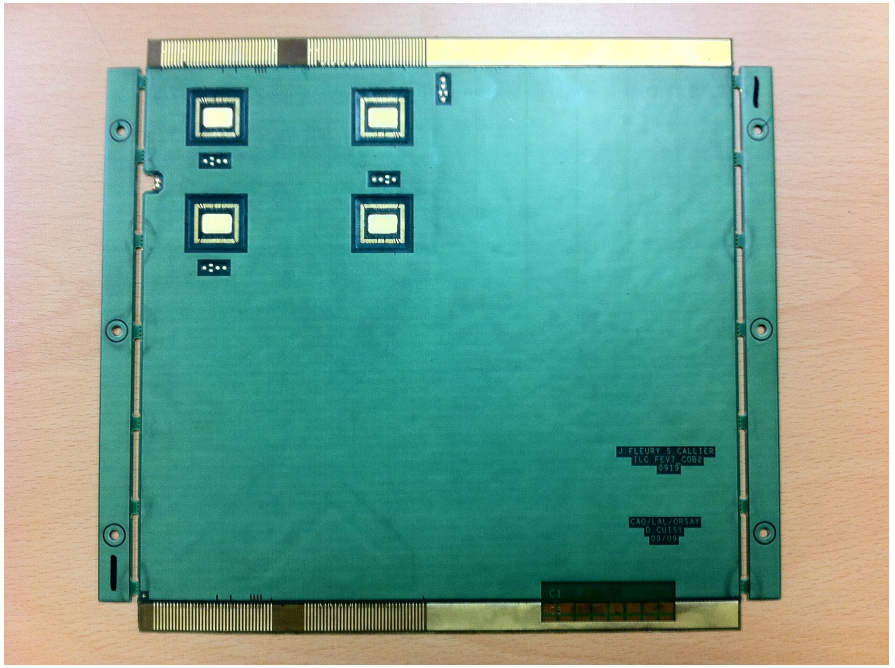
  Long term effects of chips and wire bonds?

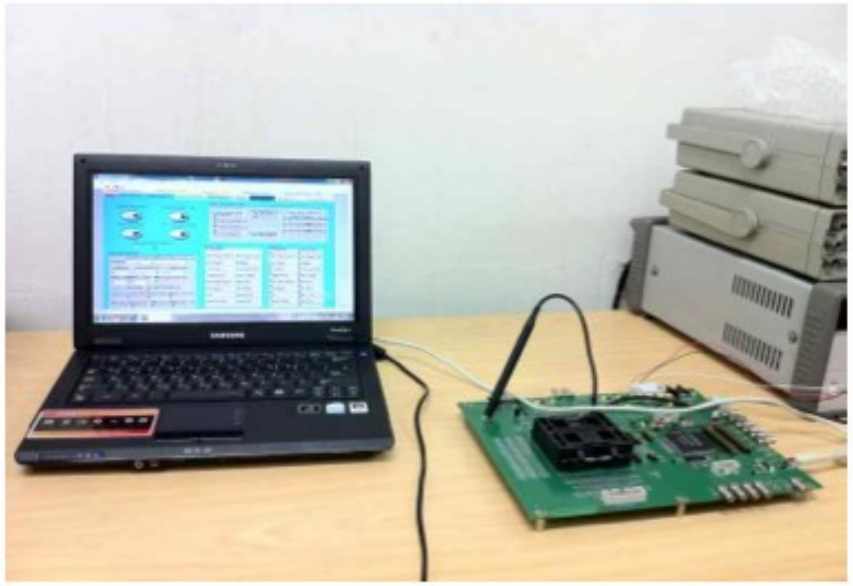
Mastering of these technological challenges is essential to meet LC detector design goals

-> A number of open points!!!

Work on Front End Electronics at SKKU – ANME Lab







Top: FEV PCB produced by EOS Company (Korea)

- Electrical tests successful
- First production
- Company needs to get acquainted to complexity

Left: Test bench for Ecal ASICs at SKKU

R&D for LC calorimeter FEE bears synergy with instrumentation for accelerators for medical applications (Isotopes for PET)

A generic DAQ system for the CALICE calorimeters (Technological Protoypes)

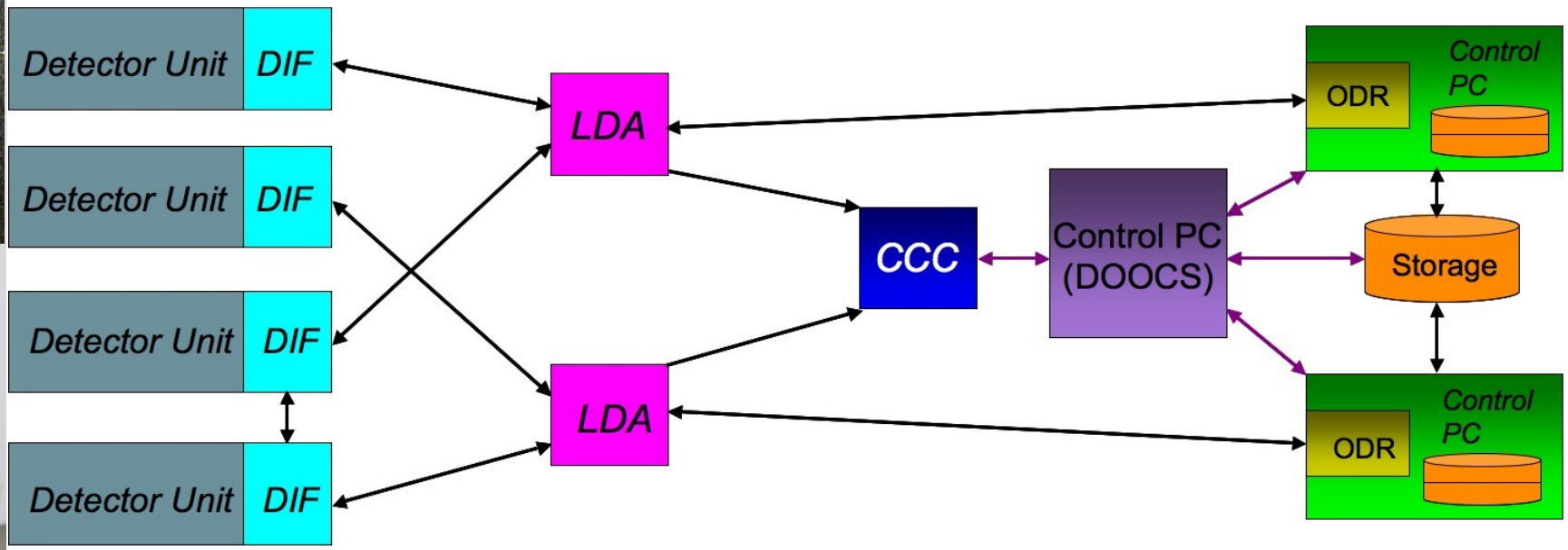
Standard

HDMI connectors
LVDS
GBEthernet
Optical links

Generic

FPGA

Scalable



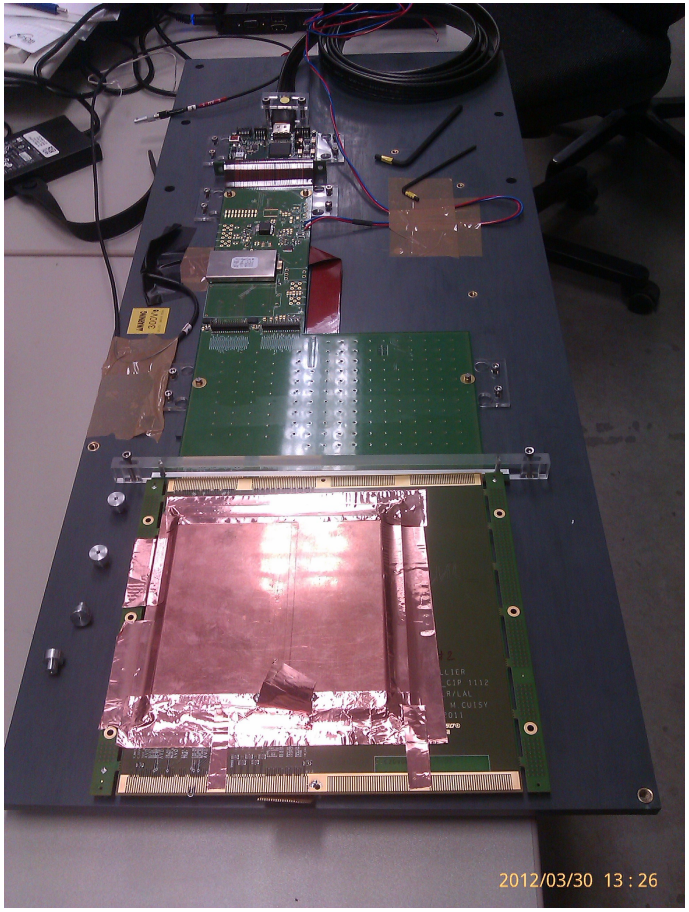
DAQ chain established using SPIROC and FEV7_CIP
Since 1st quarter of 2012 SKIROC and FEV8_CIP
-> beam test in March 2012 at DESY

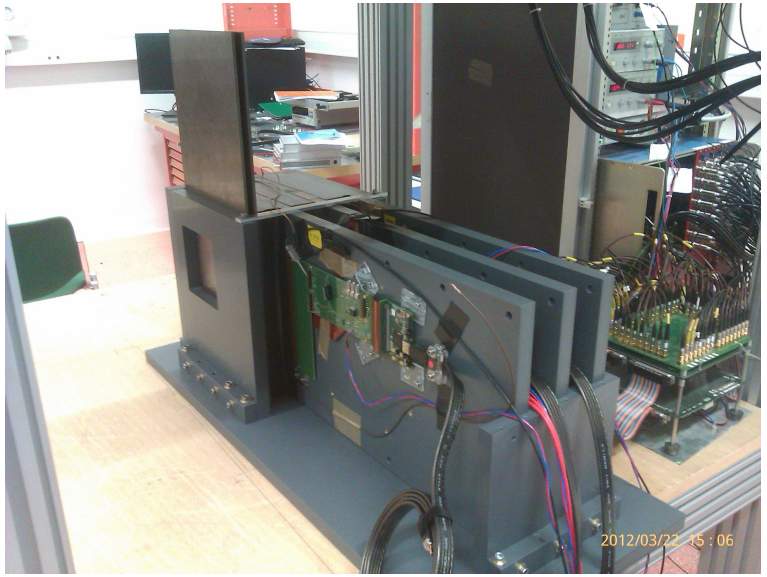
Beam test setup

- wafer 9x9 cm^2, 324 pixels 5x5 mm^2
- **2 slabs SKIROC (4 ASICs)**

  2 channels with 2 pixels and 22 channels

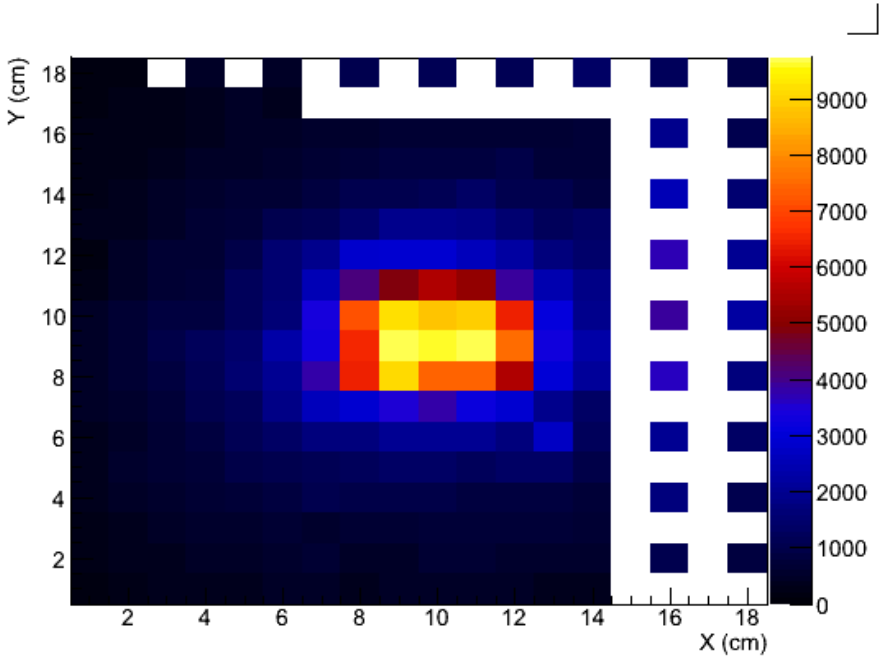
  with 4 pixels
- 2 slabs SPIROC (4 ASICs et 1 ASIC)
- Structure PVC modulable (2 configurations)
- 6 Tungsten plates of 4mm thickness

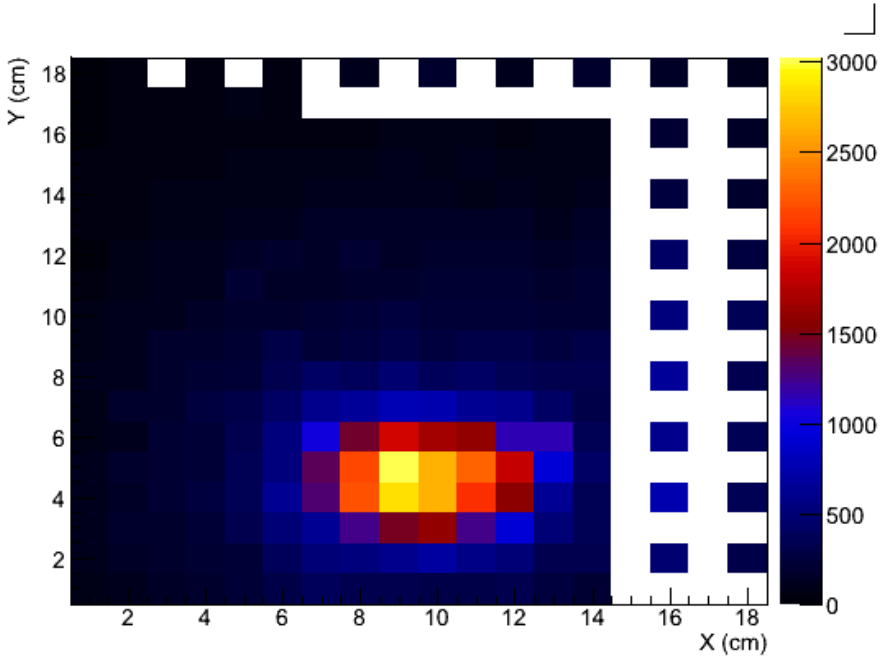




Purpose of beam test
was to bring together
for the first time the entire
equipement
-> regain of project's
momentum

First Results





Beam spot
In the middle
of layer

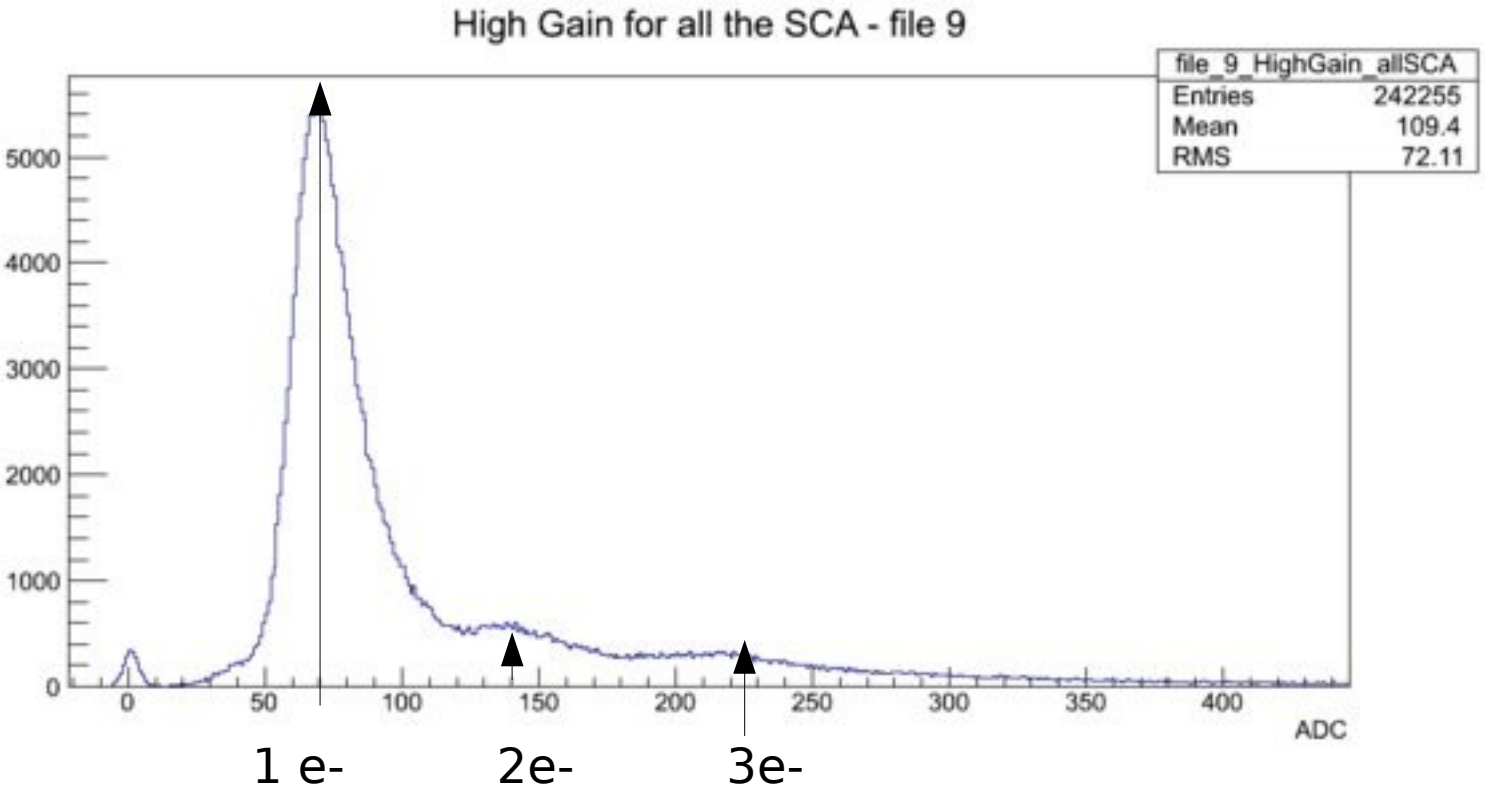
moves

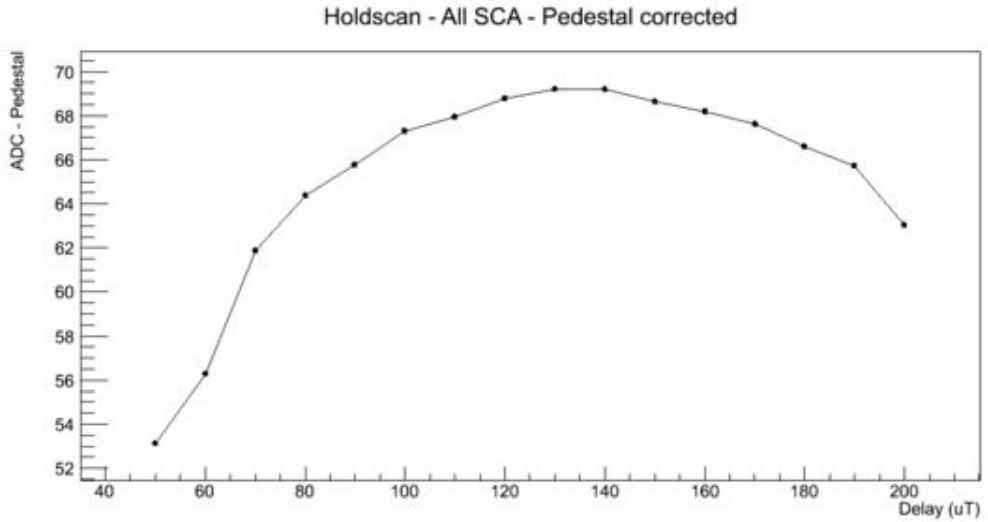
Accordingly to
Beam sport

Success after a real cold start

Congrats to those who
Put together the SKIROC/FEV8
Setup out of the box

MIP signals and further studies





Hold scan
Curve as expected

Summary and outlook

- SiW Ecal group is working in technological solutions for a highly granular Ecal

  - Mechanical concept validated (Demonstrator 2009 and now full size prototype)
  - Silicon Wafer technology at hand
    ... but still intensive R&D necessary
    Regular communication with Hamamatsu, more contacts to be (re-)established
  - Front End Electronics is be challenging
    Embedded into calorimeter layers: **No compromise for precision physics**
    Power gating
  - ASICs – SKIROC - and (conservative) versions of PCBs for Ecal now under test

- New collaborators in France (LPNHE), Japan (Kyushu), progress in Korea

- Beam test in March at DESY with first 2nd generation detector layers
  Encouraging results, however still a long way to go
  Next months consolidation and extension of setup
  Beam test with larger setup in July 2012

- Supported within EUDET (2006-2010), AIDA (2011-2015) and French ANR (2011-2014) + New Japanese ILC funding (2011-2016)

-

Major issues of R&D – Beyond SiW Ecal

- Master current technological prototypes with up to 500000 channels
  e.g. Power management of considerable systems

- Establish contacts to industrial partners
  Development of cost effective solutions

- Prepare the step towards 'real' detectors
  Prototypes now: up to 500000 channels
  Final detector: > 10^8 channels

- Development of system simulation tools

- Invent procedures to assure utmost reliability of detector equipment
- Prepare procedures for mass production of detectors

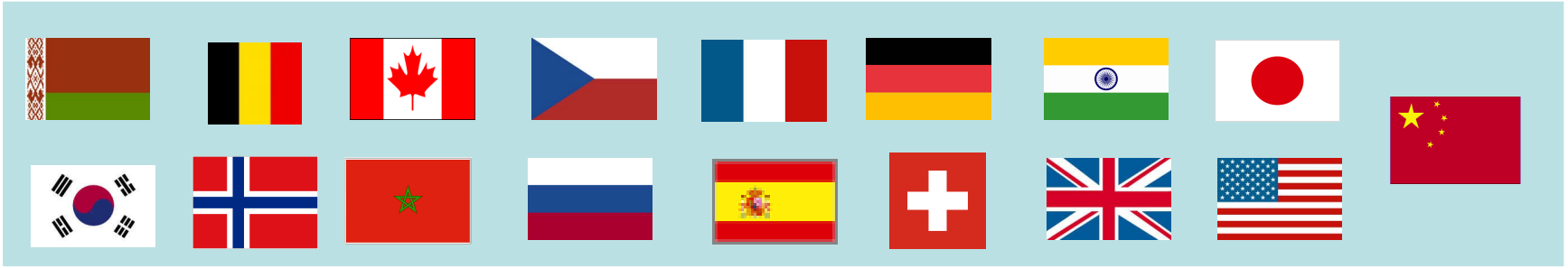
- (To say the least) Difficult to conduct with current resources (funding and manpower)

Backup Slides

The CALICE Collaboration

Calorimeter for ILC

Calorimeter R&D for a future linear collider



~330 physicists/engineers from 57 institutes
and 17 countries from 4 continents

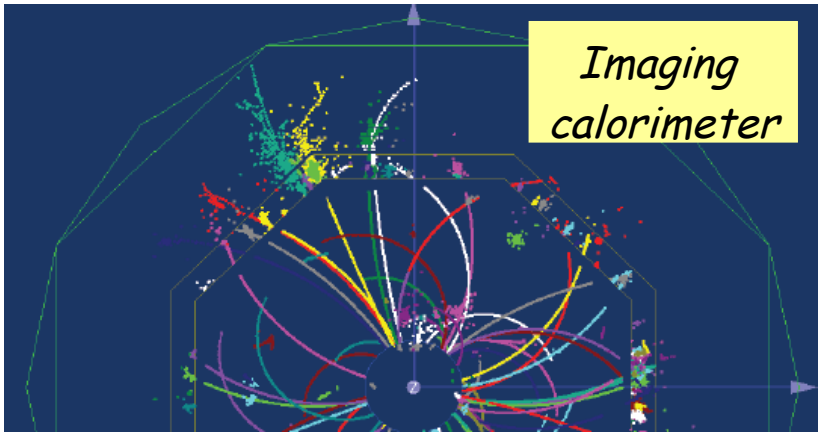
- Integrated R&D effort

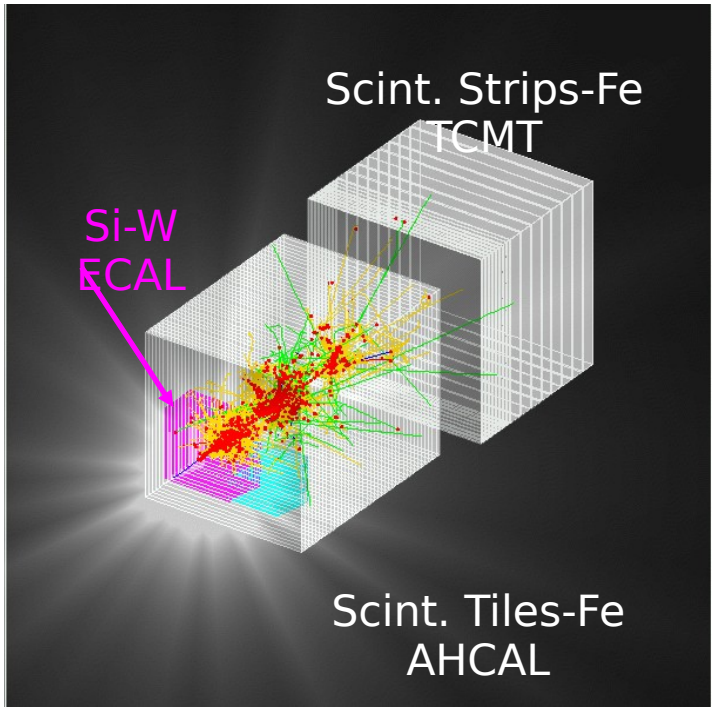
- Benefit/Accelerate detector development due to *common* approach

The Calice Mission

Final goal:

A highly granular calorimeter optimised for the Particle Flow measurement of multi-jets final state at the International Linear Collider



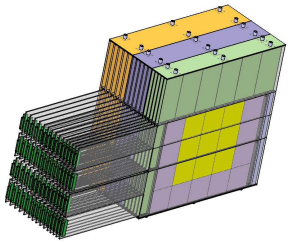


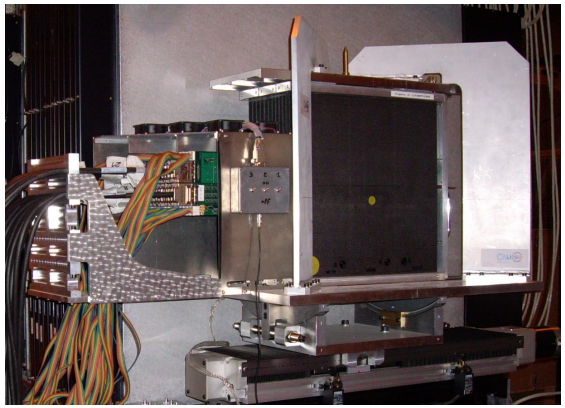
Intermediate task:

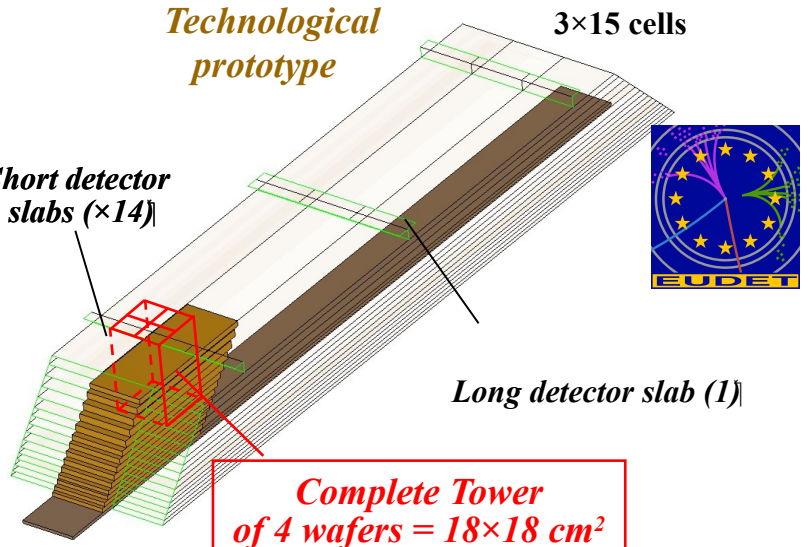
Build prototype calorimeters to
- Establish the technology
- Collect hadronic showers data with unprecedented granularity to
  - tune clustering algorithms
  - validate existing MC models

Technological Prototype

- Physics prototype: Validation of main concept
- Techno. Proto : Study and validation of technological solutions for final detector
- Taking into account industrialisation aspect of process
- First cost estimation of one module



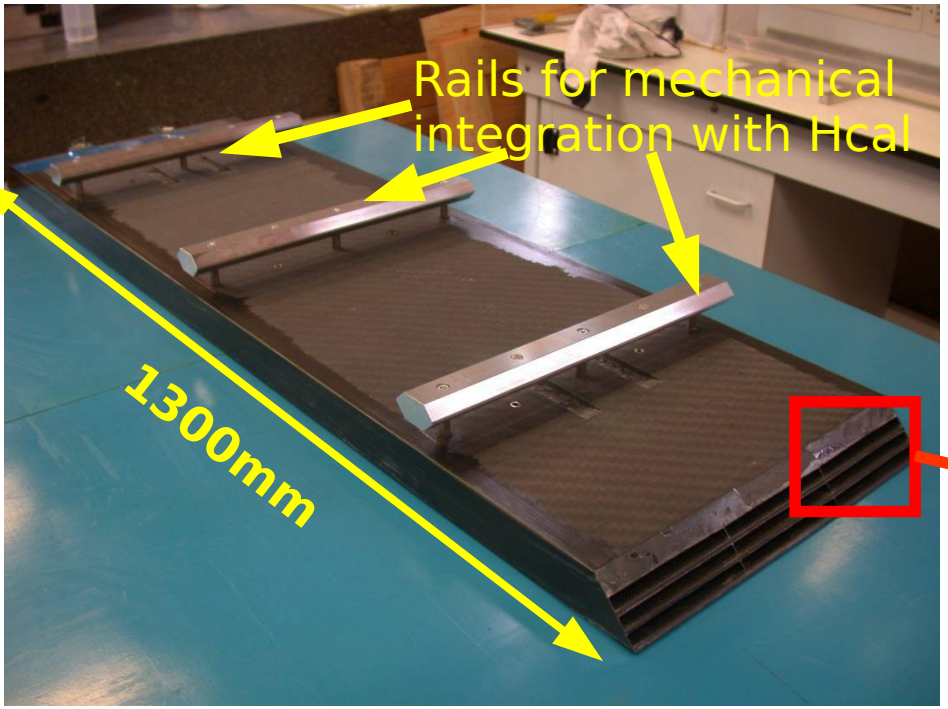


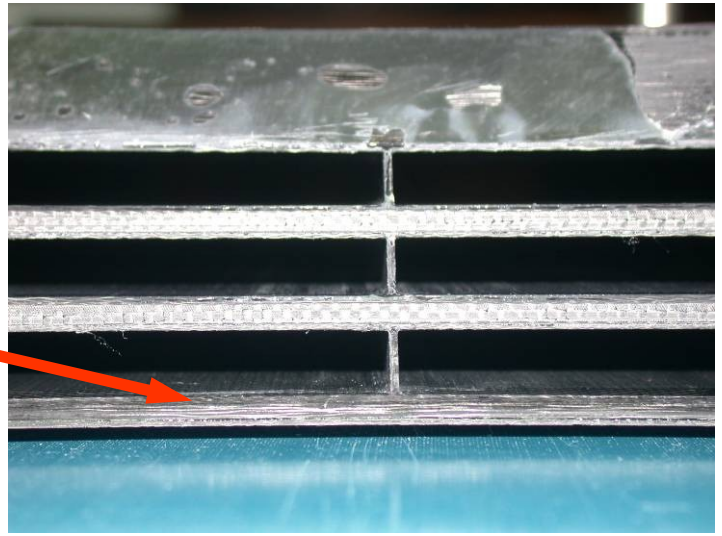


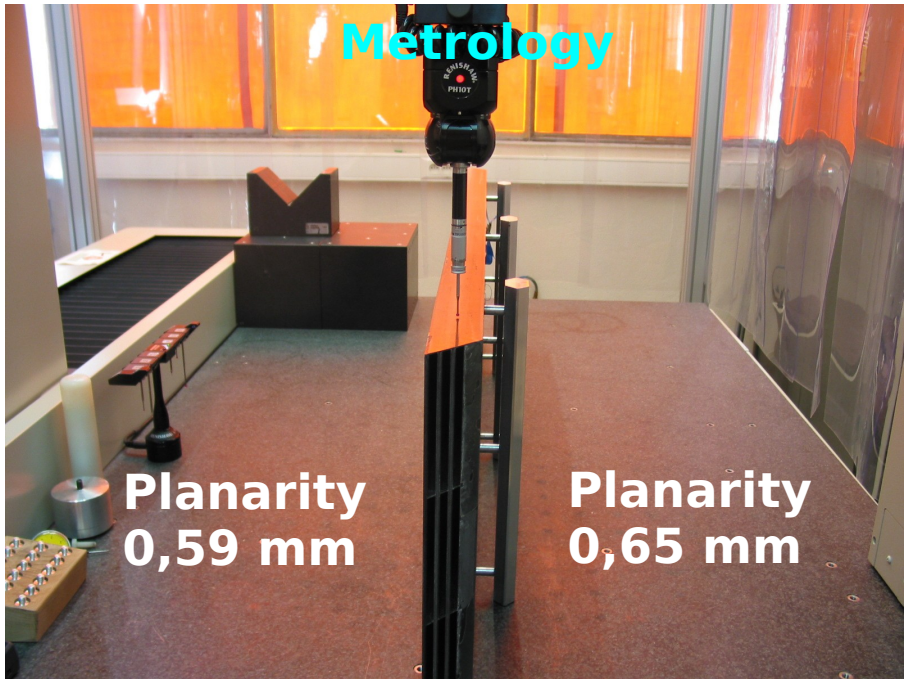
- **3 structures : 24 X_0 (10×1,4mm + 10×2,8mm + 10×4,2mm)**
- **sizes : 380×380×200 mm3**
- **Thickness of slabs : 8.3 mm (W=1,4mm)**
- **VFE outside detector**
- **Number of channels : 9720 (10×10 mm²)**
- **Weight : ~ 200 Kg**

- **1 structure : ~ 23 X_0 (20×2,1mm + 9×4,2mm)**
- **sizes : 1560×545×186 mm3**
- **Thickness of slabs : 6.8 mm (W=2,1mm)**
- **VFE inside detector**
- **Number of channels : 45360 (5×5 mm²)**
- **Weight : ~ 700 Kg**

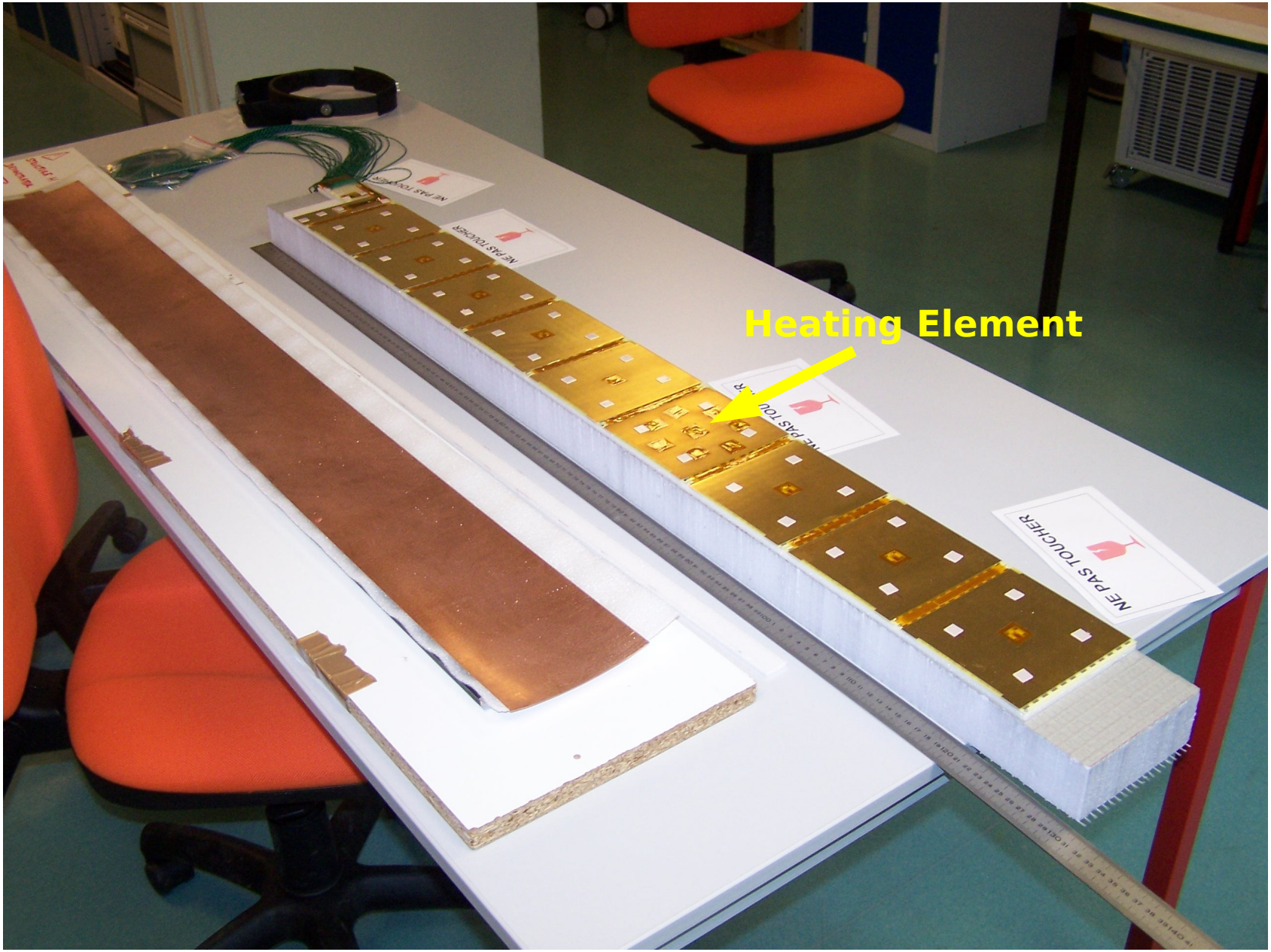
First step: Demonstrator





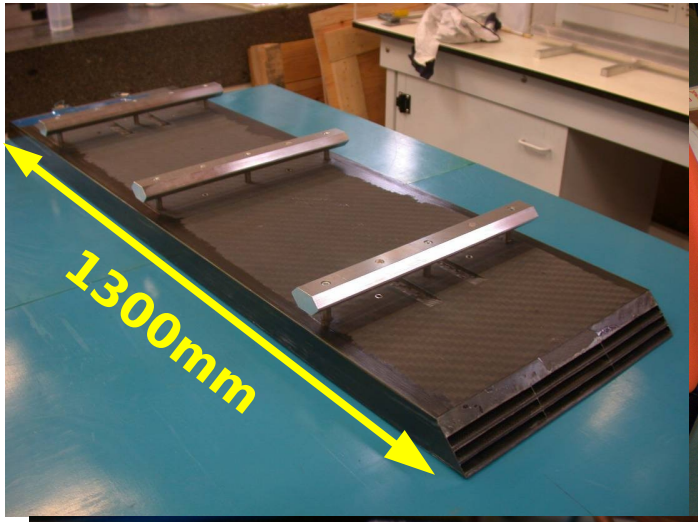


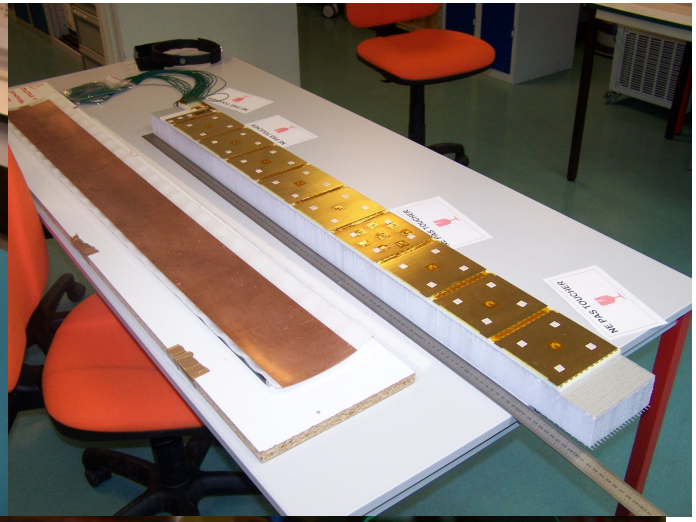
Developping the Techniques for Layer Construction – Thermal Layer

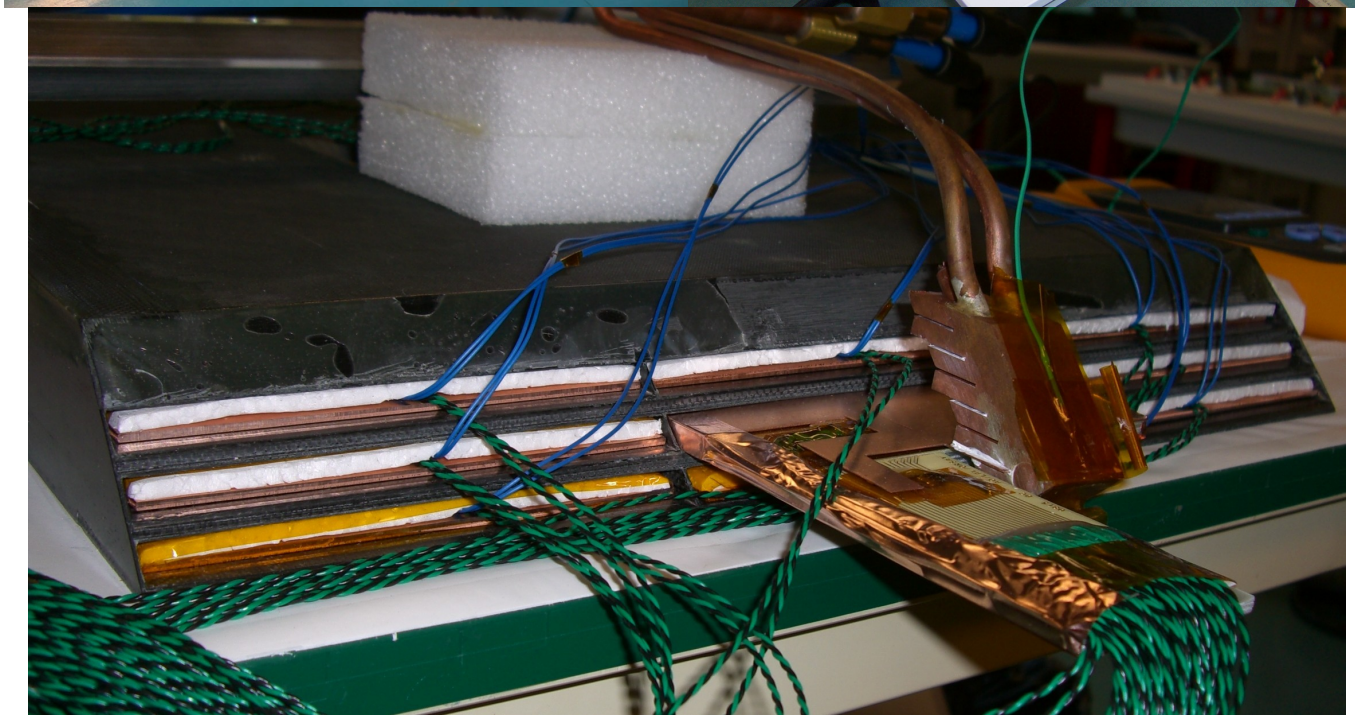


Proof-of-principle to build long layers

First step: Demonstrator



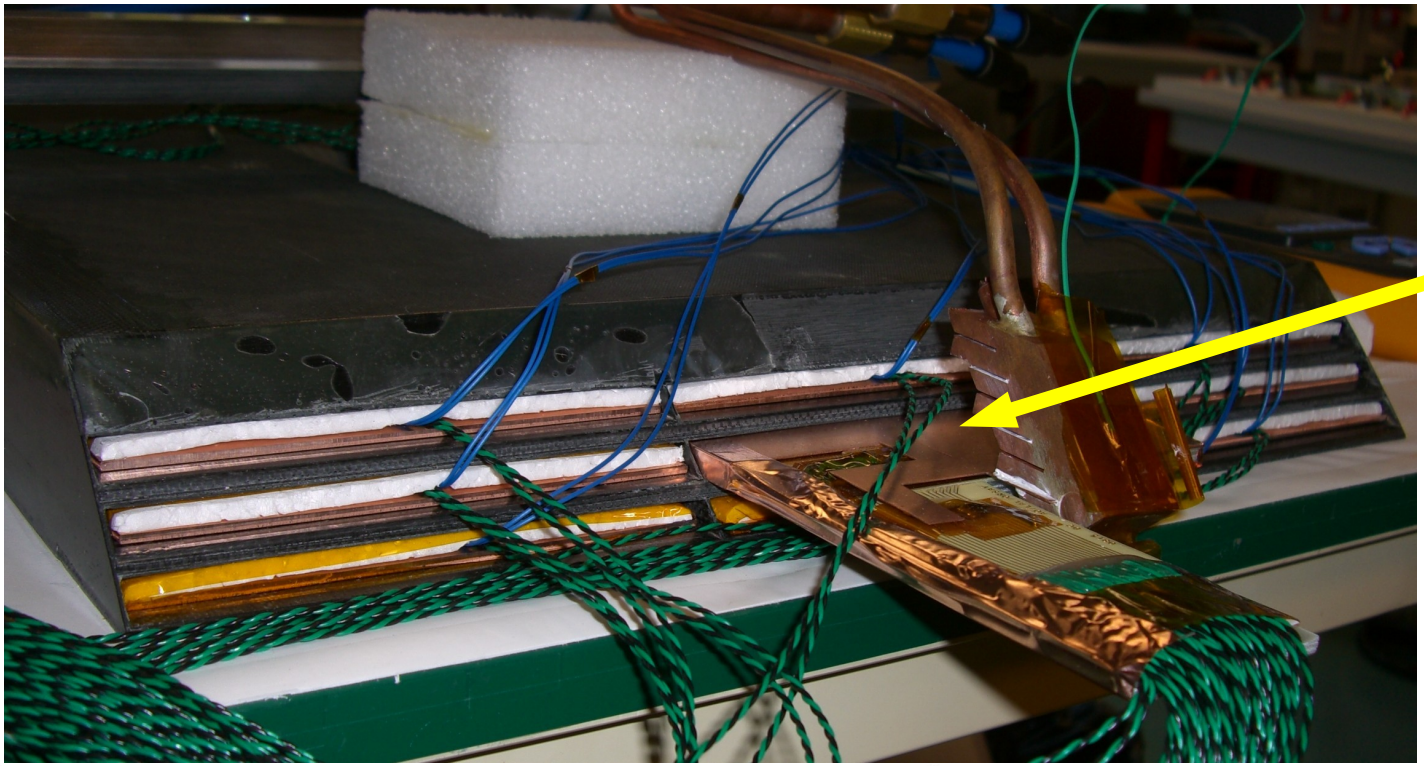


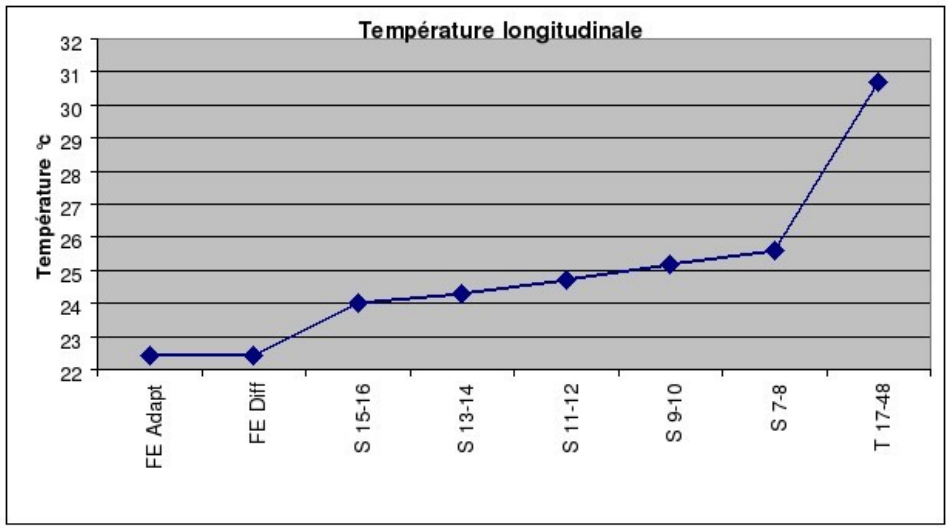


- Detector module realised (from mechanical point of view)
- Demonstrator subject to a thermal test

Thermal Test

To study thermal behaviour of detector module





Ambient Temperature	22		
Alveolar Slot	Left	Middle	Right
External		23.5	
Upper	24.8	24.8	24.6
Lower	25	30.7	25.2
Bottom	25.1	25.2	25.1

- Detector Module realised
  from mechanical point of view
- Thermal test important for DBD

Parties Involved

6 Laboratories are sharing out tasks in according to preferences and localization:

Assembling of A.S.U. (industrialization, gluing ests) + backend system (DIF support) + services

of wafers

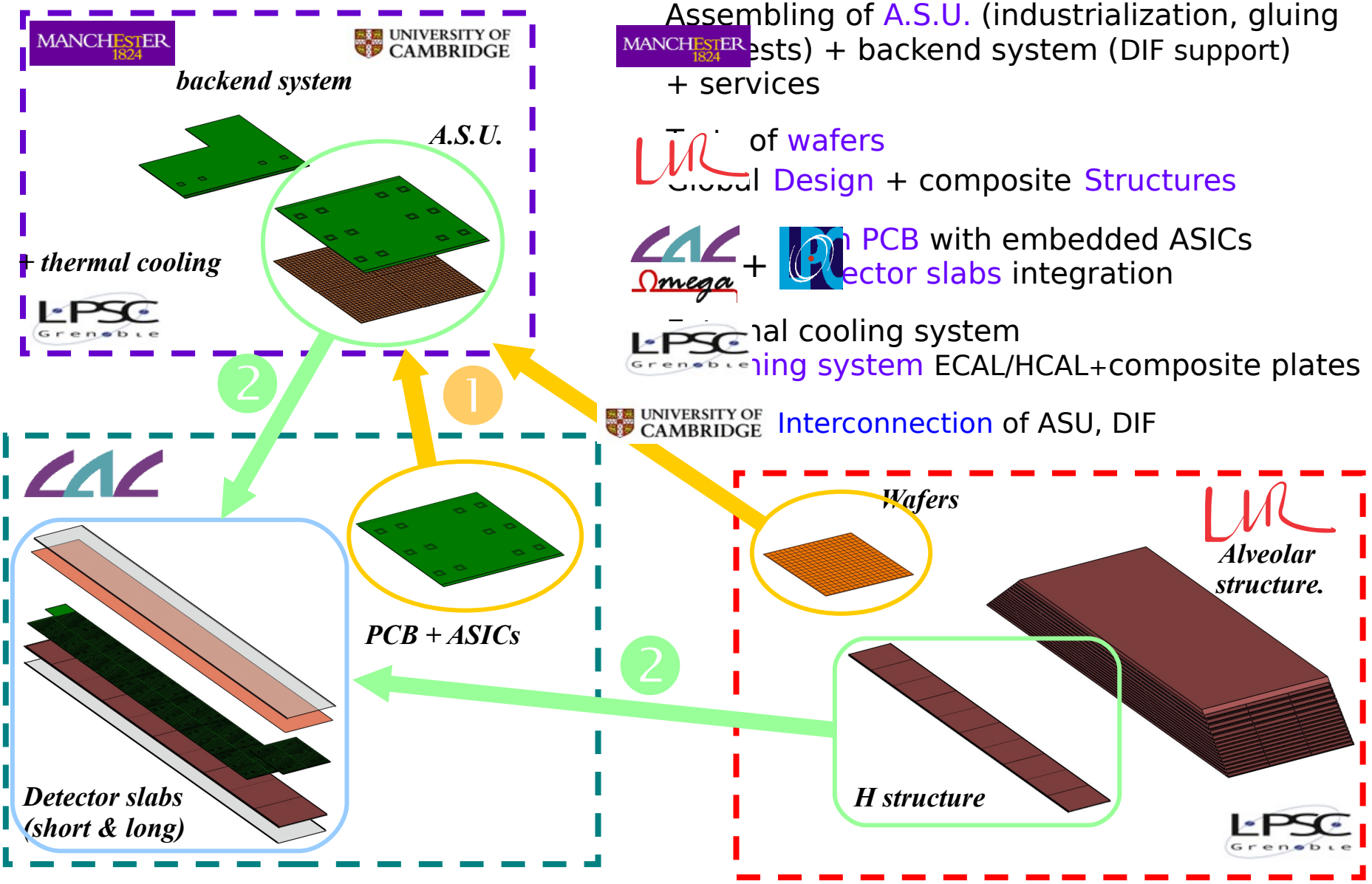
l Design + composite Structures

PCB with embedded ASICs + ector slabs integration

al cooling system

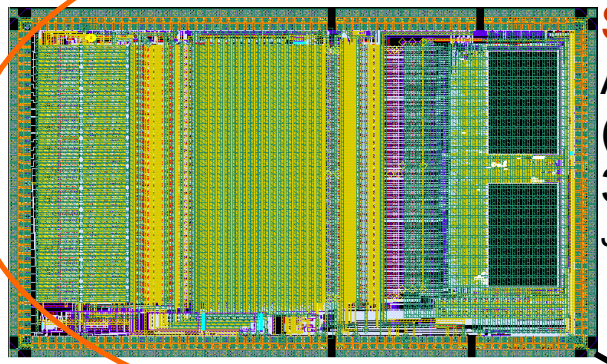
ing system ECAL/HCAL+composite plates

Interconnection of ASU, DIF

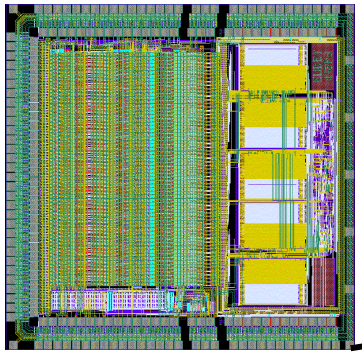


ASICs Frontales: Les Chips ROC

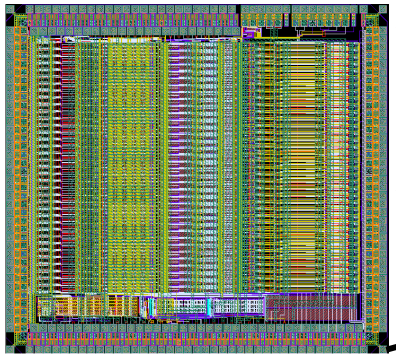
- Prototypes EUDET: modules à grande echelle (~2m)
- Financement partiel par EU (06-09)
- ECAL, AHCAL, DHCAL



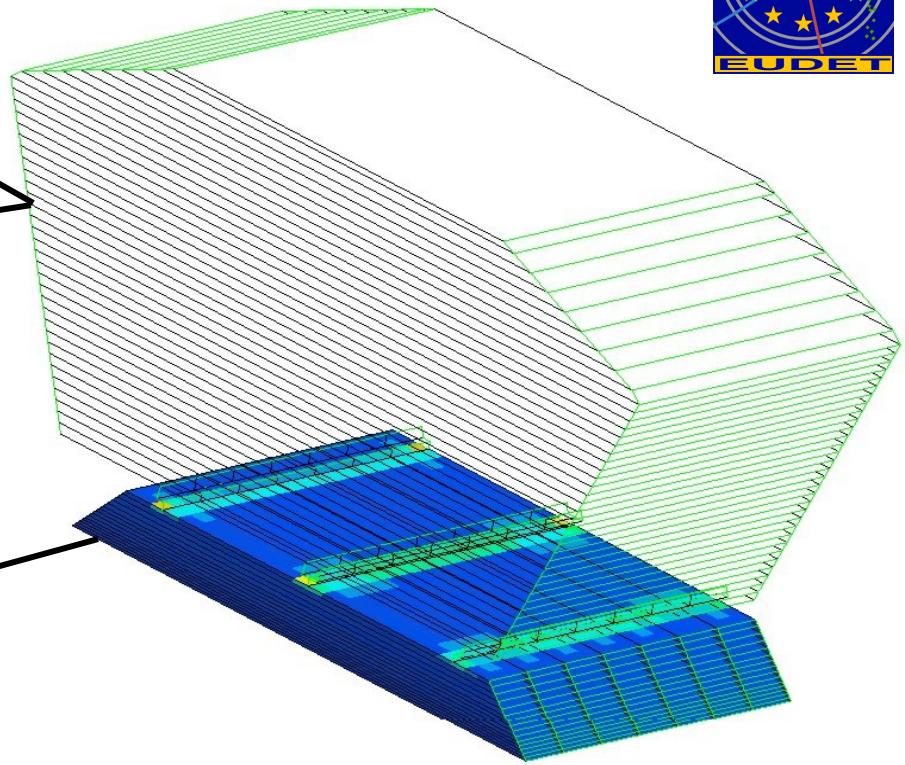
SPIROC
Analog HCAL
(SiPM)
36 ch. 32mm²
June 07



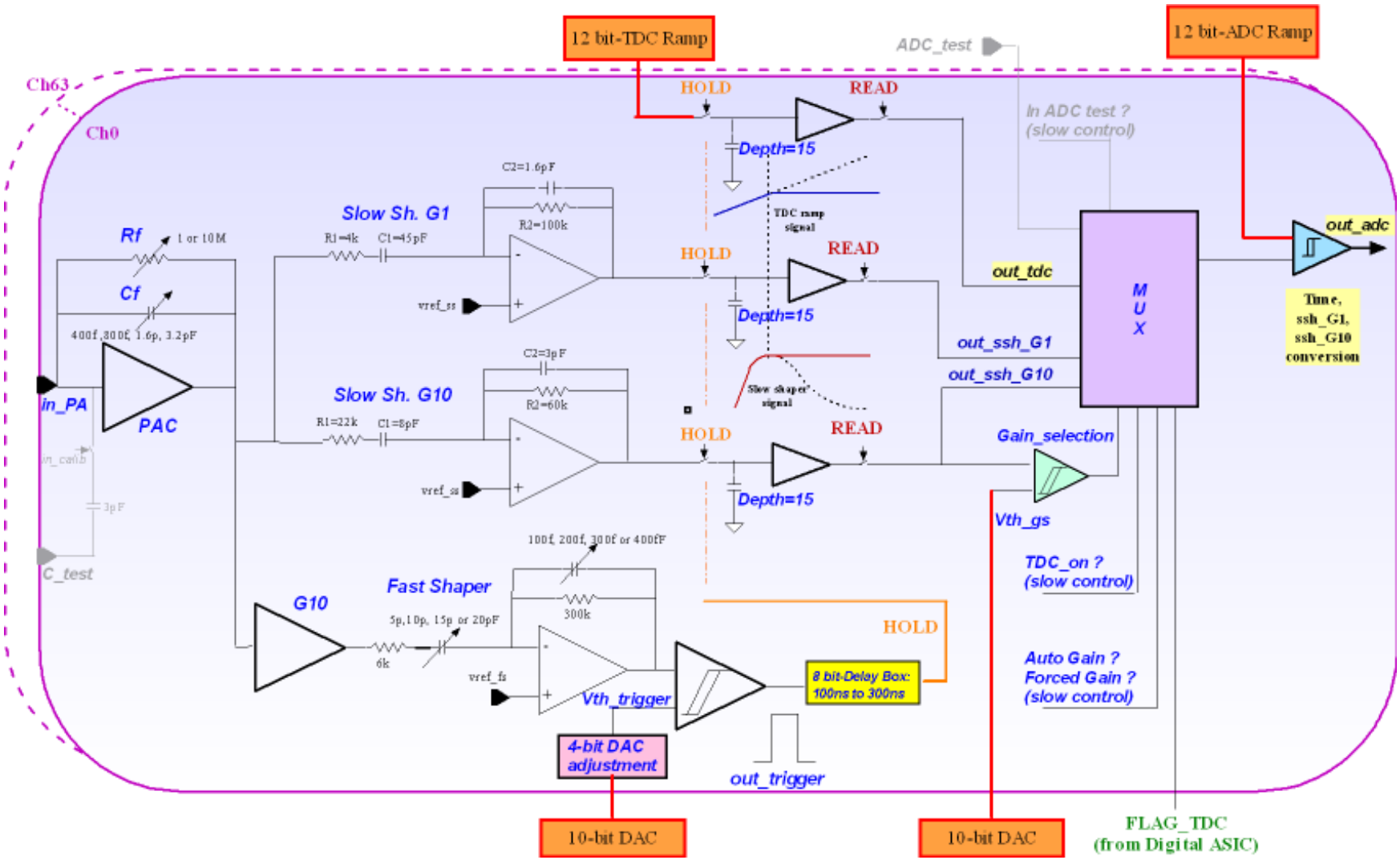
HARDROC
Digital HCAL
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06



SKIROC
ECAL
(Si PIN diode)
36 ch. 20mm²
Nov 06

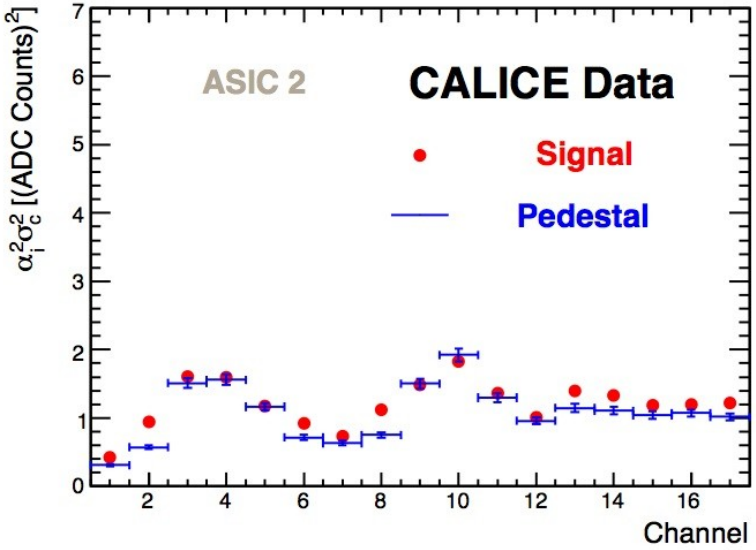


SKIROC 2 block scheme

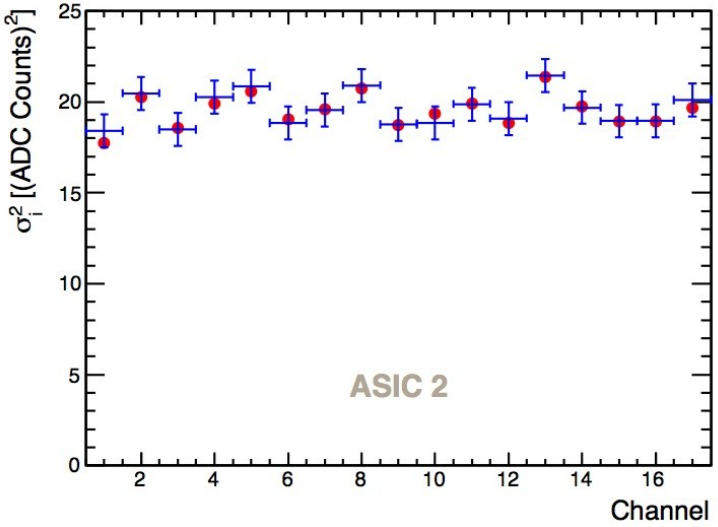


Detailed noise analysis

Coherent noise

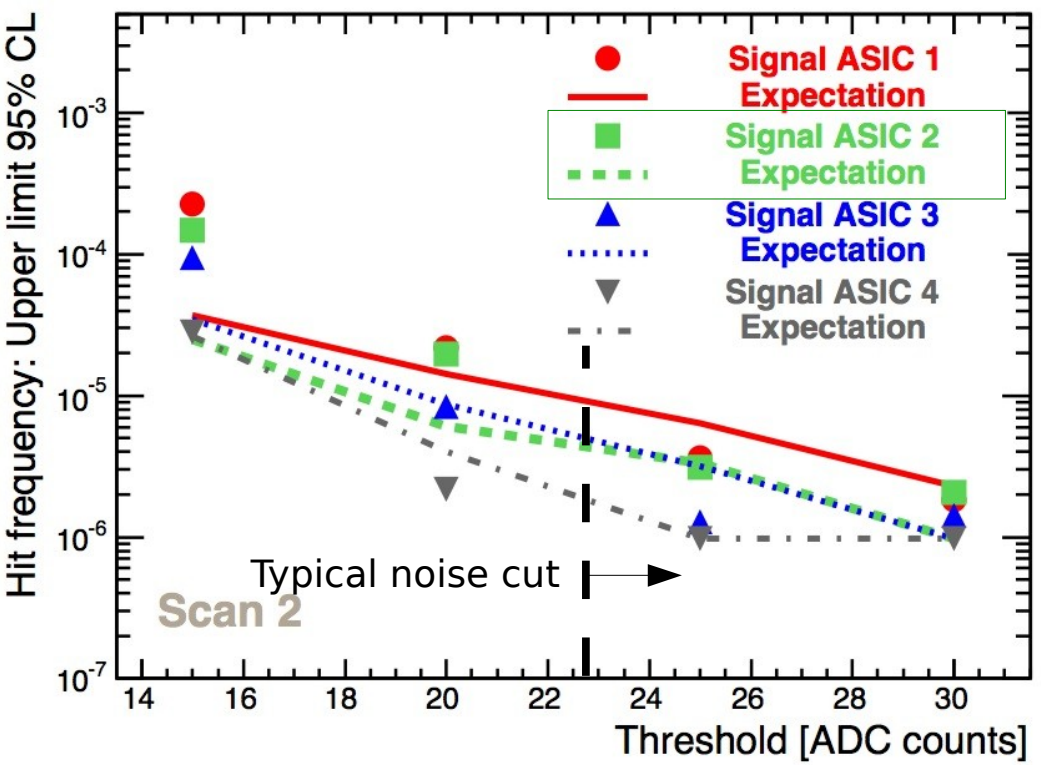


Incoherent noise



Noise pattern unchanged by shower particles

Upper limits on parasitic hits – 95% CL



Chip in beam

- Frequency of parasitic hits comparable with regular electronics noise
- < 10^{-5} above typical noise cut

Compare with 2500 cells in typical ee-> tt event