TRACKING AND VERTEXING SUMMARY

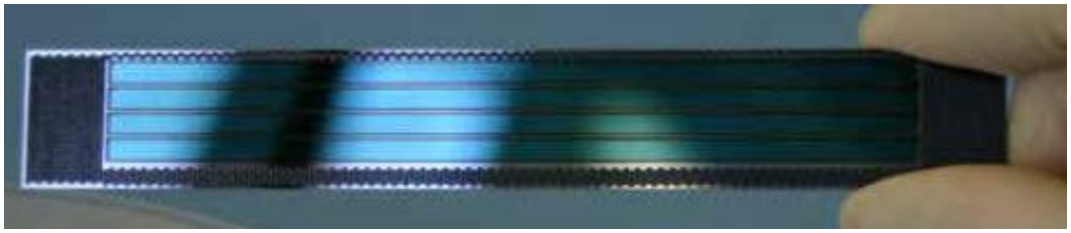
Suyong Choi
Korea University

Outline

- Vertex/tracking detector for ILC
- Vertex detector for CLIC
- LCTPC

DEPFET

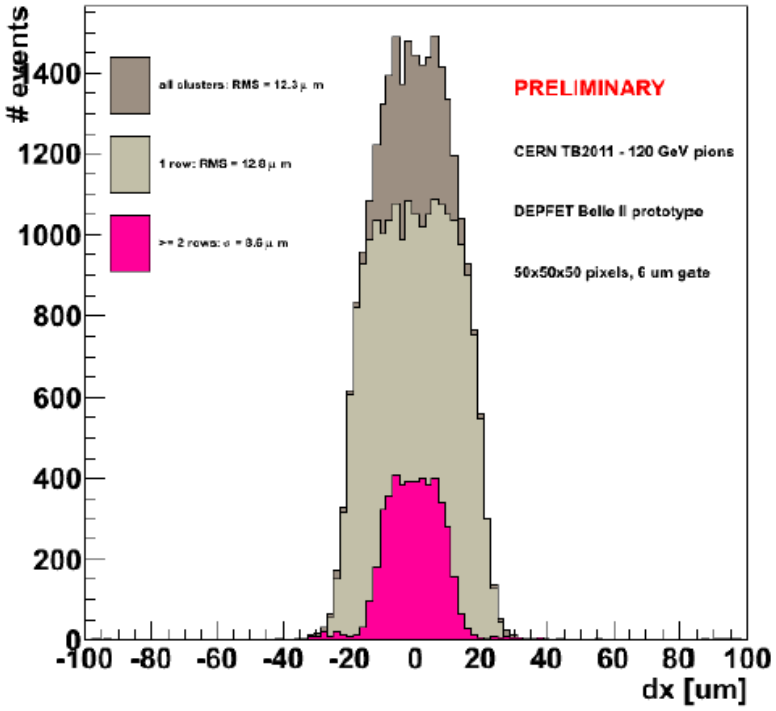
DEPFET



- Applications
  - Belle-II - 50x75 μm^2 , 75 μm thick
  - ILC - 25x25 μm^2, 50 μm thick
- PXD6 Sensor Production
  - 50 micron thick sensors (50x75 and 50x50 μm^2) produced
- PXD9 Sensor
  - Final design for Belle, 75 micron thick
  - Plan: Prototype run followed by production run
- ASICs
  - Close to final designs ready, produced and working
  - DHP02 needs to be moved to TSMC 65nm process
- DCD (drain current digitizer)
  - fully functional at full readout speed (600MHz)

DEPFET Test Beam

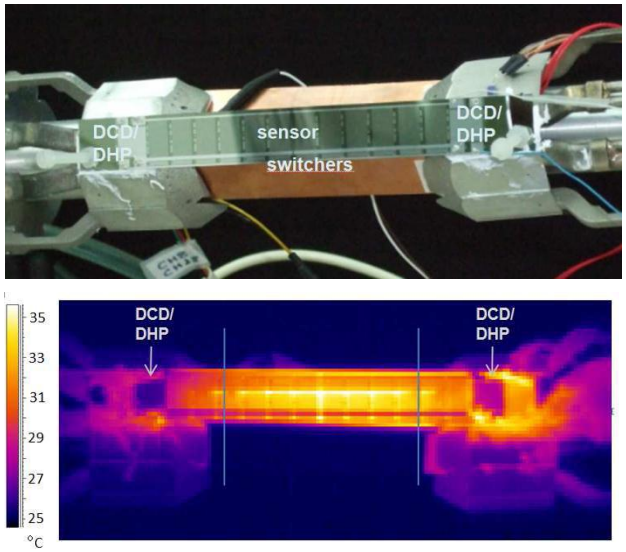
- PXD6 and ILC designs readout at 100MHz or 320 MHz
- Results
  - ILC design: S/N: 20 ~ 40
    - 25x25 μm^2, 450 μm thick sensor
  - Belle2 design:S/N ~ 40 for 50 μm thick sensor
    - translates to S/N ~ 60 for 75 μm thick
  - Position resolution for Belle2 design 12 μm slightly better than binary RMS (14.4 micron)
- Thin sensor performance demonstrated!



DEPFET – Cooling

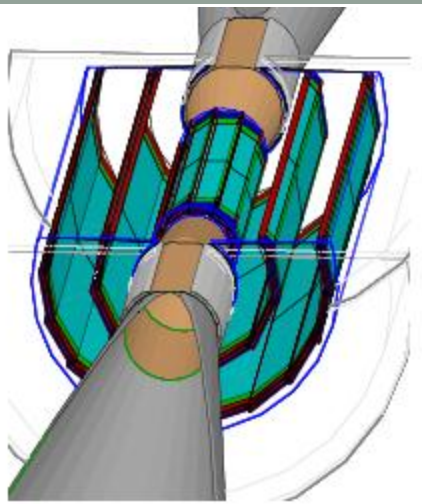
- Cooling
  - Mockup and simulation tools used
  - Belle-II (air + liquid cooling), ILC (air cooling)
  - 1 m/s air flow needed for sufficient cooling
    - 2 μm deformation for 2 m/s, 0.7 μm amplitude vibration
- ILC cooling
  - Power pulsing exercised
  - FEM analysis set up
  - Port belle-2 mock up to ILC
- By DBD, full measurements + simulations

- Mockup for Belle II

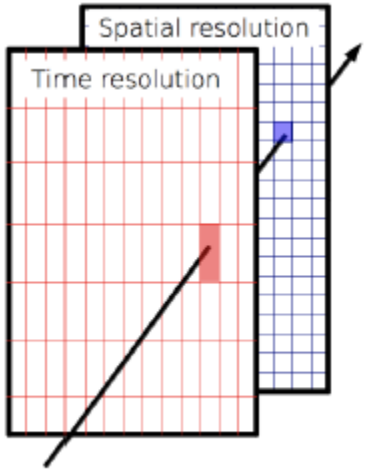


CPS – CMOS PIXEL SENSOR

CPS for ILD-VXD



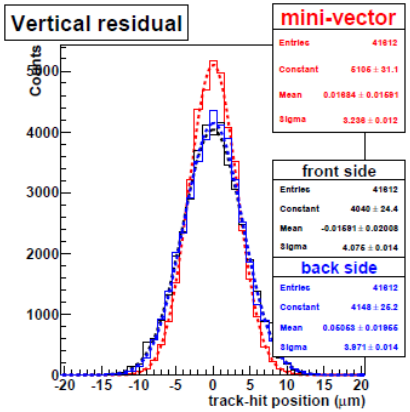
- Two types of CPS
  - Inner layer – 300 cm^2, resolution
  - Outer layer – 3000 cm^2 , power consumption

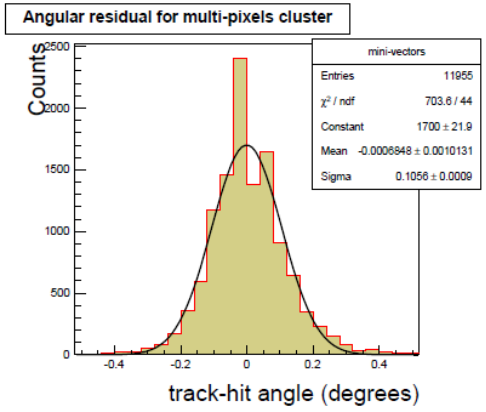


- 2-sided concept for inner layer
  - 16x16 μm^2 for spatial resolution t_{ro}~$50\mu s$
  - 16x80 μm^2 for time resolution t_{ro}~$10\mu s$
    - For time stamping
- Sensor prototypes produced in Q4/2011
  - Mimosa 30 – inner layer prototype
  - Mimosa 31 – outer layer prototype

CPS

- Double sided detector:
  - 6 mimosa-26 on each side of ladder, 8M pixels
  - Test beam in Q4 2011 @ CERN SPS π^- >100 GeV beam





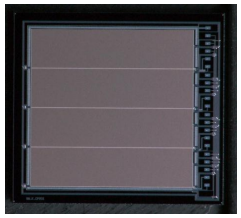
- New 0.35% X_0 prototype under construction
  - Beam test in Q4 2012

CPS

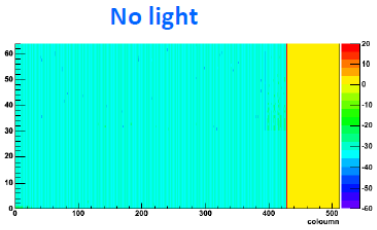
- Mimosa 30
  - 8x256 with 16x16 μm^2 pixels, 8x64 with 16x64 μm^2 pixels
  - 15e ENC with 10 μs readout
  - Beam test in Jun/Jul
- Mimosa 31
  - 48x64 with 35x35 μm^2 pixels
  - Beam test in 2013
- Meets VXD specs for $\sqrt{s} = 500$ GeV
- For $\sqrt{s} = 1$ TeV
  - 0.35 $\rightarrow$ 0.18 μm process
  - Faster readout 2(inner)/10(outer) μs with accelerated read out techniques
  - >20% Less power consumption, good sensor throughput
  - Mimosa 32 - exploratory chip under test
  - Prototypes for validating architecture to be submitted Q3/Q4 2012
  - Full scale block in 2013
  - Full scale prototype in 2014/15

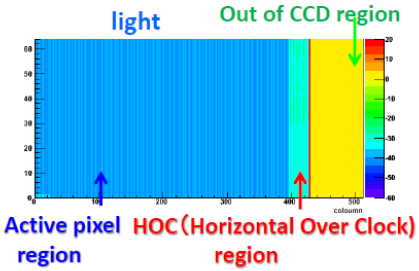
FPCCD – FINE PIXEL CCD

FPCCD



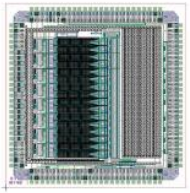
- 2nd FPCCD readout ASIC
  - Total noise 16e < 30e
  - prototype power consumption: 30.9 mW/ch > 6 mW/ch





- 3rd FPCCD readout ASIC
  - Changes to analog and digital readout
  - Process: 0.35 μm to 0.25 μm
  - 5.4 mW/ch
  - DNL and INL improved to within ±1LSB and 0.38%

3rd prototype layout

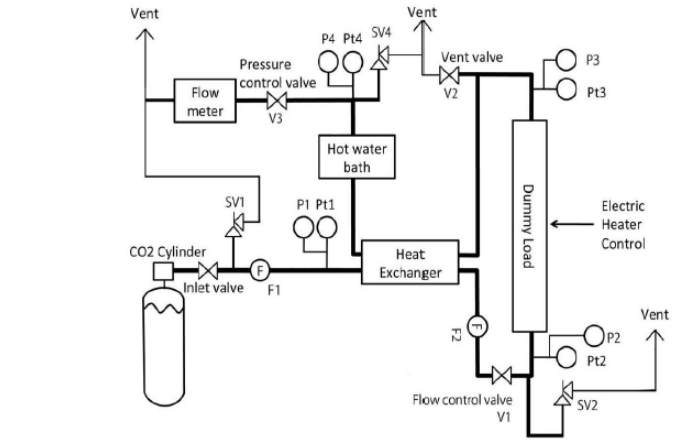


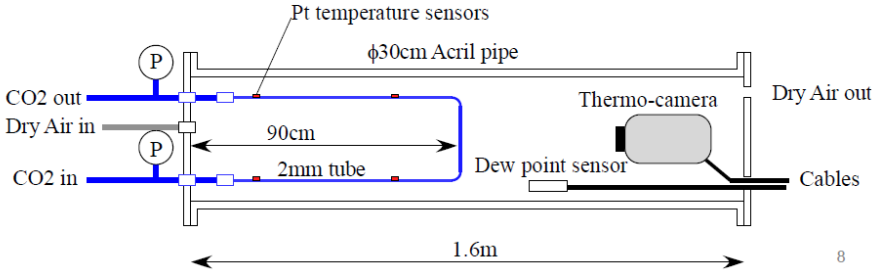
- Plan
  - 2nd Prototype - test using radiation sources
  - 3rd prototype – chip arrival in Oct

Cooling of FPCCD Vertex Detector

- To minimize charge transfer inefficiency due to radiation damage cooling to -40 C is optimal
- Use two-phase CO_2
  - Large latent heat of C02
  - Smaller flow rate
- Cooling system test mock up
  - No condensation
  - Heat penetration 20W/m measured
- Plans
  - Cooling test of dummy ladder/end-plate
  - Circulating system

- CO_2 cooling blow system between -40C and 15 C

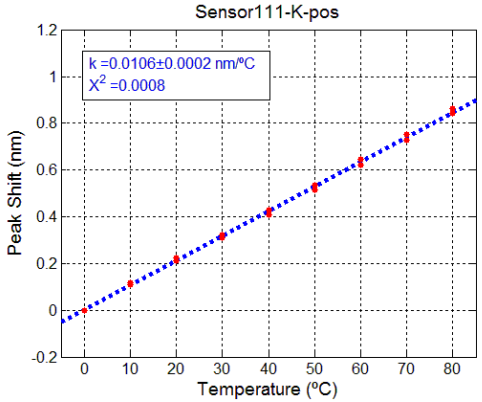


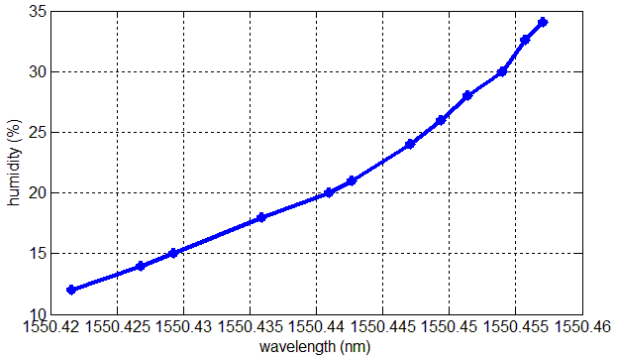


FORWARD TRACKING

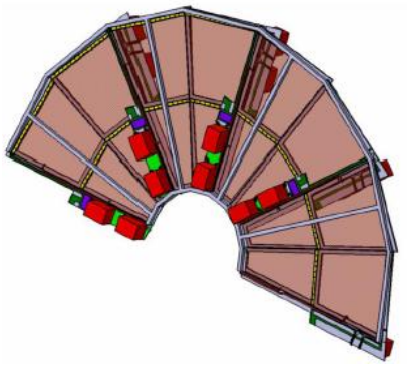
Fiber Bragg Grating sensor for FTD

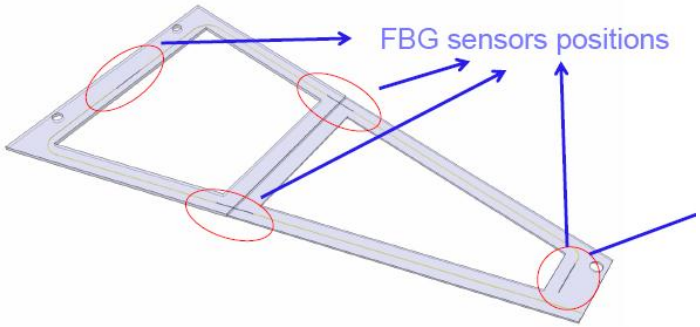
- Temperature and humidity measurement with FBG





- Sensitive to strain and deformations



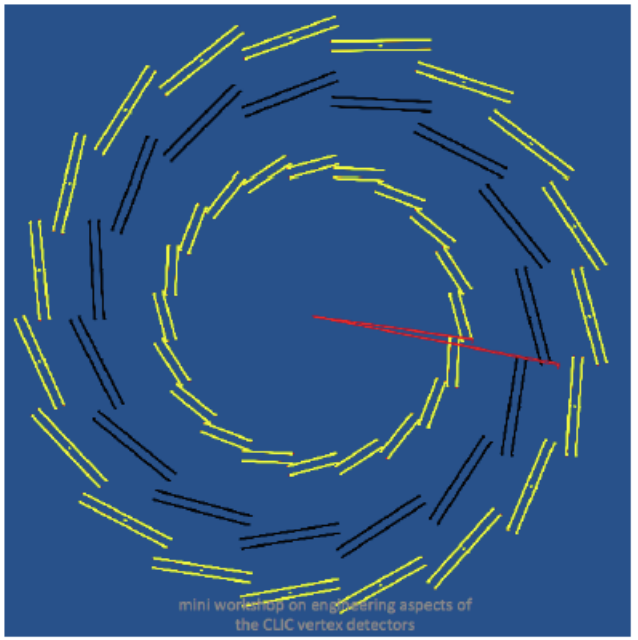


CLIC VERTEX DETECTOR

VTX requirements for CLIC

- Vertex requirements
  - Efficient tagging of heavy states: 3 μm spatial resolution
  - <0.2% X_0 per layer
  - Coverage to 7°
  - Occupancy ~ A few %
  - Time stamping with 10ns accuracy to suppress bkgs.
- No technology that fulfills all requirements
  - Simulation – impact of layout
  - Integration/assy. , power pulsing, cooling
  - R&D on sensor and readout

- Post CDR design
  - Minimize cabling, vertical integration
  - inactive regions, Lorentz angle

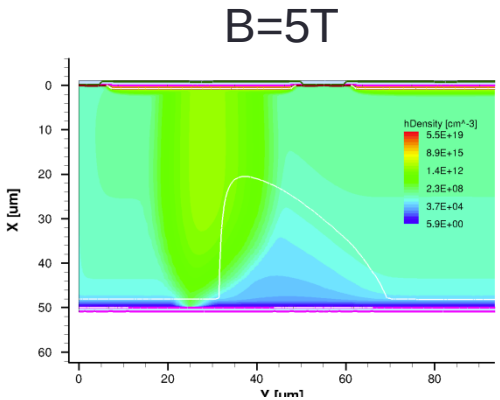


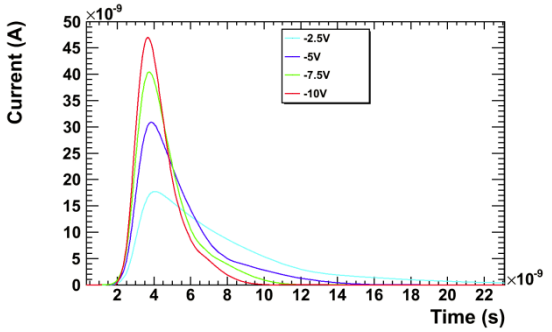
Vertex Detector R&D for CLIC

- Pixel technology
  - 25x25 μm^2
  - 10ns time stamping
  - 0.2% X_0: 200 micron thick Si –incl. support and cables
- Hybrid
  - Thinned detector (50 micron thickness) + readout chip (50 micron thickness)
  - Need low mass Interconnect
  - Hard to reduce material, difficult/expensive interconnect
  - CLICpix: 65nm process, 25x25 μm^2 ,~2015
    - Test structures on 65nm tested OK
    - Demonstrator prototype to be submitted 2012: 64x64 pixel array
- Integrated tech
  - 3D integration of sensor and readout chip
  - Charge collection in epitaxial layer $<1\mu m$
  - More Difficult to achieve good time resolution with sufficient S/N
  - TSV (medipix 3), edgeless sensors

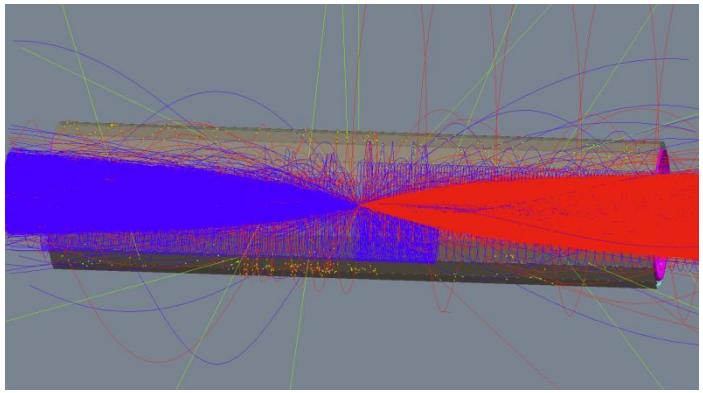
Simulations

- Sensor
  - Charge collection
  - Charge sharing
  - Signal rise time



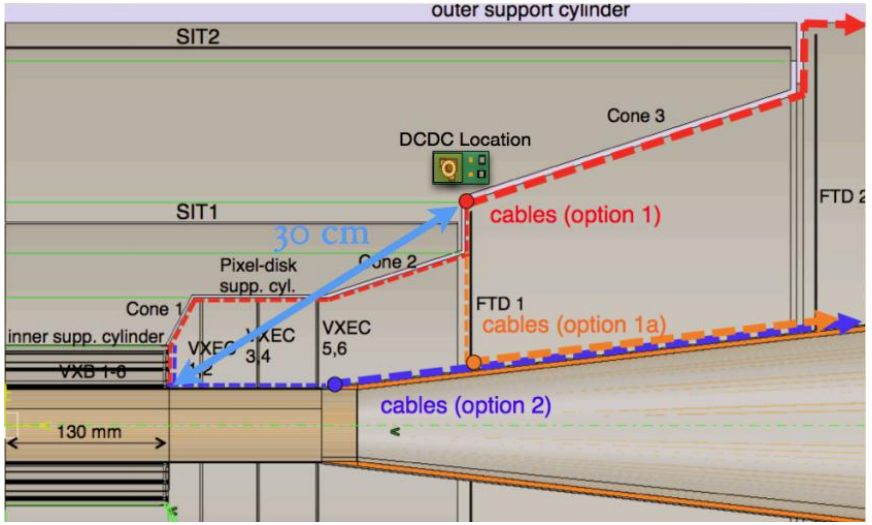


- Backgrounds
  - 5~10 hits per cluster for innermost vertex barrel layer from incoherent pair backgrounds
  - 0.5%~1% occupancies

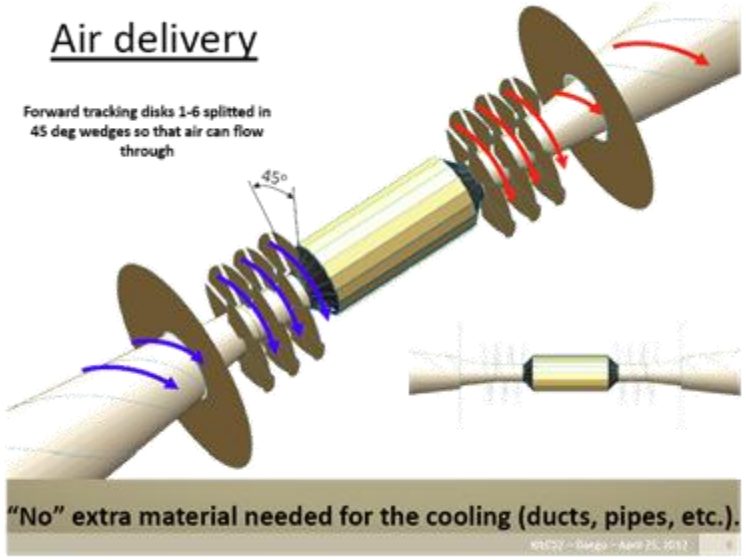


Power and Cooling

- Power
  - Kapton flex cable
  - Deal with large and short current peaks
  - Large currents along ladders
    - stitching across modules



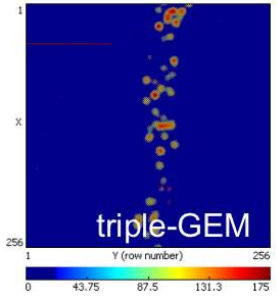
- Cooling
  - Helical motion of air through double walled beam pipe and support
  - Air speed: 11m/s at inlet
  - Sensor deformation: ~ $2\mu m$
    - Due to special barrel support
  - Looks promising

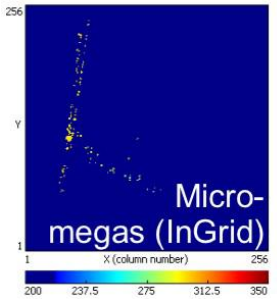


LCTPC

LCTPC Status

- MPGD Technologies
  - DESY GEM - ($50\ \mu m$), triple GEM, new module tested end of summer
  - Asian GEM - ($100\ \mu m$) modules, double GEM, new processing, new readout electronics in 2013
  - Micromegas – new modules with integrated electronics should be tested in large prototype in DESY in July
- Timepix
  - Readout with both GEM and Micromegas
  - Full module work started 120 timepix chips, 8M pixels
- SALTRO16
  - power pulsing reduces power by 1/60.
  - Work started on final version (GdSP) for LCTPC





LCTPC

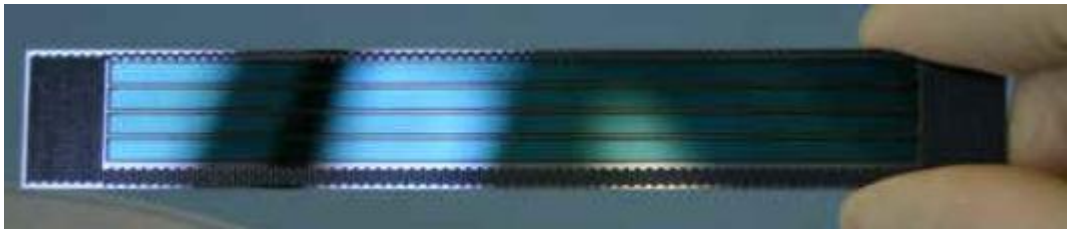
- Prototypes
  - LP1 test beam at DESY (1-6 GeV electron beam)
  - LP2 – upgrade from LP1
    - Magnet using cryocoolers
    - new end plate(realistic material budget) ⟶
    - new cage field (end of 2012)

- Simulation suggests ion back-drift in amplification cause 60 micron distortion. Gating system may be needed.

- Plans
  - Upgraded test beam facility to test momentum resolution
  - Hadron beam to test multitrack environment

BACKUP

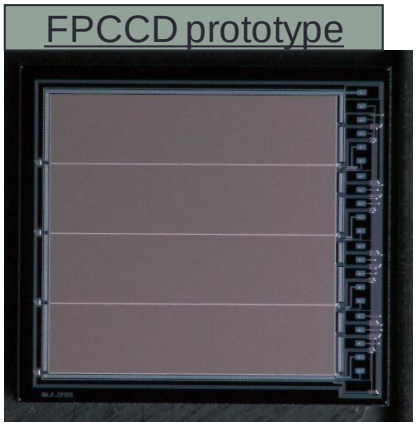
DEPFET



- In-pixel amplification, thin active sensor, low power consumption
- All silicon module - one material, self-supporting sensor
- Application: Belle-II and ILC
  - Belle-II requirements: 0.15% X_0 /layer, higher occupancy (x4) and radiation (x10) than ILC
  - Belle-II - 50x75 μm^2 , 75 μm thick
  - ILC - 25x25 μm^2, 50 μm thick

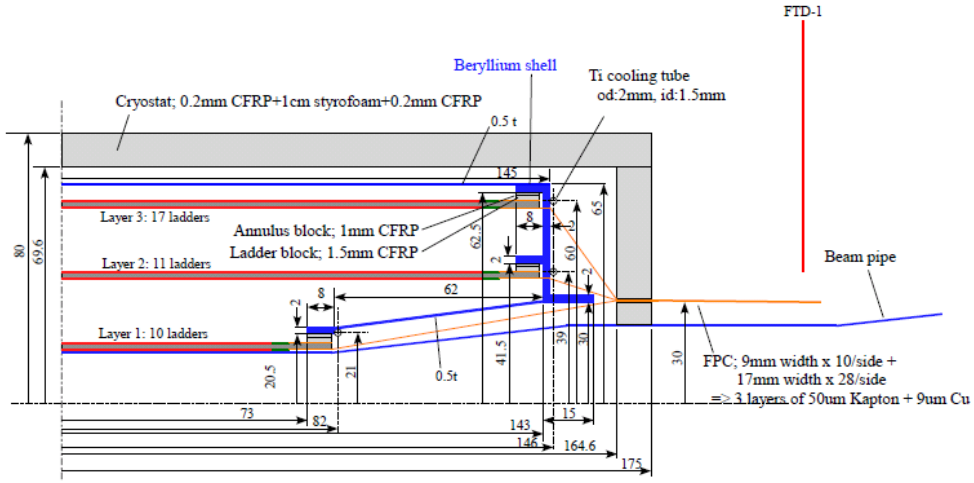
FPCCD vertex detector

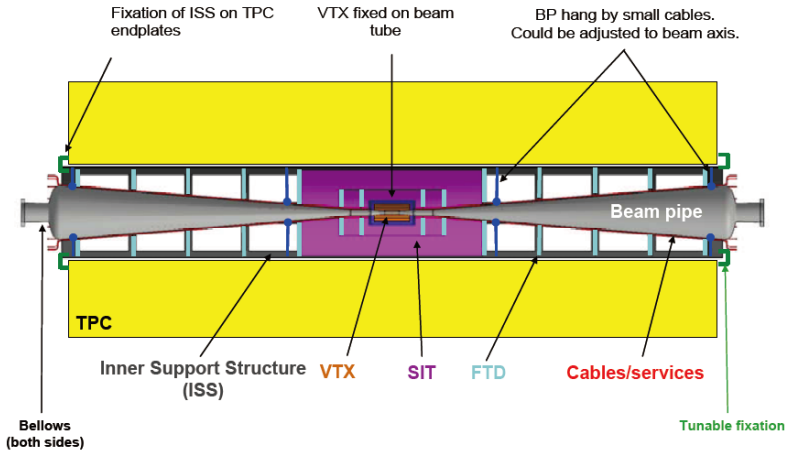
- Fine Pixel CCD
  - Pixel size ~ 5μm
  - Fully depleted epitaxial layer
  - Read out between trains (No power pulsing)
- FPCCD vertex detector
  - Double-sided ladder
  - 1.6×10^{10} pixels
  - Sensors and front-end ASICs inside a cryostat
  - Power consumption > 50W inside the cryostat
- Readout ASIC
  - Total power < 100W
  - 10 Mpix/sec
  - Noise + ADC accuracy < 30e (signal size 500 e)



CO_2 cooling for FPCCD VTX

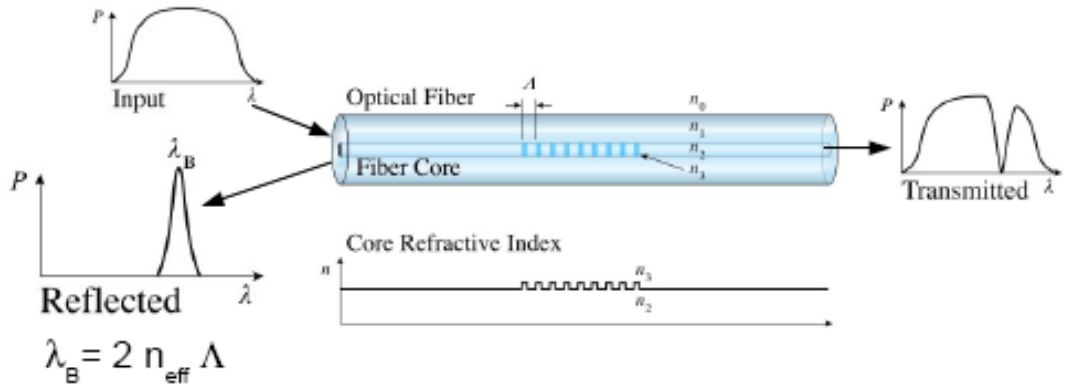
- Cooling tube is attached to VTX end-plate and heat removed by conduction through CFRP ladder
- Return line of CO2 will be used to cool the electronics outside the cryostat (~200W/side)
- Inner support tube should be air-tight and filled with dry air/nitrogen in order to prevent condensation on the CO2 tube





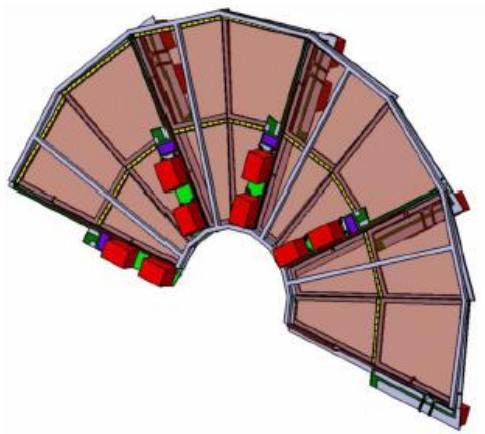
Fiber Bragg Grating Monitoring

- Fiber Bragg Grating sensor principle

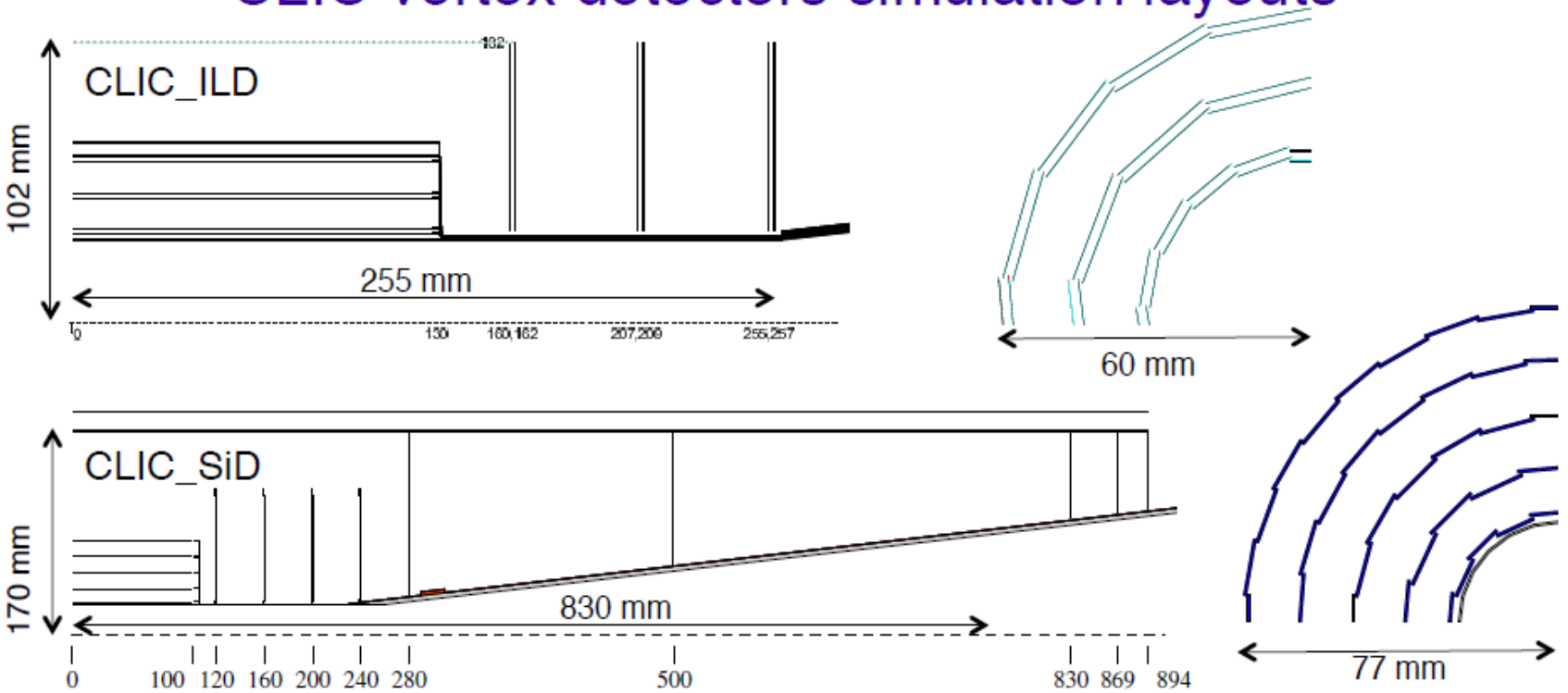


λ_B is sensitive to strain and T: $\left[\frac{\Delta\lambda_B}{\lambda_B}\right] = C_S\epsilon + C_T\Delta T$ { ~10 pm/K, ~1 pm/με

- Environmental and structural monitor
  - Low material budget
  - Immune against high EM fields
  - Can be used in high and low temp.
  - Suitable in radiation environment



CLIC vertex detectors simulation layouts

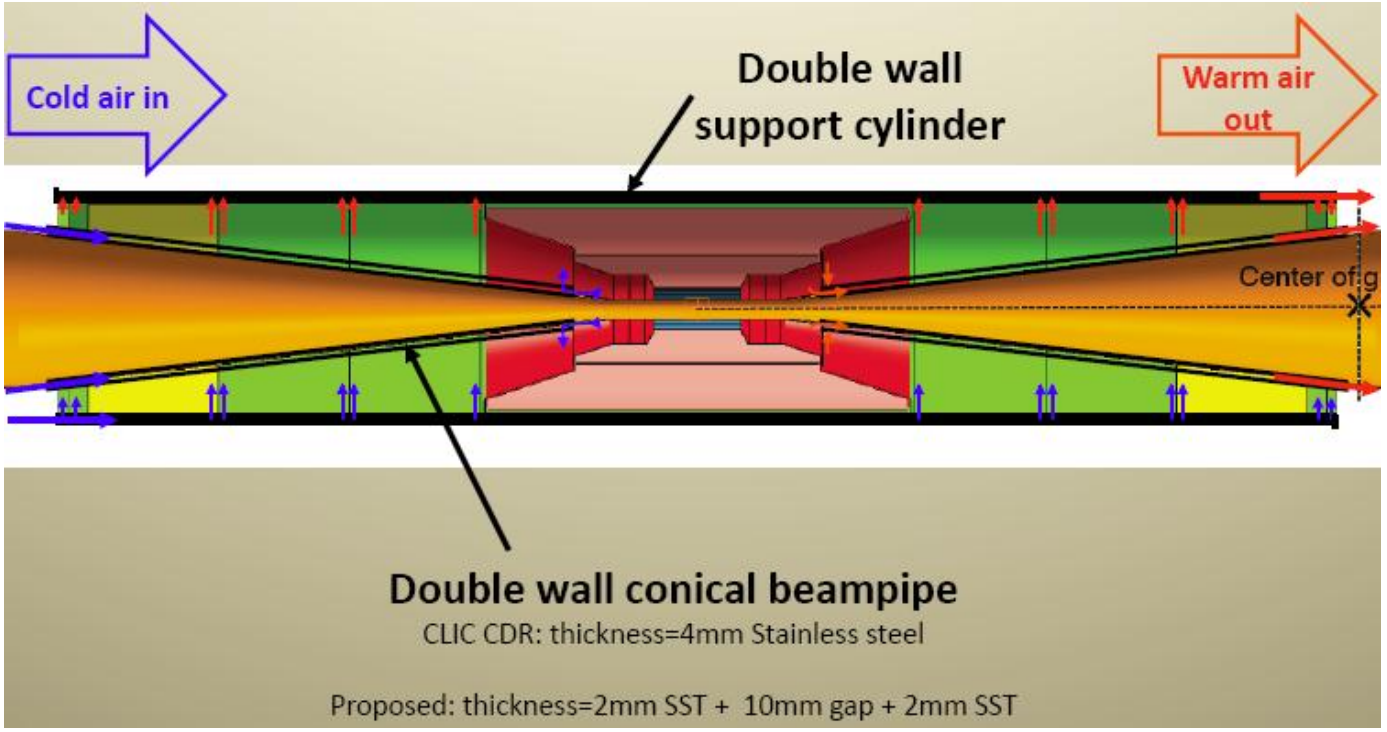


	CLIC_ILD	CLIC_SiD	CMS
Material X/X0 (90°)	~0.9% (3x2 layer)	~1.1% (5 layer)	~10% (3 layer)
Pixel size	20 x 20 μm²	20 x 20 μm²	100 x 150 μm²
# pixels	1.84 G	2.76 G	66 M
Time resolution	~10 ns	~10 ns	<~25 ns
Avg. power/pixel	<~0.2 μW	<~0.2 μW	28 μW

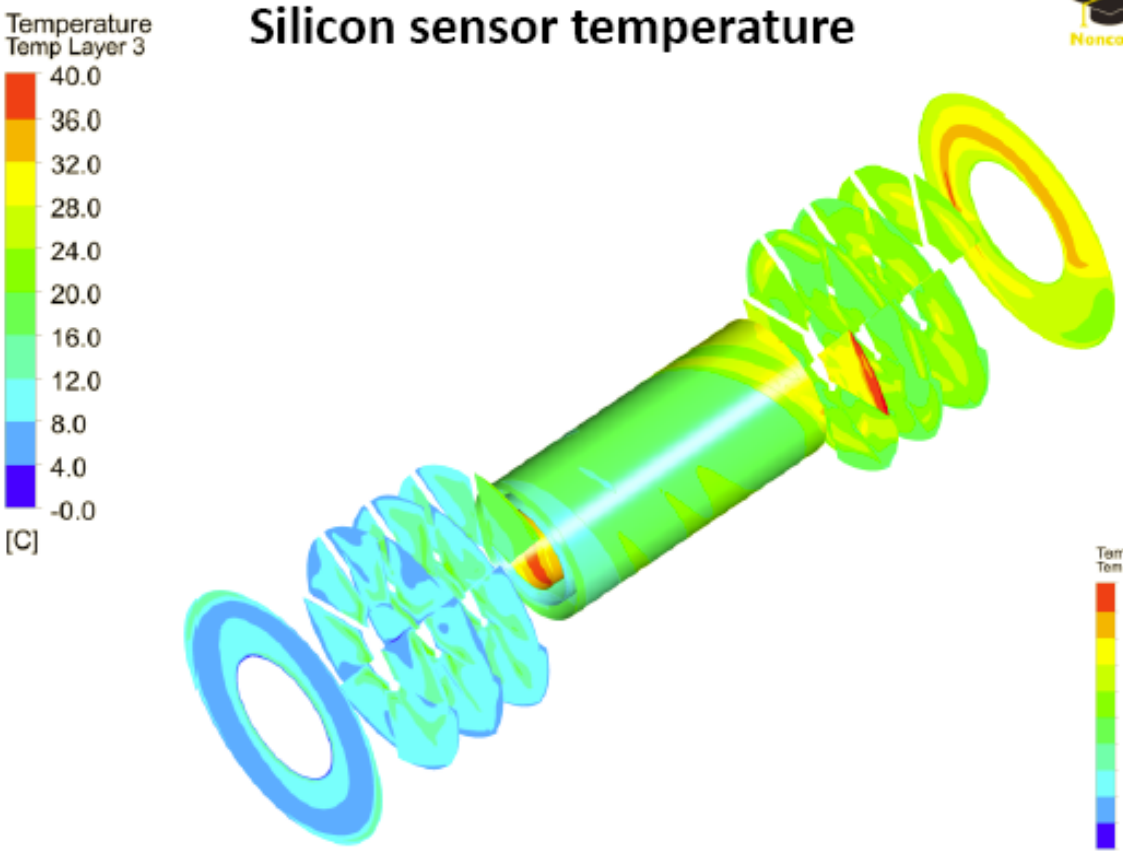
Cooling

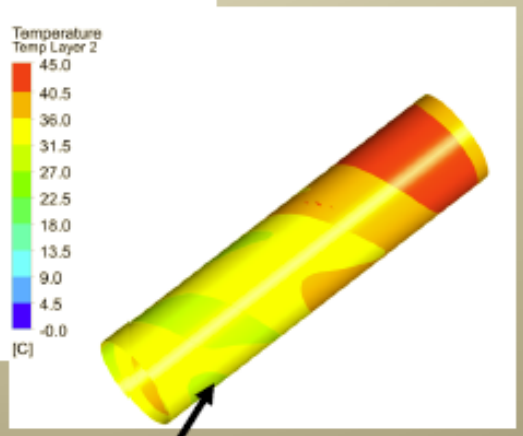
- Power: 500W (50mW/cm^2)

- Forced dry air – baseline for barrel region



Silicon sensor temperature





Barrel support geometry will need further optimization
(temperature at barrel layer 2 above 40 C)
Otherwise temperature is kept below 30 C