Clock module for TB spring 2012

R.Degele, P.Kiese, U.Schäfer, A.Welker
Mainz

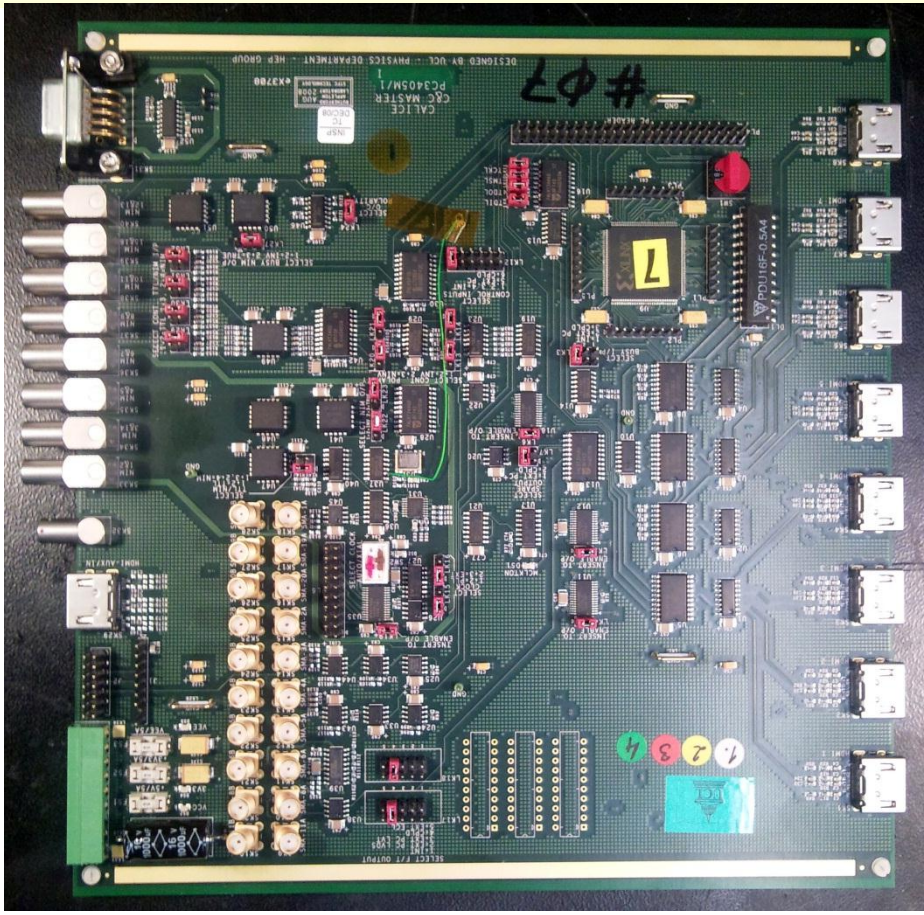
Clock module: CCC

Handling of trigger and machine signals, trigger fan-out, busy logic.

Current status:

- UK-developed CCC exists and is being used for clock distribution in beam tests and in the lab
- Mature design, based on CPLD and discrete fan-out / drivers
- Jitter specs seem rather unclear
- CPLD seems rather full
- Not designed for future use : Calice integration with EUDET / AIDA TLU ("Timing Logic Unit") / beam telescope

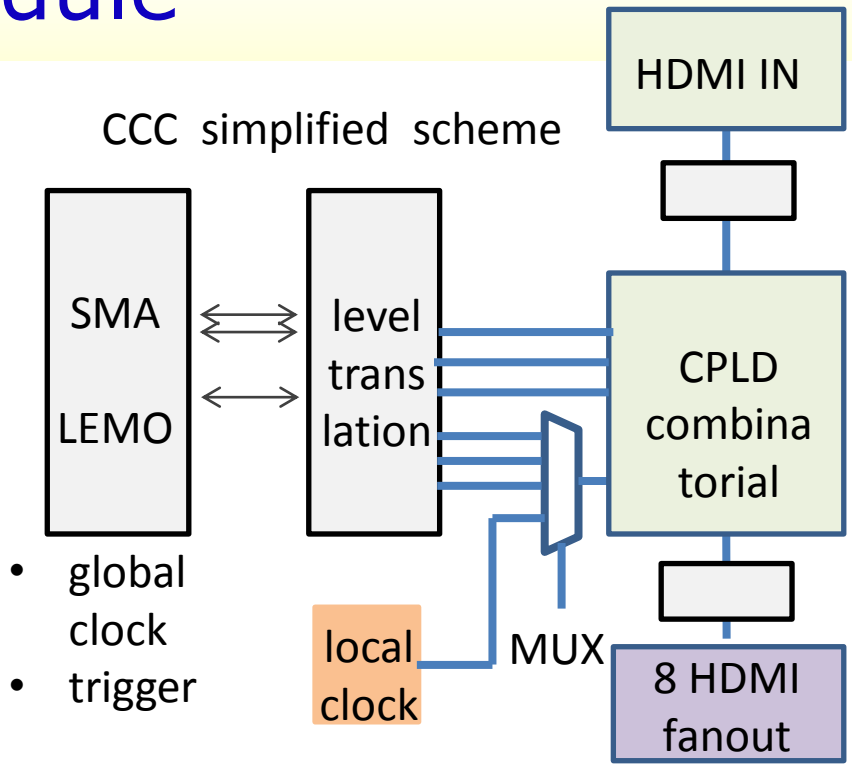
(Disclaimer: That's my personal level of (mis-)understanding)



Clock module

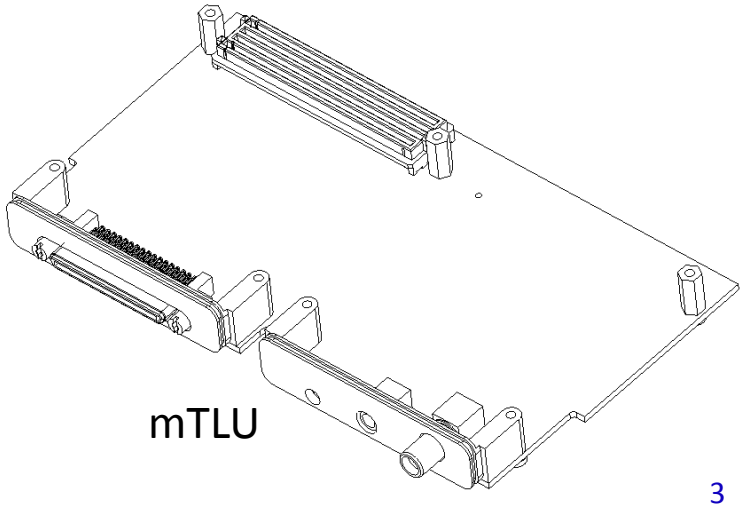
CCC situation has been discussed at CALICE & AIDA mini workshop (9/10 Nov, 2011, Palaiseau)

→ Provide improved/extended module at a timescale spring 2012 (beam test), addressing main issues. Scope for further improvements thereafter.



Mini TLU design has been presented by D. Cussans/Bristol

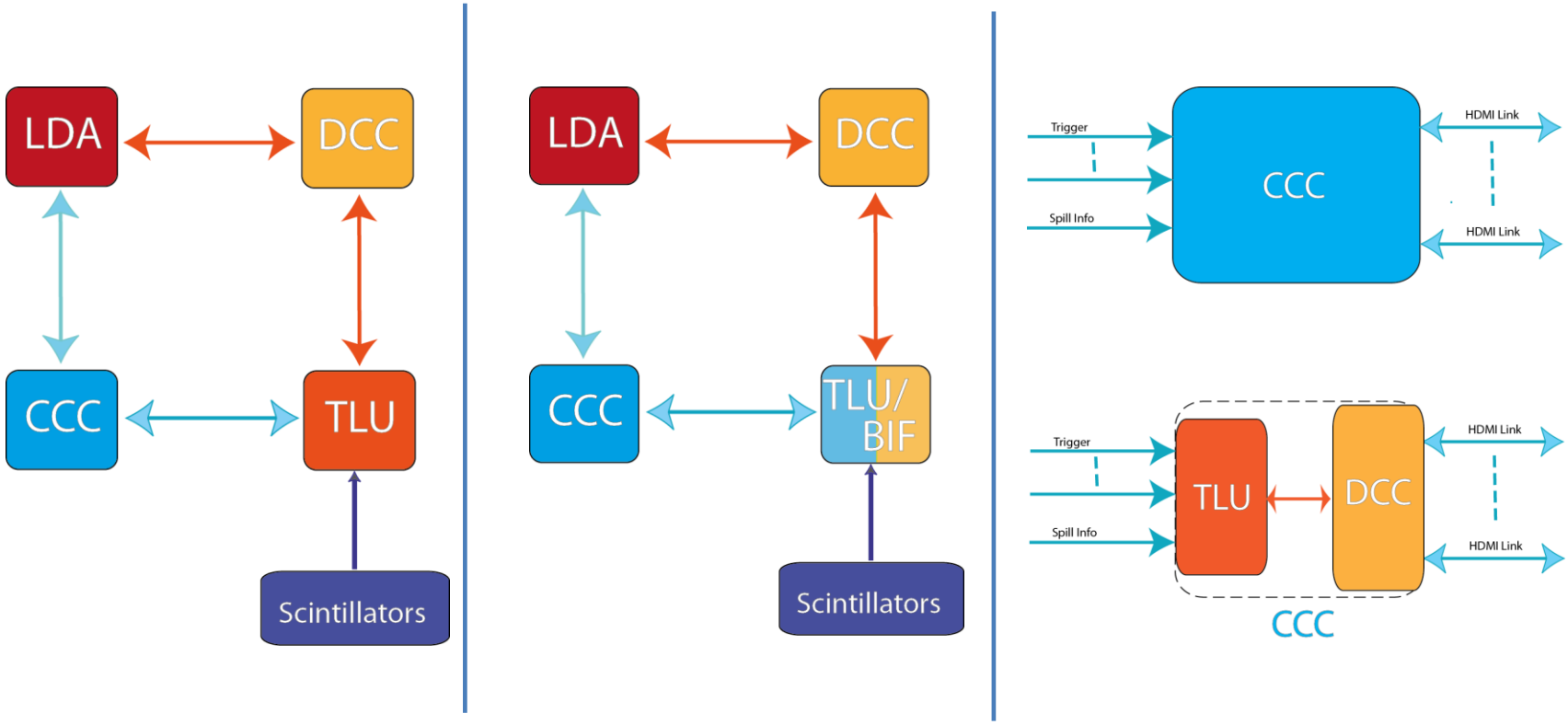
→ Meanwhile: discussions with D. Cussans on a common hardware development for Calice clock module / mini TLU



TLU integration

Sketch by D. Cussans:

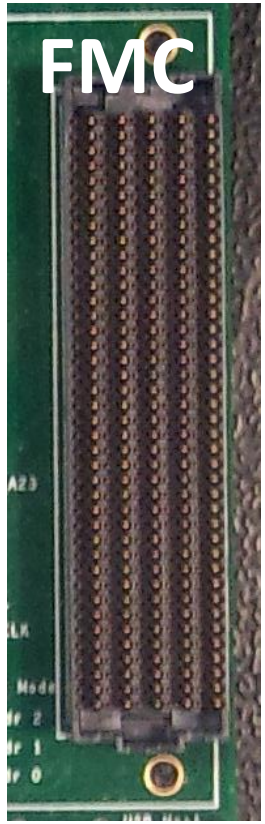
Combining TLU / BIF and CCC



Some preferences / issues

As of Nov.2011 (Palaiseau) for future electronics we would consider:

- FPGA based modules
- Custom designs make use of FMC standard (mezzanine modules)
- Think about crate based modules rather than table-top (VME-6U?)
- For readout and control consider Ethernet (direct FPGA-based, not micro controller(core))



Medium term (common test beams): Remember need for integration of Calice clock modules with EUDET/AIDA TLU

- Agreed with UoB on common hardware development effort for Calice clock module / mini TLU
- TLU distributing synchronous triggers,
  Calice (CCC) triggers are asynchronous signals !!!

Something to think about (for the experts)

- It has been suggested to go for FPGA based modules
- Asynchronous code in FPGAs is **horrible**.
- TLU is operating on synchronous signals for exactly that reason

Can we operate Calice detectors/electronics on synchronous triggers ?

- Measure phase of all incoming signals on machine interface (scintillators, test beam signals,…) wrt to global clock (TDC)
- Issue synchronized (to global clock - or multiple -) trigger signals to LDAs → detectors
- These triggers have a maximum jitter of one clock tick
- Send TDC data into DAQ for offline corrections

Questions:

- What's acceptable trigger jitter if **not** using offline correction ?
- What's required resolution of TDC if using offline correction ?

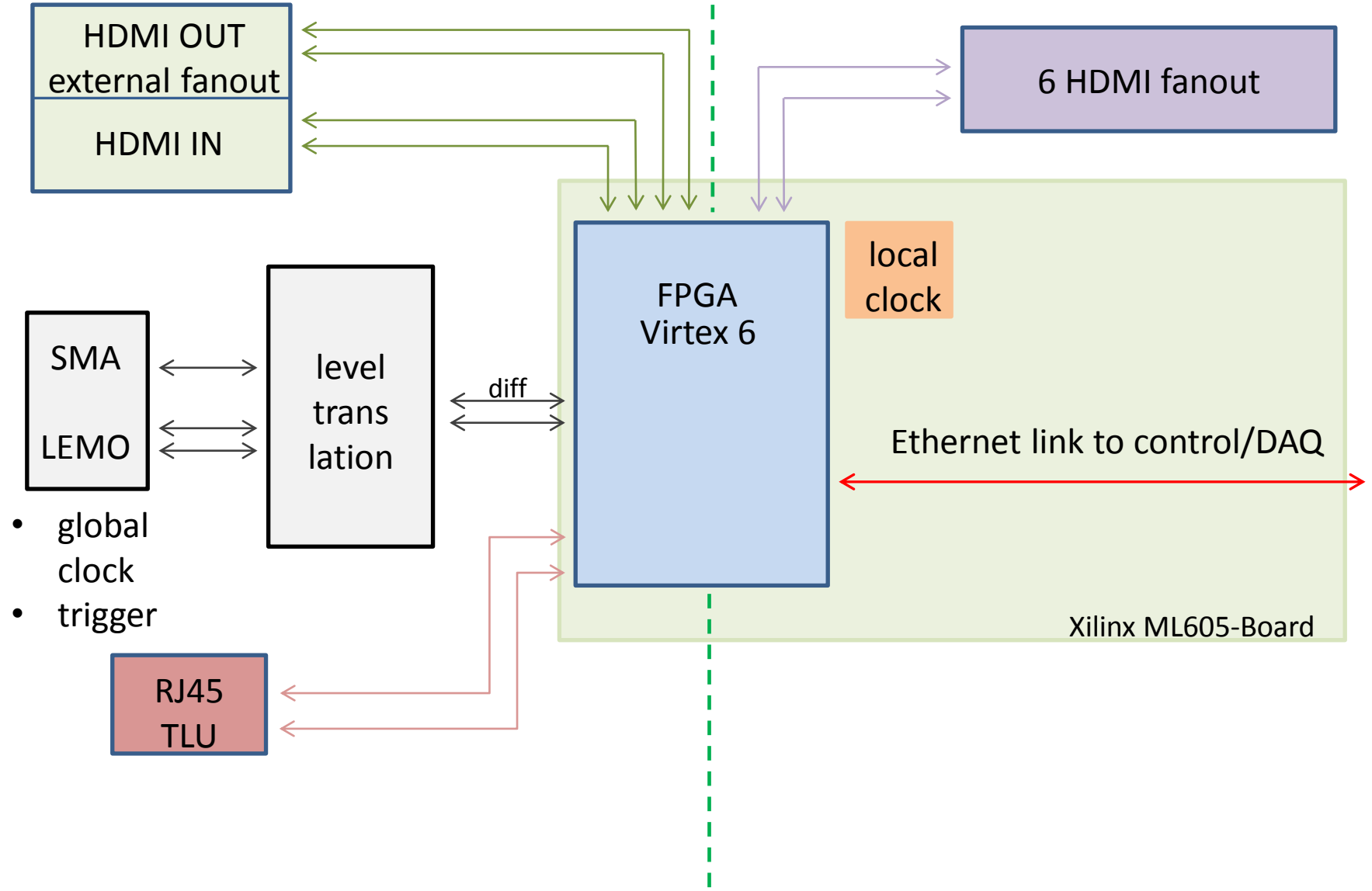
Quick fix TB spring 2012

- Go ahead with module development as discussed:
  - Functionality → FPGA (Xilinx ML605 evaluation board)
  - Connectivity (connectors, drivers/level translators) → mezzanine (FMC)
- Route all signals through FPGA
  (In case it turns out later that we do require asynchronous operation, bite the bullet and do that horrible code)
- Control jitter and skew to required levels (???)
- Replicate CCC functionality
- Integrate TLU functionality for connection to beam telescope
- Control via Ethernet (IPBus / Bristol)

Your input is required:

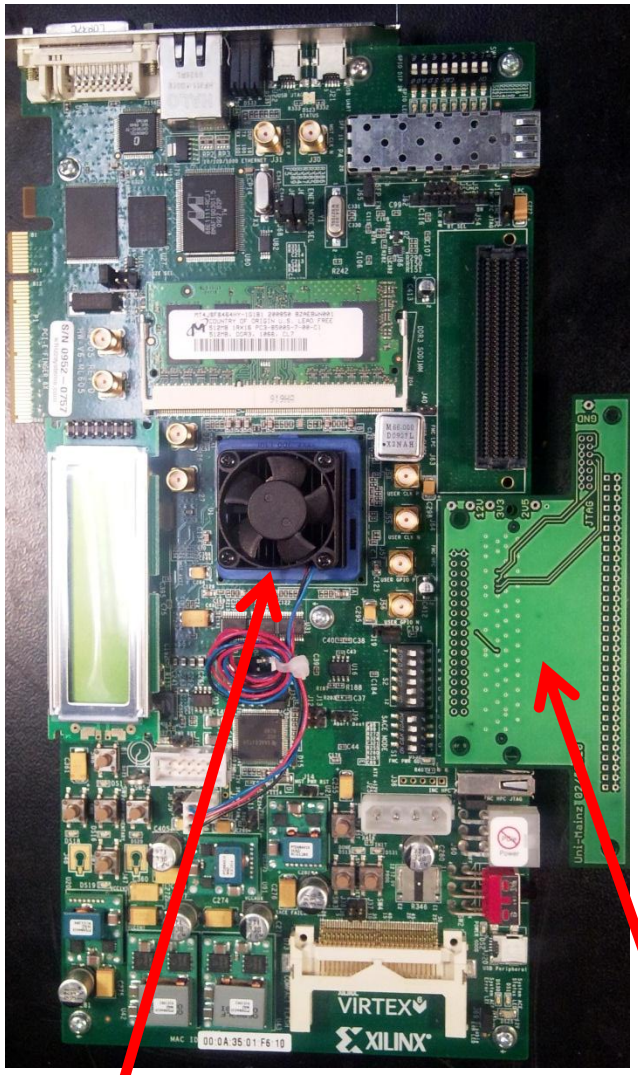
- In case there were a strong bias against synchronous triggers we'd rather know now. Might have to go for quite different scheme
- Need to verify need for replication of full CCC functionality
- Need to learn about insufficiencies of current CCC

Clock module



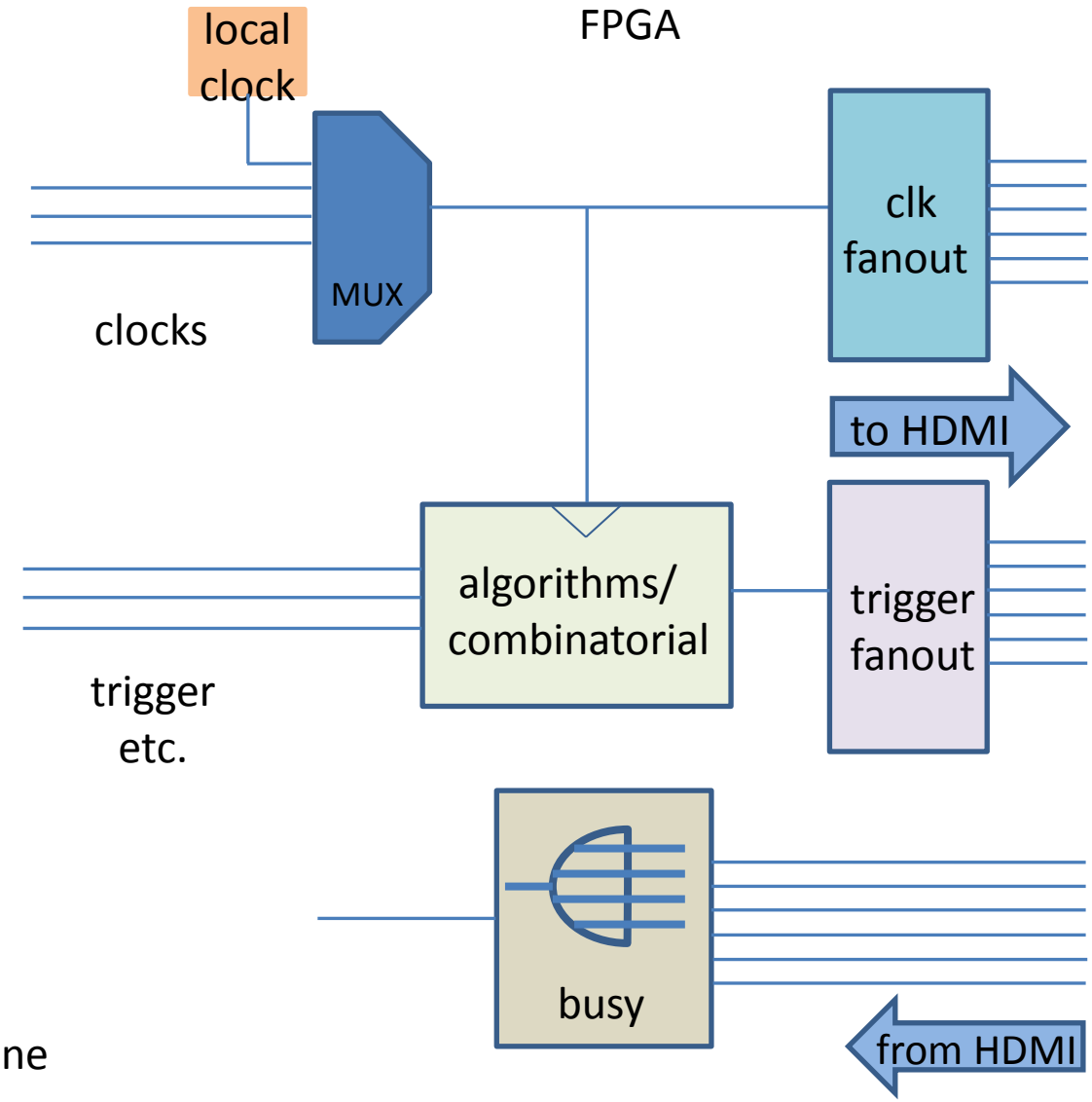
- global clock
- trigger

ML605/mezzanine -- FPGA internal



FPGA

mezzanine

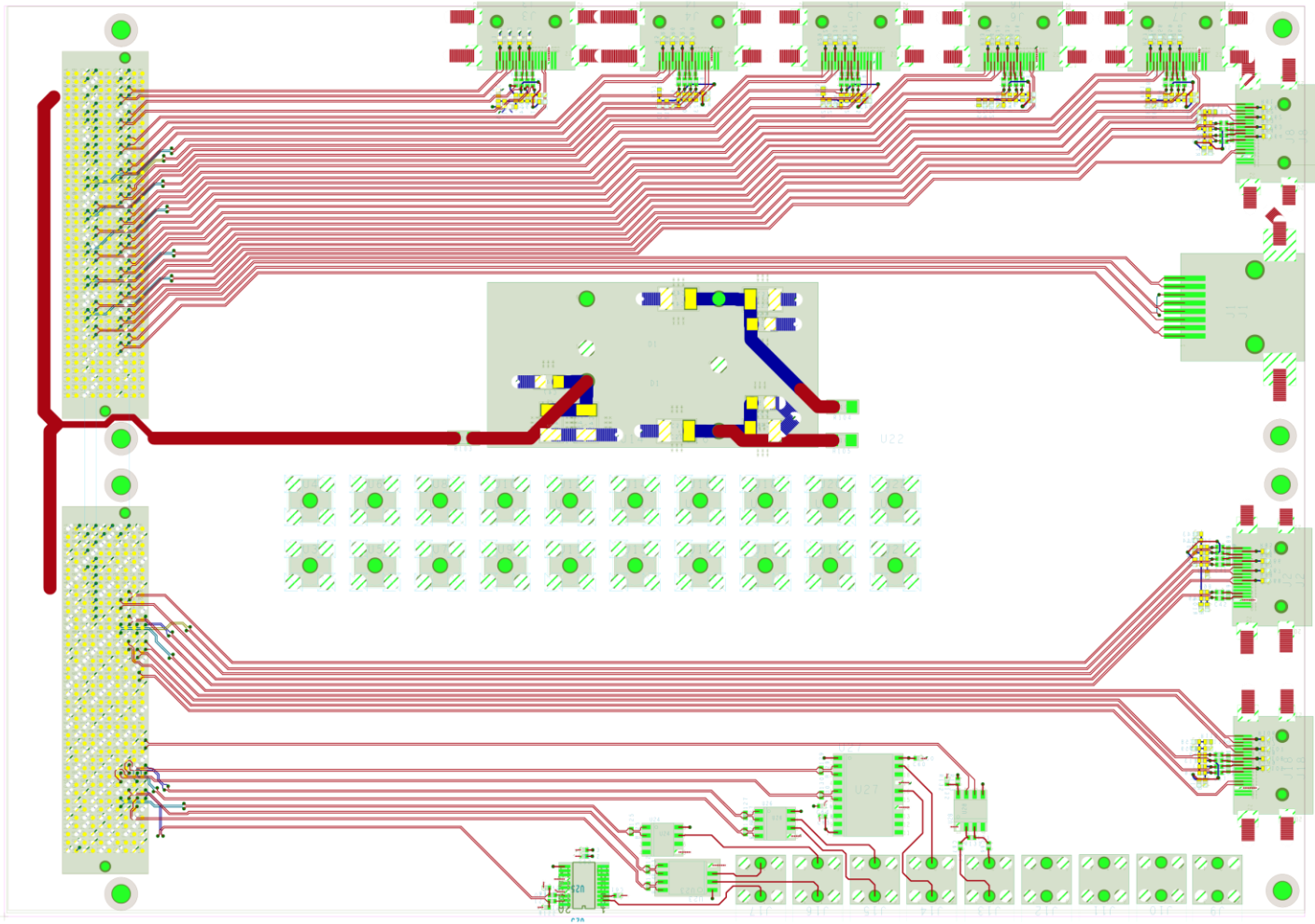


Clock module: current status

- Reverse engineered current CCC
  no requirements, no specs, just schematics
- Schematic capture almost finished
- Initial floor plan available
- Layout started
- Machine interface and trigger generation well isolated from trigger replication
  - Using both FMC connectors on ML605 board
  - “HPC” connector to machine interface and TLU style interface
  - “LPC” connector to HDMI trigger fanout

www.staff.uni-mainz.de/degele/Calice/CCC/CCC_XILINX.SCH.pdf

Layout and PCB Stack



	Subclass Name	Type	Thickness (MM)
1		SURFACE	
2	TOP	CONDUCTOR	0.03048
3		DIELECTRIC	0.2032
4	GND	PLANE	0.03048
5		DIELECTRIC	0.2032
6	SIGNAL1	CONDUCTOR	0.03048
7		DIELECTRIC	0.2032
8	GND1	PLANE	0.03048
9		DIELECTRIC	0.2032
10	SIGNAL2	CONDUCTOR	0.03048
11		DIELECTRIC	0.2032
12	3V3	PLANE	0.03048
13		DIELECTRIC	0.2032
14	GND2	PLANE	0.03048
15		DIELECTRIC	0.2032
16	BOTTOM	CONDUCTOR	0.03048
17		SURFACE	

Summary

- Initial version of new/interim clock module ready for production
- Open for modifications/improvements
- To be finalised very soon
- Input required **now**
- Some firmware required
- Online-software ?
- To be ready for 2012 beam test