GDCC

Gigabit Data Concentrator Card

The Concept

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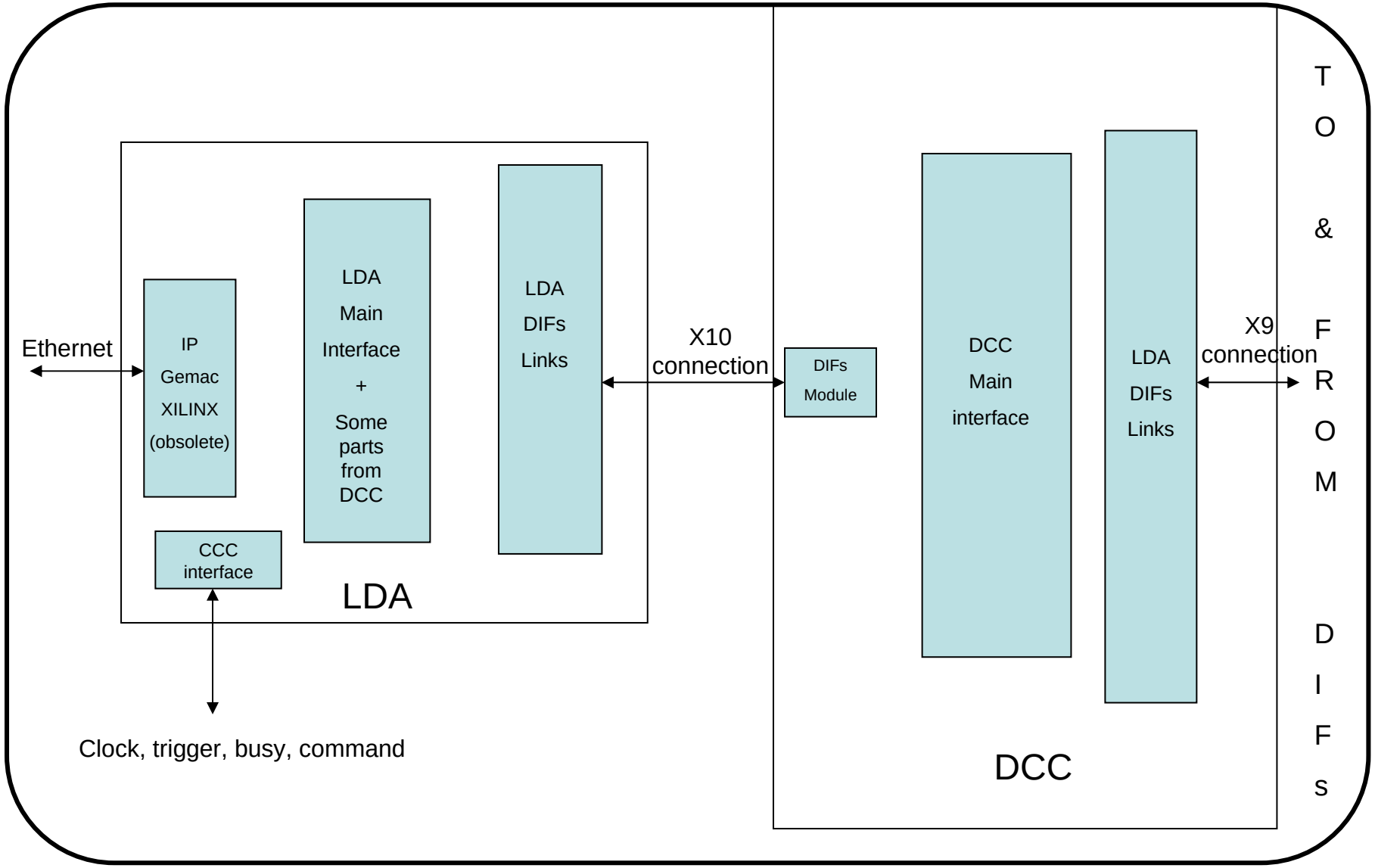
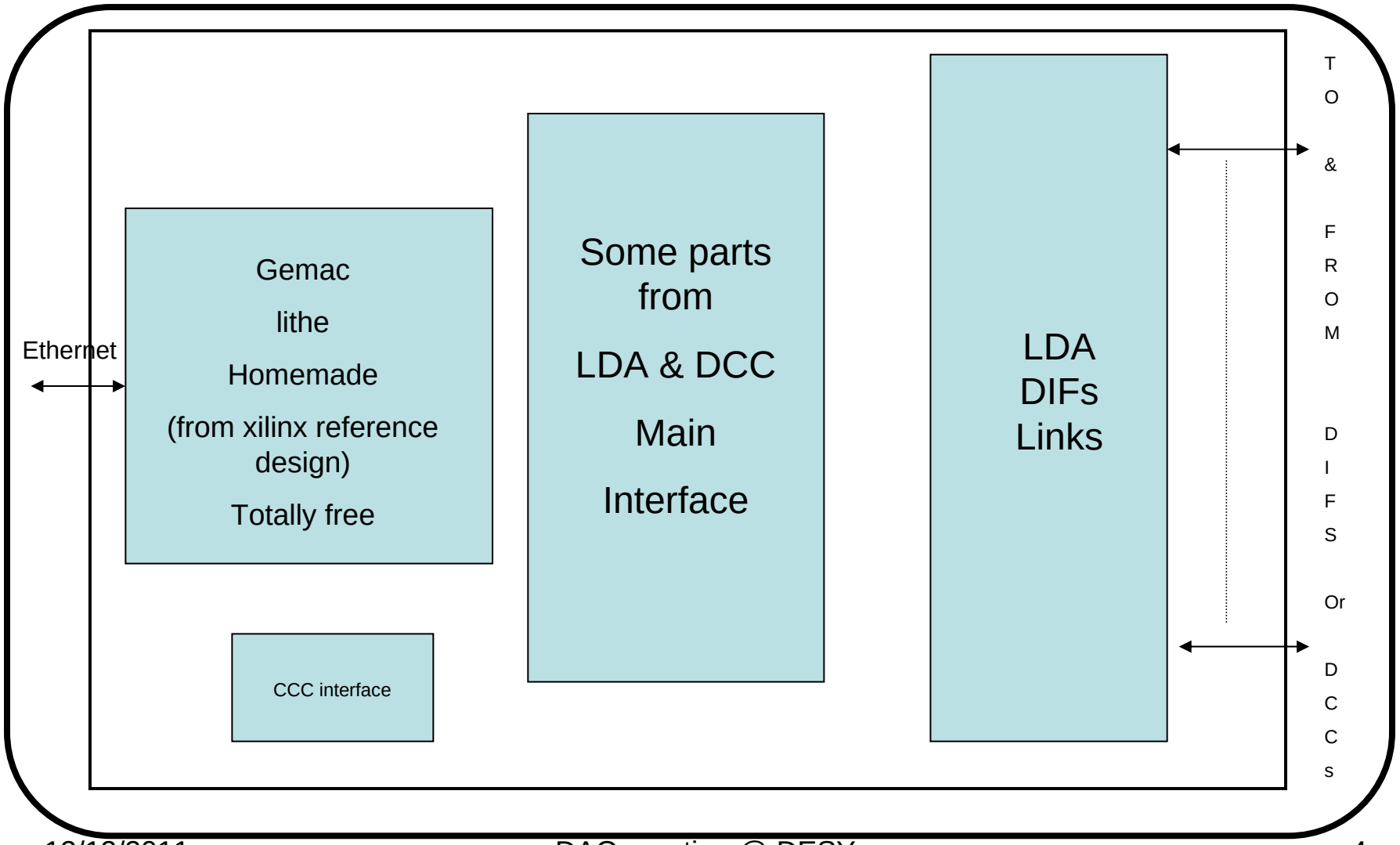
LDA - DCC overview



GDCC project

- Why?
  - Improve the LDA
    - The LDA is a good prototype card but…
      - Not enough reliable & rugged for our experience environment
        - » Grounding & shielding
        - » Strength of connections
    - Complex maintenance for the firmware
      - GEMAC Xilinx IP core obsolete
      - We are not owner of this license
      - Must be use with XILINX software ISE11
        - » Nota : the currently version is ISE13
- How ?
  - Firmware
    - Reusing some blocs from LDA and DCC
    - Replace the GEMAC IP by a free module with the same behavior
    - Make several simulations to ensure a correct behavior compared with the current DAQ
  - Card
    - In first step:
      - Using an evaluation card (located in the LLR) to validate the concept associated with a HDMI mezzanine card (also located in the lab)
      - Evaluation of gigabit Ethernet transceiver chip : Marvell 88E1111
    - In second step :
      - fabricate a card with VME standard format and reliable the HDMI connection.
- And don’t forget the grounding and shielding…
- *For the future…*
  - *A little early but think at the integration in ILC: connection, card size, maybe new communication protocol,…*

GDCC overview (draft)



Firmware

- Reuse some VHDL module from LDA and DCC
- Improve the functionalities that weren't perfect during the DHCAL test beam
- Add new functionalities *that have been forget or not thought*…
- Simulations and tests on Xilinx evaluation board (SP601)

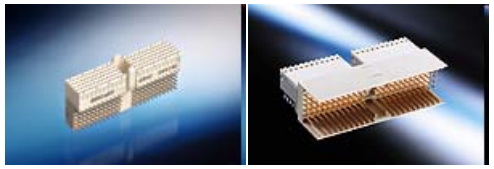
Firmware code would not be the main problem.

Above all, we must follow the rules to implement the correct firmware in the new generation of FPGA.

In our case, XILINX series 6 or next series 7 and the new XILINX tools Planahead, ISE replacement

Board concept

- Here is our first brainstorming
  - Format : VME 6U (chassis with only J1 connector)
  - Main component : Spartan or Virtex 6
    - Configuration in stand-alone and in remote
  - USB access for slow-control or debug
  - Ethernet access via special component (Marvell 88E111), copper or fiber
  - Reliability of mezzanine connector for user board
    - CALICE : HDMI board
      - Samtec or Erni connector



Interconnection with other boards

- DIF board :
  - we keep the HDMI connections

- CCC board :
  - In first approach, we need to kept the same kind of signals than currently DAQ (DHCAL)

    5 LVDS signals

    - Clock : 50 Mhz
    - trigger
    - busy (ram-full)
    - command

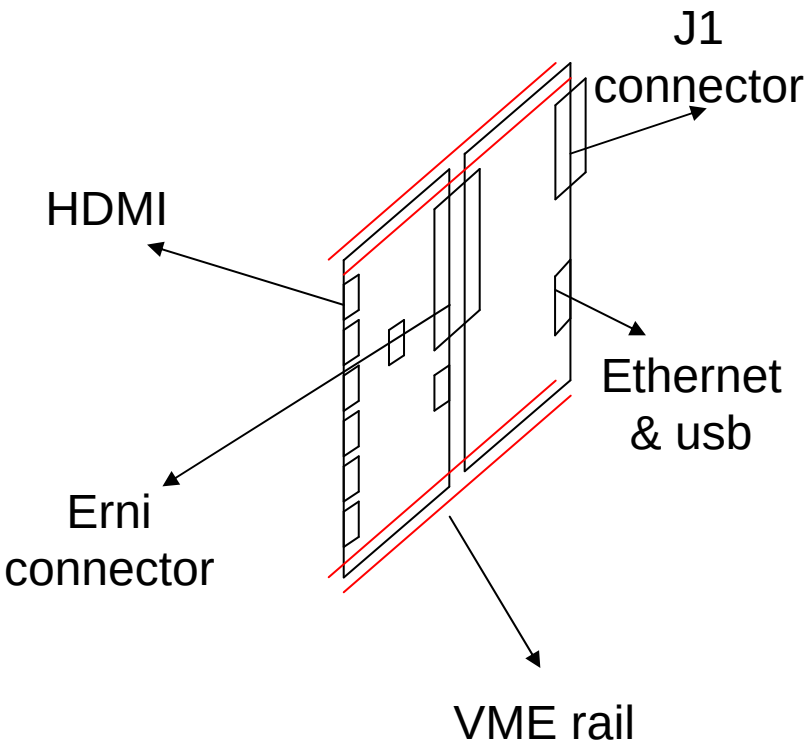
    For that, we will let a HDMI connector for the UK CCC.

    But …

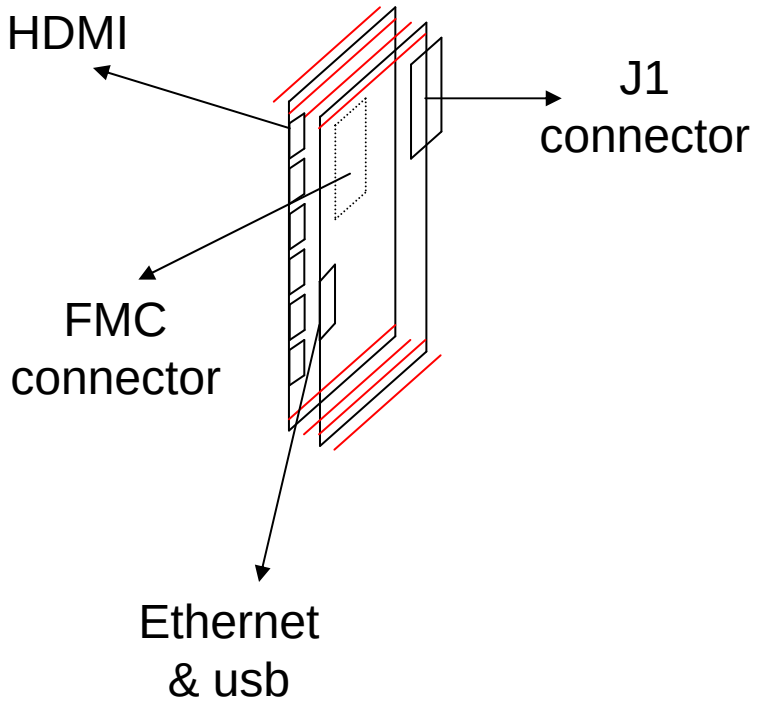
    We will go to preserve a place to implement a connection than we can define with Mainz team and also the signals to exchange.

Board integration

Board to board solution



Mezzanine solution



FPGA choice (to be define)

FPGA	SPARTAN 6 (XC6SLX75) Package : FG676 Speed grade : 2	VIRTEX 6 (XC6VLX75T) Package : FF484 Speed grade : 1	VIRTEX 6 (XC6VLX75T) Package : FF484 Speed grade : 2	VIRTEX 6 (XC6VLX75T) Package : FF784 Speed grade : 1
Logic cells	74637	74496	74496	74496
Block RAM(Kb)	3096	5616	5616	5616
I/O pins	408	240	240	360
MGT (transceiver)	NA	12	12	12
Ethernet MACs (hard IP)	NA	4	4	4
Cost	102 $	531$	660 $	610$

Remark :

Spartan 6 seems to be an optimum choice despite that we have not “hard IP mac” or MGT.

A range of Spartan 6 contains MGT, but Xilinx advises us to pay attention to their utilization. (stress on the pins around the MGT)

The Virtex 6 has many resources, but the initial investment is high for entry level and we can quickly reach the maximum number of pins.

Cost estimation (<5 boards) Prototype part

- With Spartan (per board)
  - Board : 200 €
  - Cabling : 300 €
  - Tools : 3000 € / 5 = 600 €
  - Component : 400 €
  - Total : 1400 €
- With Virtex
  - Total : near 2000 €

Conclusion

To do list until summer 2012

- Continue brainstorming until February and write the first specification document
- Exchange the ideas with Mainz group on the interface with next CCC generation
- Put in place the firmware on evaluation board
- Continue the GDCC schematic and start the board routing
- Consider to send in fabrication a first board at the end of summer 2012