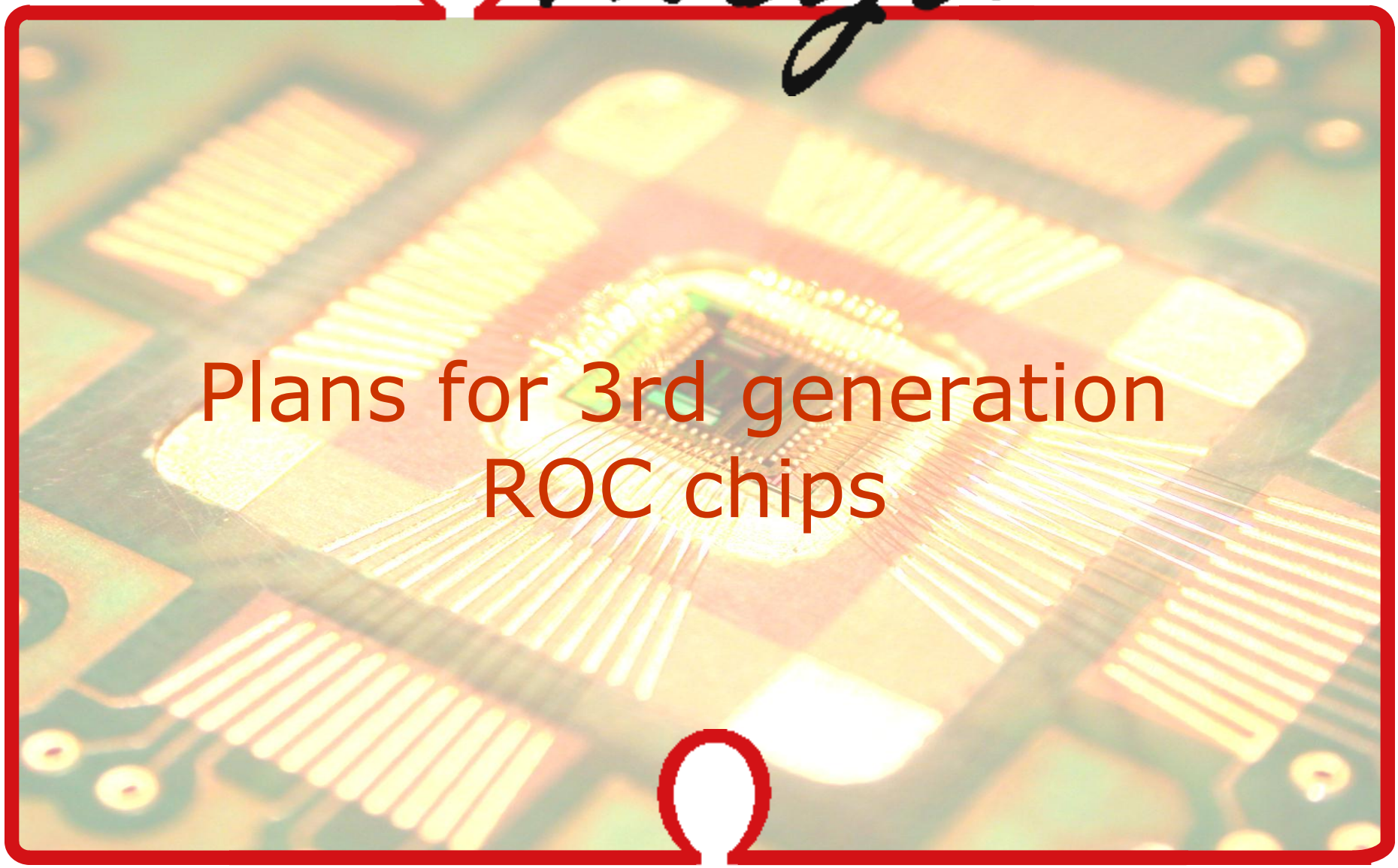


Plans for 3rd generation ROC chips

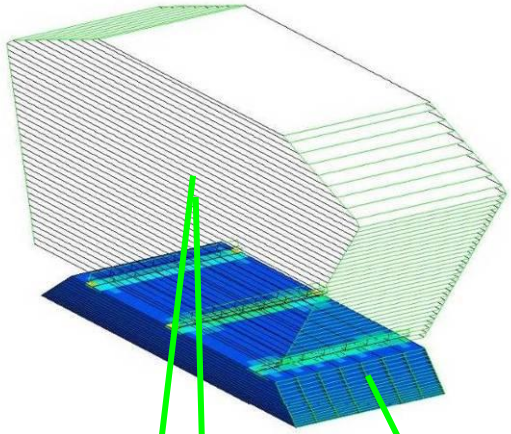
Orsay MicroElectronic Group Associated

AIDA WP9.5: 3rd generation of ROC chips

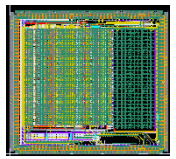
- **1st year (2011)**
  - Caracterisation of the 2nd generation ROC chips
  - Testbench/testbeam mesurements

- **2nd year:** 3rd generation of ROC chips

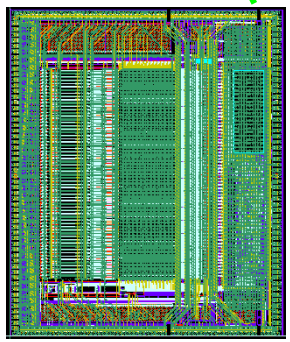
  Main modifications:
  - **Digital part much more complicated:**
    - New Slow Control with I2C link (while keeping the « old SC » system)
    - Independent channels (= Zero suppress)
      - 64 address pointers
      - ReadOut, BCID, SCA (Spiroc and Skiroc) management etc
    - Circular memory
  - **Analog part**
    - NMOS preamp for SPIROC3 (rate dependency)
    - New TDC (“à la Parisroc ”) to avoid dead time:
      - For SPIROC3 and also for SKIROC3
    - SCA : depth=8 instead of 16



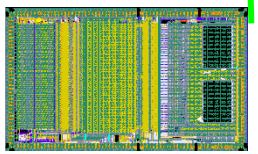
HARDROC2
SDHCAL RPC
64 ch 20 mm²



SKIROC2
ECAL Si
64 ch. 70 mm²



SPIROC2
AHCAL SiPM
36 ch 32 mm²

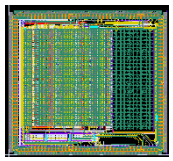


AIDA WP9.5: MILESTONES and SCHEDULE

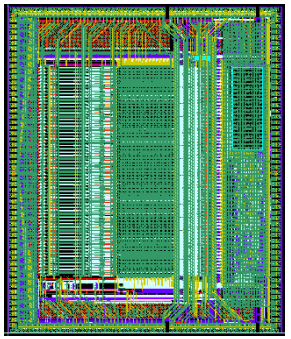
- Milestones: Report in **August 2013**

- **Schedule presented at the AIDA Kick Off meeting**
  - 1st chip
    - Submission March 2012
    - Reception June 2012
    - 1 year for tests and report
  - 2nd chip
    - Submission March 2013
    - Reception June 2013
    - 1 year for tests

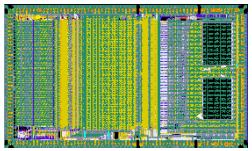
HARDROC2
SDHCAL RPC
64 ch 20 mm^2



SKIROC2
ECAL Si
64 ch. 70 mm^2



SPIROC2
AHCAL SiPM
36 ch 32 mm^2



- Budget for 3rd generation of electronics:
  - 78 k€ (equipment) => 2 chip submissions (Hardroc3 and Spiroc3)
  - 30 ppm

- Cost:
  - Multi Project runs (MPW): 1k€/mm2
  - Packaging: $3500
  - Testboard: 1500 €

OMEGA SUBMISSIONS PROPOSAL

- **1st submission (March 2012): SPIROC2C**
  - NMOS Voltage preamp (see Bbroc measurements)
  - SC: old one (No I2C)
  - Pin to pin compatible with spiroc2b so noise measurements can be performed « easily » at the system level (HBU)
  - Die size: 32 mm2 => MPW run 32 k€ (CALICE funding)

- **2nd submission (June 2012): HARDROC3**
  - « Simple » chip compared to Spiroc3: I2C, independent channels, circular memory, 1 RAM/channel, new Band gap, temperature sensor (Vbe), probe register
  - No major modifications in the analog part
  - HR3 not pin to pin compatible with HR2 and probably in a different package: TQFP208 instead of TQFP 160 (same size and thickness)

  ⇒ New 1 m2 RPC chamber to be built to test HR3 at the system level
  - Die size should be ~30 mm2 => 30 k€ (AIDA funding)

- **3rd submission (March 2013) SPIROC3: Complex chip**, many parts still to be tested on test bench and at the system level
  - I2C, independent channels but also new PA, TDC , SCA
  - Hardroc3 and Spiroc2c test feedback necessary before submitting Spiroc3
  - Digital part (Fred. Dulucq) : in post layout simulation phase
  - Size should be ~40 mm2 => 40 k€ (AIDA funding)

DETAILED MODIFICATIONS

Digital part: in « post layout simulation » phase (for SPIROC3)

- **Independant channels +I2C interface**
  - 8 bits serial interface but parallel distribution inside the chip
  - 500 to 1000 SC parameters/chip
  - Keep old SC => internal Serializer=> 1000 to 2000 wires inside the chip
  - Interface already designed and tested by IPNL (Yannick), but about 1 month needed to redo the layout accordingly to the SC distribution of SPIROC3
- **RAM**: a new one to be bought?
- **POD:** minor modifications: Independant channels => 2 clk tics instead of one

Analog part

- **Bandgap:** layout to be redone
- **Delay box:** modifications of the existing one
- **SC with triple voting** => new SC cell (already designed and tested in SPACIROC)
- **SCA:** depth of 8 instead of 16, same design but layout to be redone. SC parameters to power ON/OFF one widlar at once instead of 8 (=> save power).
- **TDC:** 2 ramps, 2 capacitors « à la Parisroc2 ».
- **Latch/ Hysteresis discri auto gain** to be added on Spiroc3
- **Temperature sensor:** measurement of the Vbe of a transistor (probe register)
- **« 0 events »:**
  - SKIROC2: none seen so far
  - SPIROC2b: first 0 events understood, random 0 : need of more latency before conversion