# τDAQ Days summary

Vincent Boudry
*École polytechnique*

***eDAQ near AHCAL meeting***
***12/12/2011***

# Milestones & needs

- SDHCAL Test Beam in **June/July 2011**
  - Missed ➔ back to USB version of the readout
- DHCAL Test Beam **October 2011**
  - 2 weeks of commissioning at PS mid-september
  - 10 days at SPS
- ECAL tabletop test **summer 2011** ✔

---

- ASAP: ECAL table & cosmics test bench
- SInce end nov. SDHCAL ➔ IPNL
- December: AHCAL table test bench
- end feb. AIDA annual meet. in DESY

## 2012+

- ≥Mai 2012:
  - SDHCAL test beam
  - ECAL test beam (1–3 slabs @ DESY ?)
  - µMegas test beam (2-3 m²)
  - τAHCAL (1+ ASU)
- Fall 2012: SHDCAL TB ?
- 31/09/2012:
  «common DAQ» AIDA specification document (= DAQ2 ⊕ EUDAQ)
- end 2012:
  DBD ILD ➔ small section on DAQ for ILD. (Power pulsing, concentration & redundancy schemes)
- 2013–2014: Combined TB ECAL + SDHCAL
  Combined CALO + Trackers ?

# DAQ Days

- Some technical choices made in emergency
  (BUSY signal passing, sequencing of readout & reset, handling of noise, grounding, SW infrastructure…)
  - The DAQ2 is also a technological prototype
    - lack of flexibility in implementation
- ➔ Review choices & possible improvement, manpower.
  *November 2011*
    - **Internal** (for developers) : friday 04/11
      - Brainstorming & review of critical tasks
    - **CALICE wide**: thursday 09/11 (+ ¾ day with AIDA groups)
      - New forces (Mainz) ➔ CCC & rethinking
      - Re-use of ODR card (RHUL part of AIDA)
      - Rethink the DAQ for the next year
        - version 2.5 (LDA free)
        - vs version 3 (better protocols, links, new CCC)

# Meetings

- **internal** (for developers) : ½ day in IPNL friday, 4th
  - 13 participants, mainly experts + C. Adloff, I. Laktineh, VB
  - Brainstorming & review of critical tasks
  - Review of encountered problems during SDHCAL TB & area of improvement
    - LDA reliability
    - HW configuration
    - Diagnosis tools
    - Stability & recovery procedure
    - Configuration management
    - Performances
    - Usability
    - (organisation)
  - Backup solution
    - USB readout until the LDA has been replaced for large setup
  - Discussions on «GigaDCC» (LDA replacement)

**Many fruitful discussions (some others not so)**

**Main conclusion:**
**LDA ~OK for small setup**
**Should be replaced for large ones**

# CALICE & AIDA

- **CALICE** : ¾ day @ LLR wednesday 9th
  http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=5404
  - 15 participants (LAPP, LLR, IPNL (rem.), LAL, DESY, RHUL & Mainz)
  - New forces (Mainz) ➔ CCC & rethinking
    - Uli Schaefer, Rainer Wanke; André Welker
  - Re-use of ODR card (RHUL part of AIDA)
    - Barry Green;
  - Rethink the DAQ for this & next year
    - version 2.5 (LDA free) ➔ USB backup.
    - vs version 3 (better protocols, links, new CCC) ➔ unified card ?

**Many fruitful discussions**
**Quite some evolutions**
**➔ new questions**
**First step**

- **AIDA** (WP8.6.2): ½ day @ LLR on thursday 10th
  https://indico.cern.ch/conferenceDisplay.py?confId=161997
  - 15 participants
    (LAPP, LLR, LAL, Mainz, RHUL , Bristol, Brussels, Lund (rem.), Geneva (rem.) )
  - Integration of CALICE & EUDET ➔ common DAQ, devt for trackers

# CALICE specific

- Check reviews by R.C. & V.B. on wednesday.
  - SDHCAL commitment: integration on UK devt + DCC
  - Big effort to finish the UK group work
    - delay in ECAL
  - Reminder that LLR work on DAQ is not a commitment but DAQ should be a collaboration within CALICE
- DAQ2 is a also a technological prototype
  - Designed as prototype for ILD (pulsed electronics & physics, trigger-less, “noiseless”, distributed concentrator cards, ...).
  - Mitigated success: 300k ch readout albeit with many[2] instabilities

# CALICE Specific (2)

- There are many remaining bugs and source of instabilities, now rather well identified (1st outcome of SDHCAL TB).
  - my impression: NO SINGLE source: HW, FW, SW, system (always s.o. else fault)
    - Most annoying one: Silent drop of Ethernet packets LDA↔PC
  - Stable enough for small set-up (ECAL, AHCAL) as is.
- Next step: consolidation
  - Protocols, FW, SW, versioning, coordination
  - Use of ODR ? (lack of expertise & time)
    - Barry Green available (in AIDA) for mod: waits for requests. **Manpower ?**
  - Most critical points:
    - manpower on CCC & DIF FW [G.Vouters, now fixed position]
    - low lvl SW: now entirely in LLR hands.
    - large test to be scheduled well in advance.
  - Precise list of task being established

# CALICE specific (3)

- Development of backup solution for SDHCAL
  - Config & readout by USB
    - “slight mod. of DIF FW” [G.V.]
  - fast signals (Clock, trigger, BUSY) by CCC+DCC
    - “slight mod. of DCC FW” [G.V. & C. Combaret].
  - will divert some man-power but «most reasonable»
- GigaDCC vs a G/CCC (Generic Calice Card / Common Card for CALICE ?)
  - CCC2 in Mainz
    - current version is very limited ➔ simplistic reset & readout sequencing ➔ instabilities
      - RHUL proposes to upgrade some of the CCC's with a double sized CPLD.
    - Needed for AIDA (external sync.)
  - Improved DCC base + FMC mezzanine ➔ GigaDCC / CCC
    - To be refined ➔ December meeting ?
    - Planning not compatible with large TB in spring ← !!!!

# AIDA

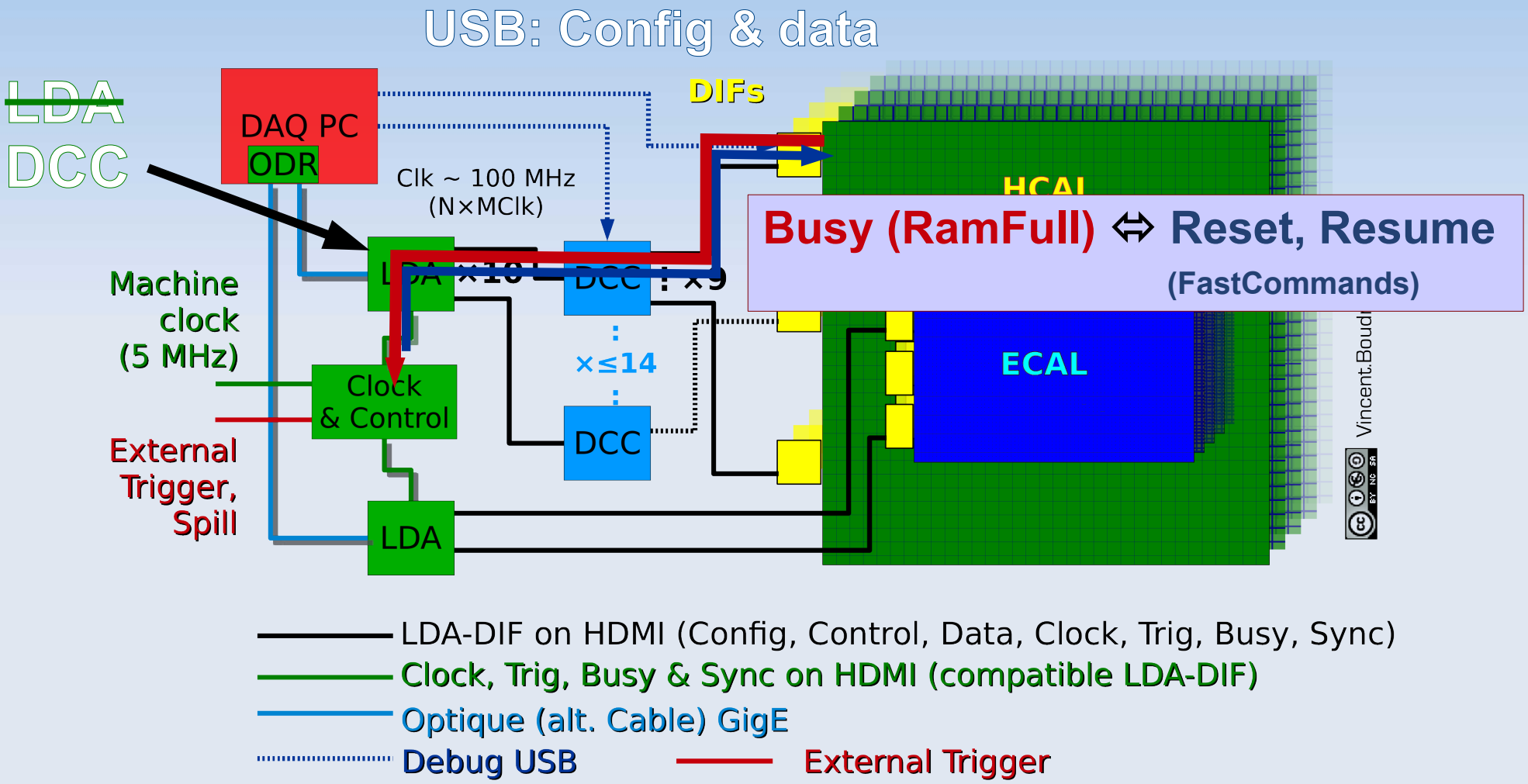
- FP7 EU funding
- Common DAQ for all ILC R&D common TB (2013-14)
- SW: personal being replaced (Geneva) or to be hired (LLR)
  - comm. EUDAQ ↔ XDAQ (Geneva ⊕ LLR)
- HW: Bristol (D. Cussans), LAPP, Mainz
  - comm. CCC2 ↔ TLU2
  - Well started;
    some direction decided at this meeting (clock, sync, …)
  - TLU2 precise implementation requires further though.
- BIF might be a mezzanine on TLU2
  - To be made in LAPP (part of task list)
  - Collaboration with D. Cussans (Bristol)

# Conclusions

- 3 days of WS with intensive & constructive discussions
- Much clearer situation after review
  - Some shift in work priority / responsibility
- Looooooong³ list of to do
  - Being structured...
  - Planning of GDCC (Giga/Generalized DCC ?)
    - how to keep the better use of scarce manpower ?
    - Partly to be discussed today
- Planning & resources to be better estimated

# News from USB readout for SDHCAL

# USB readout for SDHCAL




ODR = Off Detector Receiver
LDA = Link Data Agregator

DCC = Data Concentrator Card
DIF = Detetcor InterFace

CCC = Clock & Control Card

# USB readout for SDHCAL

- Modifications required
  - DCC FW: Almost nothing... (removing of code)
  - DIF FW:
    - ≠ encoding of FC
    - Modif. of legacy USB FW (was OK for M2 RPC & µMEGAS TB)
- SDHCAL $m^3$ ➔ Lyon end november
  - with all Electronics & set-up
- DCC & DIF FW modified
  - Works on table top (a few DIFs)
  - M3: Grounding needs more effort (➔ USB crashes)
- XDAQ code has been cleaned-up (but kept compatible with prev. solution)