Status of the AHCAL engineering prototype - Summary

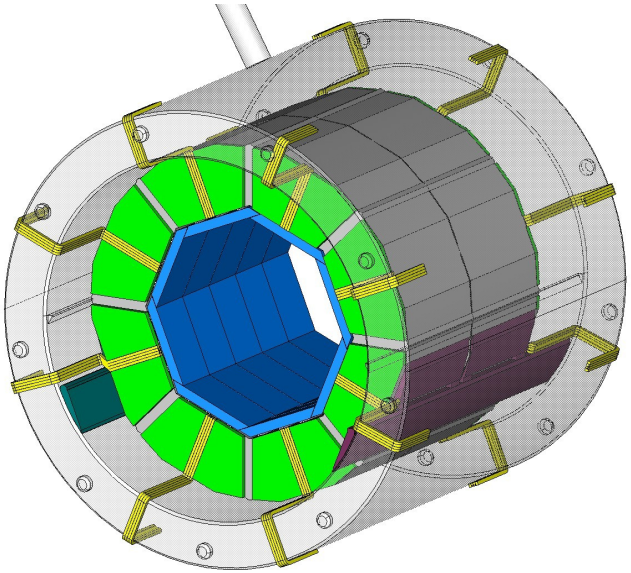
Mark Terwort

HCAL main meeting

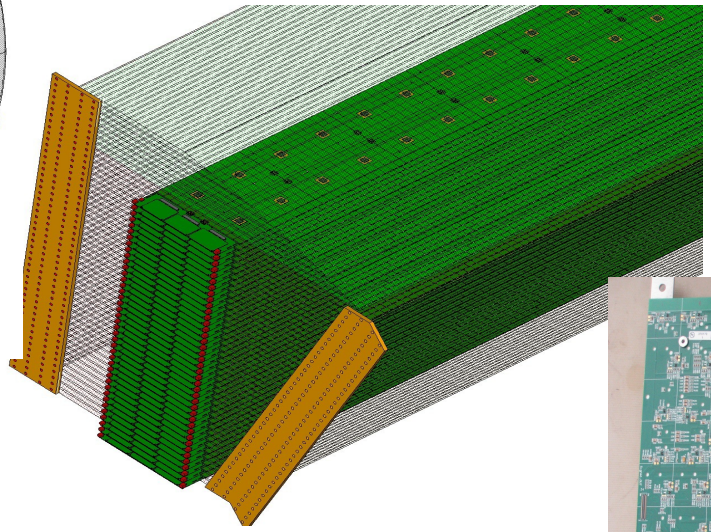
Hamburg, December 13th, 2011

The engineering AHCAL prototype

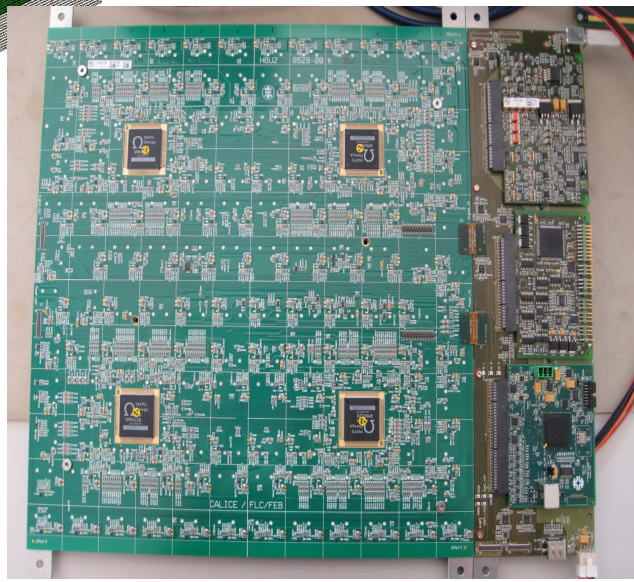
Development of **scalable LC detector** based on successful experience with physics prototype



Octagonal shape, 16 equivalent wedges, segmented in two along z



PCB with 4 ASICs, 144 scintillator tiles, SiPM readout



Challenges:

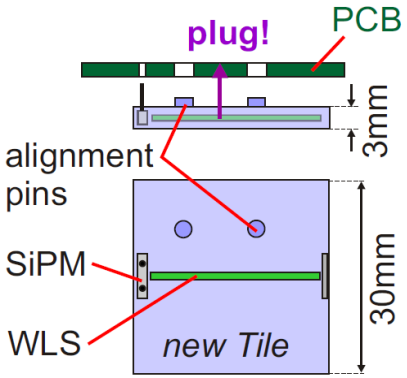
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

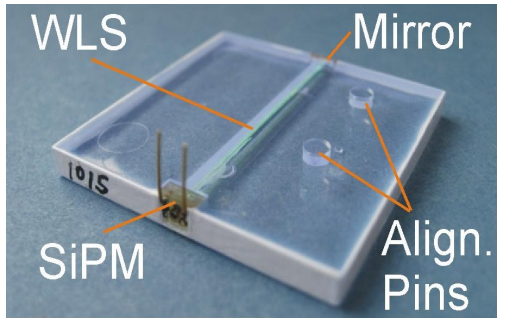
→ Integrated readout electronics

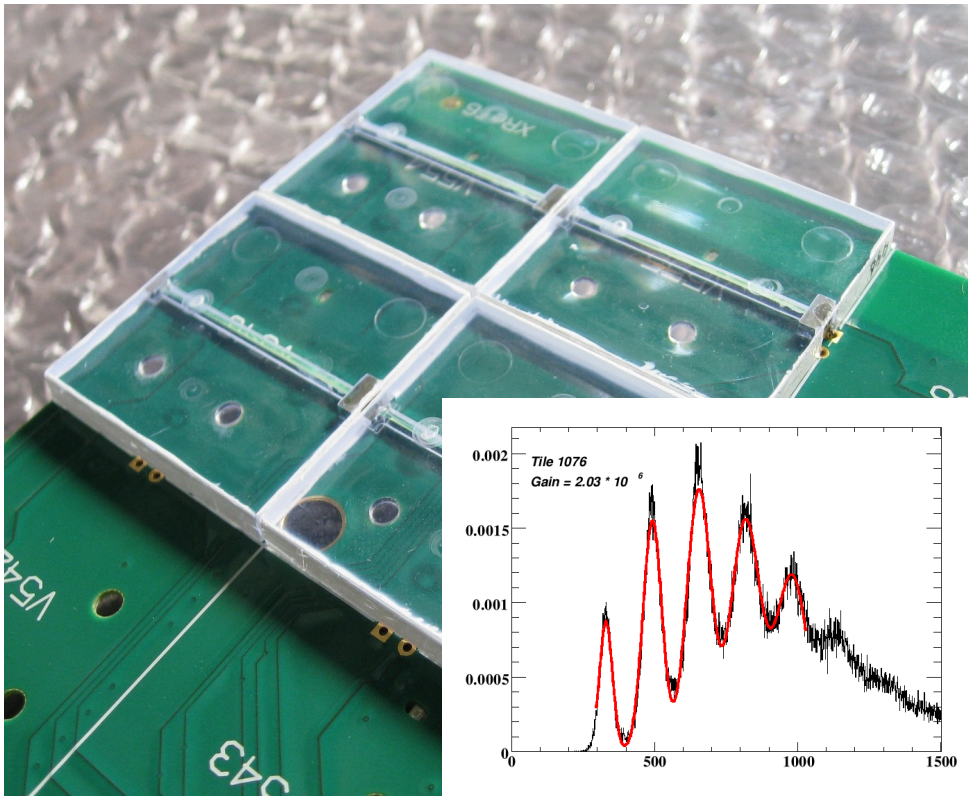
Scintillating tiles

- Signal sampled by scintillating tiles
  → 3x3x0.3cm^3, 2592 tiles per layer
- **450 new tiles** arrived from ITEP
  - Gain of ~270 tested
  → Good results (see Marcos talk)
- Sample of 150 tiles to be shipped to Heidelberg for further tests
- New batch of tiles will be delivered until end of January
  → Equipment of 3 new HBUs

→ Important step to multi-HBU-setup now possible!





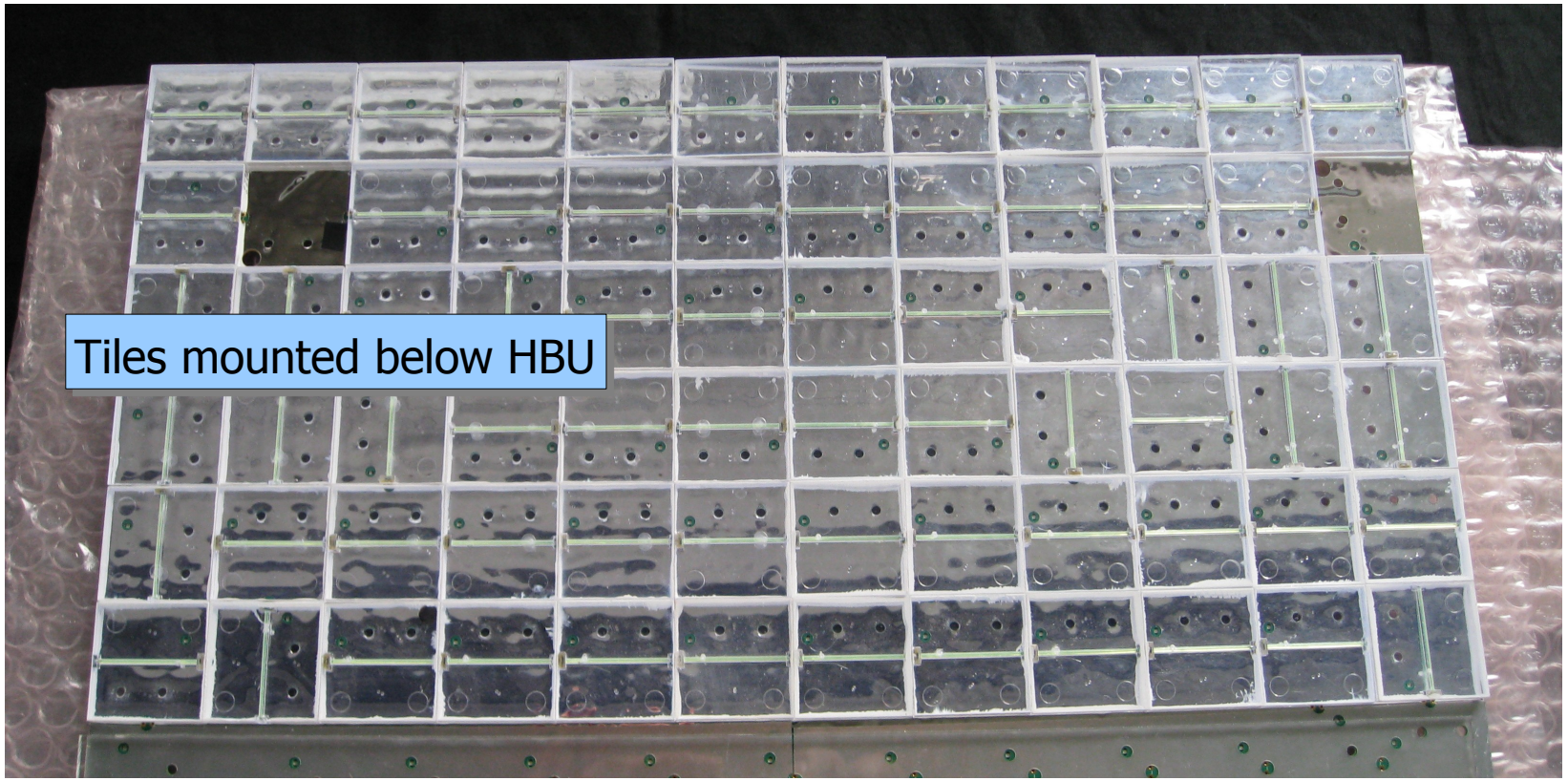


Scintillating tiles

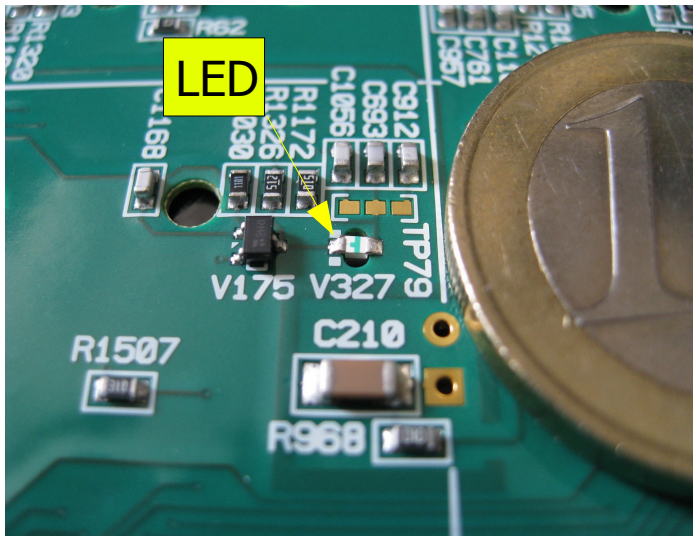
- 70 tiles already mounted below new HBU2

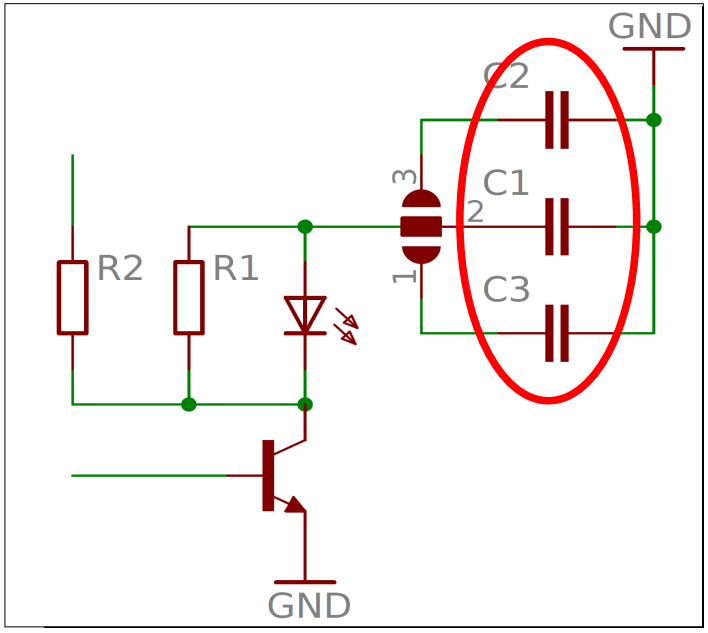
  → Larger tests of calibration system and **SiPM gain in HBU2 environment**

  → Test of **light yield** in DESY test beam



LED calibration system





Wuppertal solution:

- Light directly coupled into tile by 1 integrated LED per channel
- Light output equalization via C1 - C3
- New design implemented in new HBU2 and is currently tested extensively

  (see Julians talk for details)

Prague solution:

- Light coupled into tile by notched fiber
- Mechanical integration difficult

  → First full layer tests planned

  (see Ivos talk for details)

The readout chip - SPIROC2b

Specific chip for SiPM readout:

- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

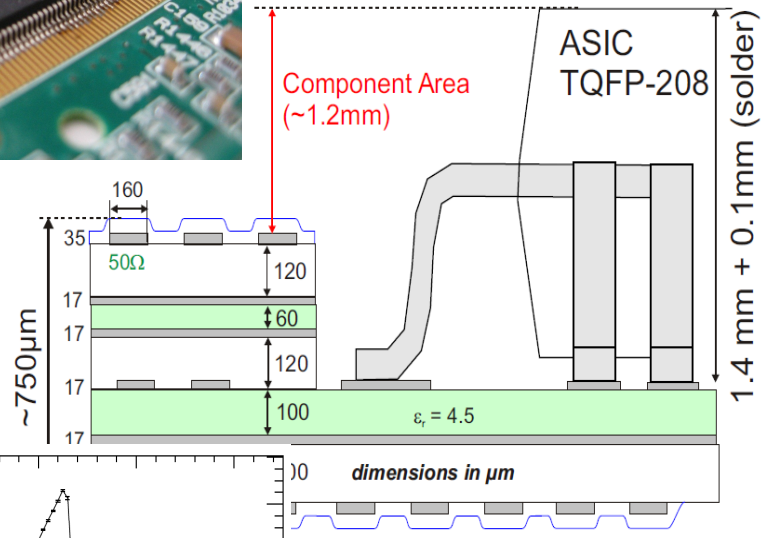
- Power pulsing → 25µW/ch (see Benjamins talk for first results in HBU2 environment)
- Dual-gain setup per channel

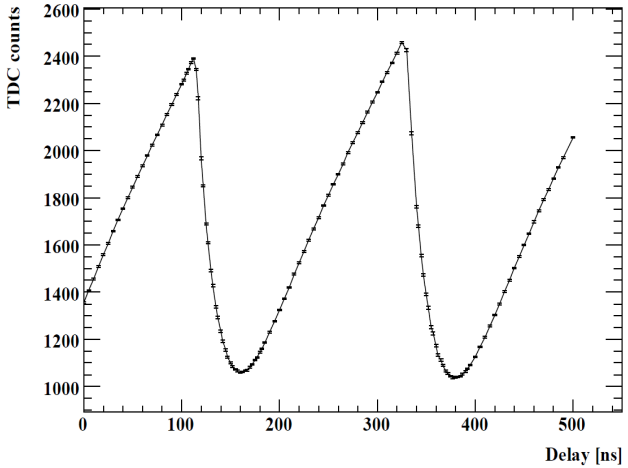
  → high gain/low gain ~ 10

  → 25fF – 1575fF per channel

  (will be used with new tiles in DESY test beam NOW)
- Auto-trigger mode (see Benjamins talk for detailed measurements)
- Time stamp (12-bit TDC) (detailed studies by Oskar)

Designed by OMEGA/IN2P3





Placement of components in PCB cutouts

→ 500µm/layer

→ 50mm in total!

New HCAL Base Unit (HBU2)

- 4 **new HBUs** in DESY lab

  → 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs
- 1 HBU2 connected to DAQ modules for first tests

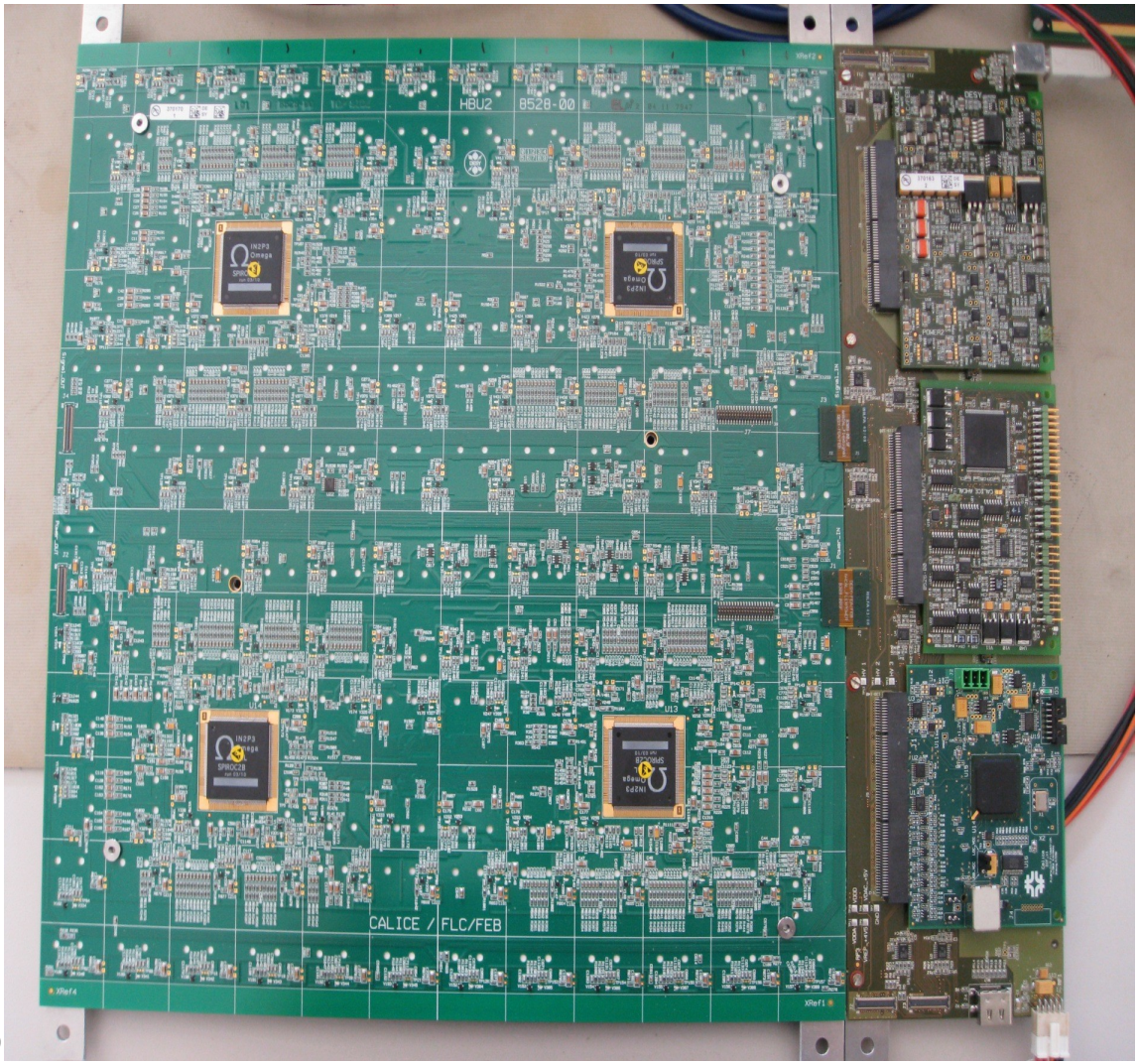
  → so far fully functioning!
- 1 HBU2 in **DESY test beam**
- We ordered 6 new HBU2s for **full slab test**:

  → Quality of electrical signals

  → Mechanics, temperature

  → DAQ

  Build small stack with ~10 layers, 1 HBU each, next year?



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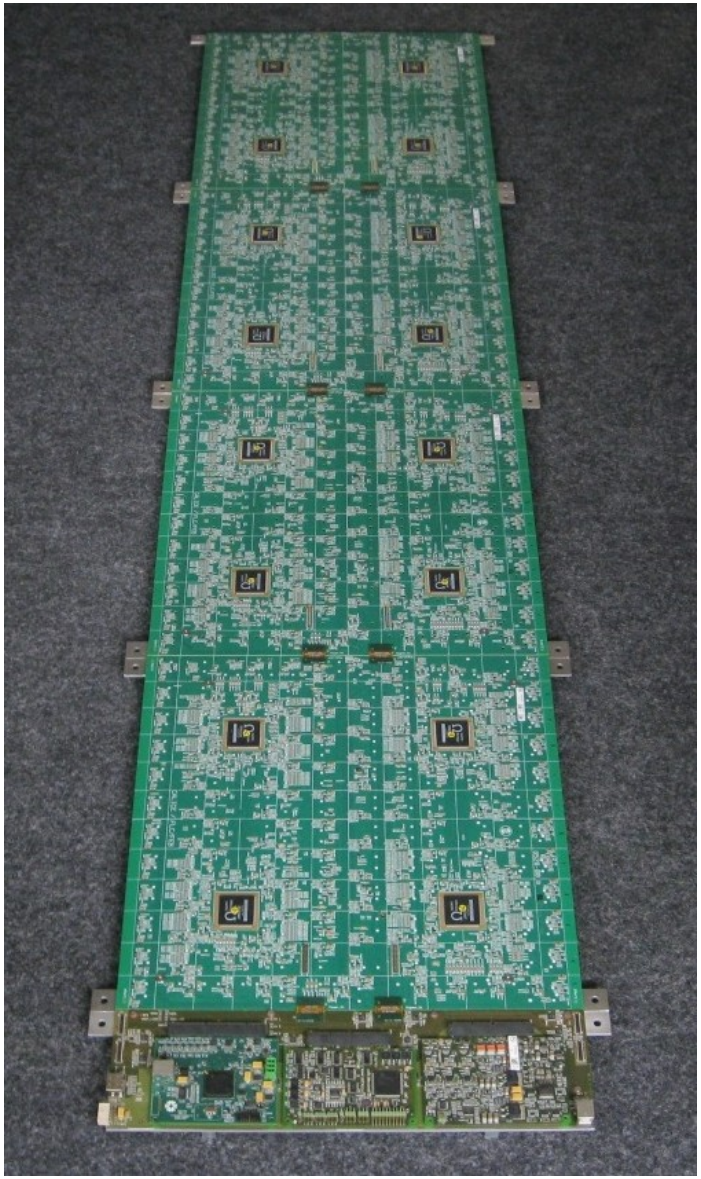

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  → Mechanics, temperature

  → DAQ

Build small stack with ~10 layers, 1 HBU each, next year?

- **Mechanics is in place** since long time

  → Use it to perform temperature tests

  → Use it for small stack

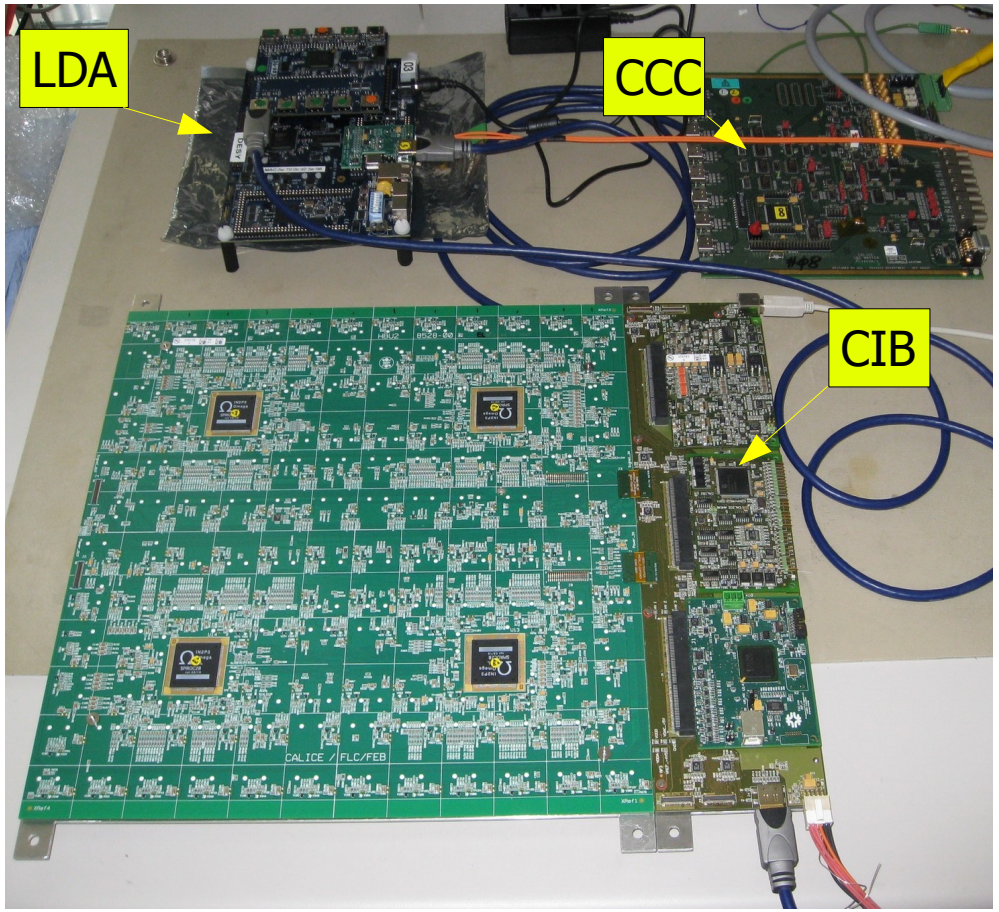
  → Cassettes are being built by Karsten

Data acquisition

- **2 options:**
  - Labview based DAQ for SPIROC2b tests and single HBU2 test beam (finished)
  - DAQ for LDA detector operation

    → Frantisek works on DIF code
- Currently 3 DIFs from NIU

  → More DIFs needed for small stack
- Mainz joined effort of **redesigning CCC** (see Ulis talk)
- For general DAQ and DCC status see Vincents and Remis talks

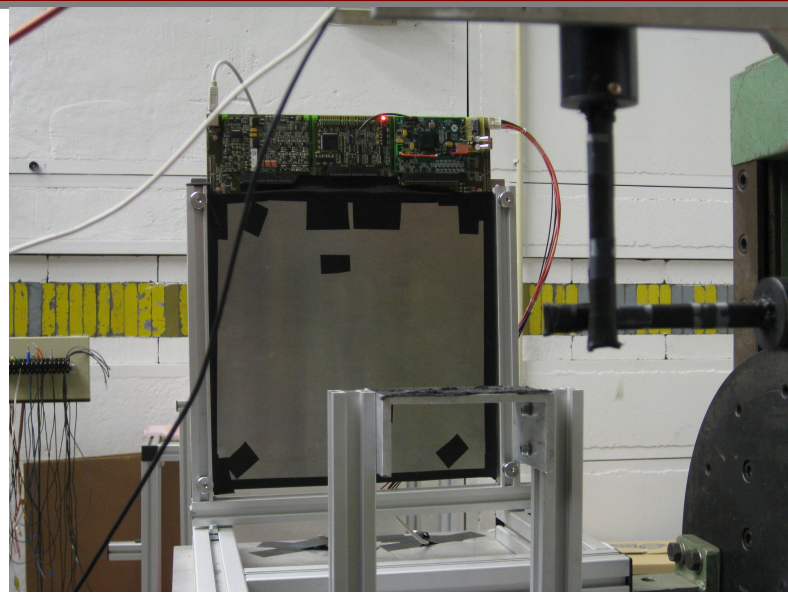


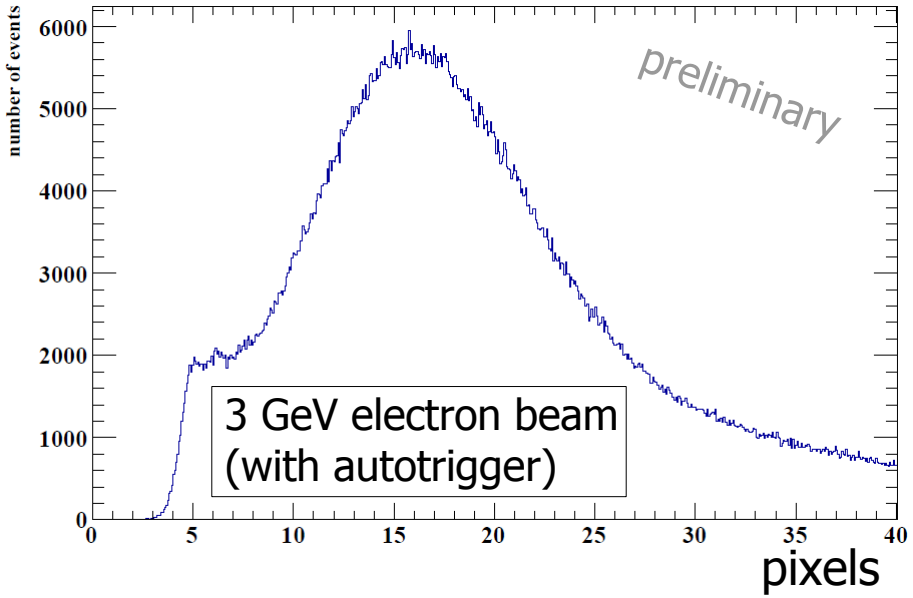
We have the man power now to do the next steps at DESY towards using all DAQ modules

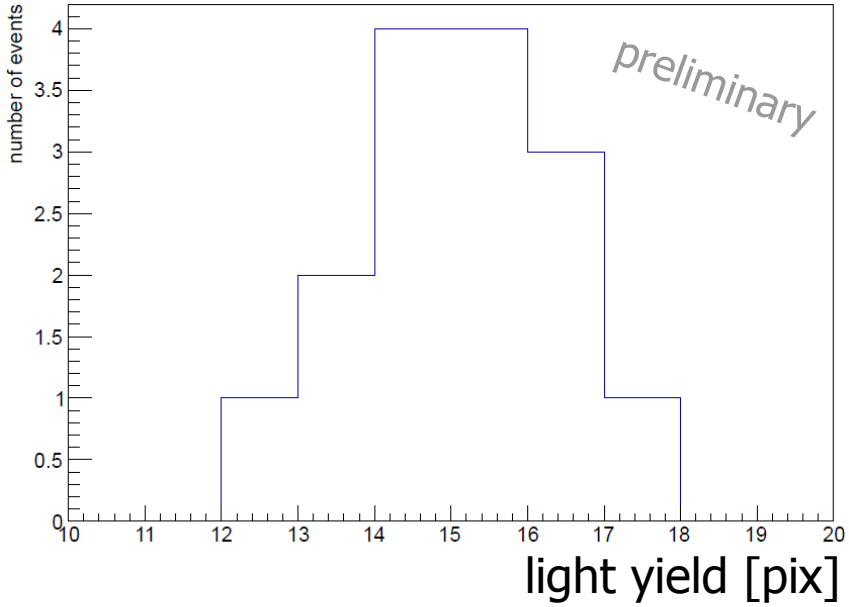
Test beam – First MIP results

- **HBU2 in DESY test beam** since 2 weeks
  - Test functionality in test beam environment
  - Measure MIPs with 3 GeV electron beam

    → **~15 pixels per MIP**
  - Test channel-wise gain and autotrigger adjustment and **optimize MIP efficiency** (see Benjamins talk)







Summary and outlook

Status:

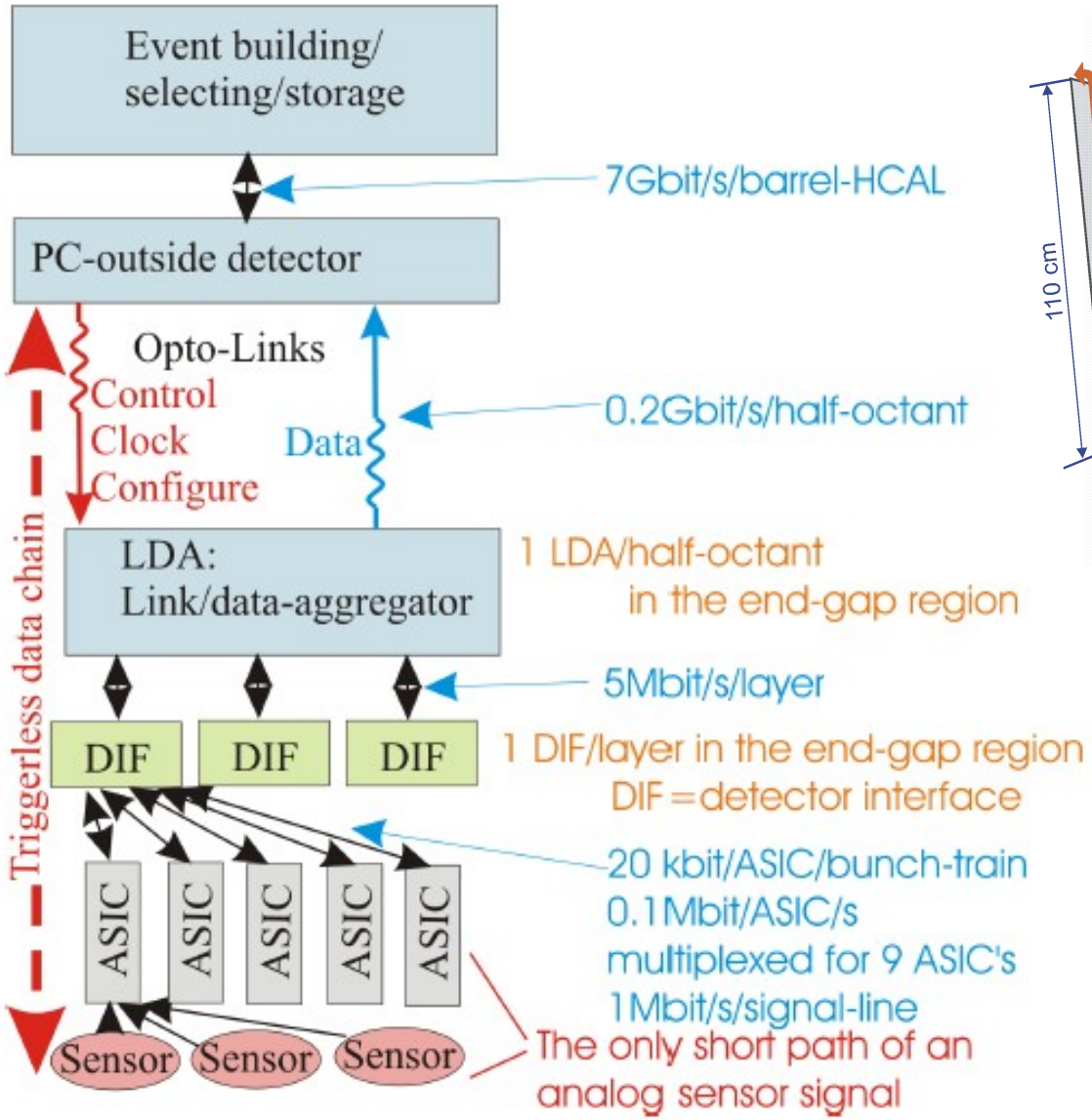
- HBU2 plus SPIROC2b in action and working fine!
- Understanding of SPIROC2b good and ready to be used in multi-channel tests
- First tests of new calibration system promising
- New tiles at DESY, plenty of tests ongoing

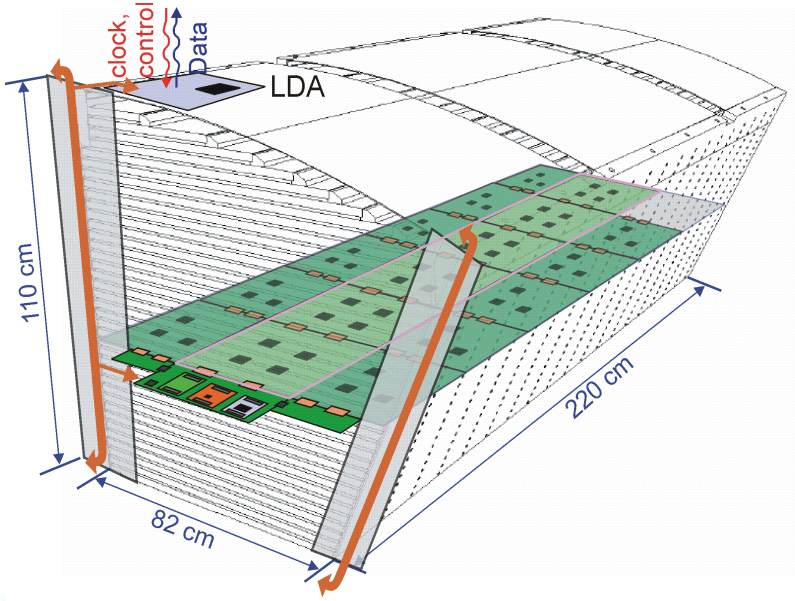
  → Results so far very satisfying!
- HBU2 tested successfully in DESY test beam
- Next step of DAQ development ongoing to
  - use more than 2 chips simultaneously
  - build multi-HBU setups

Plans:

- Full slab tests as soon as more HBUs available
- Maybe small stack (~10 layers) in few months
- Large layers in hadron test beam in fall

Data acquisition

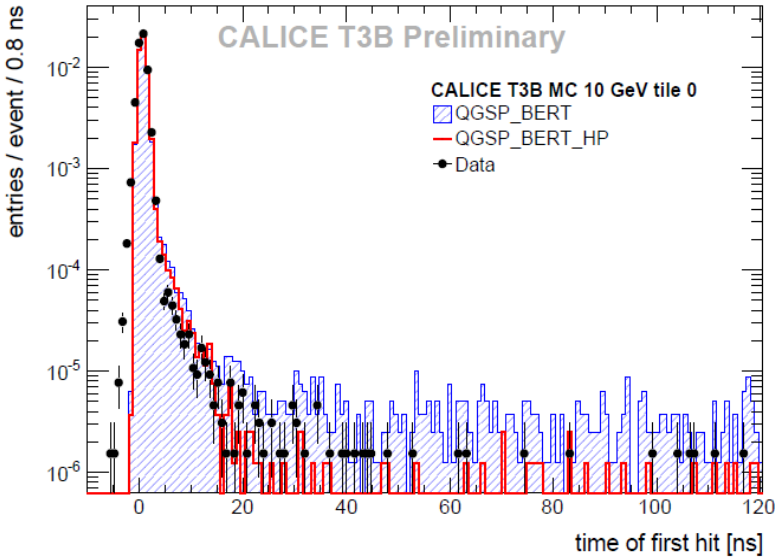


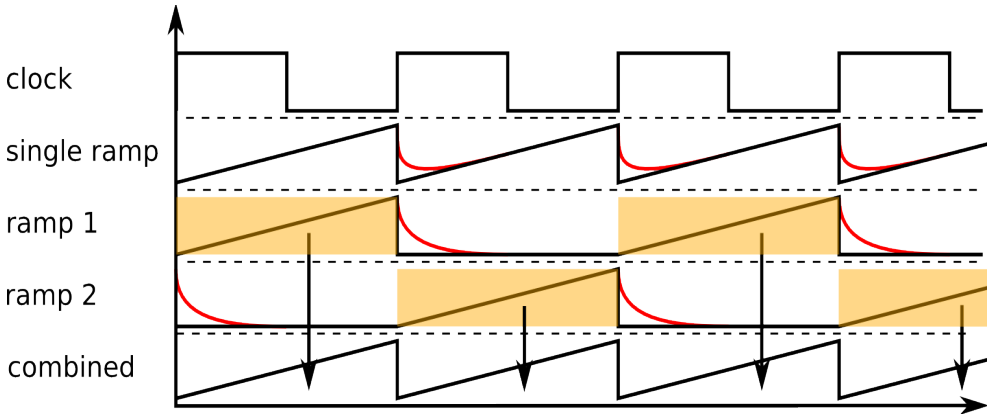


- Moderate data rates using channel-wise self-triggering

  → No need for further front-end event selection

SPIROC2b – Time measurements





- T3B measured radial development of shower in time in one row of last layer

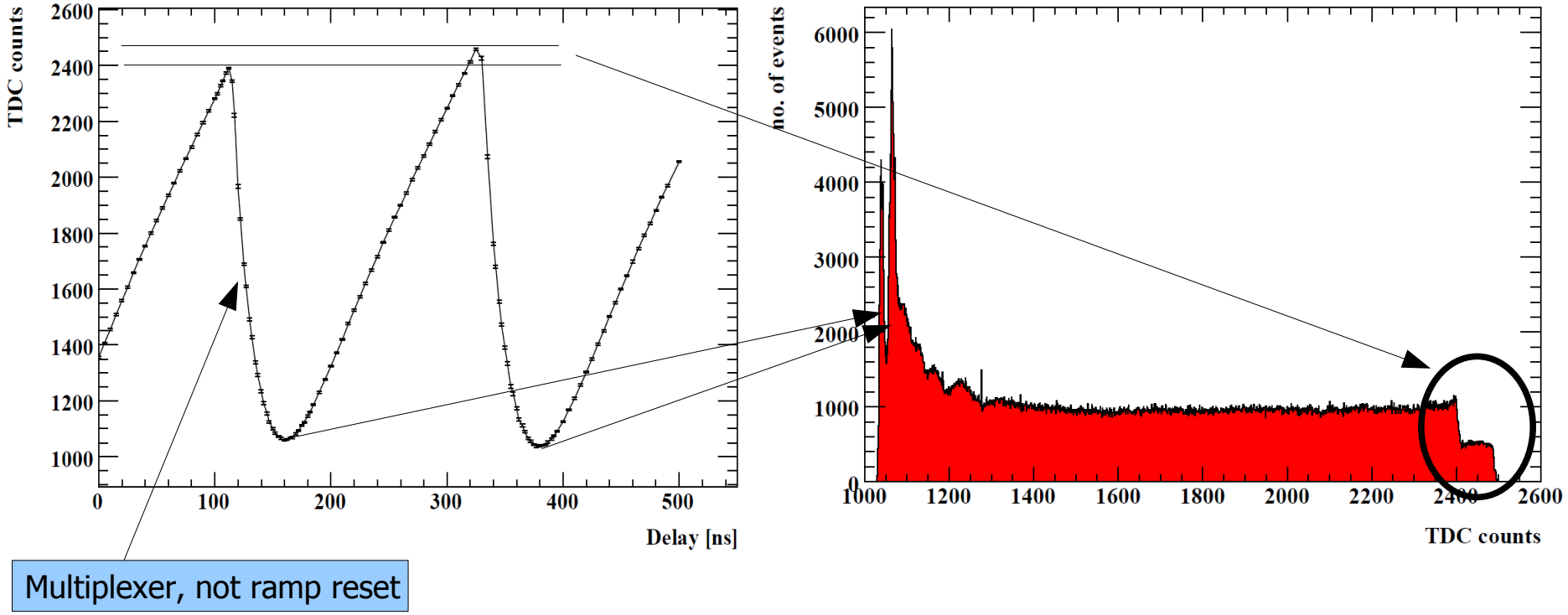
  → Repeat measurement with full layer or even multiple layers
- SPIROC2b measures time in auto-trigger mode relative to bunch clock

  → 2 ramps to reduce deadtime due to ramp reset

  → ILC mode = 200ns ramp, testbeam mode = 5µs ramp (less dead time)

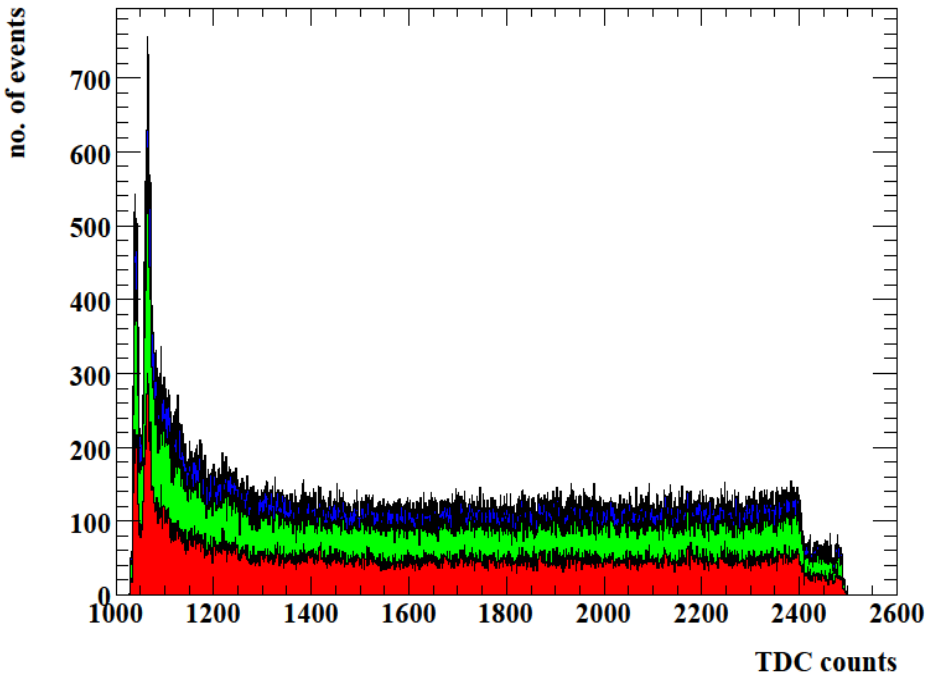
  → Investigate time resolution to optimize ramp slopes (and lengths)

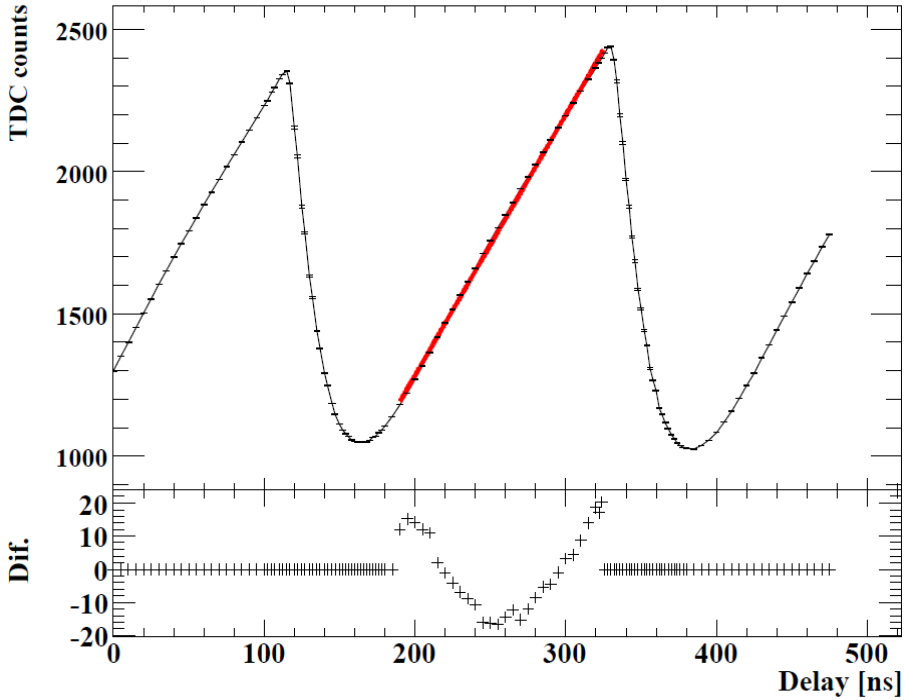
SPIROC2b – TDC (ILC mode)



- First tests of TDC ramps in SPIROC2b show promising results
- Resolution in ILC mode: ~250-350ps (dominated by linearity)
- The 2 ramps have different slopes/heights in ILC mode
- A few aspects will change in SPIROC3, but we have to use SPIROC2b!

SPIROC2b – TDC (ILC mode)





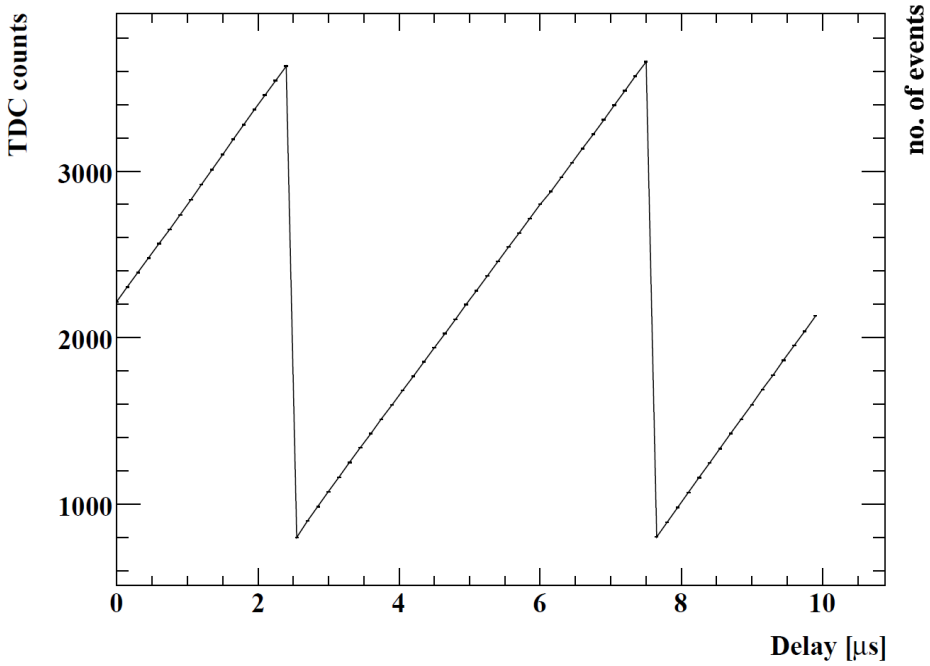
- No correlations visible between ADC and TDC measurements
- Resolution in ILC mode limited by linearity (~1ns)

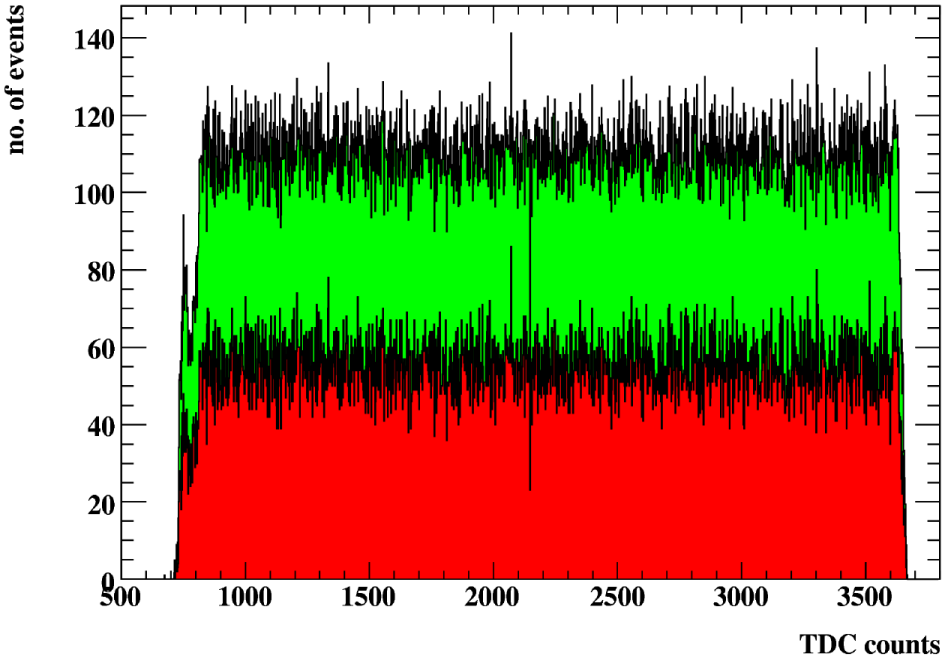
  → Linear fit reveals clear structure

  → Fit of 2 linear functions improves resolution (~300ps)

  → What is the most reasonable measurement/fit strategy?

SPIROC2b – TDC (testbeam mode)

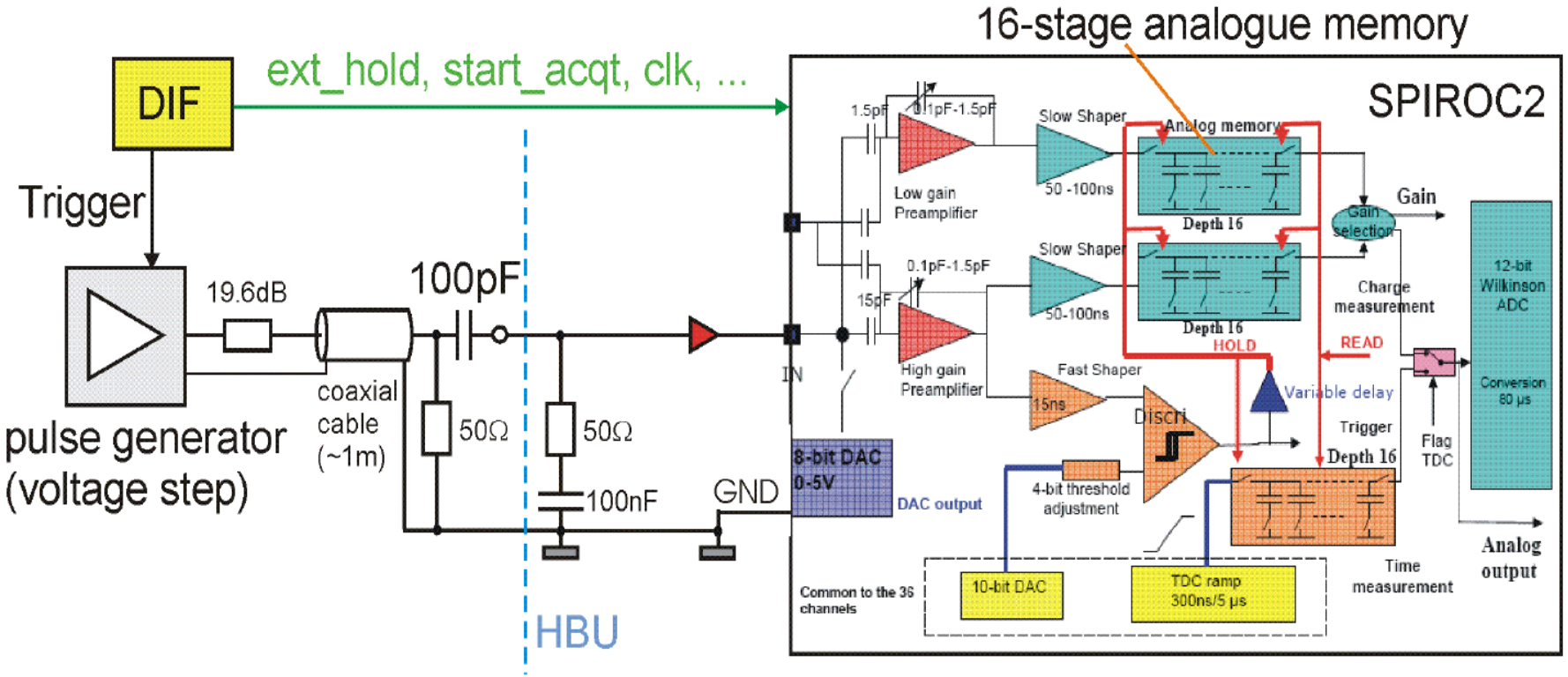




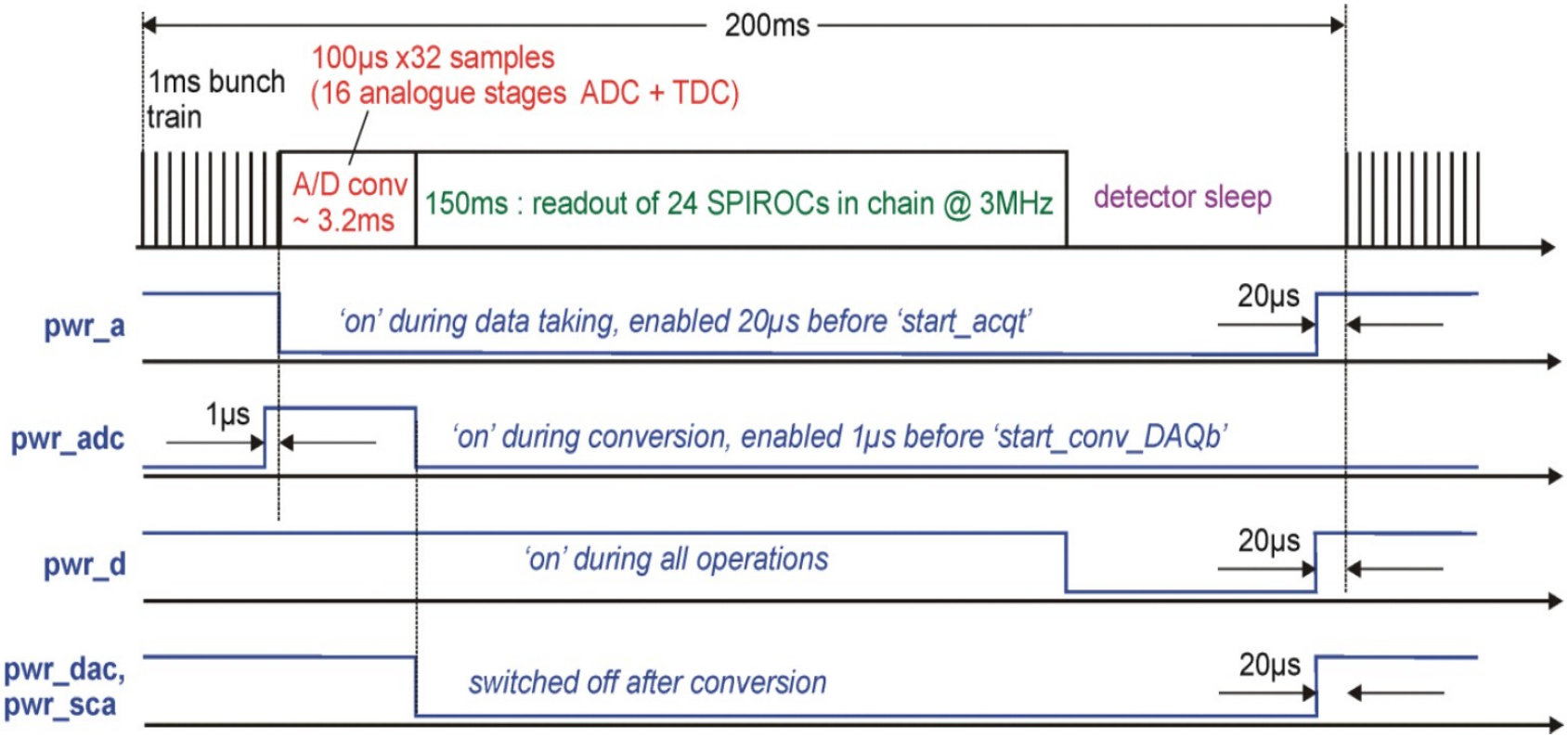
- Multiplexer deadtime very small in testbeam mode (longer ramp)
- Resolution in testbeam mode: ~3ns
- Very small differences for the two ramps in testbeam mode
- Resolution of ~1ns possible by optimizing ramp slopes (and dynamic range)

  → Tests with 1.25µs ramp promising

SPIROC2b

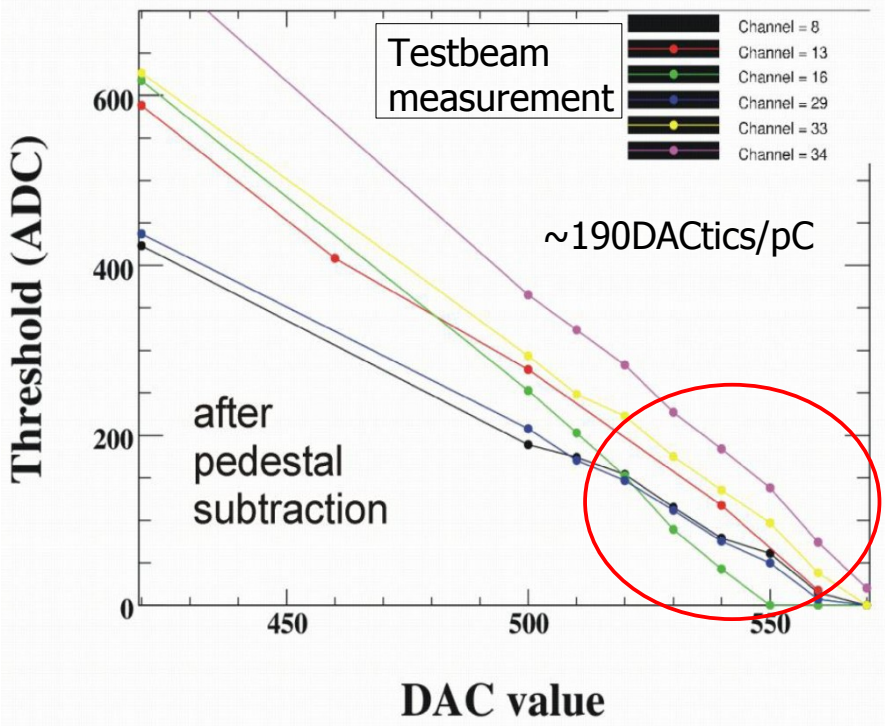

16-stage analogue memory
DIF
ext_hold, start_acqt, clk, ...
Trigger
19.6dB
100pF
coaxial cable (~1m)
pulse generator (voltage step)
50Ω
50Ω
100nF
GND
HBU
IN
SPIROC2
1.5pF
0.1pF-1.5pF
Low gain Preamplifier
Slow Shaper
50 -100ns
Analog memory
Depth 16
Gain selection
Gain
0.1pF-1.5pF
15pF
High gain Preamplifier
Slow Shaper
50-100ns
Depth 16
Charge measurement
HOLD
READ
Fast Shaper
15ns
Discri
Variable delay
Trigger
Depth 16
Flag TDC
12-bit Wilkinson ADC
Conversion 80 µs
8-bit DAC 0-5V
DAC output
4-bit threshold adjustment
Common to the 36 channels
10-bit DAC
TDC ramp 300ns/5 µs
Time measurement
Analog output

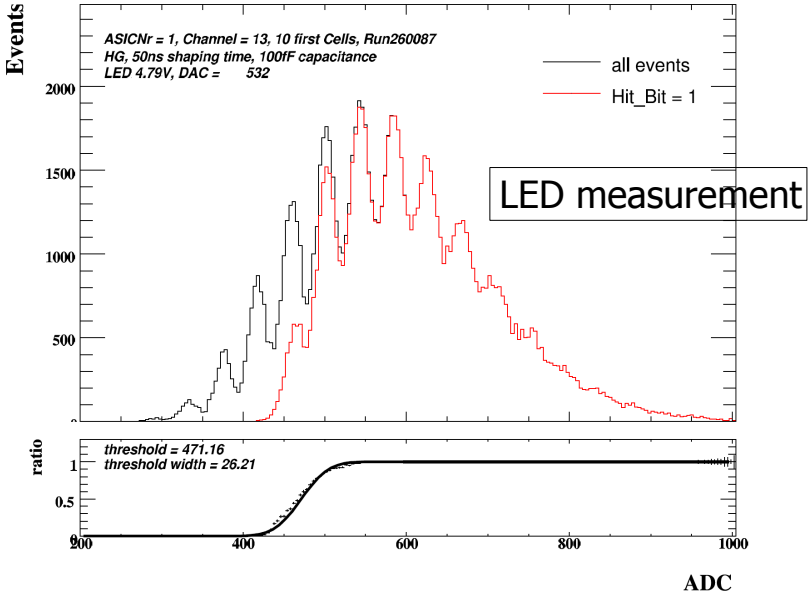
Power pulsing

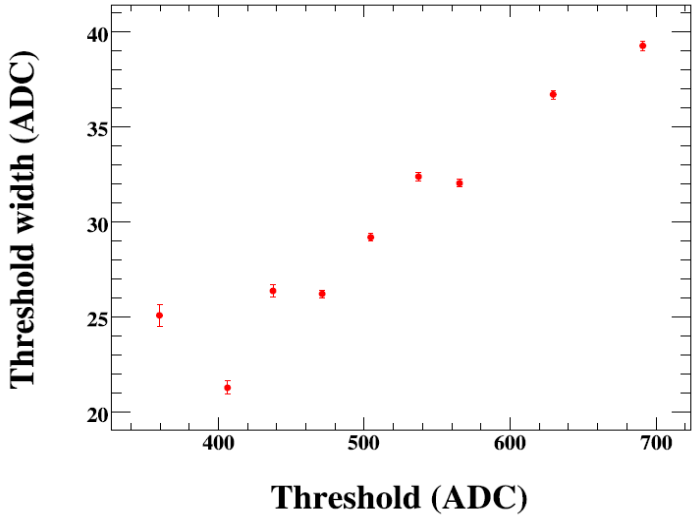


Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency

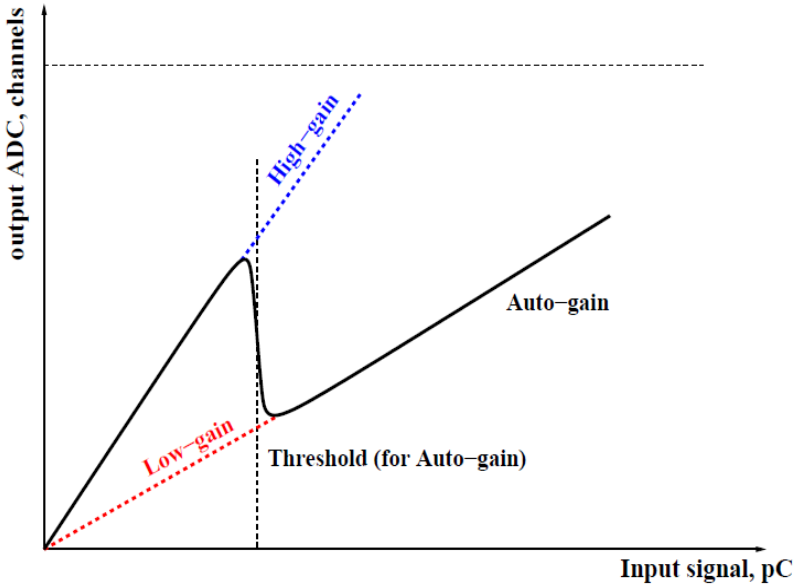


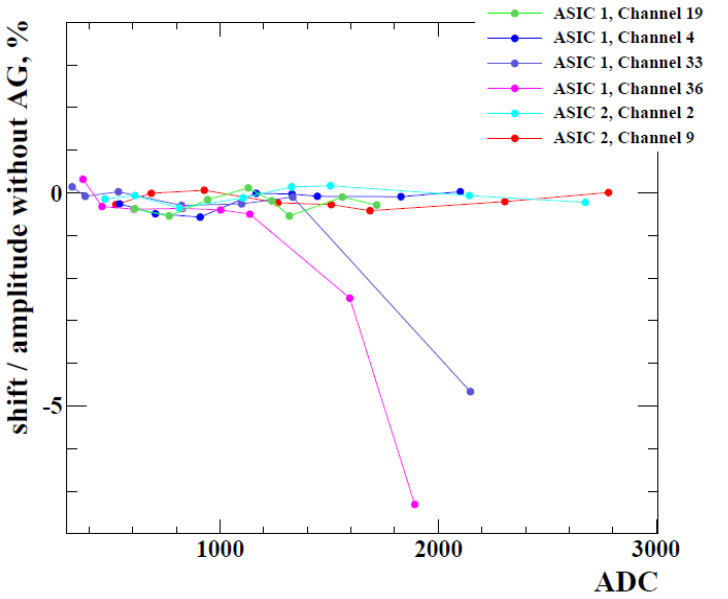


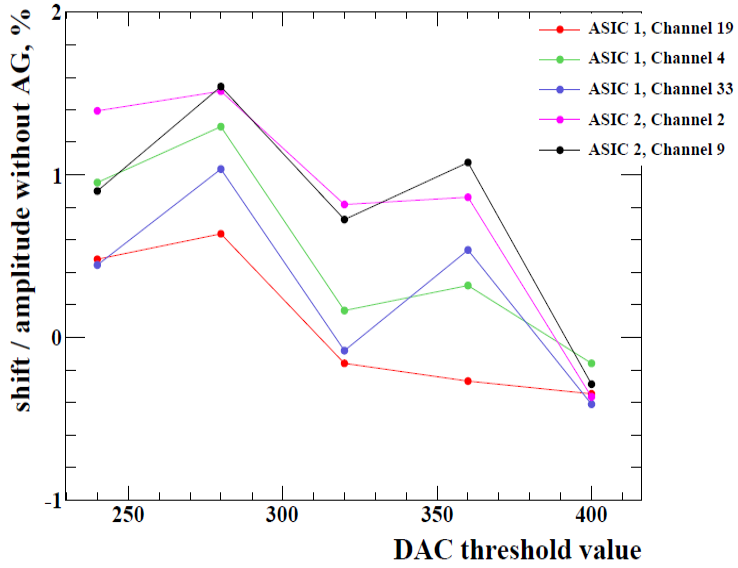


Autogain performance - Linearity

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, but still slightly depends on:
  - Amplitude
  - Distance to threshold

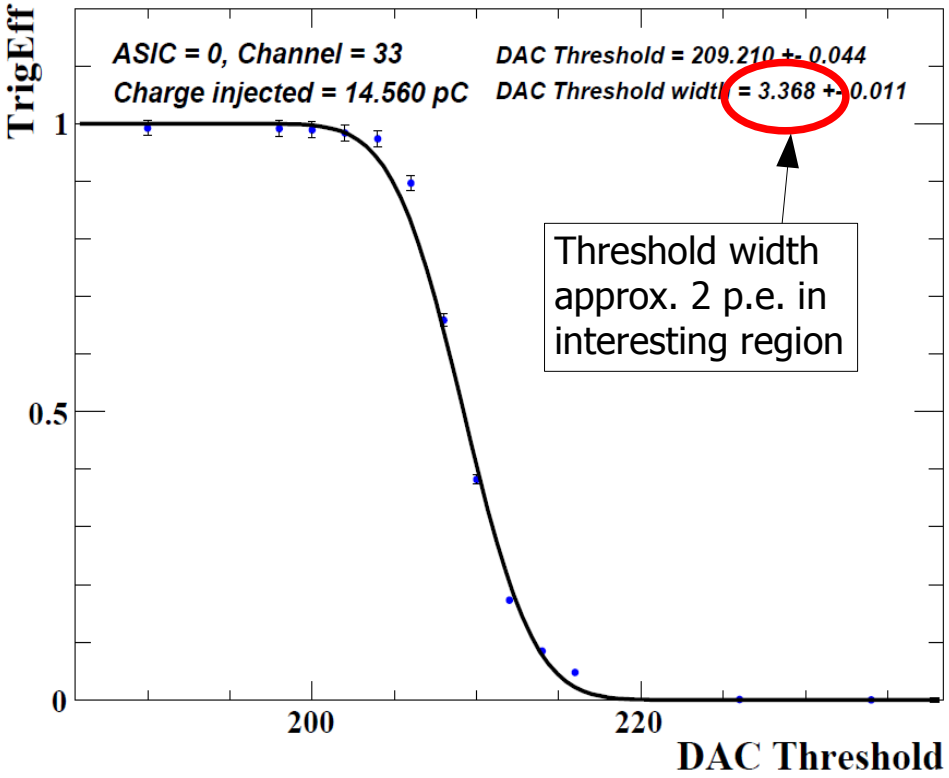


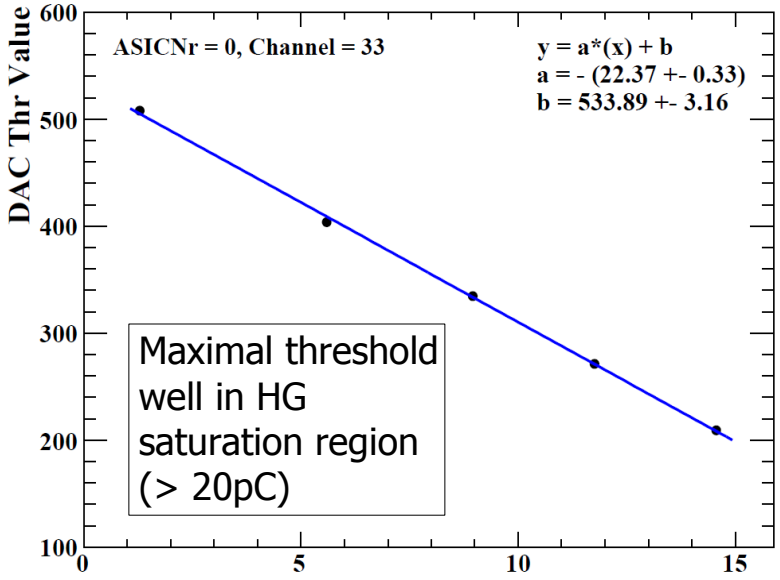


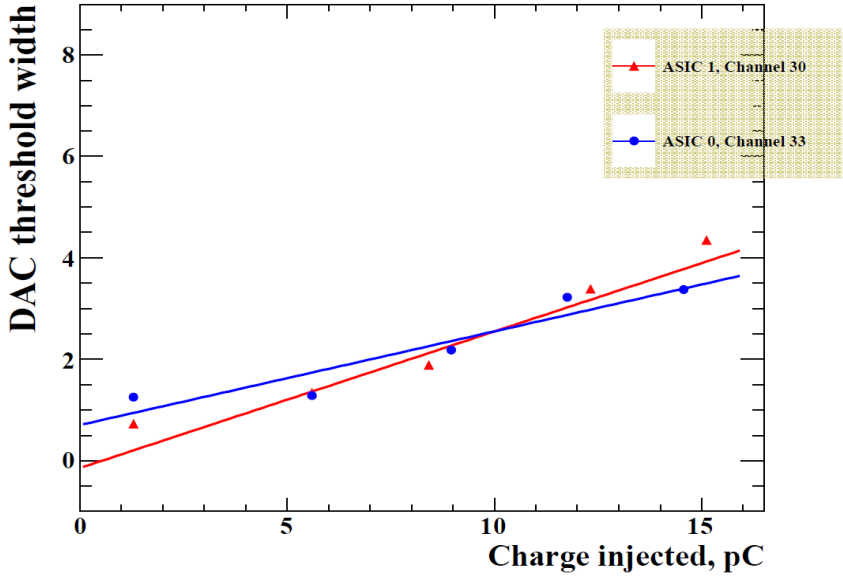


Autogain performance - Thresholds

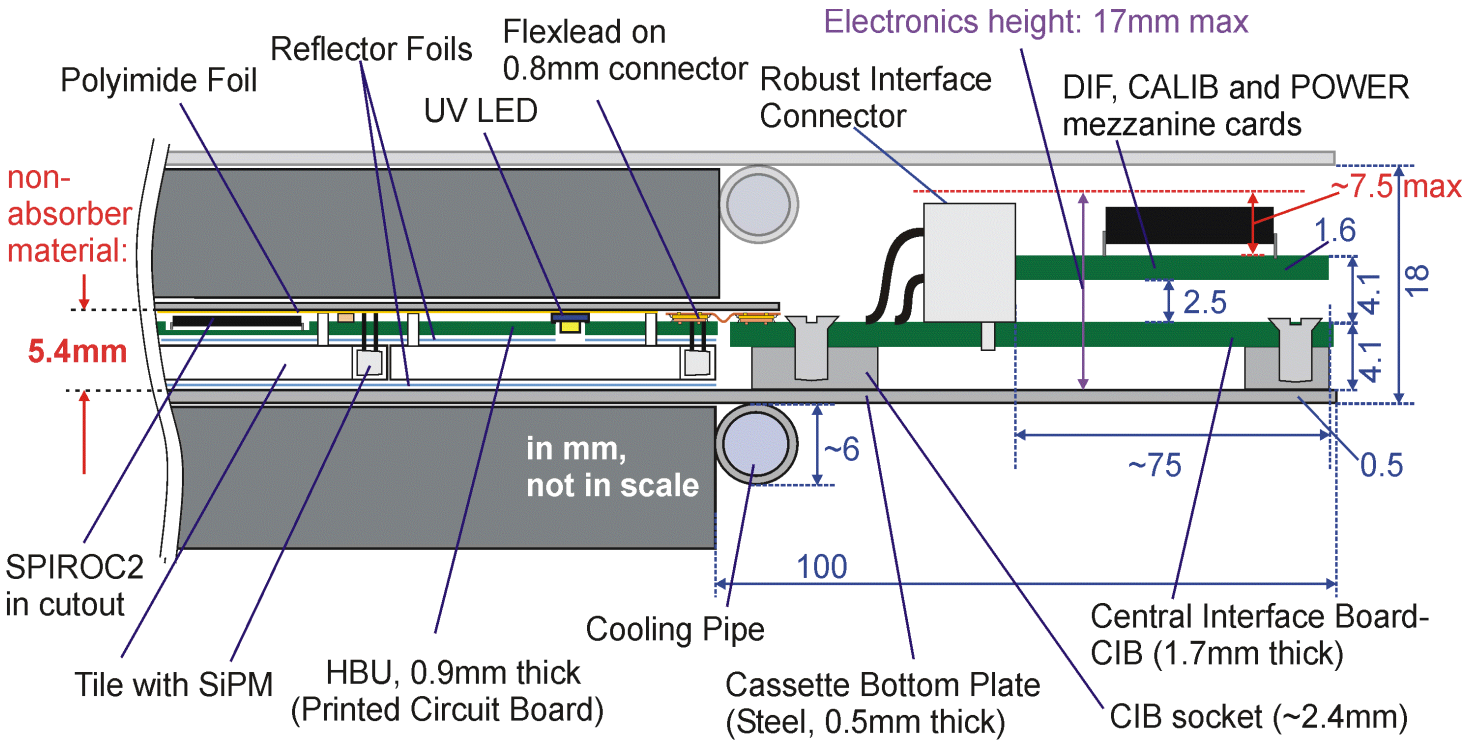
- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Similar performance as for autotrigger

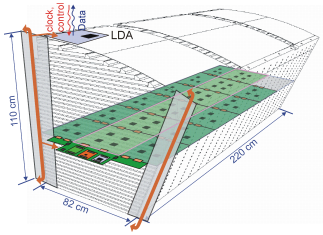






AHCAL layer – cross section





Abbr.	Name
DIF	Detector Interface Board
CALIB	Steering for LED calibration
CIB	Central Interface Board
HBU	Front-end board

- Compliant with steel and tungsten options
- Redesign and production of components almost finished