



SKIROC2 measurements

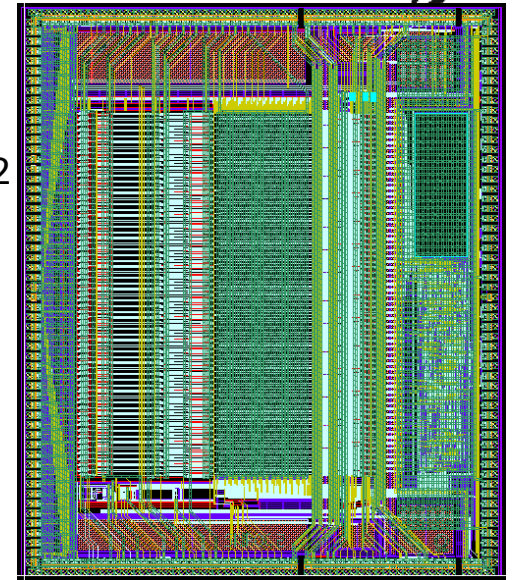
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Frédéric DULUCQ, Giséle MARTIN-CHASSARD,
Nathalie SEGUIN-MOREAU

20 December 2016

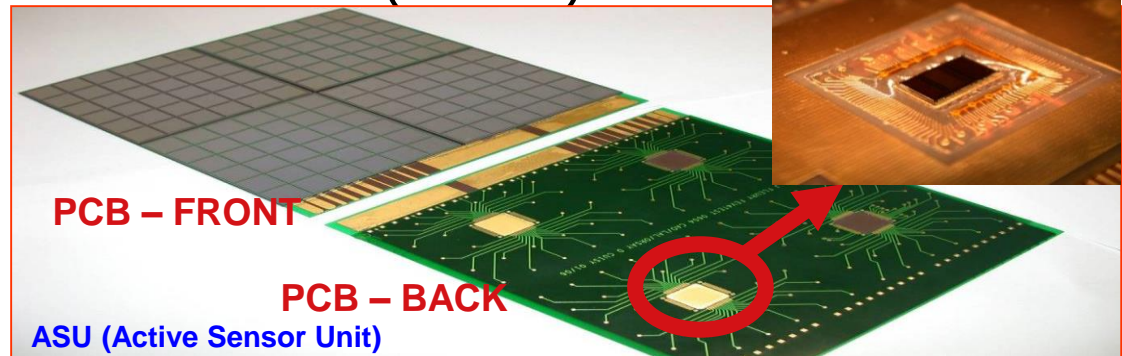
Orsay MicroElectronics Group Associated

SKIROC : ECAL readout

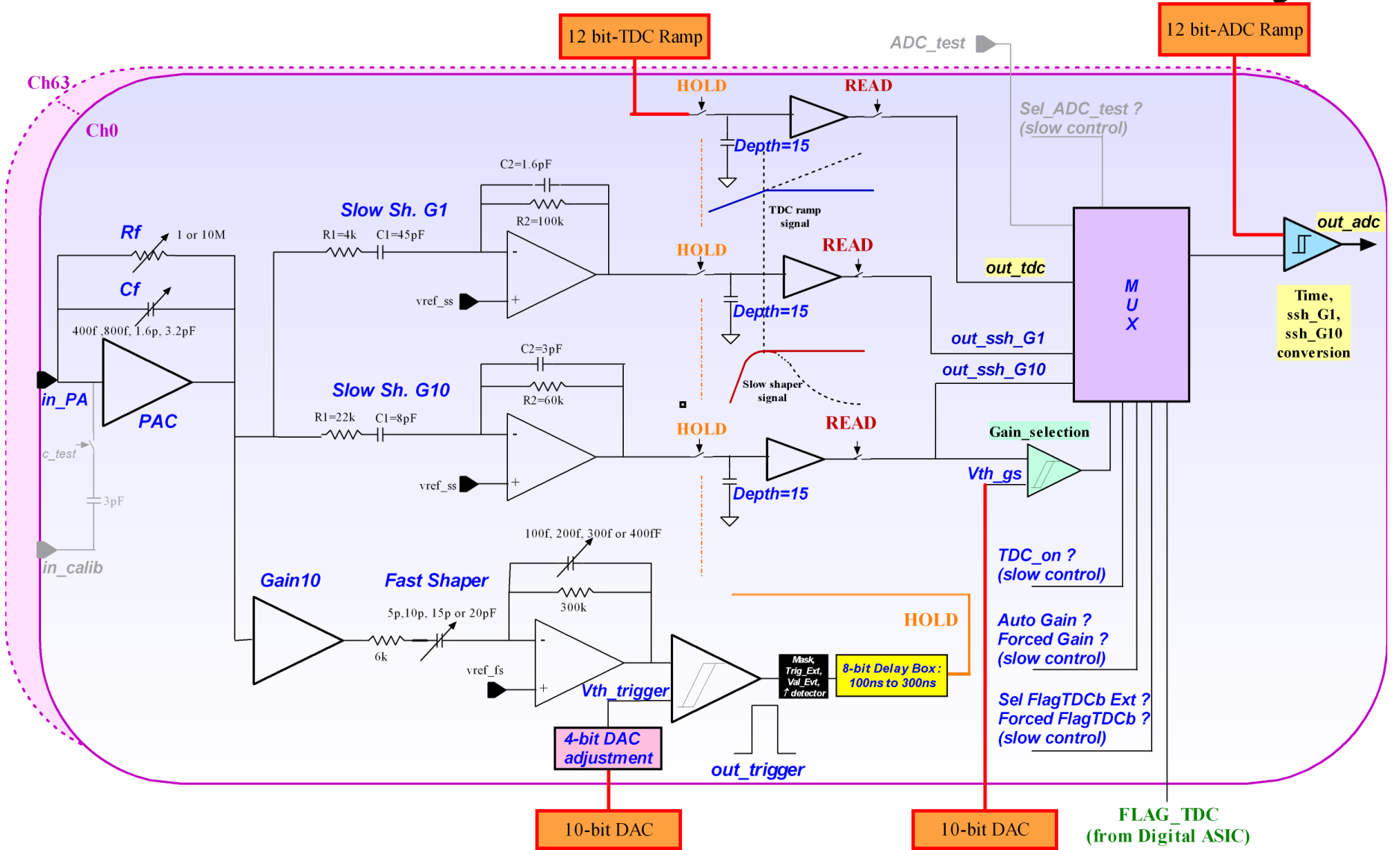
- SKIROC2 : Silicon Kalorimeter Integrated Read-Out Chip
 - 64 channels, AMS SiGe 0.35 μm , 70 mm^2
 - **Very large dynamic range:**
 - HG for 0.5-150 MIP, LG for 150-2500 MIP
 - Auto-trigger, Analog storage, Digitization & Token-ring ReadOut
 - Testability at wafer level
- Front End boards crucial element
 - Collaboration with LLR and SKKU (Korea)



C detector with PCB ≈ 20 pF

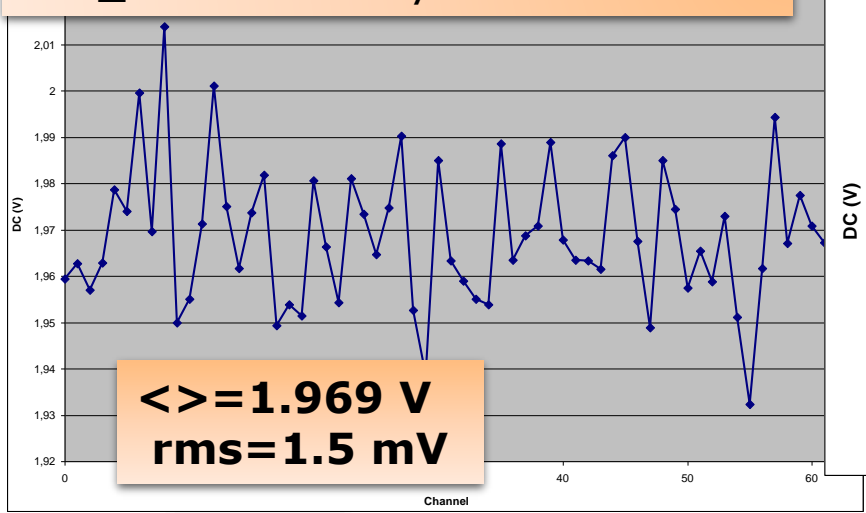


SKIROC2 Analogue core

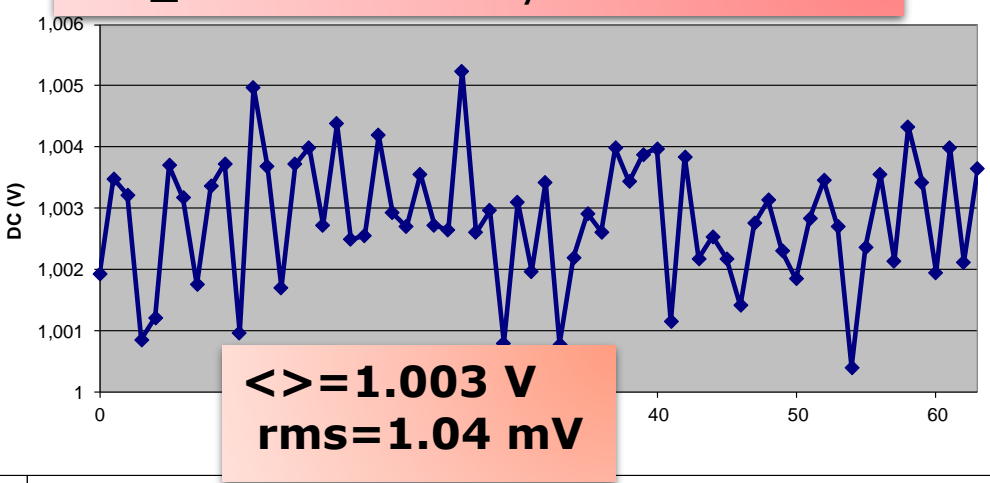




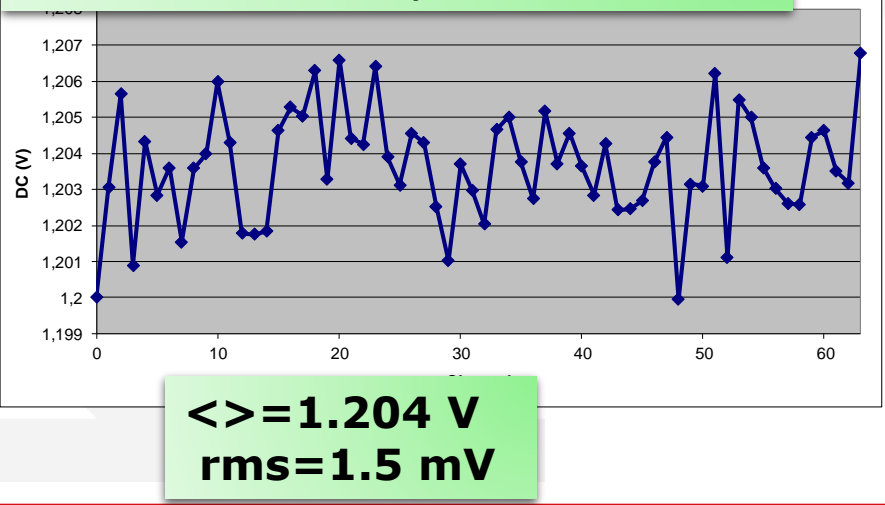
Out_PA: uniformity of the DC level



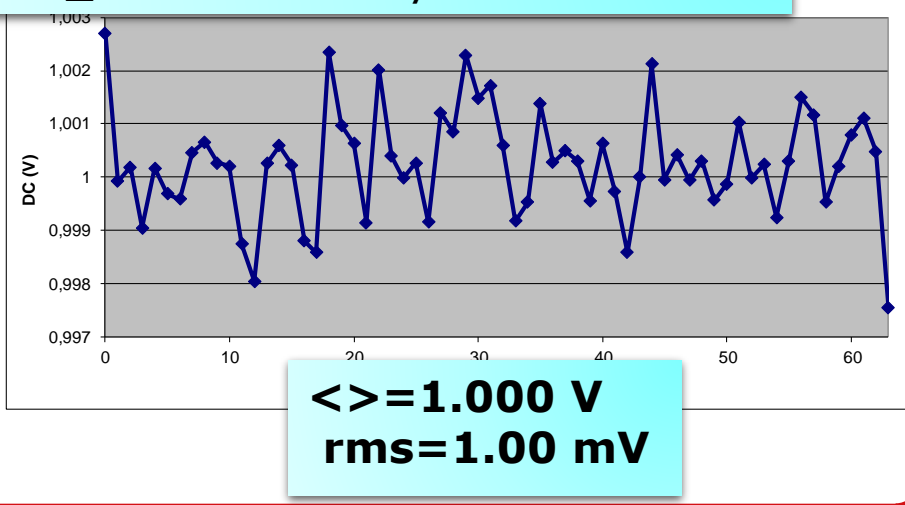
Out_SS10: uniformity of the DC level



Out_FS: uniformity of the DC level



Out_SS1: uniformity of the DC level



DAC Threshold Linearity



Slope 2.2 mV/DAC Unit, DNL ± 1 LSB INL = ± 1.7 LSB

Setup | Slow Control 1 | Slow Control 2 | Probe, SCA Read | FPGA Registers | Debug | Info SKIROC2 | Info pcb1011 (1) | Info pcb1011 (2) | Analogue Test: S-Curve

Analogue Test: DAC | Analogue Test: DC | Analogue Test: Full | Digital ASIC Debug / DAQ

DAC Current Value 0

Test DAC

Max Value: 880

DAC choice: Threshold

V_{bandgap} (DAC): 2,5028223 V

Fit Slope: 2,20711m | Max Value: 2,77029

Fit Intercept: 828,321m | Min Value: 829,628m

Max DNL Value: 1,461 LSB

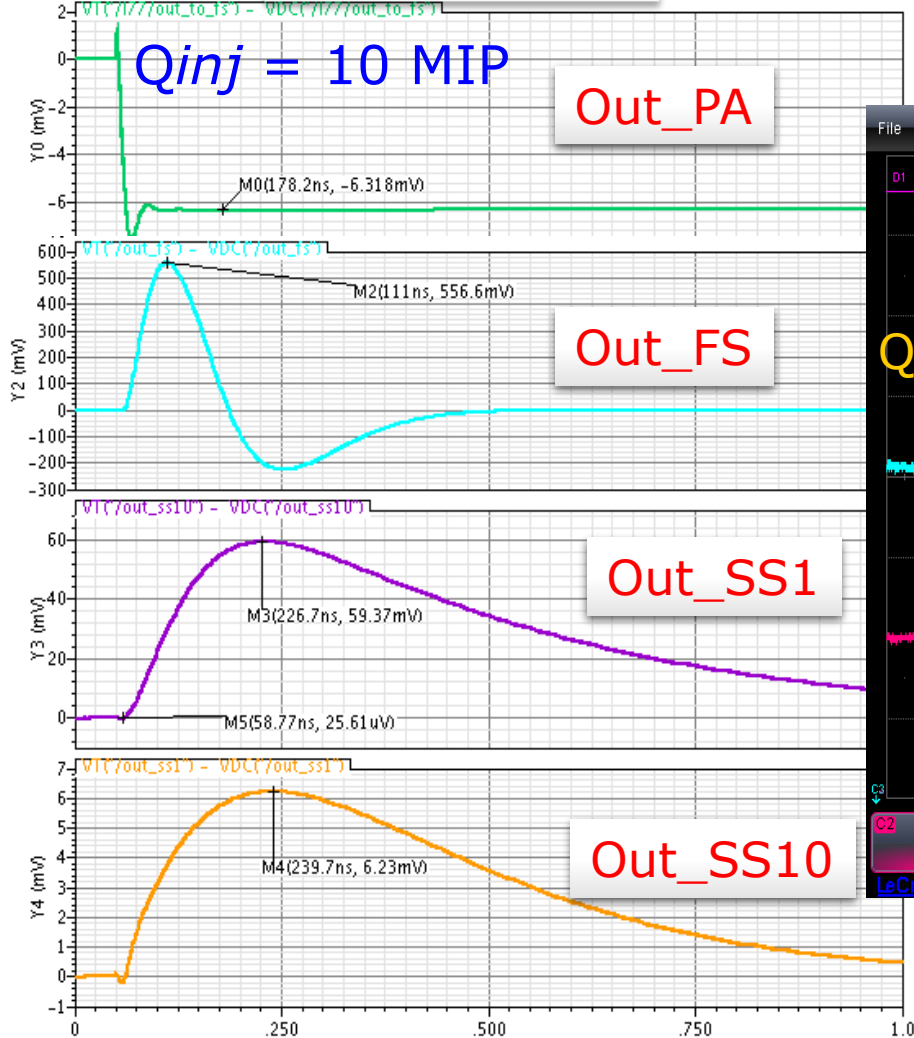
Min DNL Value: -0,5135 LSB

Max INL Value: 1,758 LSB

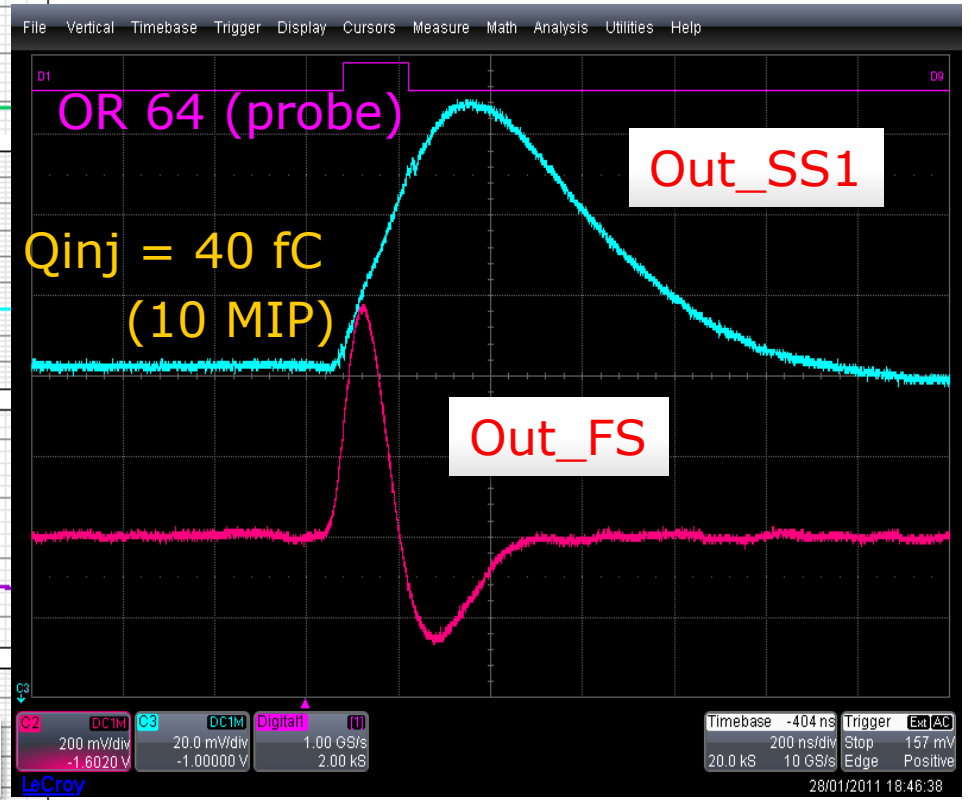
Min INL Value: -1,754 LSB

Parameter	Value
Max DNL Value	1,461 LSB
Min DNL Value	-0,5135 LSB
Max INL Value	1,758 LSB
Min INL Value	-1,754 LSB

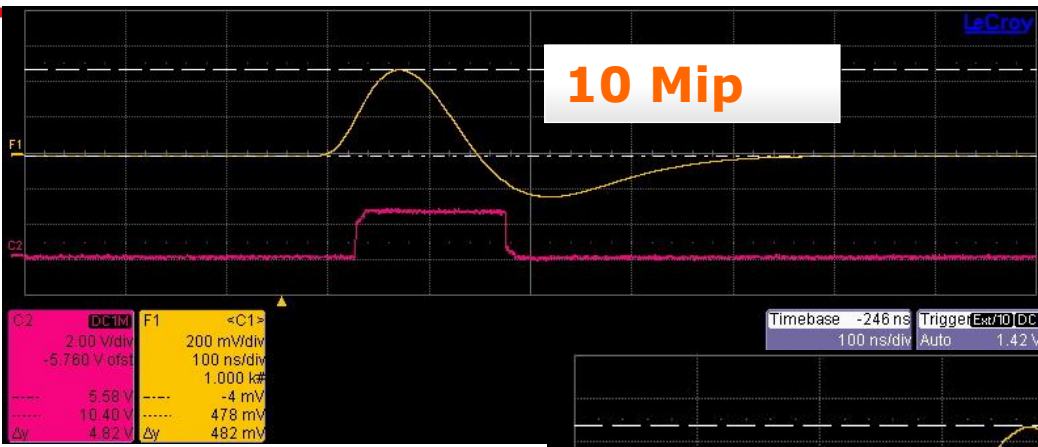
SIMULATIONS



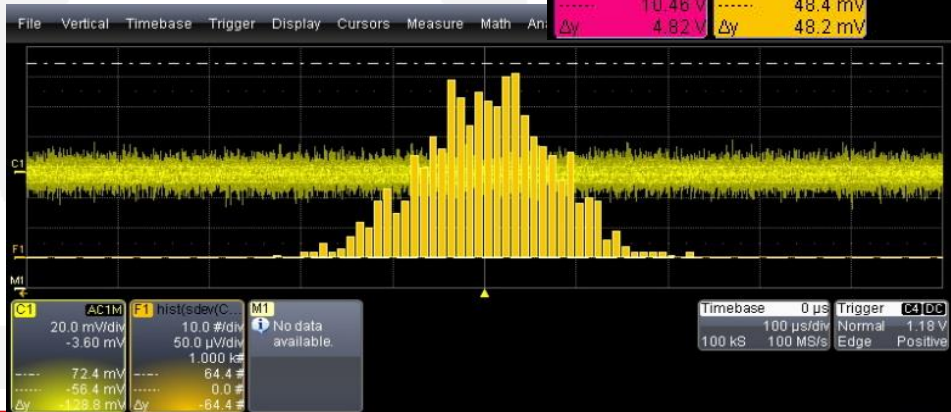
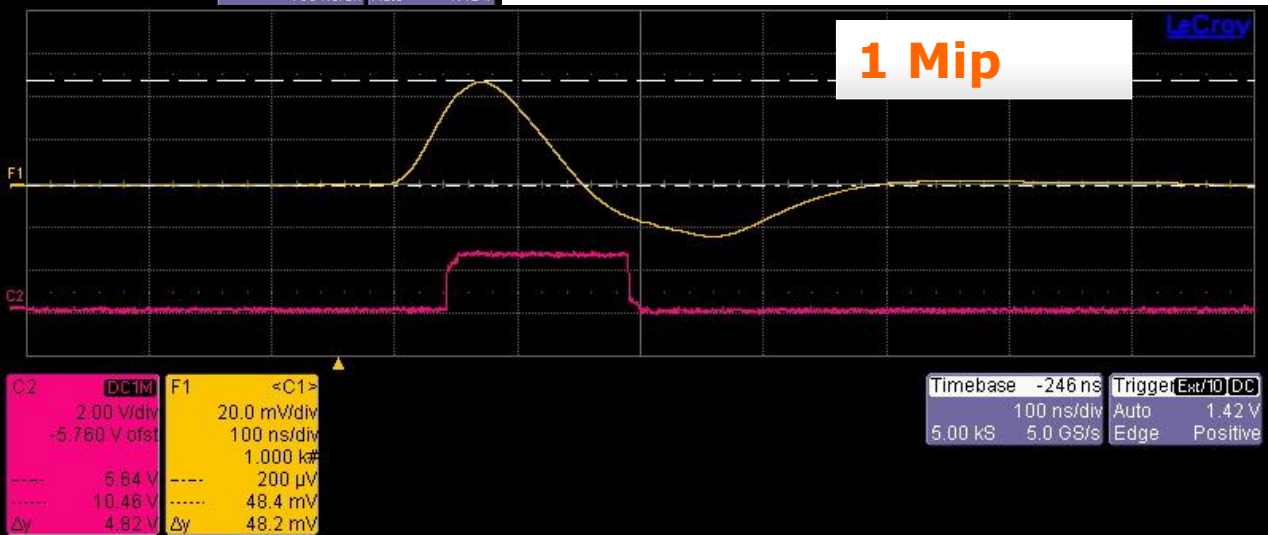
MEASUREMENTS



SKIROC2: Fast Shaper noise



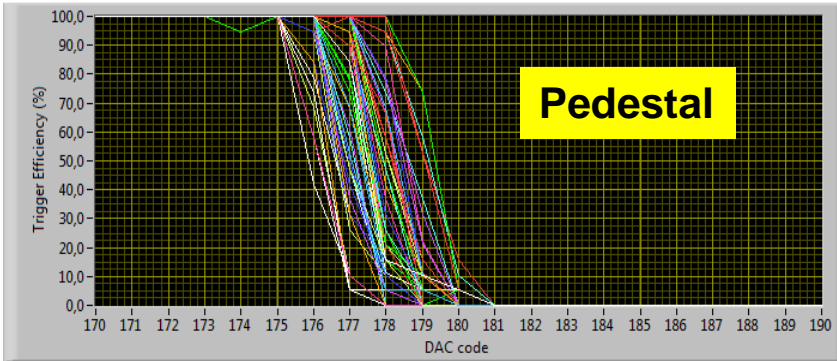
**Fast Shaper
~ 48mV/Mip**



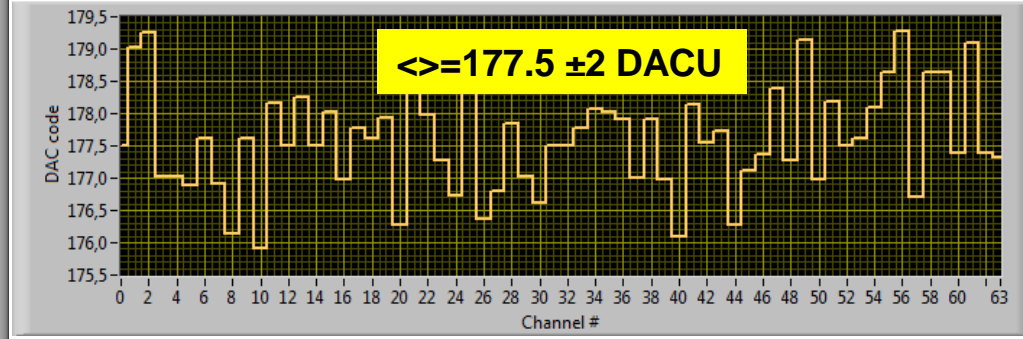
**rms noise= 5.3 mV ie 1/9 MIP
S/N=9**

Trigger efficiency (1)

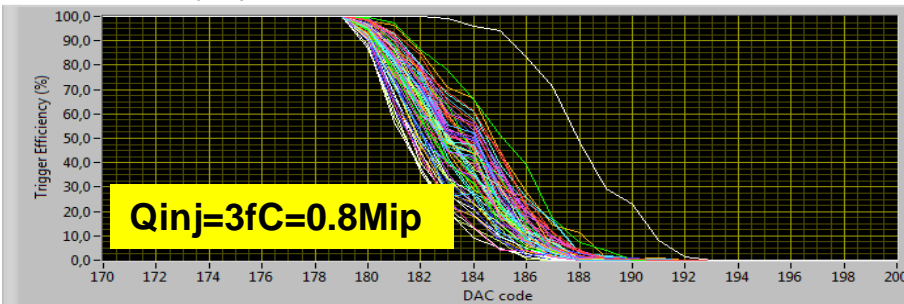
Test S-Curve vs Threshold (all ch.)



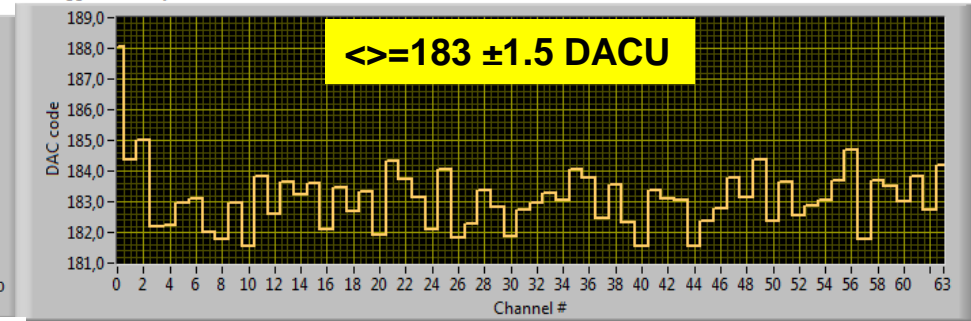
50% trigger efficiency



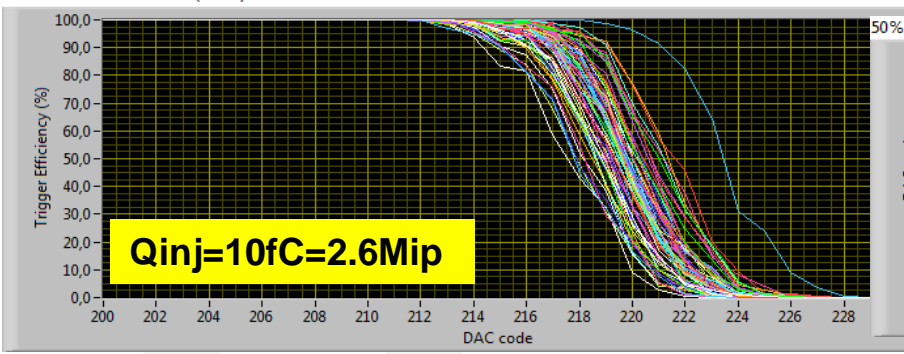
Test S-Curve vs Threshold (all ch.)



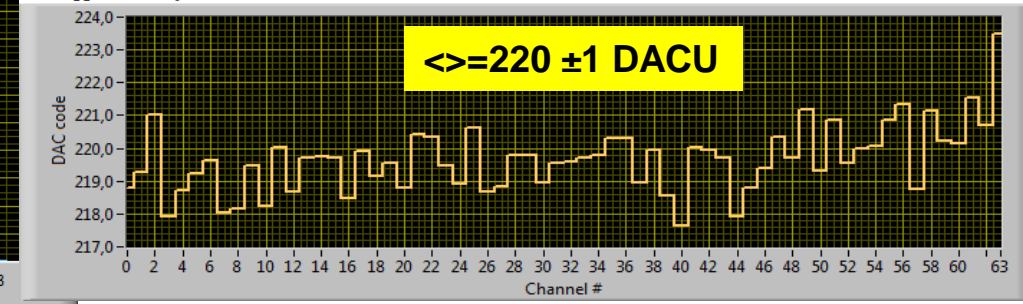
50% trigger efficiency



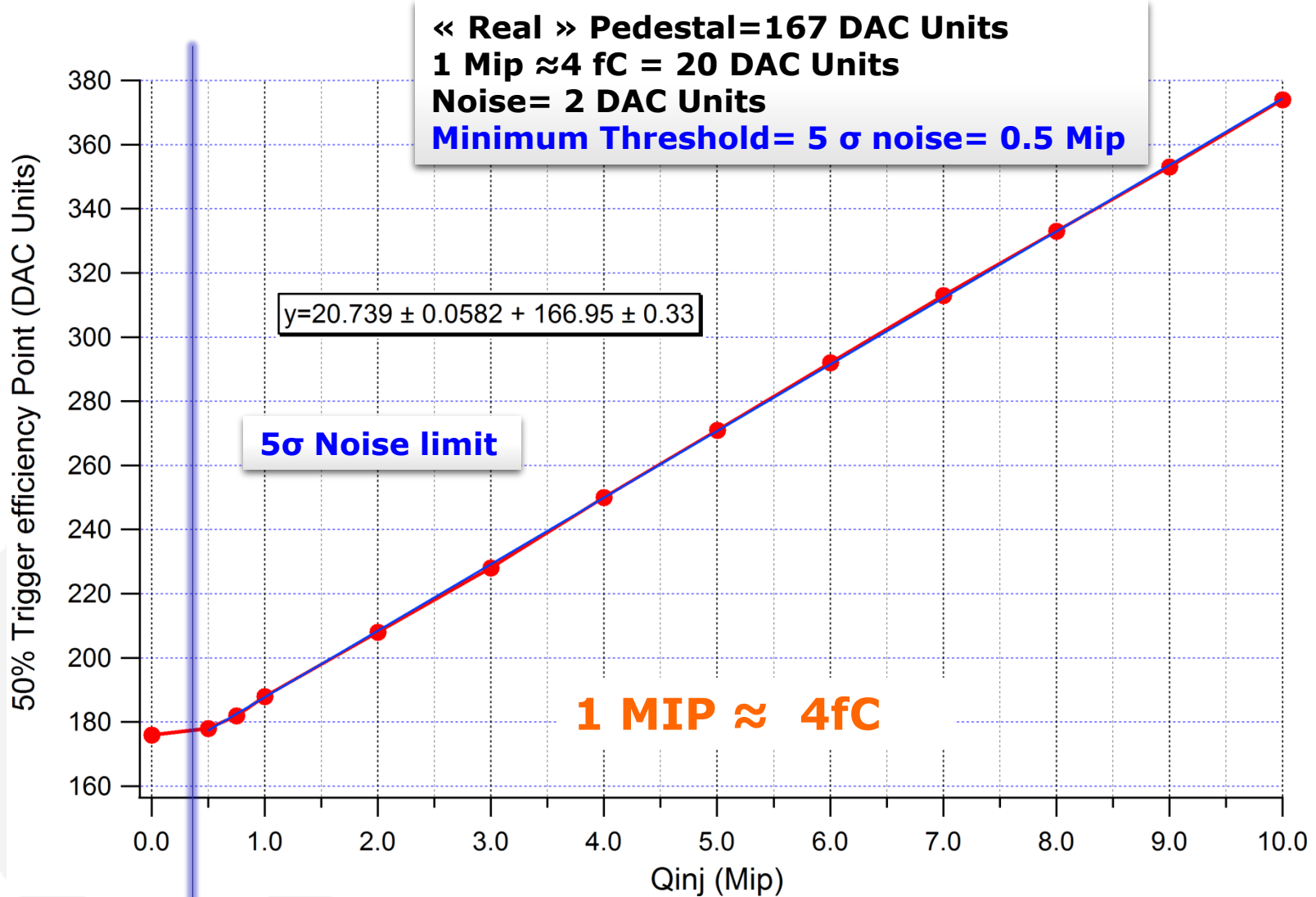
Test S-Curve vs Threshold (all ch.)



50% trigger efficiency



Trigger efficiency (2)



SKIROC2 : PreAmplifier ENC

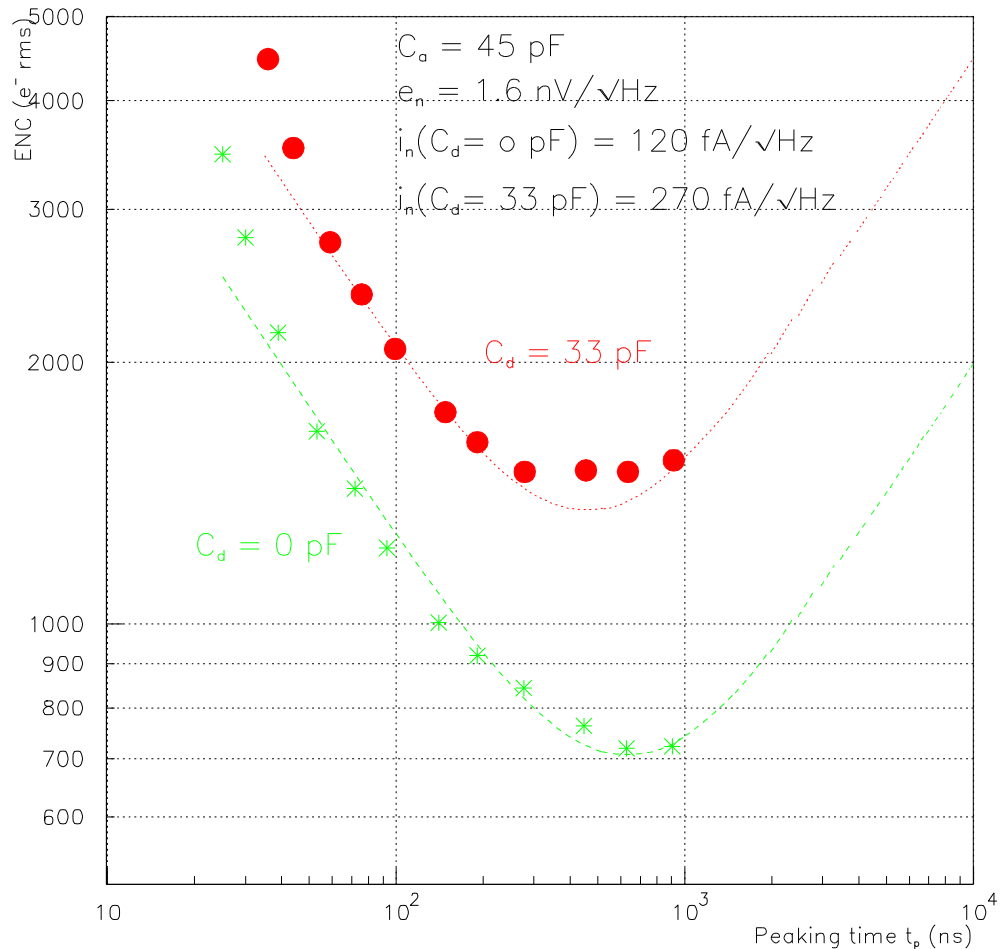


SKIROC2

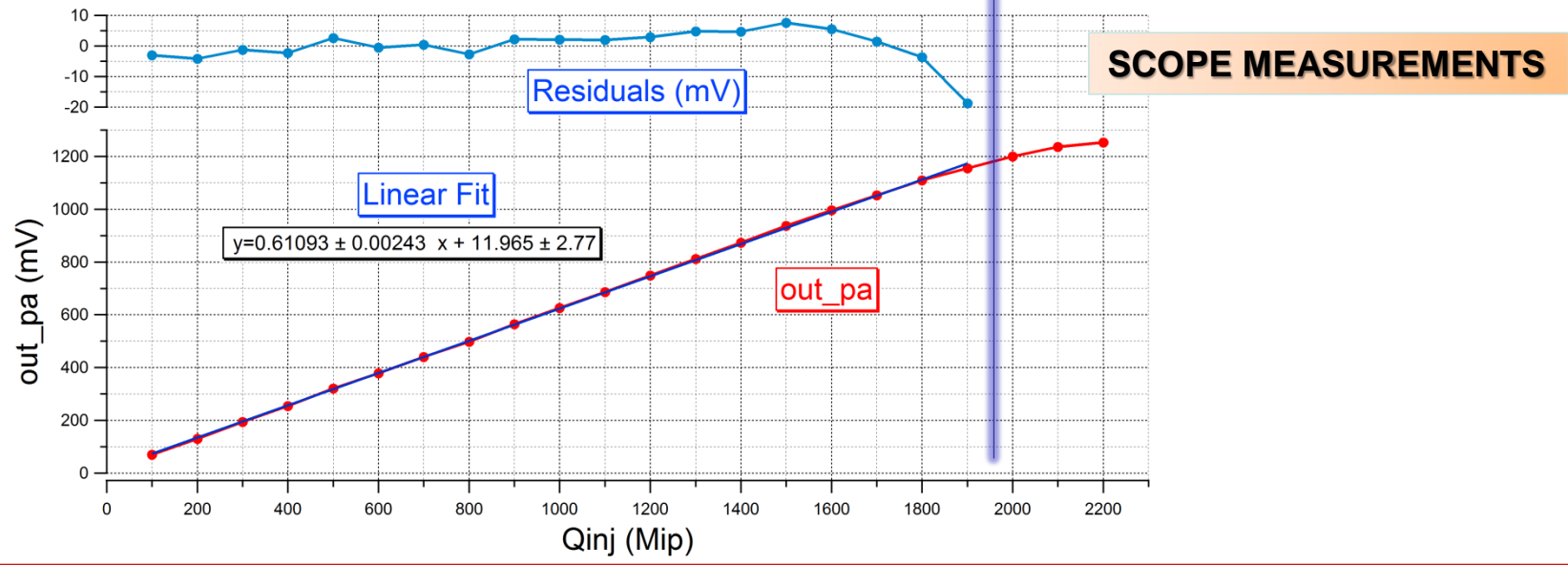
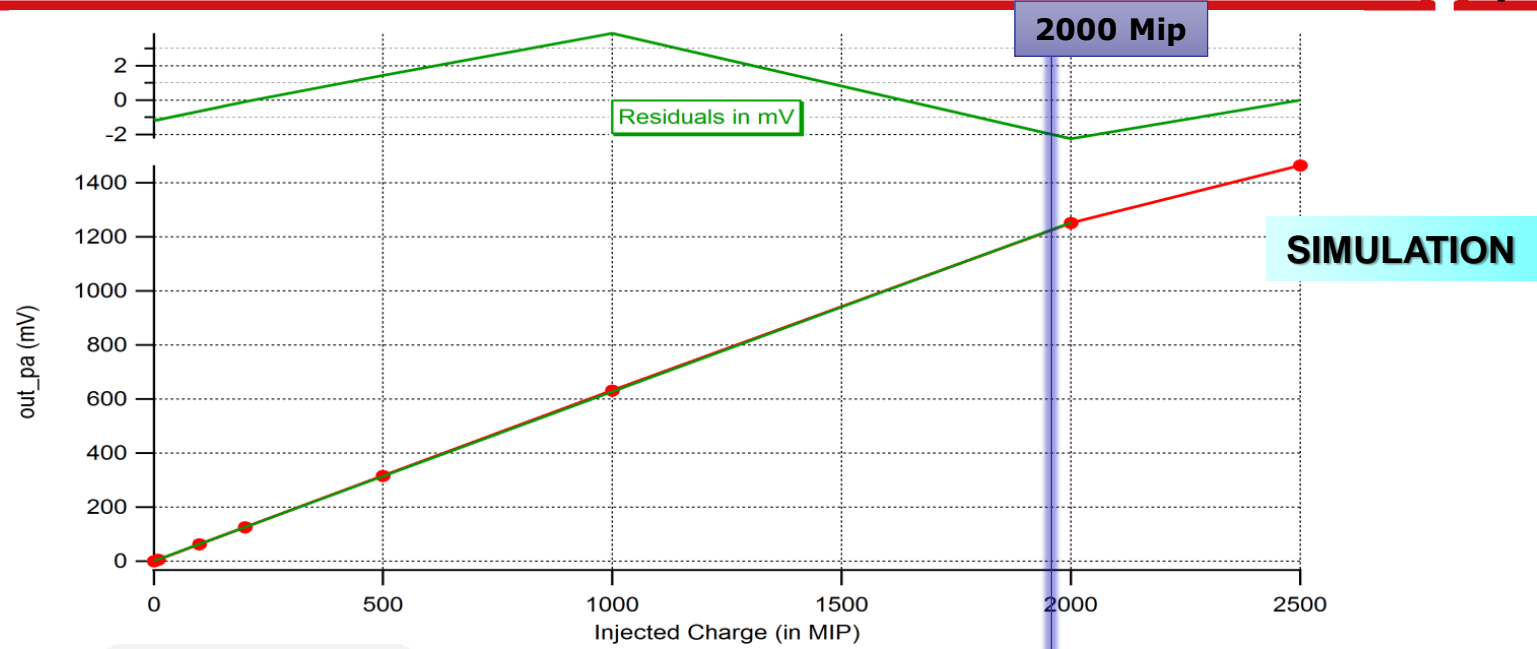
$C_f=6\text{pF}$, $Q_{inj}=2510^6 e^-$
CRRC2 x 100

C_d (pF)	A	A*181.5	B	C	$e_n \times C_t$
0	0.4	72.6	664700	0	72.6
33	0.7	127.05	1400000	0	127.05

e_n nV/sqrt(Hz)	i_n fA/sqrt(Hz) ($C_d=0\text{pF}$)	i_n fA/sqrt(Hz) ($C_d=33\text{pF}$)	C_a pF
1,6	120	270	45



Linearity of the Charge Preamp

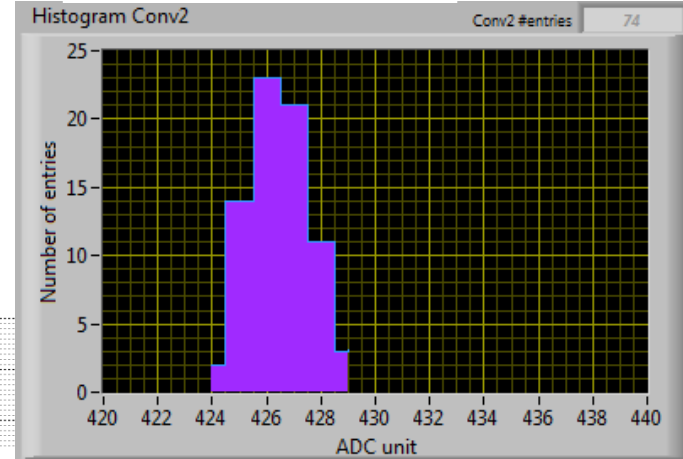
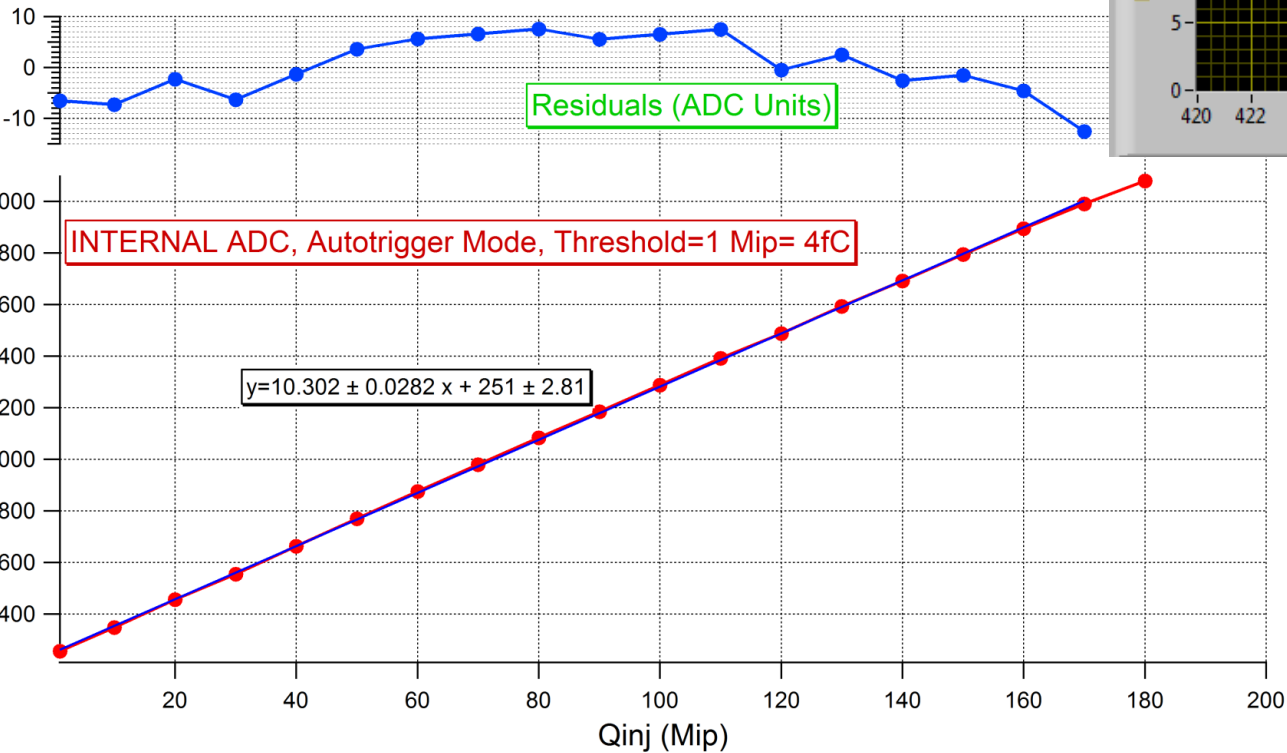


Linearity of High Gain Shaper

Noise = 630 μ V
1 Mip gives 5.7 mV
S/N=9

SS10@20 MIP
Rms = 1.16 ADC
U=600 μ V

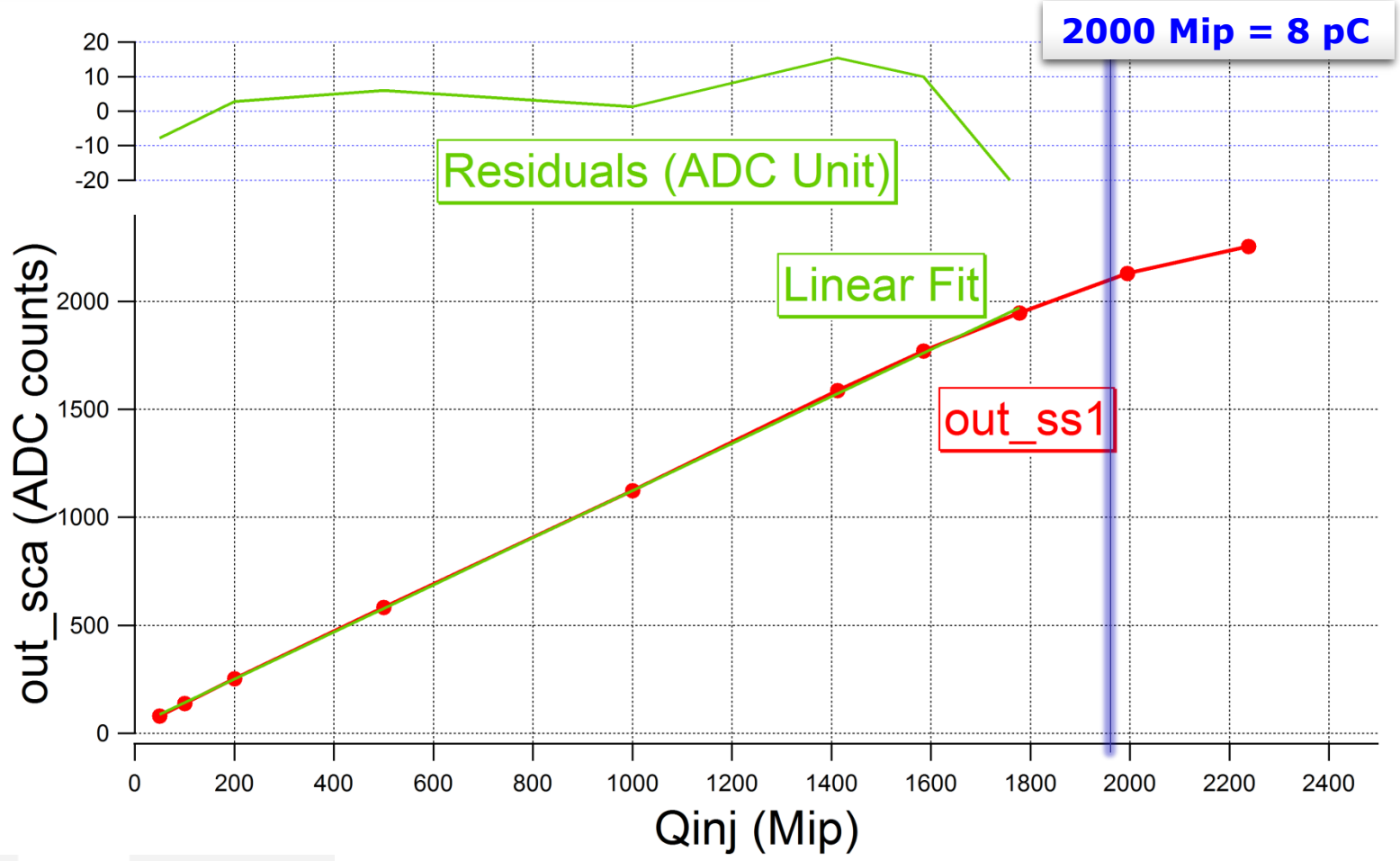
MEASUREMENTS using SCA and internal ADC
Autotrigger mode
1 MIP (4fC) threshold



Linearity of the Low Gain Shaper

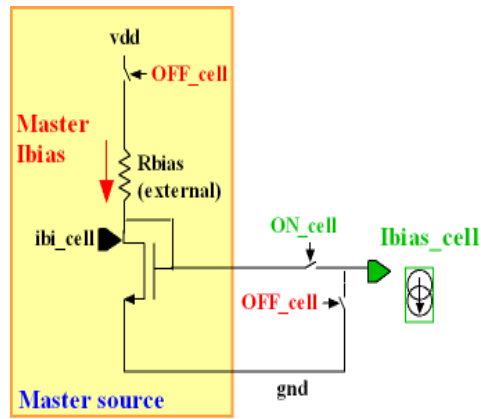
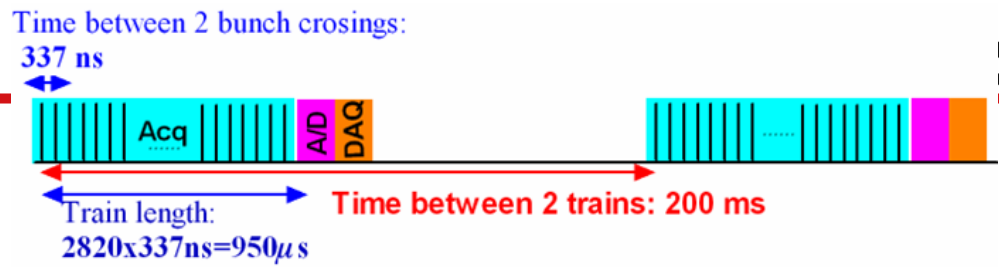


MEASUREMENTS using SCA and internal ADC
Autotrigger mode
1 MIP (4fC) threshold



POWER PULSING

- Requirement:
 - 25 $\mu\text{W}/\text{ch}$ with 0.5% duty cycle
 - 500 μA for the entire chip

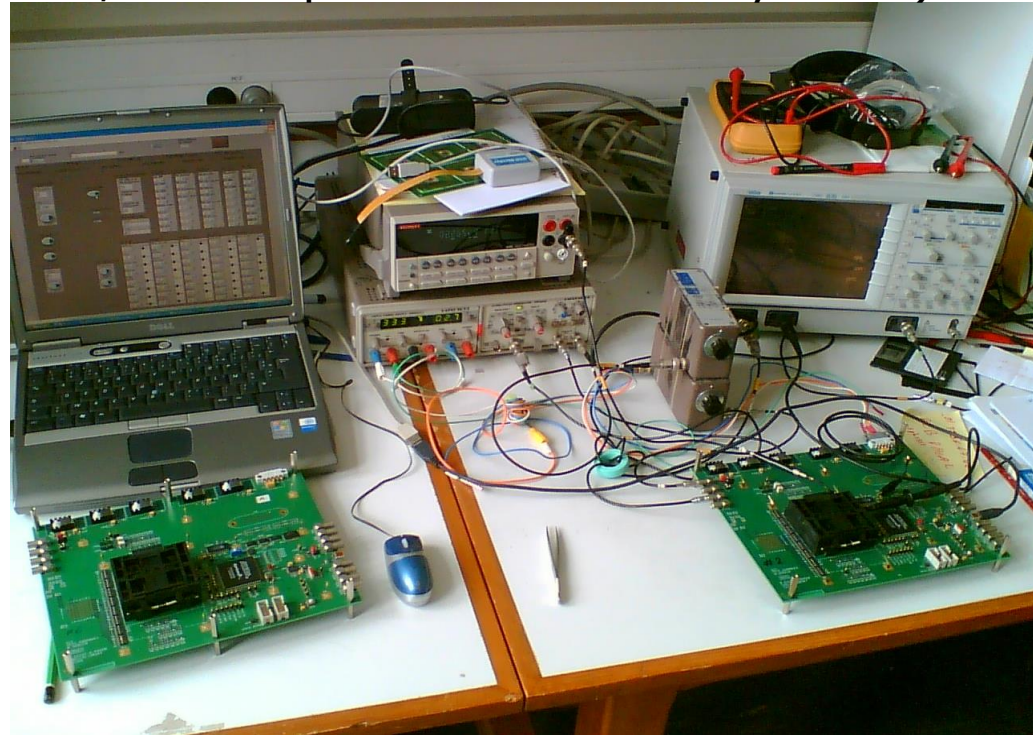


- Power pulsing:
 - Bandgap + ref Voltages + master I: switched ON/OFF
 - Shut down bias currents with vdd always ON
- SK2 power consumption measurement:
 - $123 \text{ mA} \times 3.3\text{V} \approx 40 \text{ mW} \Rightarrow 0.6 \text{ mW}/\text{ch}$
- 4 Power pulsing lines : analog, conversion, dac, digital
- Each chip can be forced on/off by slow control

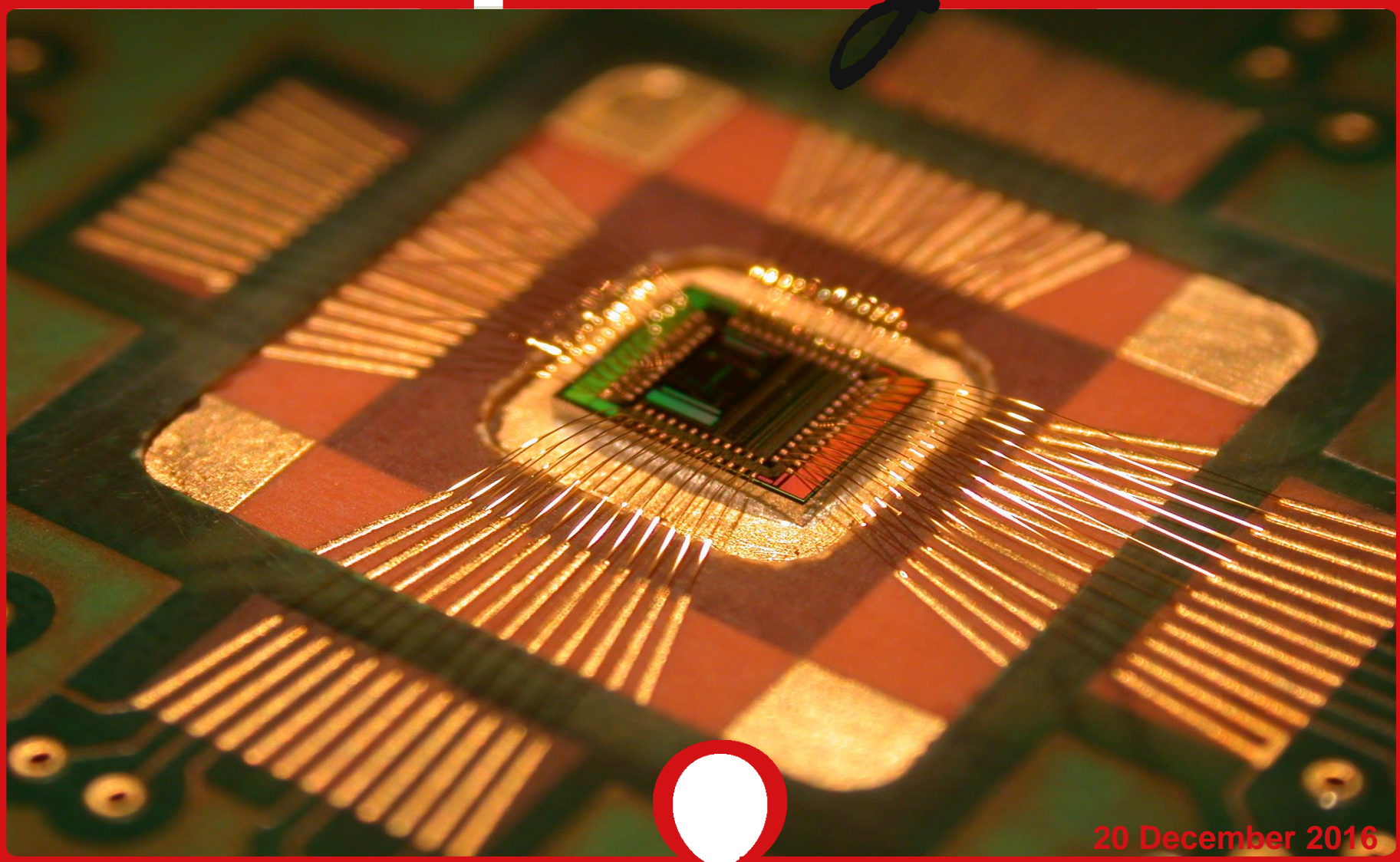
Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 $\mu\text{W}/\text{ch}$

- Good performance of SKIROC2:
 - 0.5 Mip (2 fC) up to 2000 Mip (8 pC) dynamic range
 - 0.1Mip noise (0.4 fC ie 2500 electrons), minimum threshold 0.5 Mip, autotrigger mode
- 300 SKIROC2 will be packaged
 - For FEV8-CIP (design complete, PCB expected end January 2012)
- Test with FEV and sensors to be done at system level (power pulsing, DAQ)
- 4 Test Board
 - 2 OMEGA, 1 LLR, 1 SKKU



Omega



20 December 2016

Orsay MicroElectronics Group Associated

BACKUP SLIDES

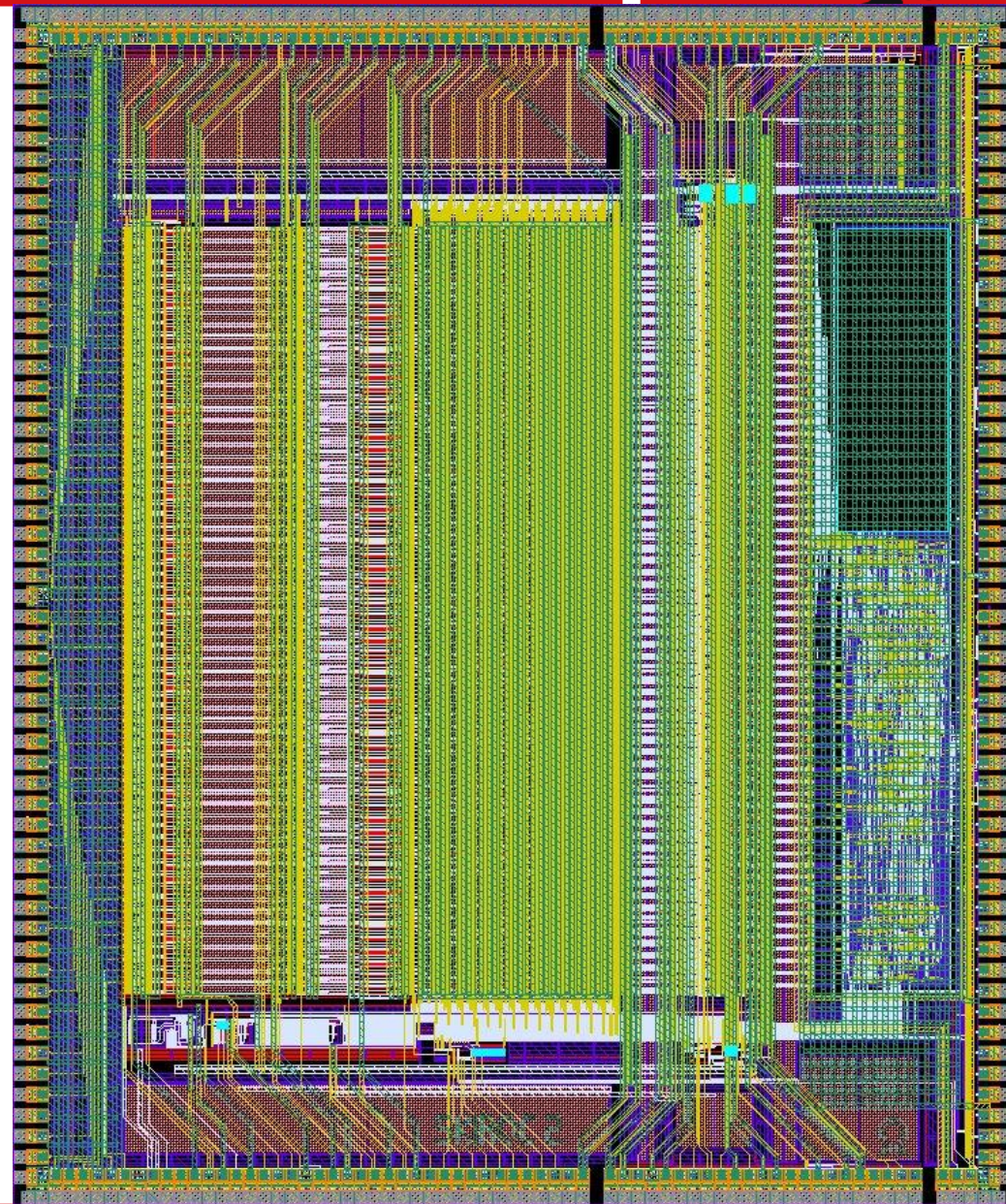
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Silikon
Kalorimeter
Integrated
Read
Out
Chip

- 64 Channels
 - Difficult layout : 1MIP = 4fC, with digital activity !



- 250 pads
 - **17 for test purpose only**
- Die size
 - 7229 μm x 8650 μm



SILICON SENSORS (WAFERS) :

- Using 325 μ m thick Silicon Wafers => 26000e⁻/MIP
- $C_{detector}$ estimated 9pF
 - Add also 10pF due to PCB pads' capacitance
- PIN diode leakage up to 10nA / channel
 - Chip has leakage current capability

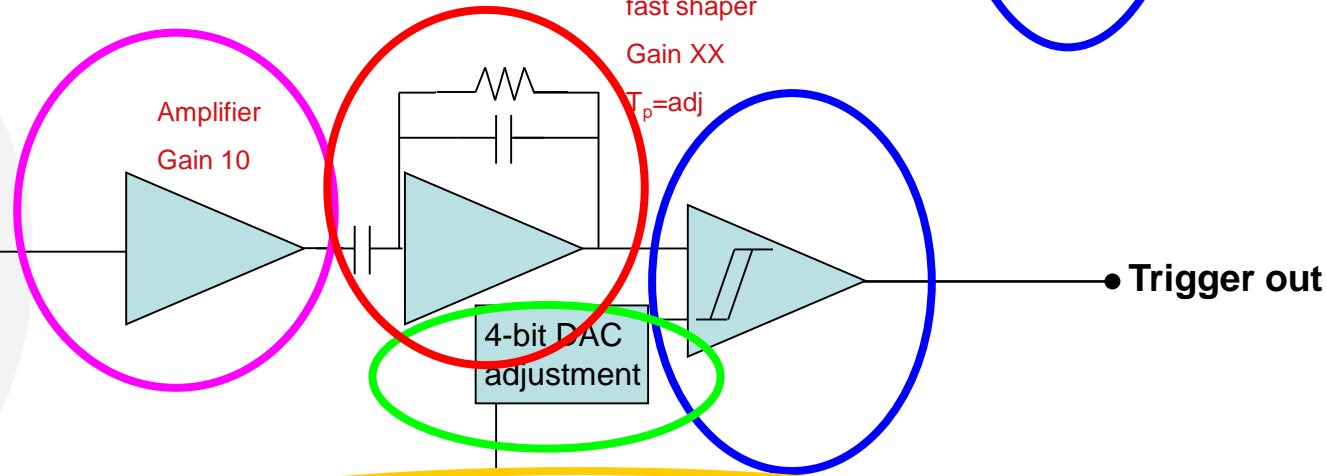
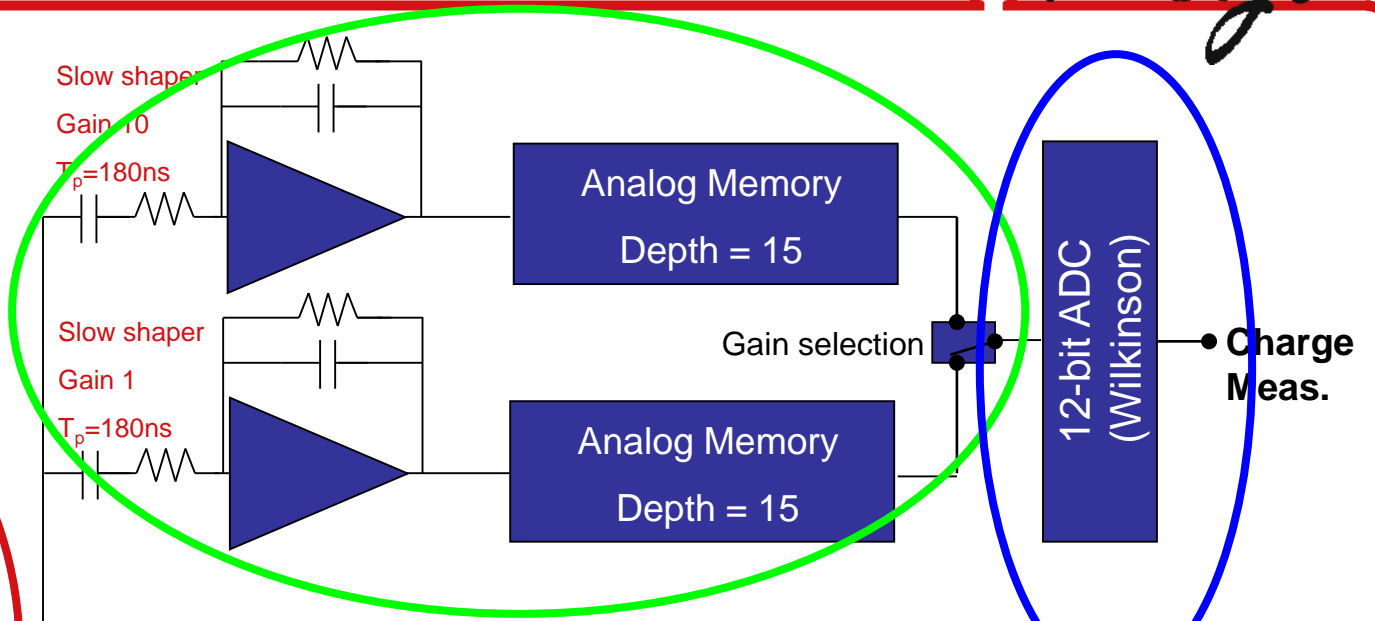
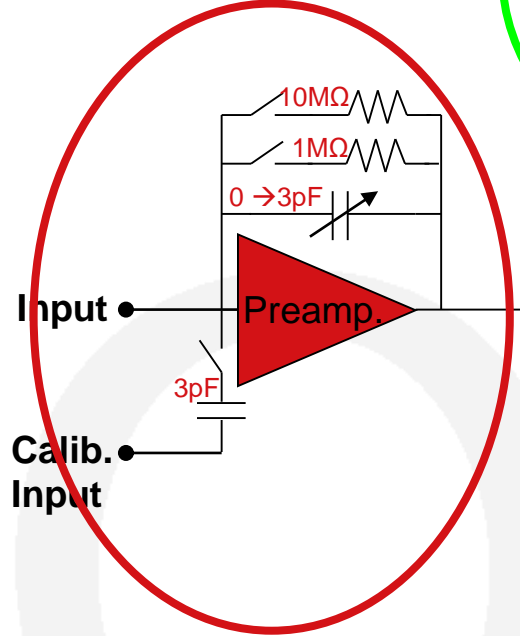
DETECTOR INTEGRATION

- Full power pulsing capability
 - 25 μ W/ch => 24h operation of full slab with 2 AAA batteries !
- Dynamic Range : from 1/2 MIP up to 2500 MIP
- Auto-trigger, Analog storage, Digitization & Token-ring ReadOut

SKIROC2 One channel block scheme



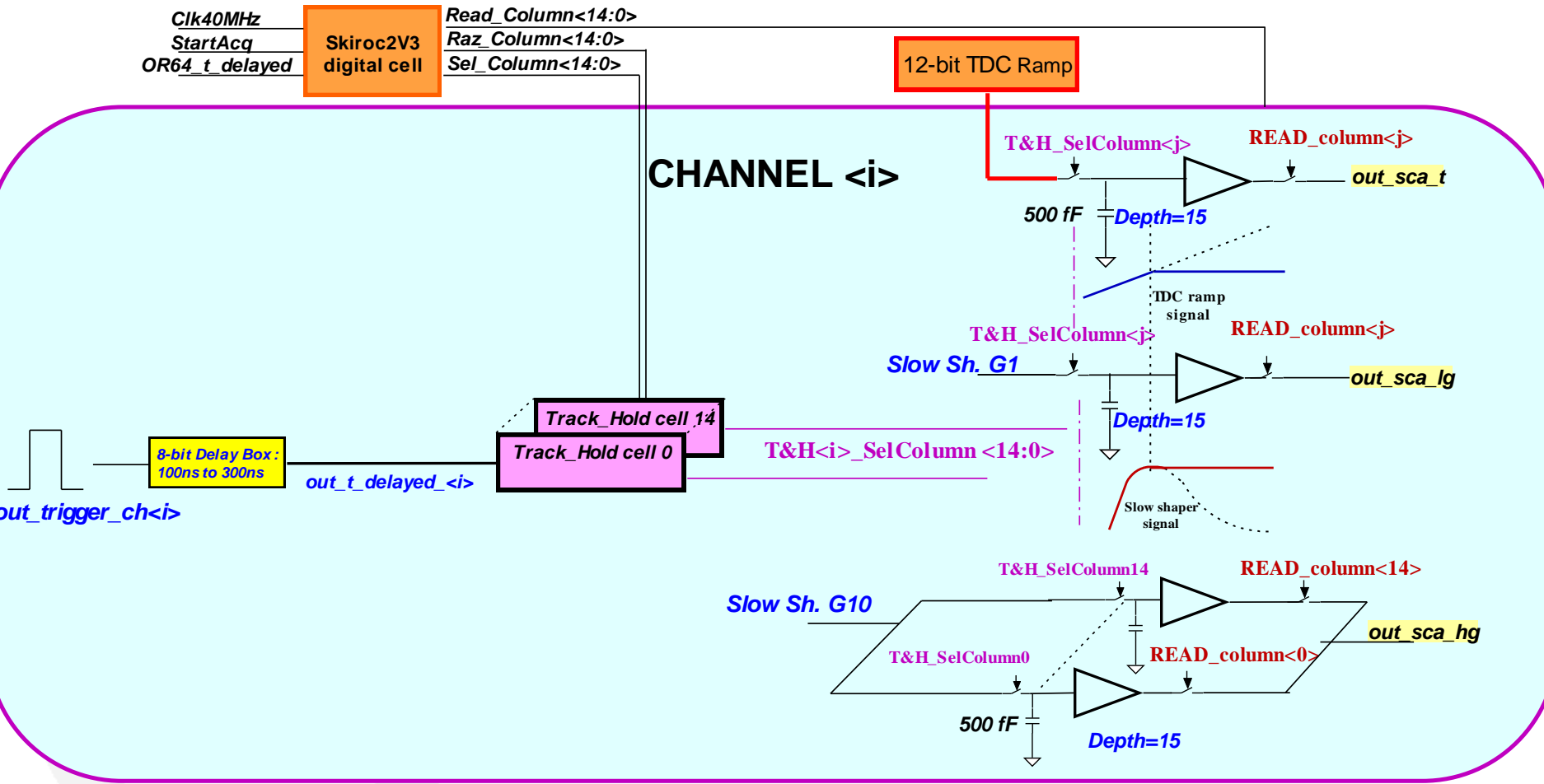
- SPIROC
- SKIROC
- HARDROC
- PARISROC



● New...

10-bit dual DAC – common to 64 channels

SCA detail



- Bandgap (reference voltage from Hardroc2b)
- Dynamic Range : from $\frac{1}{2}$ MIP up to 2500 MIP
 - With $C_{detector} = 20\text{pF}$
- Analogue channel muting capability (PA can be shut down)
 - Common 4-bit adjustable gain
 - PIN diode leakage current swallow capability (up to 10nA)
- 180ns shaping time Slow Shapers for charge measurement
 - Optimized S/N
 - Antisaturation system in Gain 10 Slow Shaper
- Analogue signal-to-noise ratio : 17 (1500 e^- noise for 1 MIP)
- 2-bit shaping time adjustable Fast Shaper (50 to 100ns)
 - Antisaturation system in Fast Shaper
- Analogue Memory depth : up to 15 events can be stored

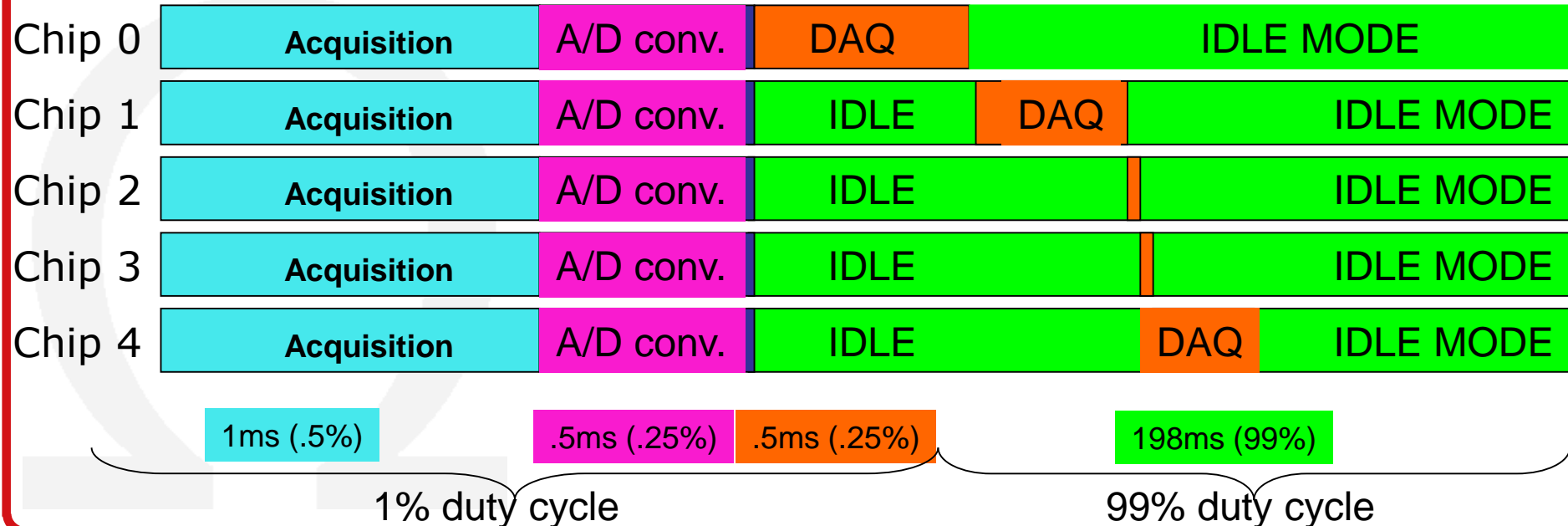
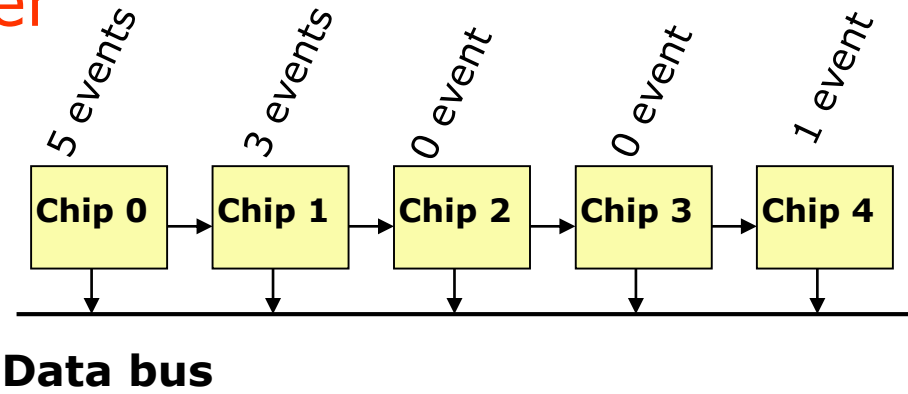
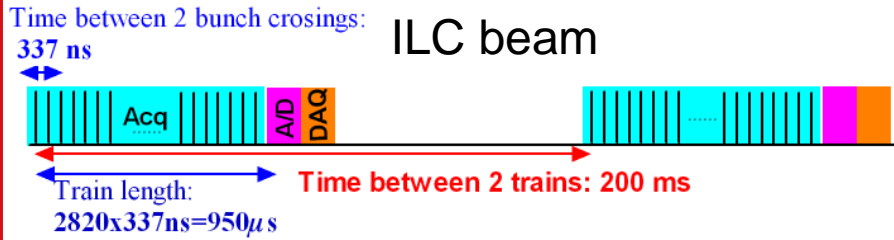
- 10-bit DAC for discriminator threshold
 - With improved 4-bit adjustment on each channel
- Trigger Discriminator for autotrigger on $\frac{1}{2}$ MIP
 - Better performance
 - Mask on each channel
- External Triggers now follow same path as internal ones
- 8-bit adjustable delay for peaking maximum signal
- (10 or 12-bit) ADC Discriminator from Parisroc
- Digitization of either time and charge or of both charges

- Common features with Hardroc & Spiroc (compatibility with any CALICE DAQ system)
 - Open Collector token-ring ReadOut
 - Multiplexed Slow Control & Probe
 - Redundancy on Data Out & Transmit On signal lines
 - 2 switchable StartReadOut Inputs & EndReadOut Outputs :
 - to prevent chip failure
- Improved Slow Control/Probe
 - Default value for Slow Control (already done in Hardroc2B & Easiroc)
- Very Complex Digital Part (~10% of the Die)
 - Manage Acquisition, Conversion, 15 SCA control, RAM, I/Os...
 - new layout (easier interconnections with analogue part)
 - minor modifications concerning some timings (allowing more latency to analogue signal during conversion)

- 1 ns TDC capability
- TDC facility to operate in ILC mode or in test beam mode
 - 200ns for ILC / 5 μ s for test beam
- Power consumption optimized
 - Power-On-Digital included for LVDS receivers
 - Each stage can be totally disabled
- Analogue and Digital probe system
- Tri-state multiplexed Analogue output
- Test purpose : few pads required, single ended 40MHz needed, default slow control configuration, "only" Acquisition/Conversion/ReadOut Command necessary

Read Out: token ring

- Readout architecture common to all calorimeters
- Minimize data lines & power



SKIROC2 Analogue Simulations

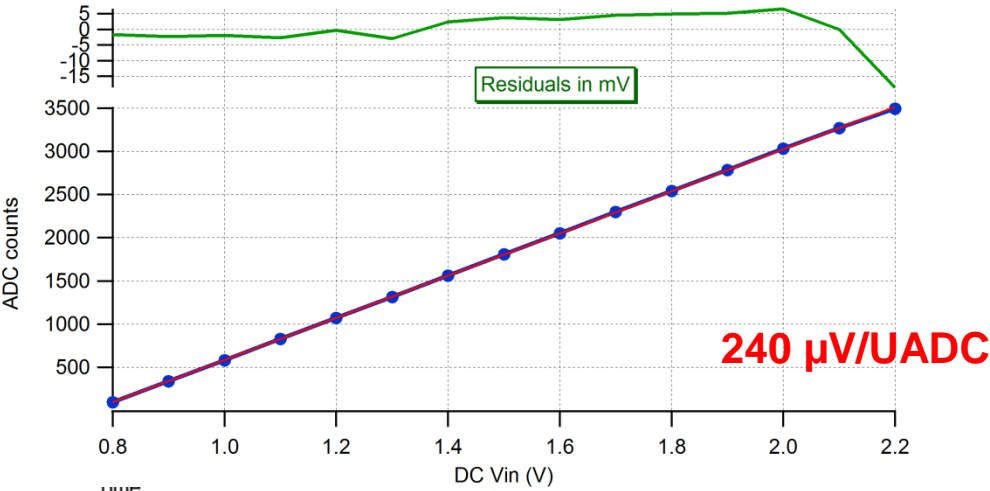


Q inj	Out_PA	Out_SS1	Out_SS10
1 MIP	639.6 μ V	623.7 μ V	6.65 mV
10	6.32 mV	6.236mV	66.47 mV
100	63.2 mV	62.33 mV	664.1 mV
200	126.4mV	124.7 mV	1317 mV
500	315.9 mV	311.5 mV	Saturation to 1.5V
1000	631.6 mV	622.4 mV	
2000	1252 mV	1234 mV	
2500	1465 mV	1437 mV	

SKIROC2 ADC Test : Board 1



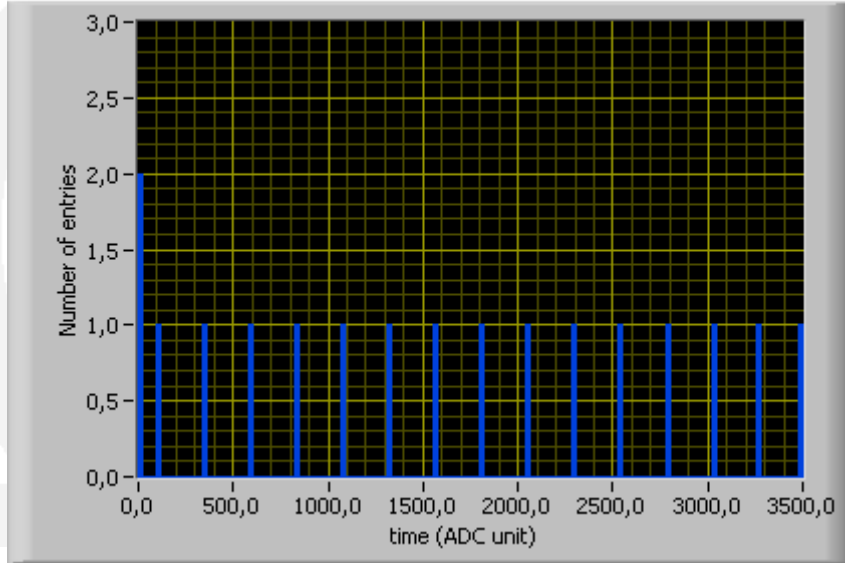
Using DC voltage as input and manual step-by-step acquisition system



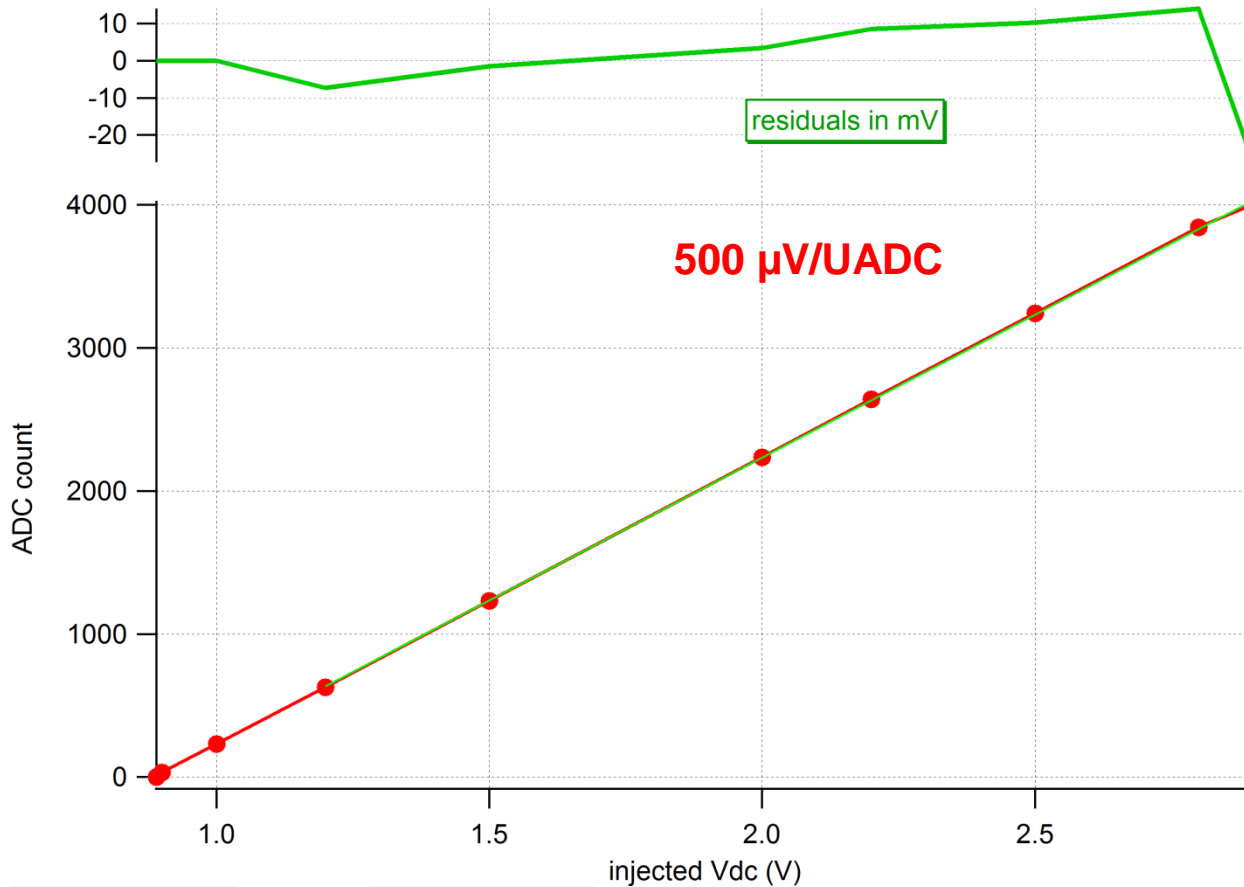
V DC	ADC count
0,6	5
0,7	5
0,8	99
0,9	342
1	586
1,1	829
1,2	1075
1,3	1316
1,4	1565
1,5	1810
1,6	2053
1,7	2298
1,8	2542
1,9	2786
2	3031
2,1	3268
2,2	3493
2,3	1

Underflow

Overflow



SKIROC2 ADC Test : Board 2

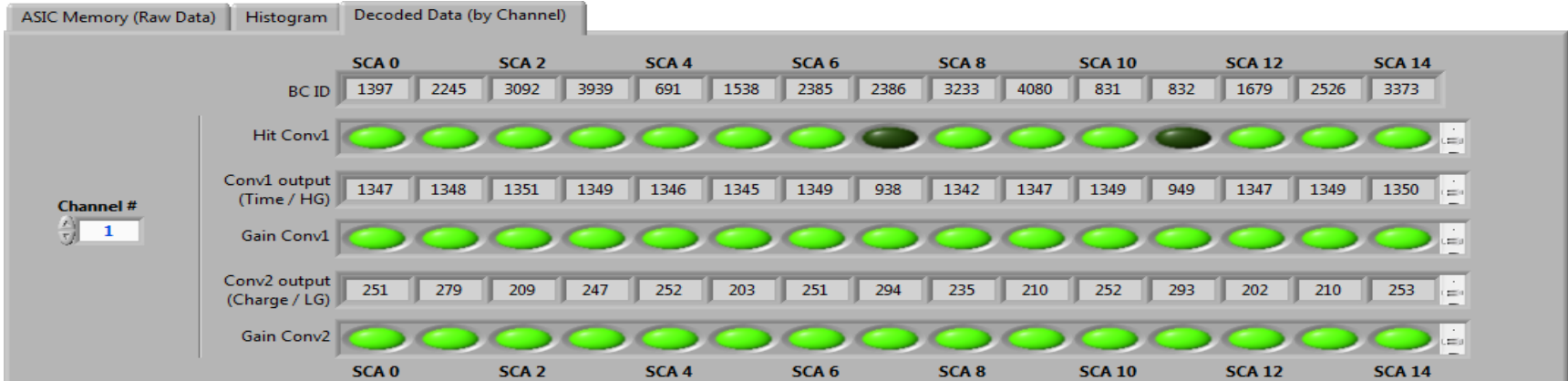


V DC	ADC count
0,89	10
0,9	36
1	235
1,2	630
1,5	1234
2	2236
2.2	2640
2,5	3240
2.8	3842
2.9	4000

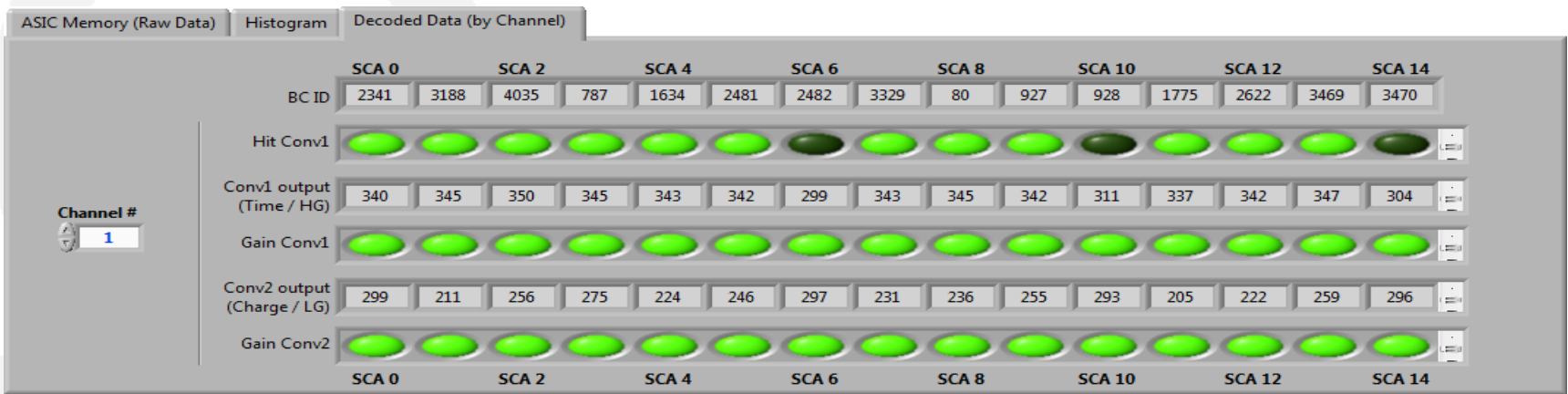
SKIROC2 : Digital Data (Board 2)



Input signal: 3.8V@20dB in 10 pF=1000 Mip
 1350 UADC ie 1V+674 mV= 1.674 V Scope measurement 1.580 V



Input signal: 3.8V@40dB in 10 pF=100 Mip
 340 UADC ie about 1.1V Scope measurement: 1.06V



**Devices bonded inside cavities, with
total thickness below 1.2 mm**

**No external
components**

Bonding @CERN