Status update of electronics

Investigation of the channel-wise adjustable autotrigger threshold in SPIROC2b and first power pulsing tests

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Motivation

SPIROC2b is a specific chip designed for ILC operation:

- Dual gain setup per channel
- Internal ADC
- **Autotrigger Mode**
- **Power pulsing**

→ Input DAC for channel-wise adjustment (36 channels)

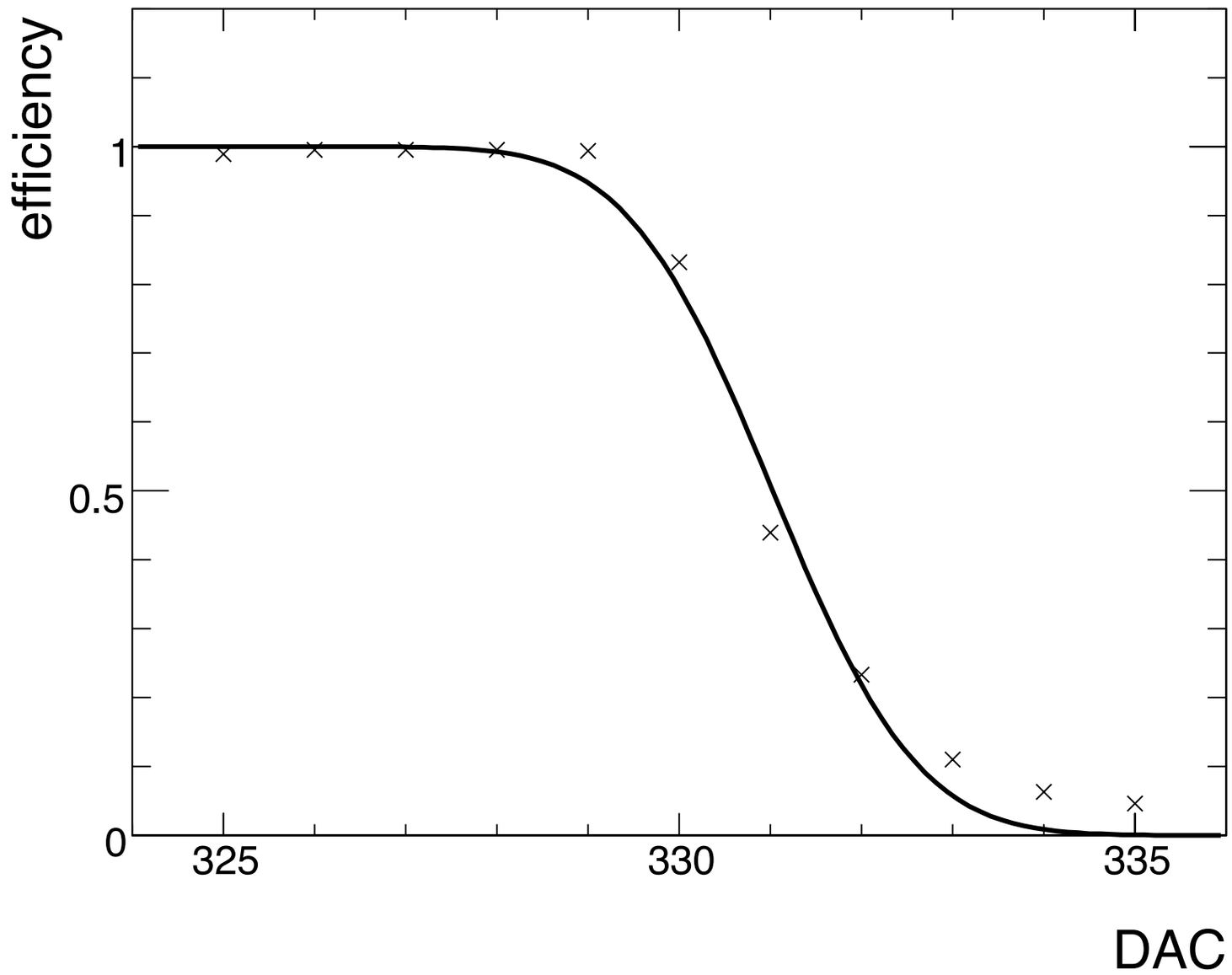
channel-wise adjustment means choose a global threshold and do fine tuning (4 bit) for each channel!

questions:

- Dynamic range of channel-wise DAC settings ?
- Interdependence of channel-wise threshold settings?

S-curve

- inject a well defined charge into one channel
- vary the DAC setting of the global threshold to scan the threshold
- fitted with errorfunction
- 50 % value is defined as the threshold position

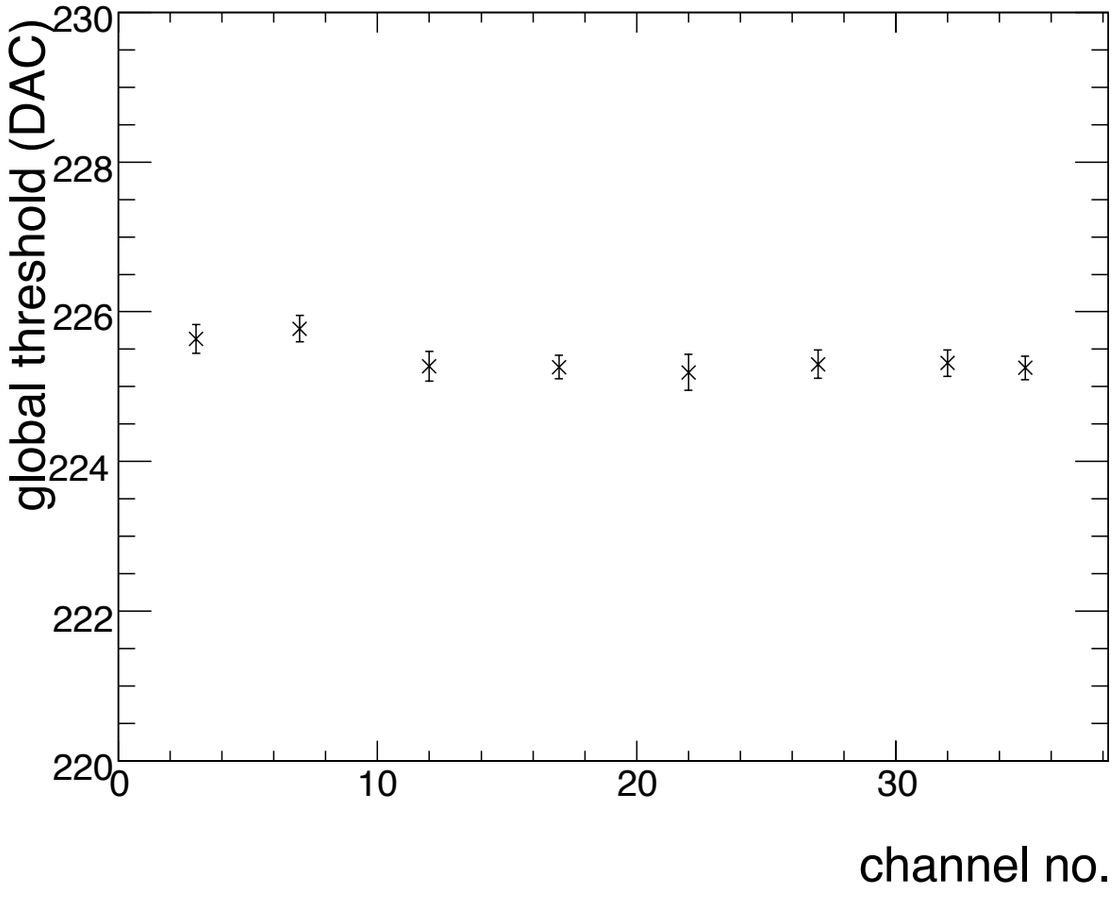


Threshold dependence on neighbouring channels

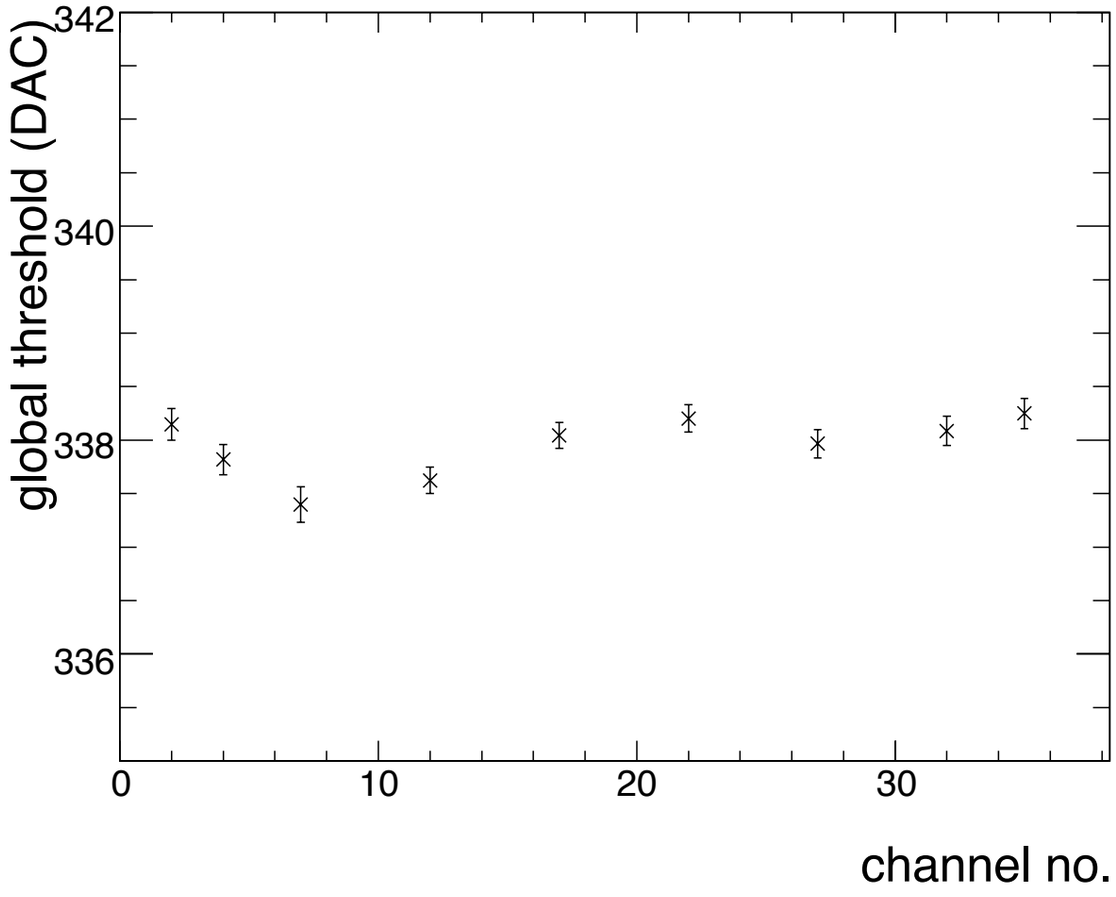
Does the channel-wise adjustment influence neighbouring channels?

> inject a charge into one channel and use the full voltage offset of the channel-wise DAC setting of neighbouring channels

channel 2

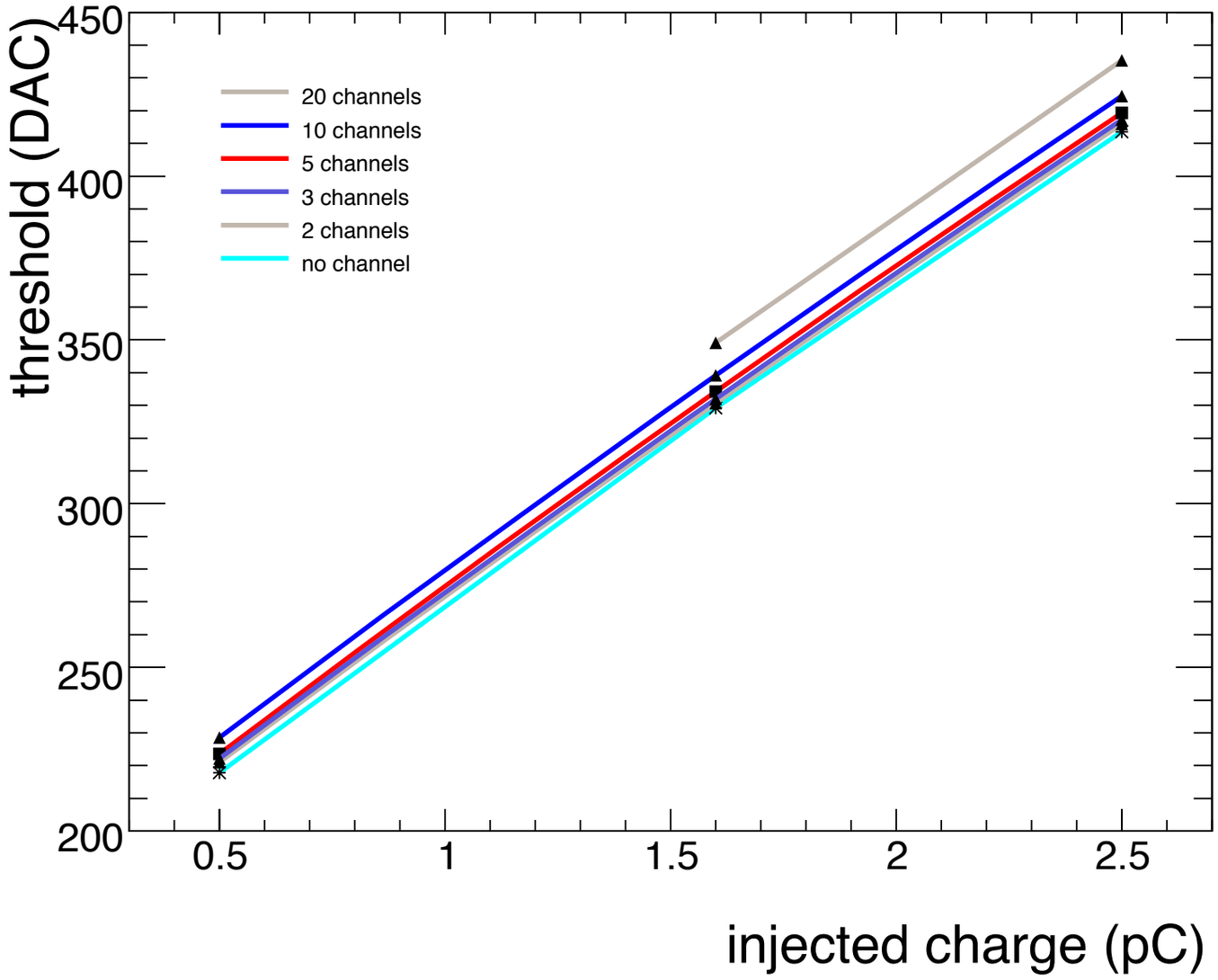


channel 3



Global threshold offset

- inject charge into one channel
- set a different number of channels up to the full range of the 4 bit DACs and measured threshold dependence for different charges
- shift of the global threshold caused by the number of active channel is constant or independent of the injected charge
- 1 MIP equates 1.6 pC at a gain factor of $1 \cdot 10^6$



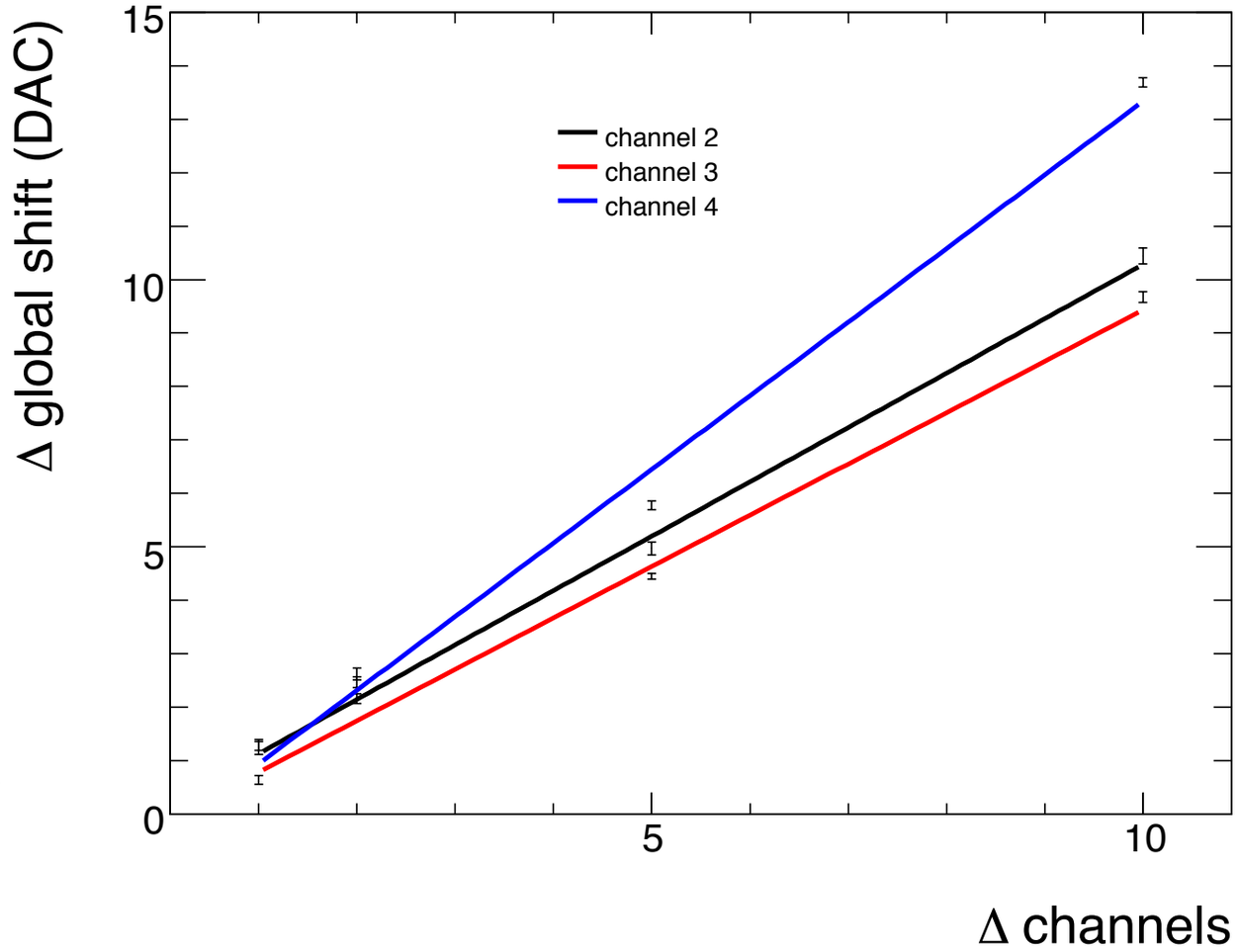
Global threshold shift

> shift of the threshold as a function of the number of channels

> for Δ 10 channels the shift of the threshold is around 13 DAC tics

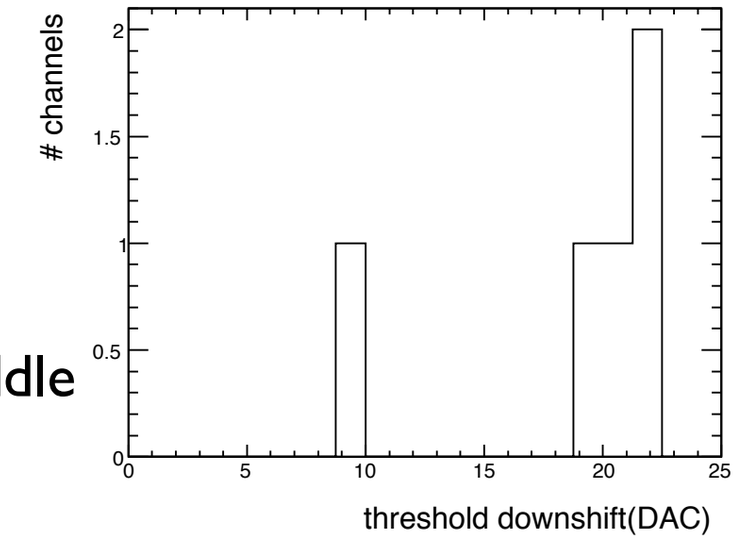
> shift of global threshold due to individual channel DACs is negligible, if only one neighbouring channel is active
⇒ important for dynamic range measurement

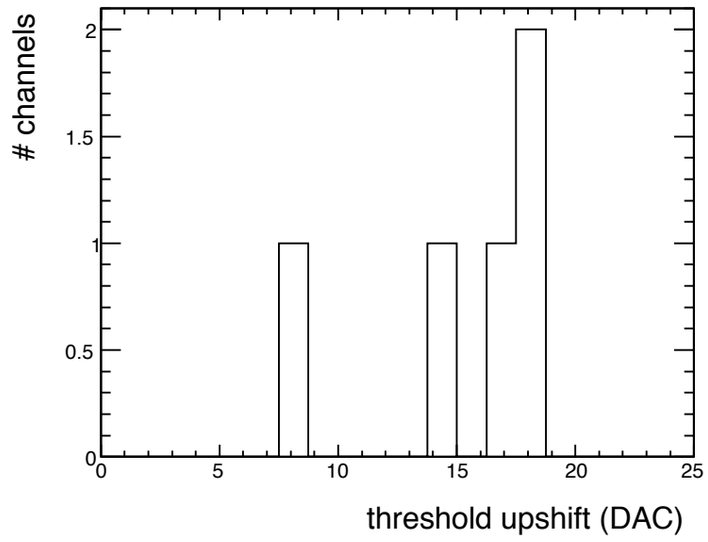
> do the global threshold shifts cancel for many channels that have a finetuned threshold?

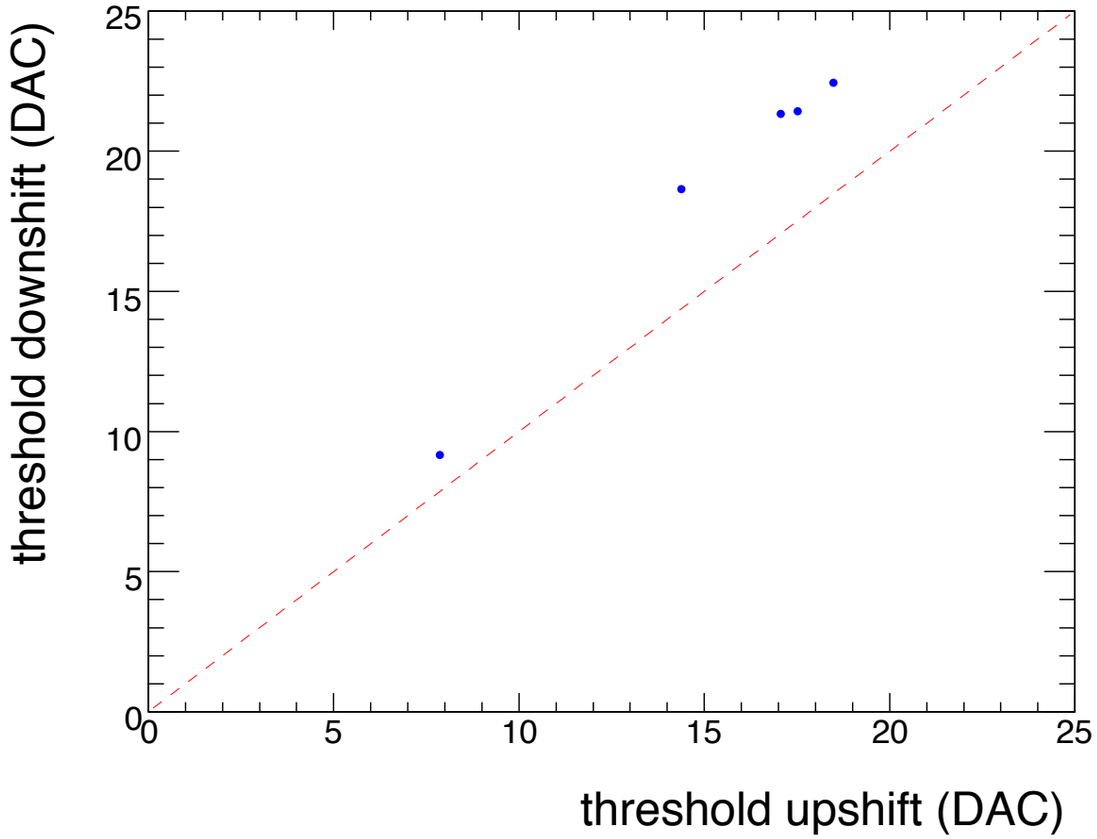


Dynamic range of individual channel DACs

- for detector operation the autotrigger mode must be capable to do fine tuning in both directions
- choose a default setup in the middle of the 4 bit dynamic range
- determine the dynamic range
- channel-wise adjustment not symmetric
- to use a default setup ⇒ regard the shift
- total dynamic range is around 40 DAC tics (≈ 0.4 pC ≈ 1/4 MIP)







Summary

autotrigger

> global threshold is not independent on channel-wise adjustment

> for Δ 10 channels the shift of the threshold is maximally around 13 DAC tics

> the dynamic range for the 4 bit DACs is around 1/4 MIP

> dynamic range depends on the offset direction (asymmetric)

> asymmetry has to be regarded for default setup

> use this information at the testbeam

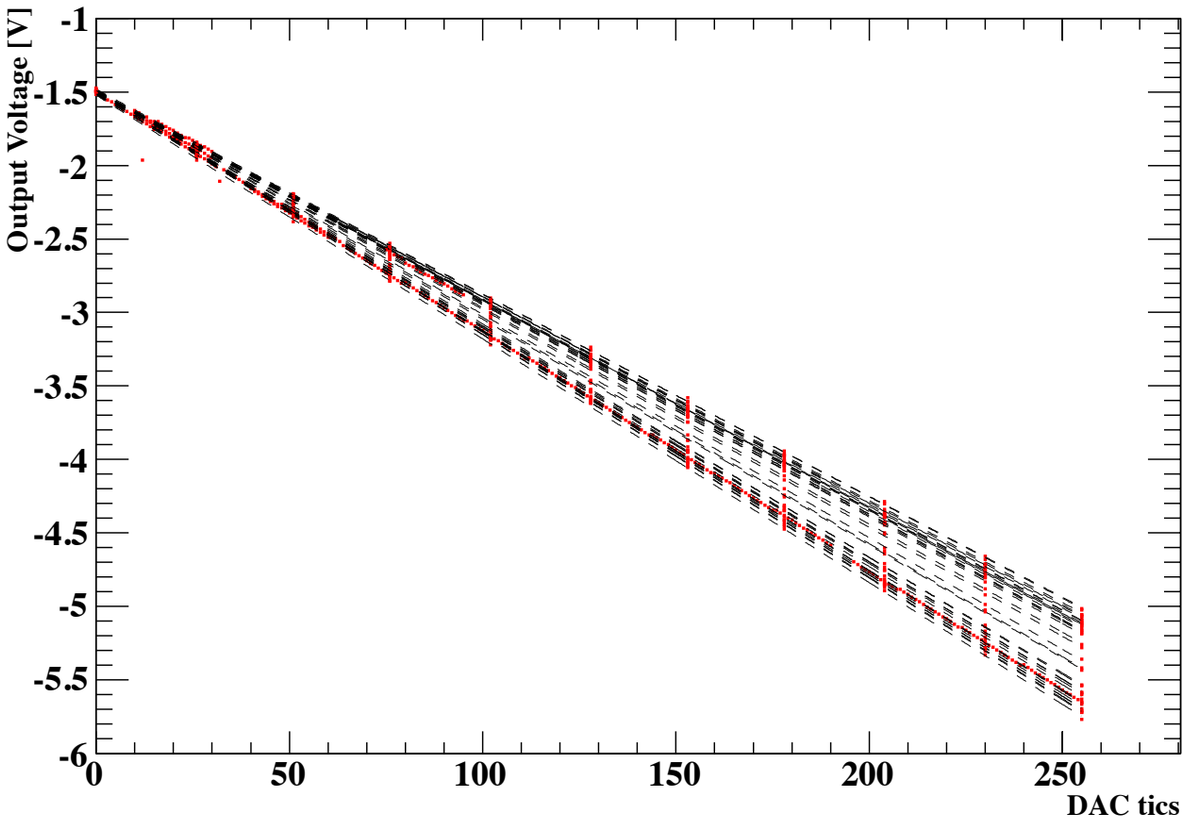
> optimize the MIP efficiency

> it is unclear if the dynamic range is capable to compensate the fluctuations of the threshold from channel to channel (testbeam could give us the answer)

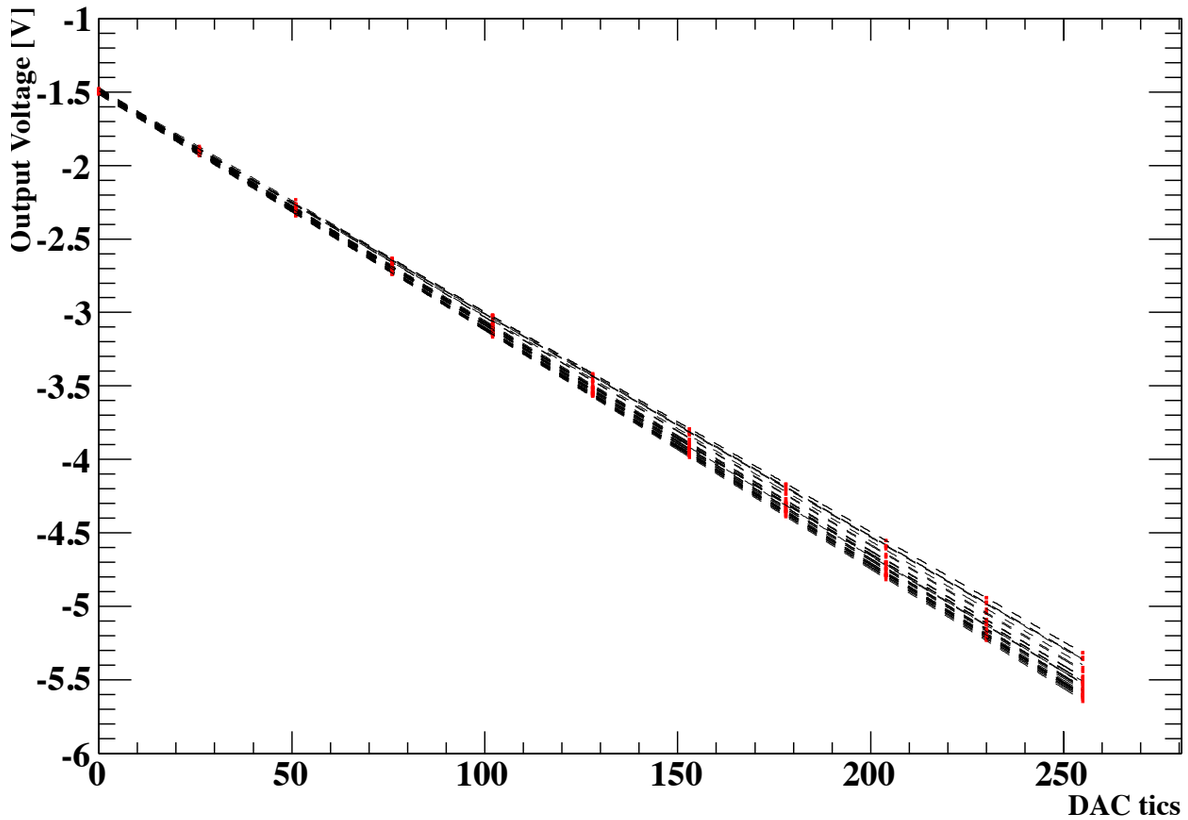
Input DACs

- Input DAC to tune bias voltage for every SiPM (we assembled 70 under HBU2)
- in principle linear behaviour
- different slope for every channel
- spread prevents the use of one general average value

  --> this makes a mass assembly of SiPMs more difficult



1.SPIROC

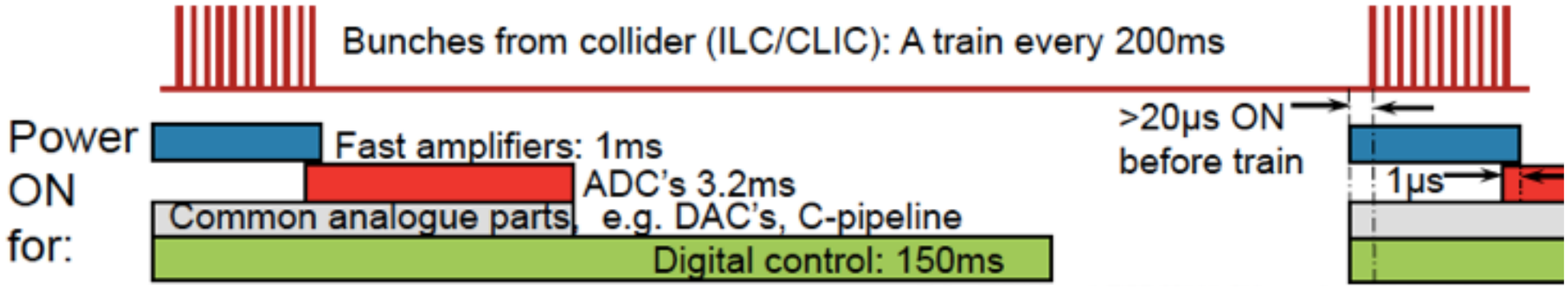


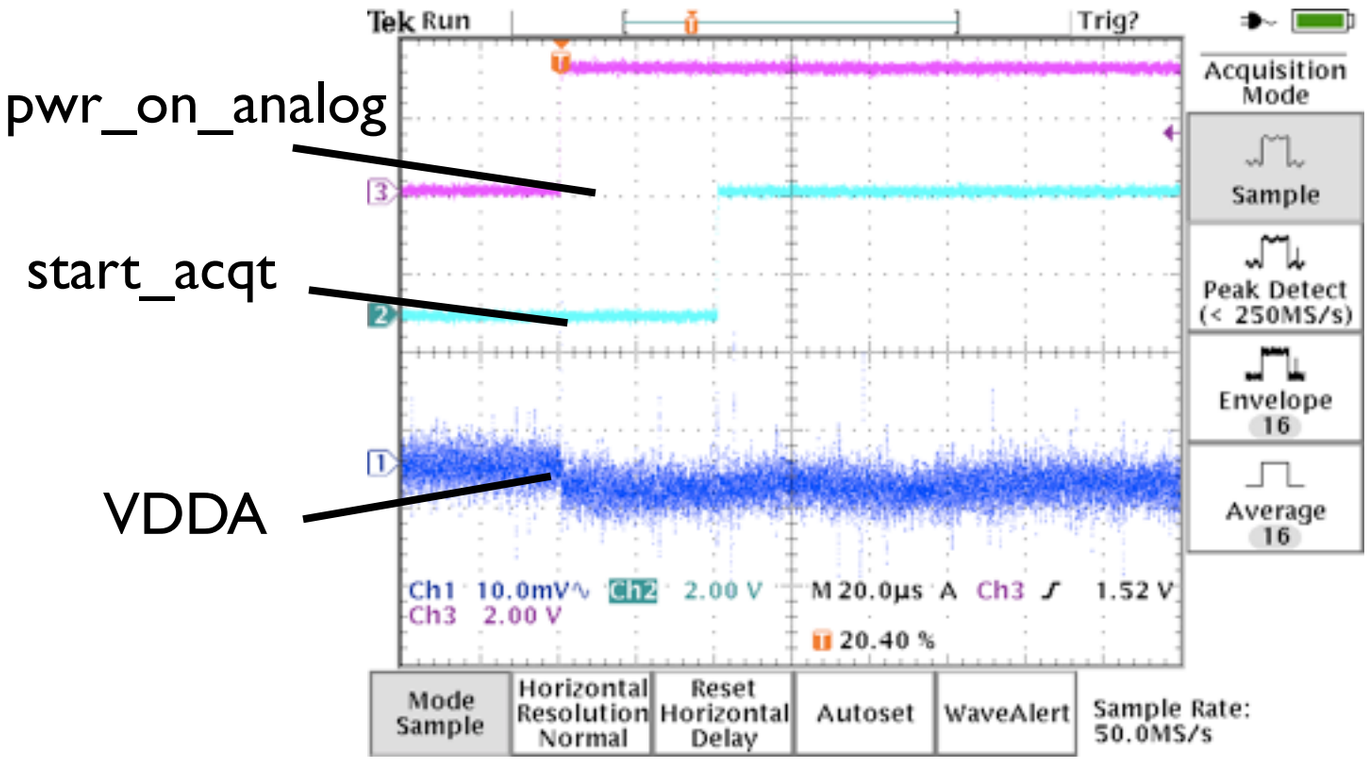
2.SPIROC

power pulsing

Reminder

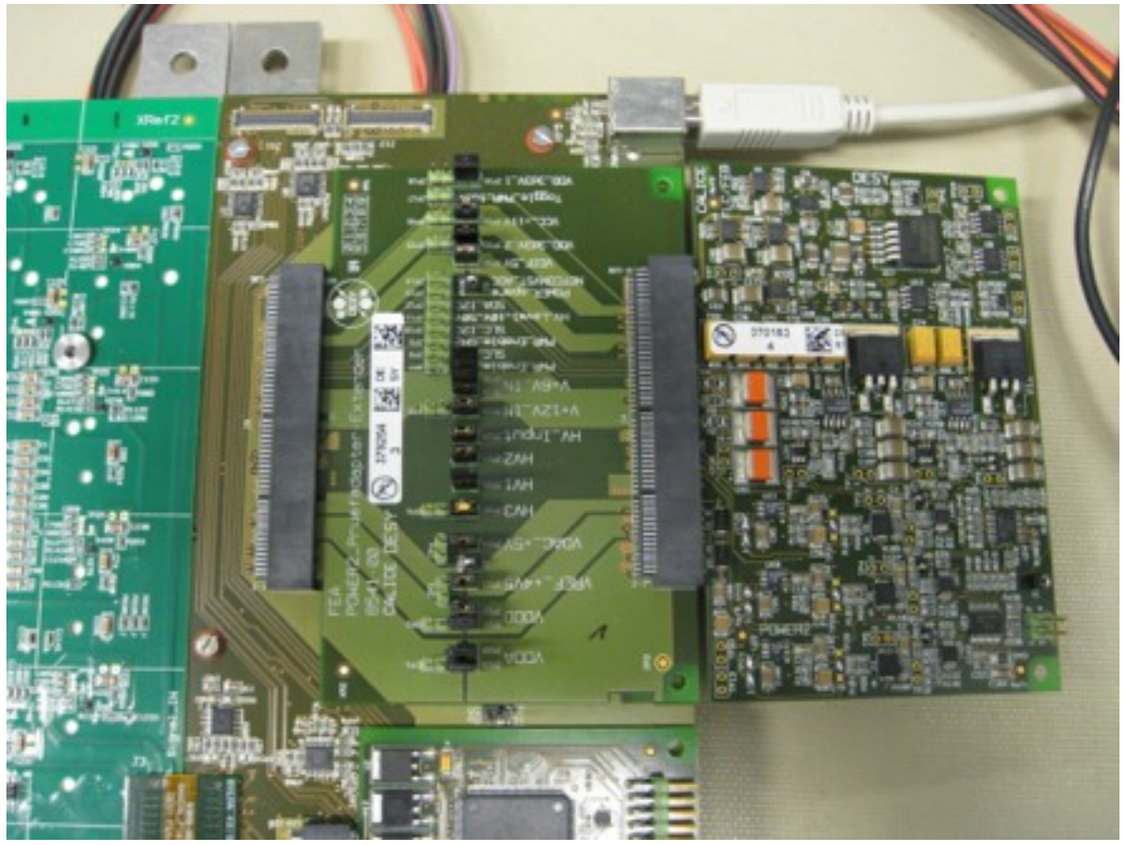
- 199 ms between train bunches
- switch off components to reduze heat development





- some trouble with first measurements
- after removing block capacitors of bias points it looks promising
- off-state currents at SPIROC2b seem to be better than SPIROC2
- on-state currents nearly the same
- data acquisition crashed sometimes - still unclear

Summary & outlook



power pulsing

- power pulsing under test at DESY, so far functioning
  - signals in the time chain look quite good
  - currents in off-state improved
- extender just arrived last week

to do

- further test to determine current settings
- investigation why data acquisition crashed sometimes
- determine time behaviour of the signals and find the best configuration for lowest power consumption
- assembly of multi HBU2 setup to analyze time effects and functionality