KNU IPBPM Electronics

13TH ATF2 PROJECT MEETING

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CONTENTS

- Simplified diagram
- Result of the test
- Further plan

SIMPLIFIED SCHEMATIC



Simplified schematic of the IP-BPM signal processing electronics.





SIMPLIFIED SCHEMATIC



Simplified schematic of the IP-BPM signal processing electronics.

- Conversion Gain 54dB
- Noise Figure < 1.8dB
- linear Range -57dB ~ -96dB



신호 발생기 Phase Control 8 - Detection LNA Power **LNA** BPF Phase shifter divider Atten. Atten. PA 신호 발생기 Pawer divider 오실로스코프 LPF BW : 40MHz OPAMP æ RF 🔸 IF1(I) LNA Π ≈ Hybrid - IF1(Q) DA Ring BPF Δ Coupler Coupler Coupler AB Mixer LNA Detector 24.2ns < 40ns Ŀ (FONT requirement) P1:freq(C1) Measure P2:freq(C2) P3:phase(F1,F2) P4:ampl(C1) P5:ampl(C2) value 23.45 mV 30.57 mV ----Δ status ACI Timebase 0 ns Trigger 20.0 mV/din 0.00 mV ofs 20.0 mV/di 0.00 mV of: 52.0 mV 24.2ns X1= -3.4 ns ΔX= -24.2 ns X2= -27.6 ns 1/ΔX= -41.3 MHz

ELECTRONICS PERFORMANCE



V_out = 3.54uV

Linearity range \rightarrow -96dBm(3.54uV) ~ -57dBm(316uV)

- For the New Low-Q IP-BPM: 0.88nm ~ 78.56nm
- For the Old Low-Q IP-BPM: 7nm ~ 632nm

Therefore, we expect our electronics can be detected 2nm beam offset.





FURTHER PLAN

- Two electronics Ver.2
 - will be tested in Jan.
- \rightarrow Modification and Fabrication Four more electronics
- \rightarrow Then three BPM test

More details will be presented by SiWon Jang.

THANK YOU FOR ATTENTION