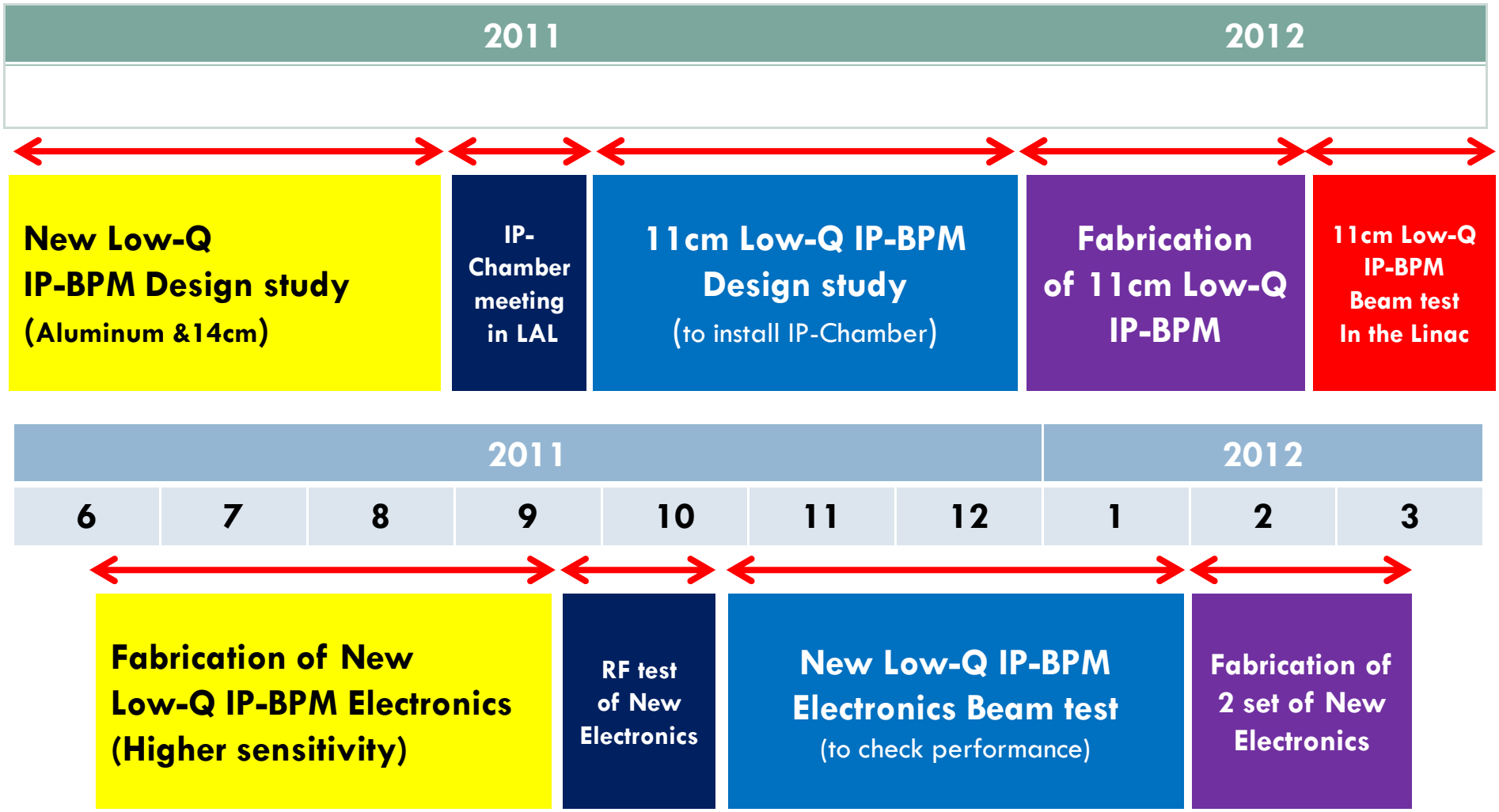
LOW-Q IP-BPM DESIGN & STUDY PLAN

Siwon Jang (KNU)

Contents

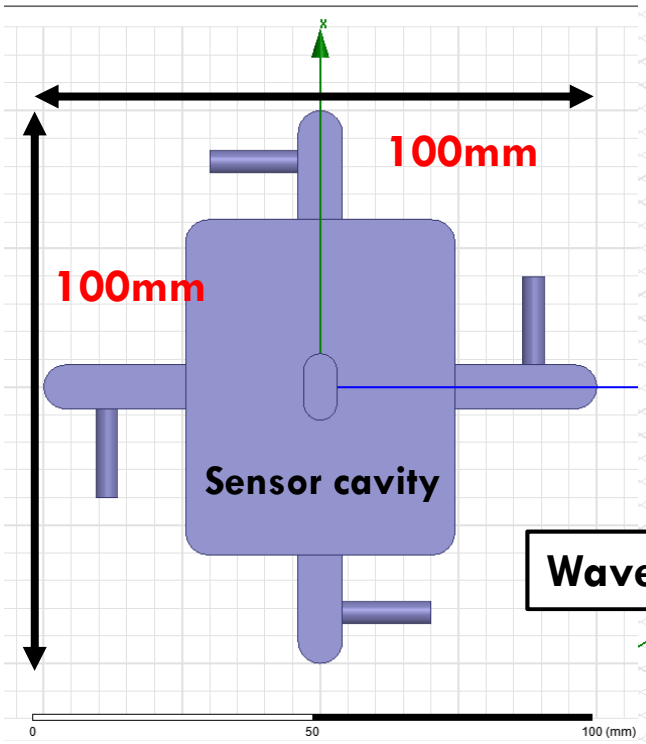
- Design study of Low-Q IP-BPM
  - Low-Q IP-BPM Progress
  - 11cm Low-Q IP-BPM Sensor Cavity Design
  - Result of HFSS simulation for 11cm Low-Q IP-BPM
  - New Reference Cavity Design
- Study plan of 2012
  - 2012 Low-Q IP-BPM Test Plan

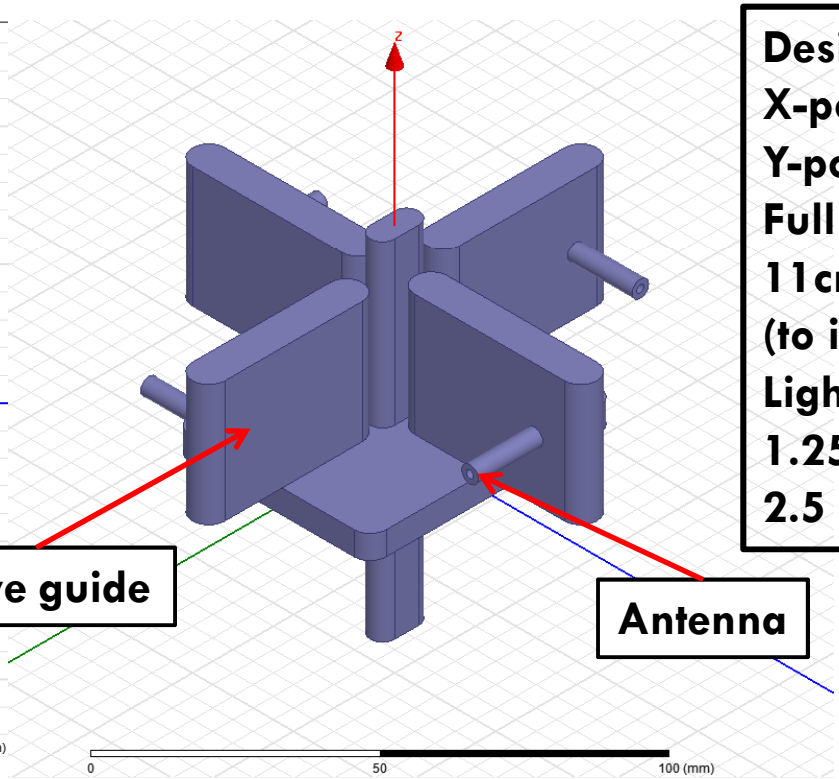
Low-Q IP-BPM Progress



11cm Low-Q IP-BPM design

- 11cm Low-Q IP-BPM drawings of HFSS

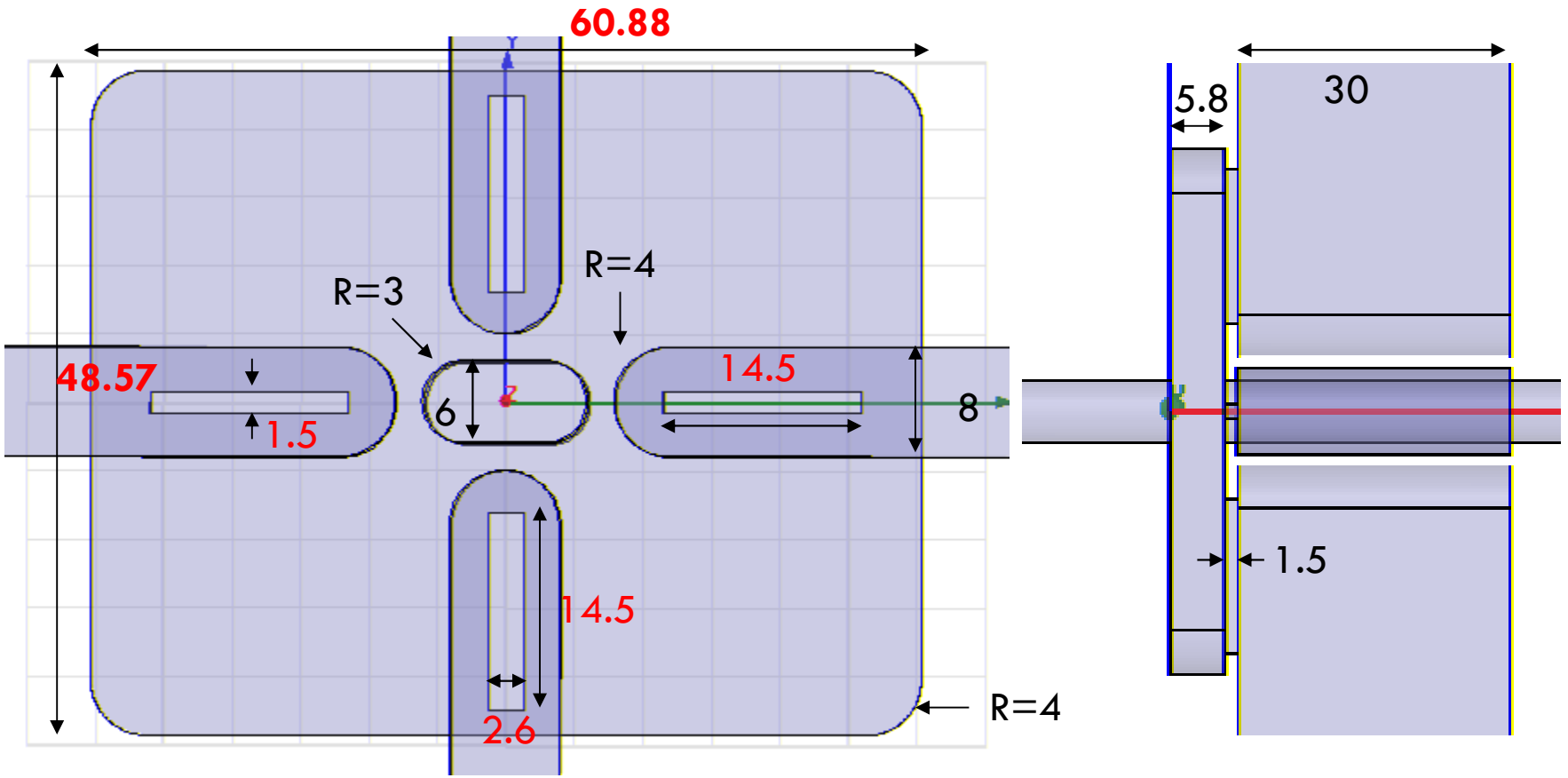




Designed frequency
X-port: 5.712 GHz
Y-port: 6.426 GHz
Full size :
11cmx11cm
(to install IP-Chamber)
Light weight:
1.25 kg (Single)
2.5 kg (Double)

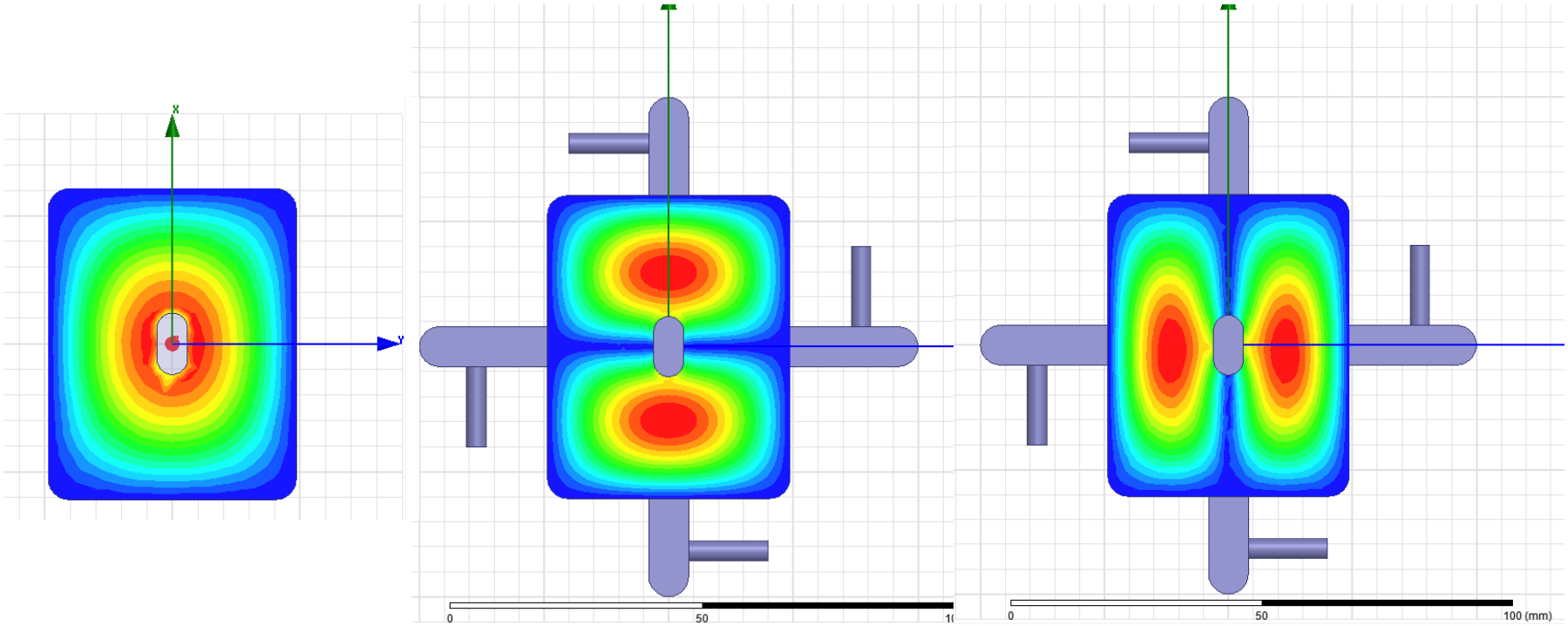
11cm Low-Q IP-BPM sensor cavity design

- **Cavity dimensions for HFSS simulation**



11cm Low-Q IP-BPM sensor cavity design

- **Electric field mapping of HFSS simulation**



Mono-pole mode :3.9808 GHz

X-dipole mode :5.7123 GHz

Y-dipole mode : 6.4255 GHz

Results of HFSS simulation

11cm AL ver.

Port	f_0 (GHz)	β	Q_0	Q_{ext}	Q_L	τ (ns)
X-port	5.7123	4.992	4026.58	806.67	672.04	18.72
Y-port	6.4255	5.684	4014.13	706.16	600.51	14.87

14cm AL ver.

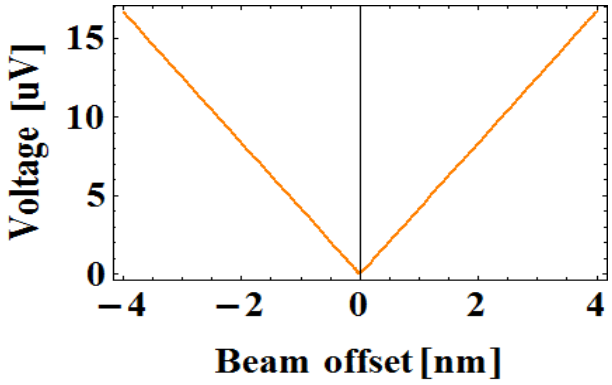
Port	f_0 (GHz)	β	Q_0	Q_{ext}	Q_L	τ (ns)
X-port	5.7050	4.48	4005.53	894.80	731.41	20.40
Y-port	6.4217	6.17	3903.95	632.36	544.21	13.49

Results of HFSS simulation

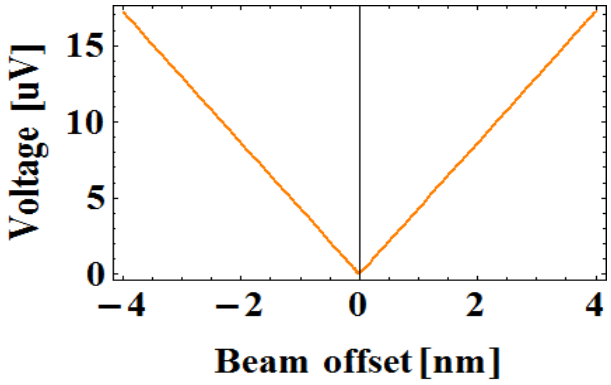
- **Output signal for Y-port**

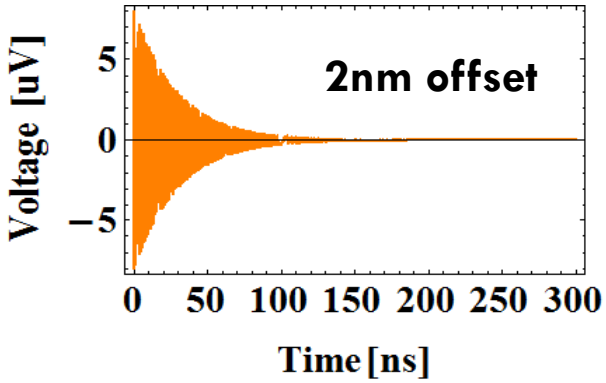
$$V_{out,0} = \frac{q\omega}{2}\sqrt{\frac{Z}{Q_{ext}}(R/Q)}\exp(-\frac{\omega^2\sigma_z^2}{2c^2}) \qquad V_{out} = V_{out,0}\exp(-\frac{t}{2\tau})\sin(\omega t + \phi)$$

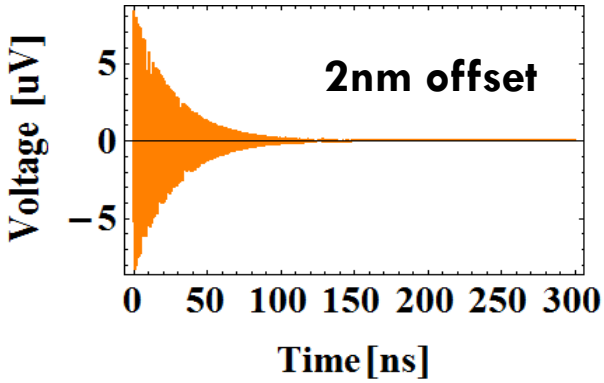
11cm AL ver.



14cm AL ver.





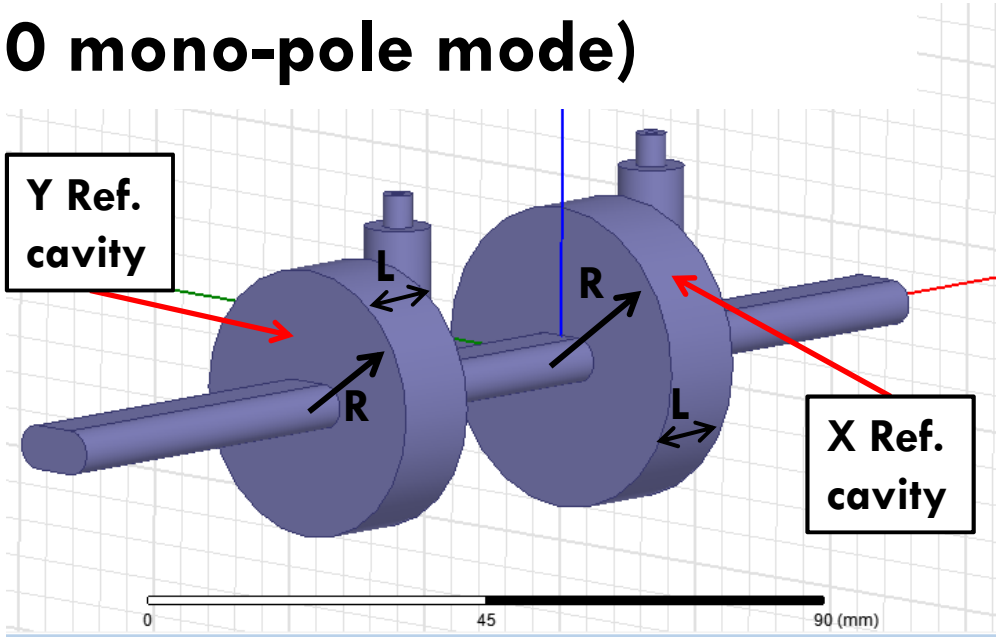


Parameter	Value	Unit
q (charge)	~ 1.6	nC
Beam energy	1.3	GeV
Bunch length	8	mm

New Reference cavity (X & Y)

- X-port & Y-port (TM010 mono-pole mode)

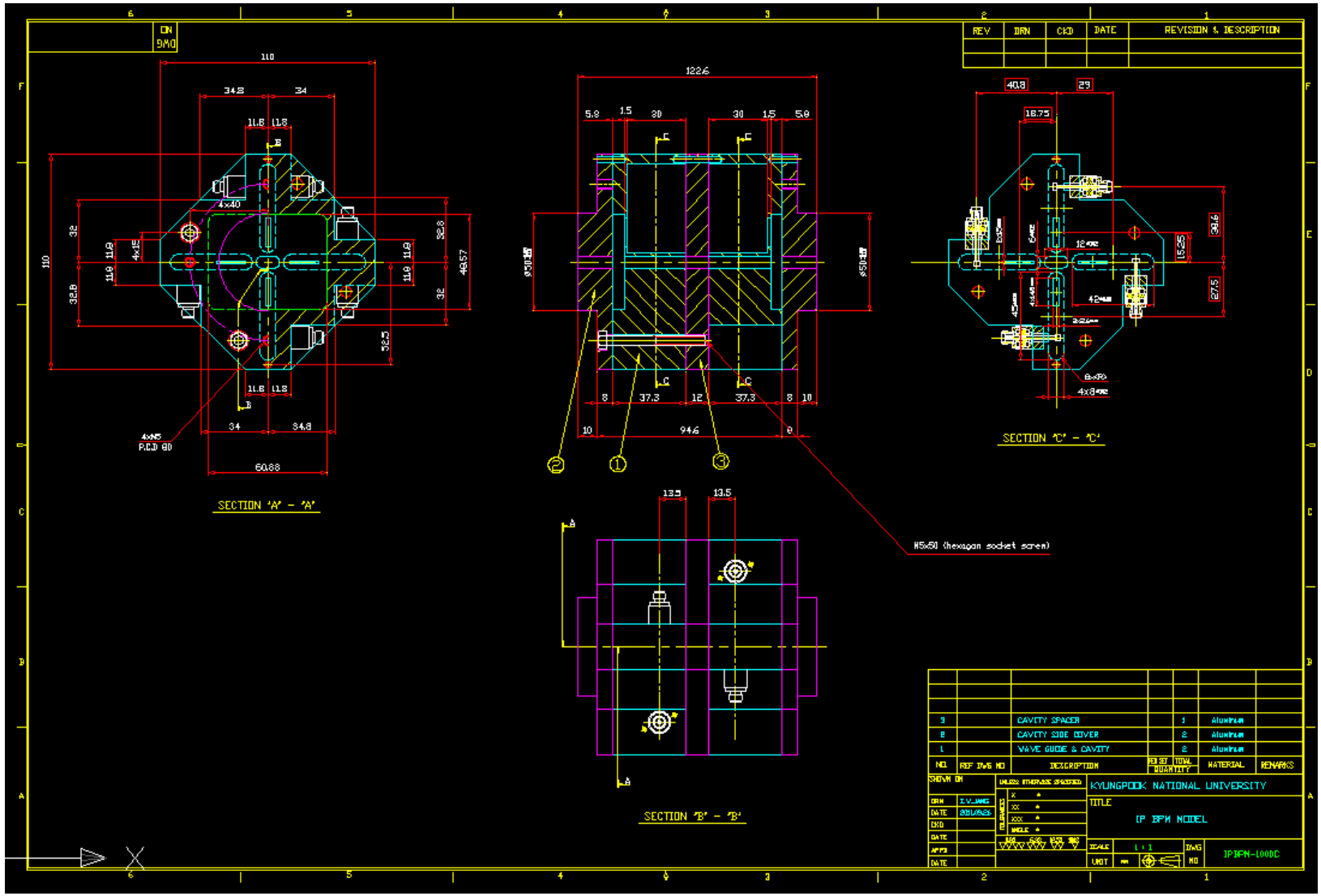
	f_0 (GHz)	R (mm)	Length
X-port	5.7117	20.52	12 mm
Y-port	6.4235	18.28	12 mm



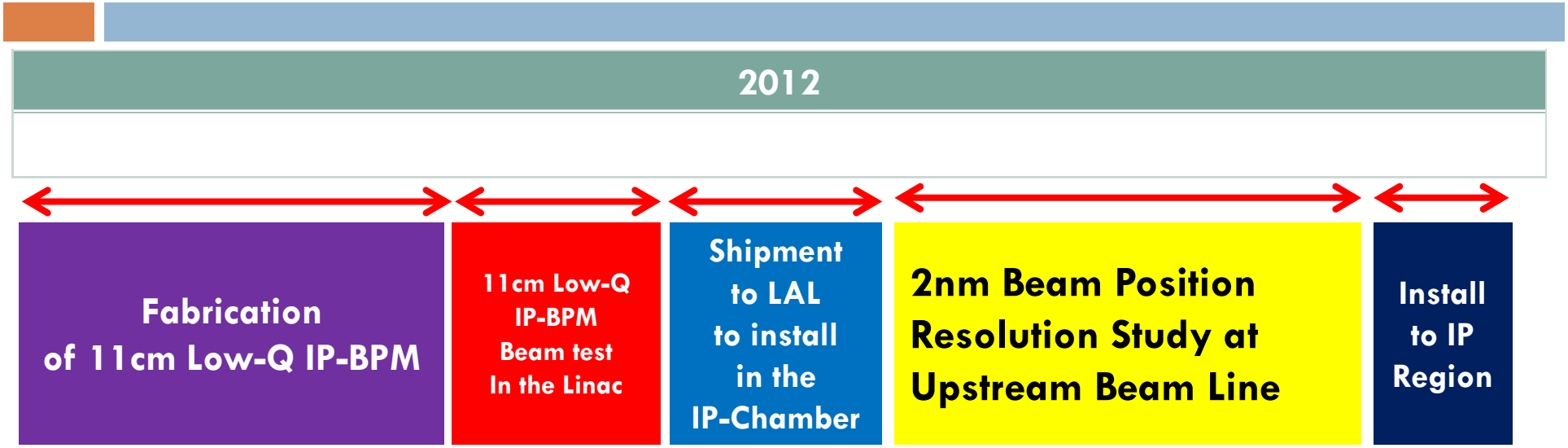
Reference Cavity

Port	f_0 (GHz)	β	Q_0	Q_{ext}	Q_L	τ (ns)
X-port	5.7115	0.01051	1177.86	112070	1165.61	32.48
Y-port	6.4235	0.01150	1181.34	102718	1167.91	28.94

Drawings of Low-Q IP BPM



Study Plan of 2012

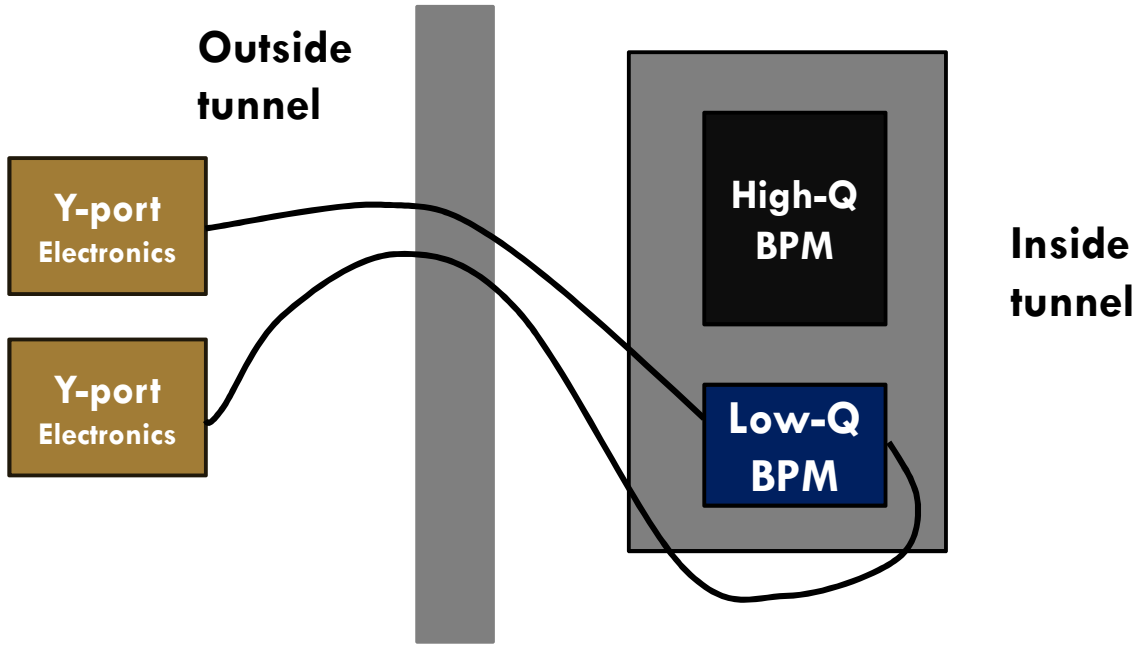


Main Test List for the Low-Q IP-BPM @ 2012

1. Y-port electronics test (Jan.)
2. Three IP-BPM beam test at end of linac with chamber (Mar.)
3. 2nm beam position resolution full study at upstream beam line with IP-chamber (May ~ June)
4. IP-region beam test (Sep. ~) (is undecided)

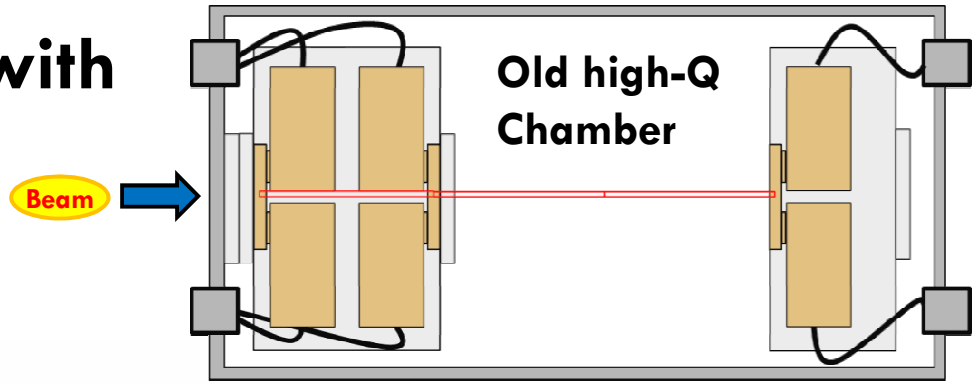
Y-port electronics test (Jan.)

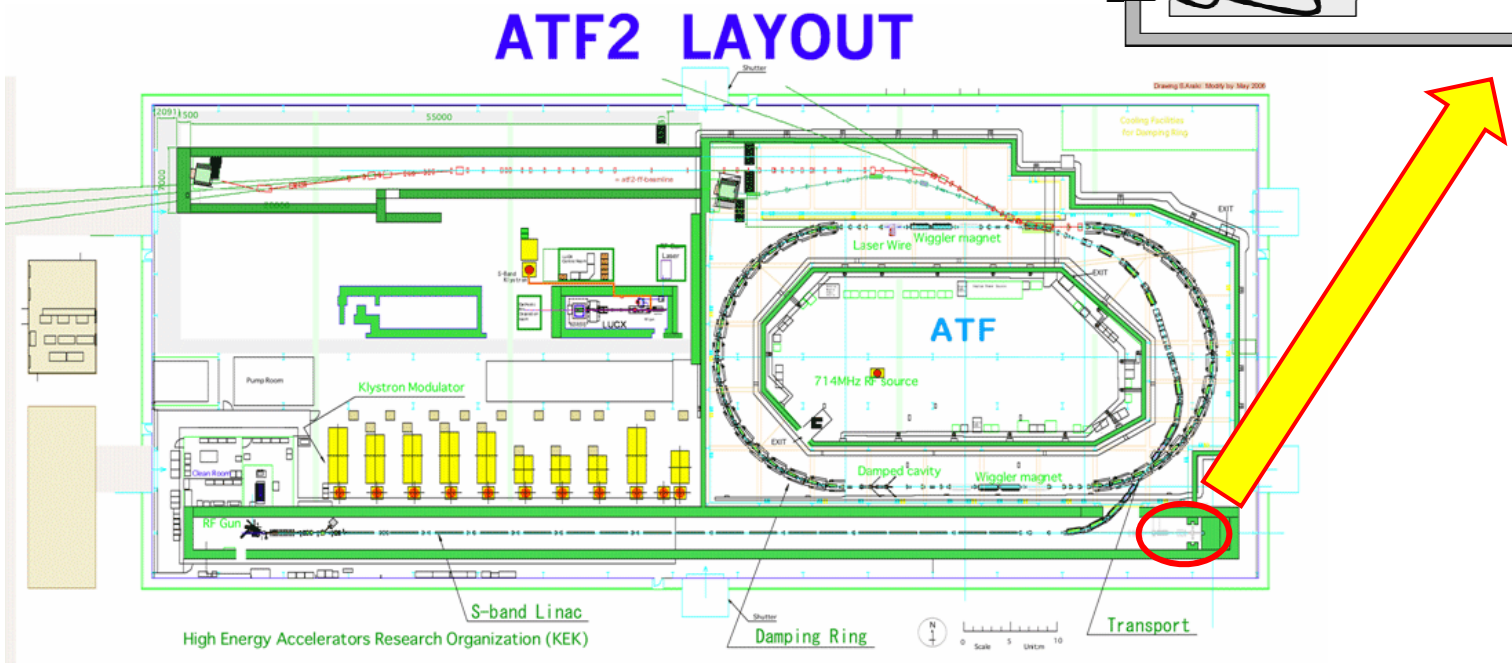
- We will test two Y-port electronics at the same time by using one Low-Q IP-BPM to check same performance of both electronics.
- Beam test scheme



Three IP-BPM beam test at end of linac with chamber (Mar.)

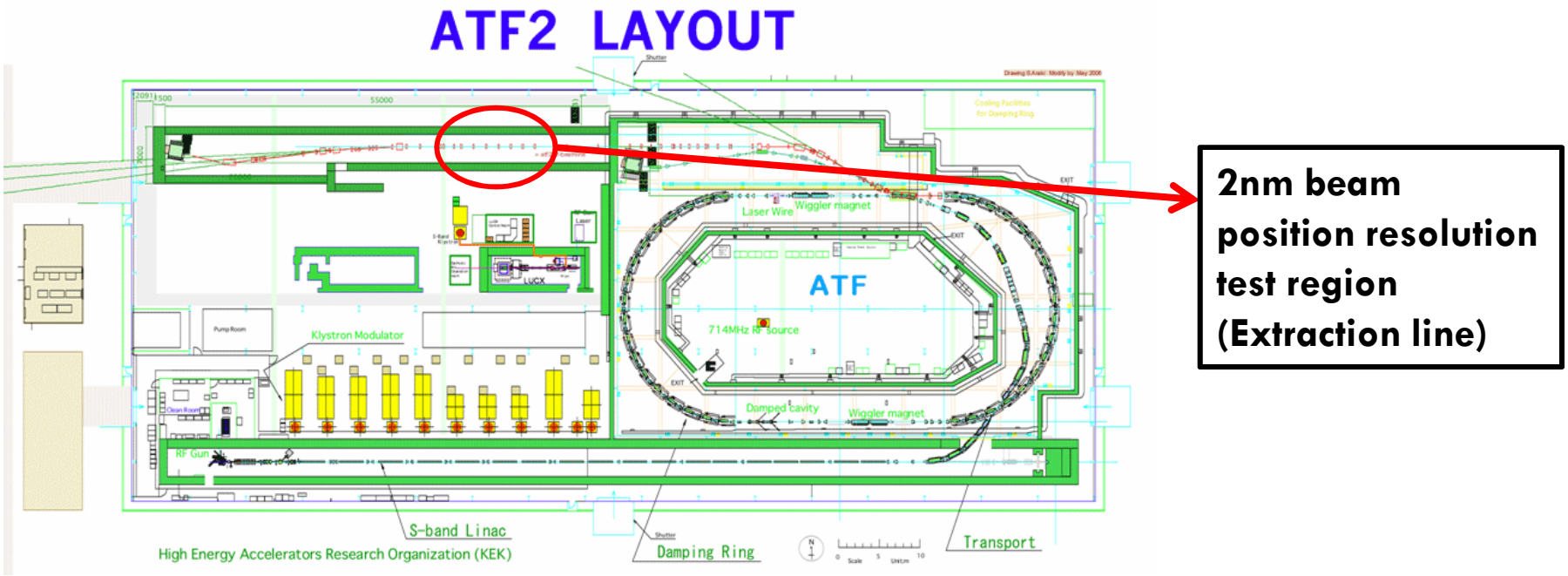
- New IP-BPMs performance will test at end of linac with old high-Q chamber.





2nm beam position resolution study (May ~ June)

- 2nm beam position resolution study will perform at extraction beam line with IP-chamber (May ~ June)
- The test scheme is not fixed. It need discuss.
  - How to test by using the IP-Chamber?



Summary

- 11cm Low-Q IP-BPM design study was done, well.
- In the January, New electronics performance test will be finished after then, the fabrication of two set of electronics will start.
- 11cm Low-Q IP-BPM performance test will perform at the end of linac during march.
- 2nm resolution test will start from May to June at the extraction beam line with IP-Chamber.

Thank you !!