Laboratoire LEPRINCE-RINGUET

École polytechnique - IN2P3/CNRS

CENTRE NATIONAL DE LA RECHERCHE SCIENTIFIQUE

IN2P3 INSTITUT NATIONAL DE PHYSIQUE NUCLÉAIRE ET DE PHYSIQUE DES PARTICULES

From today design … to

Final and realistic design

Why a difference

❶ lessons from last 3 years that some technical challenges are just dreams of physicists and just not realistic for engineers/producers….

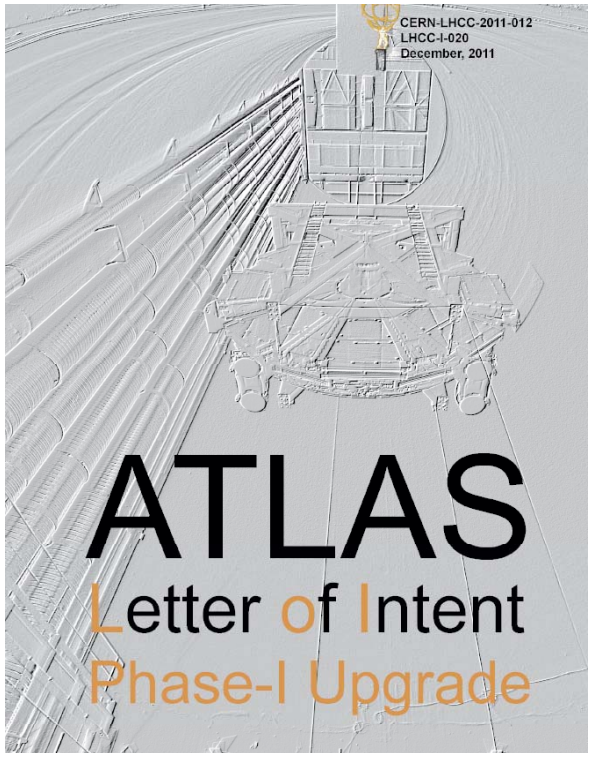
❷ The cost estimation looks more than ever unfavourable (choose cheaper techno.)

❸ read again "The 10 Commandments" for a real detector
- minimise the number of technology
- minimise the risk (moderate number of innovative technology)
- minimise the difficulty of assembling (simpler is better)
- OF COURSE, COST in part of the choice

Etc….
and last but not least, a full detector is not a prototype in larger size !!!!

❹ Remember that the manpower will not be there , when compare to previous detector construction (Upgrade LHC detectors and HEP physics in the poor parents now)
…… production and construction more comparable to space science

see next slide

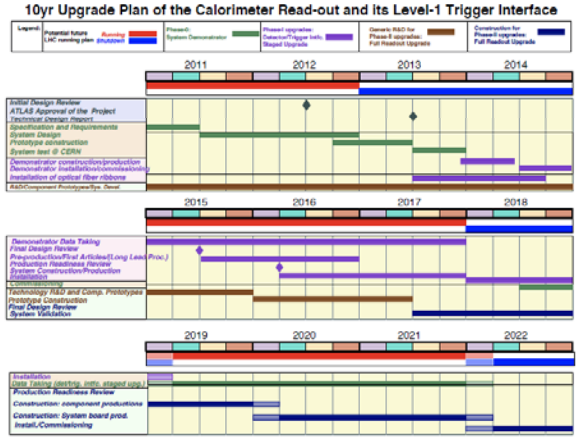


Funding , manpower in the next 8 years

> financial crisis

> LHC upgrade

> HEP versus applied science → Impact on manpower resource !!!!



Today manpower resource on ECAL ….. is very modest

In any case, much smaller than the 1st prototype time
While this proto. was based on classic technologies

"Chercher l'erreur"

For a “known” technology, it took 5 years to establish the feasibility and readiness of the mechanics of one “barrel” module of ECAL

we can’t really be ready in 3-4 years with VERY INNOVATIVE solutions , where many years of R&D for feasibility study are needed

Readout system

Since we have not 10 years of R&D and
Since there is not 50 people working on the subject….

- forget the DC coupling
  By far, too much sensitive to noise and ground loops and leaks and …

- forget the autotrigger (or constraint it by external clock/trigger)
  it is too much dependant on the level of noise in the detector !!
  (device behavior, environment condition, …)
  The system must be able to survive whatever the condition

- VFE optimise running at ILC, but possibility to test in TB
  (external trigger and memory pile adapted i.e. 6 events in pile is by far too short)

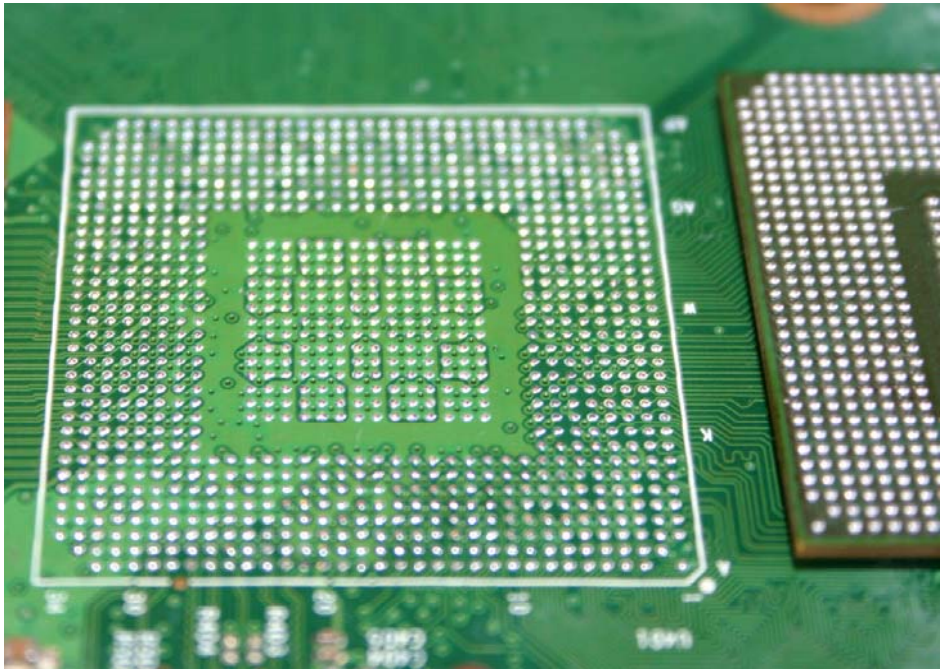
- A SPECIAL VFE chip , with lower dynamics (up to 5 mip), to be used to validate and calibrate the wafers in TB (special case)
  (better precision in smaller time of TB due to smaller noise)

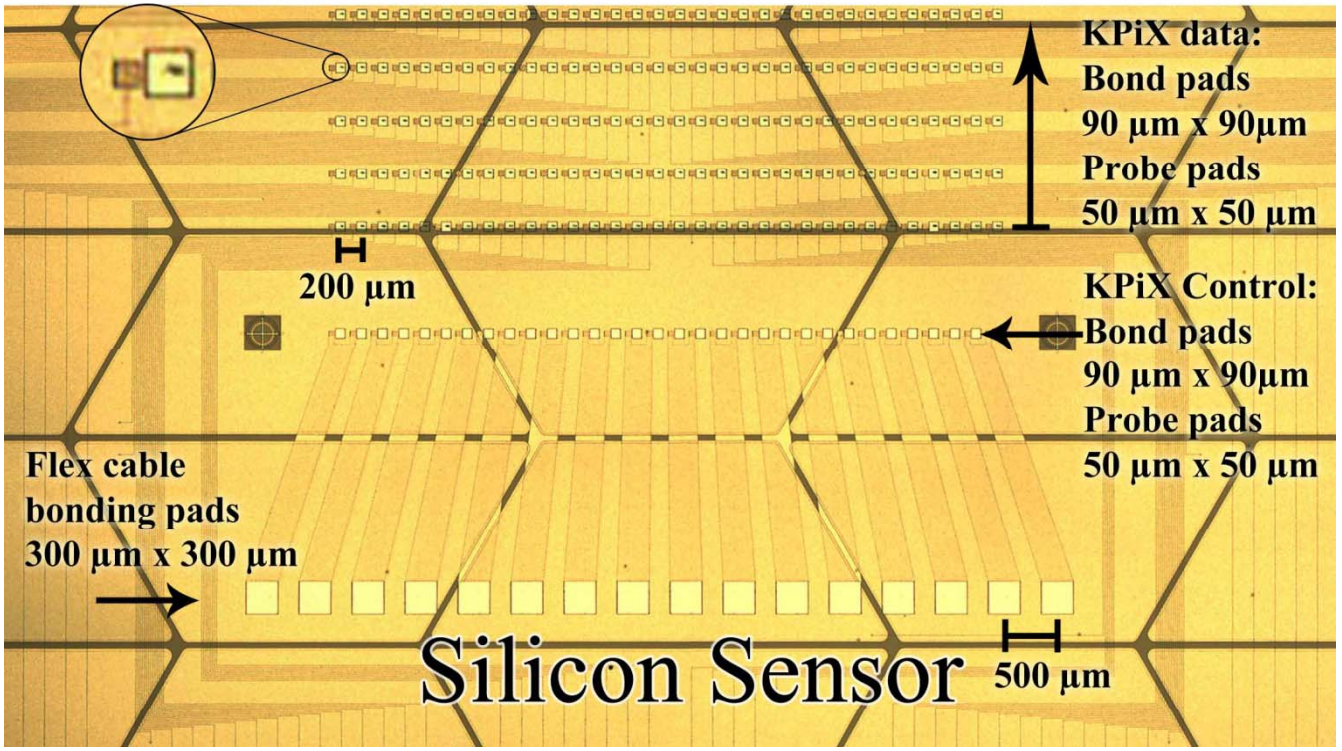
VFE CHIP

Due to silicon wafer cost, it is MANDATORY to burn out the chip before use !!!

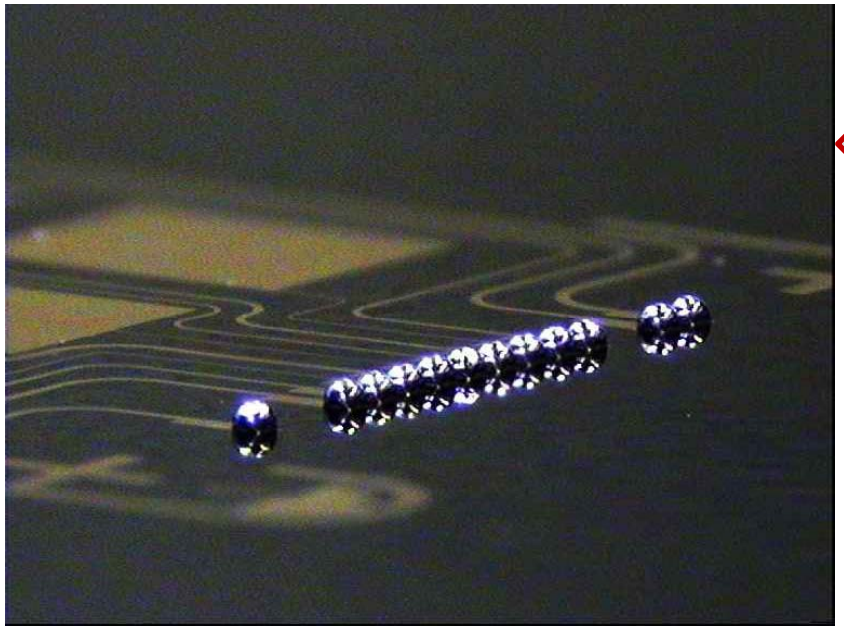
→ VFE MUST be packaged in thin but cheap techno.
(possible 1 mm thick ?) ➲ ADAPT chip design to this requirements

→ connection …. Bump bonded, ?? Different geometry (not a square)
(1 ADC/ch. (or faster ADC for > 1 ch.) ??





SiD ECAL



For cost optimisation, bump bonding, directly on silicon wafer is not recommended

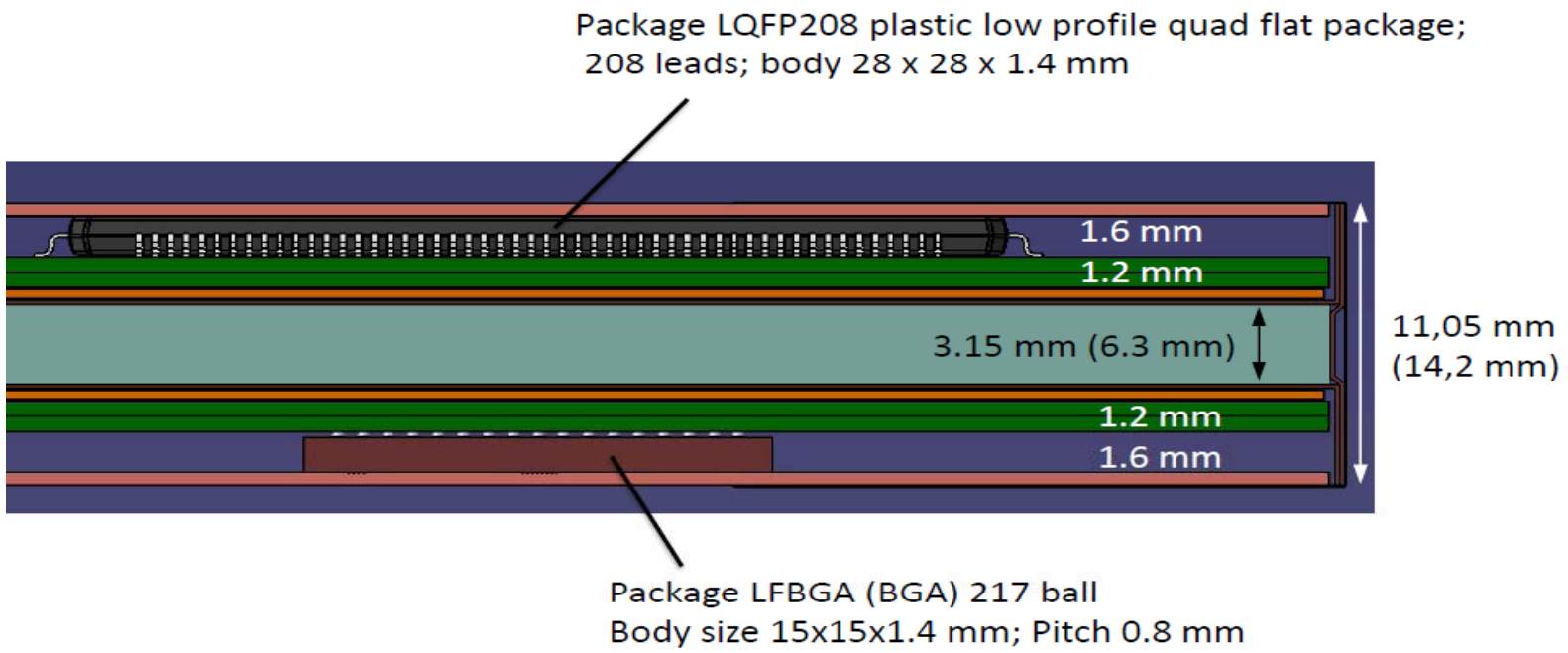
But , why not on PCB !!
(if it is a standard industrial process)

PCB

It is MANDATORY to use "STANDARD" producers in "Classical" techno

→ thickness 0.8 mm in our dream
1.2 mm today (with difficulty)

1.5 or more for final design ?



20 layers

The uncertainty on the silicon cost, lead to the possibility that 15-20 layers could be the maximum number of layers affordable by HEP community….

➲ It reduce the cost by the silicon surface, but not only

i.e. the tungsten is cheaper when thicker

For the DBD, the assembling scheme must be given !!!!

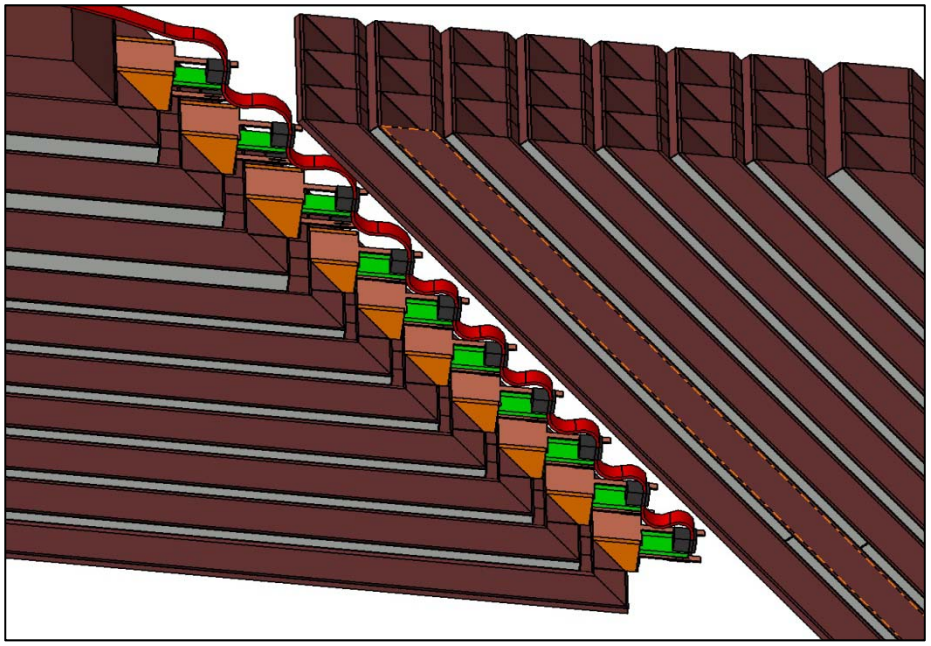
The assembling time, the organisation, the manpower in m/y, etc…

Exemple :

a simple flex kapton running all along the alveoli is better than DIF board

i.e. any electronic (DIF) in the 4 cm gap is challenging, costing and it is not simple to unplug

➲ Displace the concentrator on the back of the module (larger surface available)



Design & picture:
Marc Anduze

CONCLUSION

It is time to go down ……..

& go back to

Technically and costly realistic choices

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What is true for si-w ecal …..