New CCC for the Test Beam

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Introduction

Motivation:

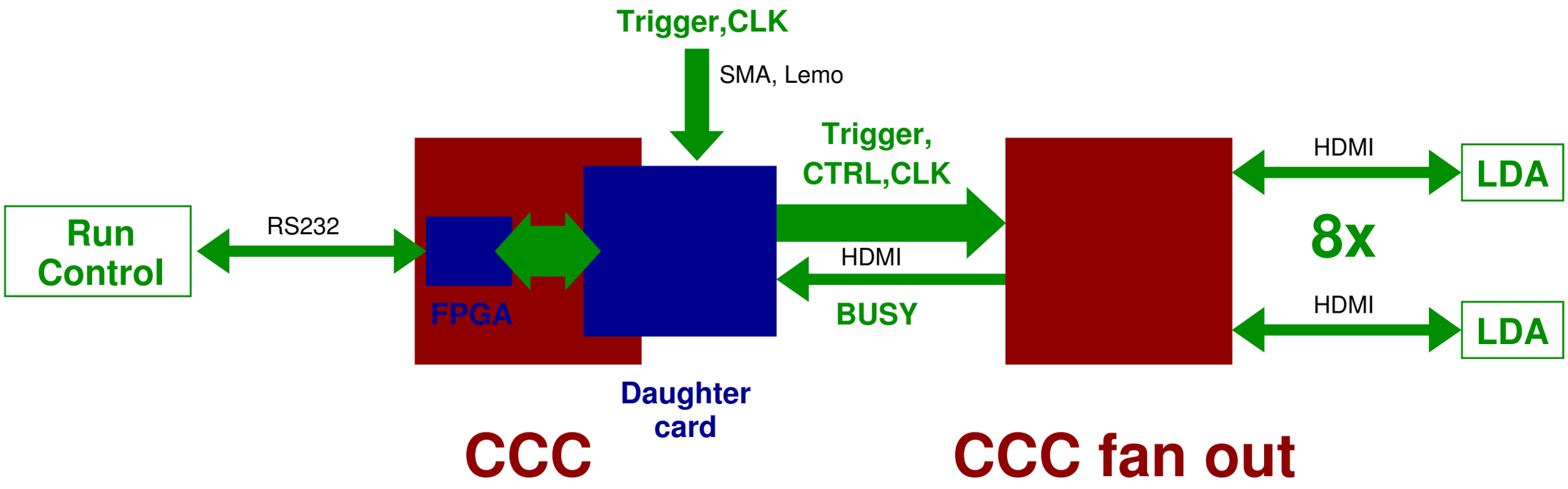
- Old CCC board not able to cope with enhanced trigger and control logic (on-board CPLD logic too small)
- Decision taken to build a new CCC for the March test-beam at DESY.
- Rather short time-scale

  ➜ "Quick & dirty" design (e.g. no plan to use daughter module for future test-beams).

General Layout

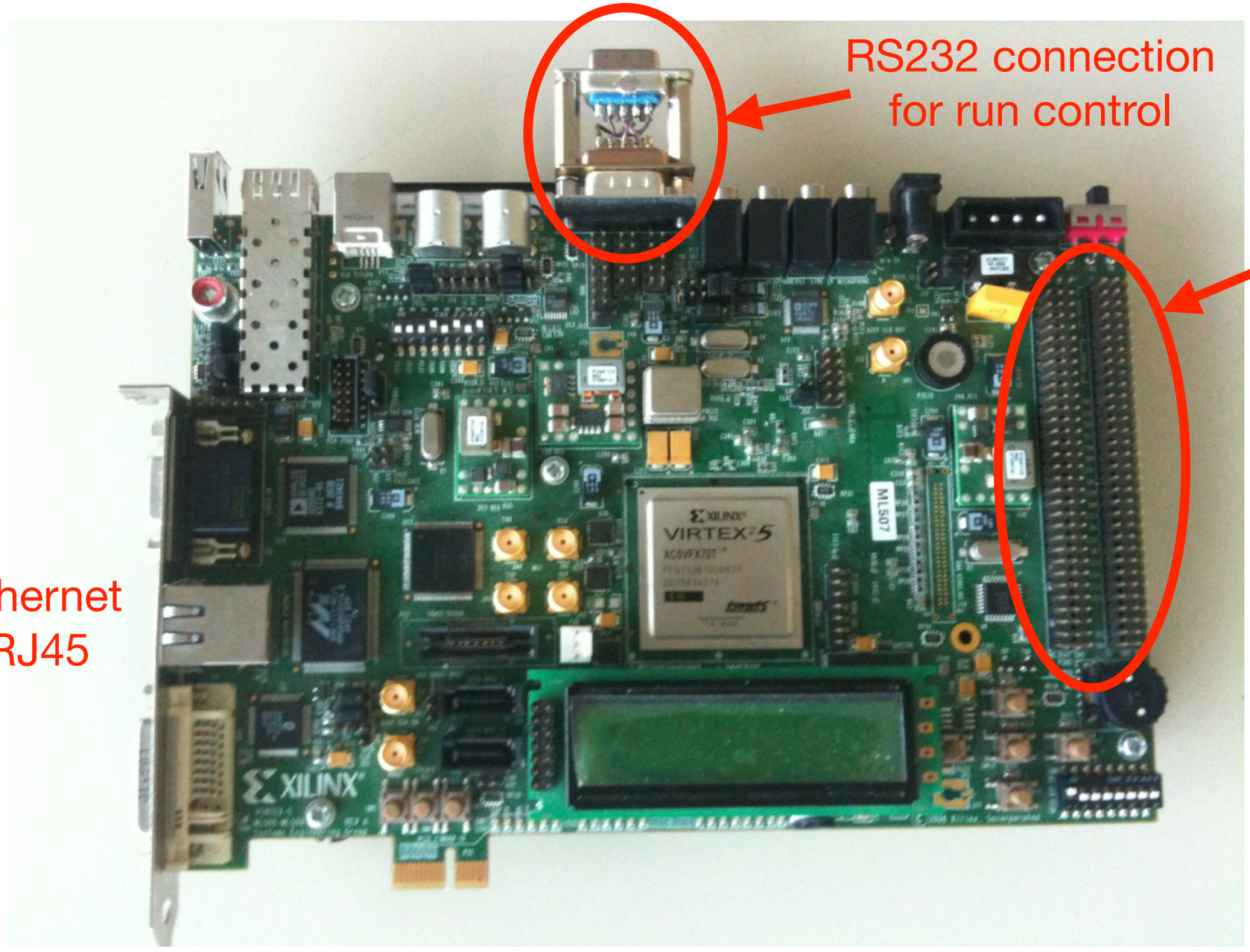
New CCC consists of two separated parts:

1. **FPGA-controlled CCC board,** able to communicate with external clock & trigger logic.
2. **Fan-out board** with no programmable logic (only logic for BUSY signal).



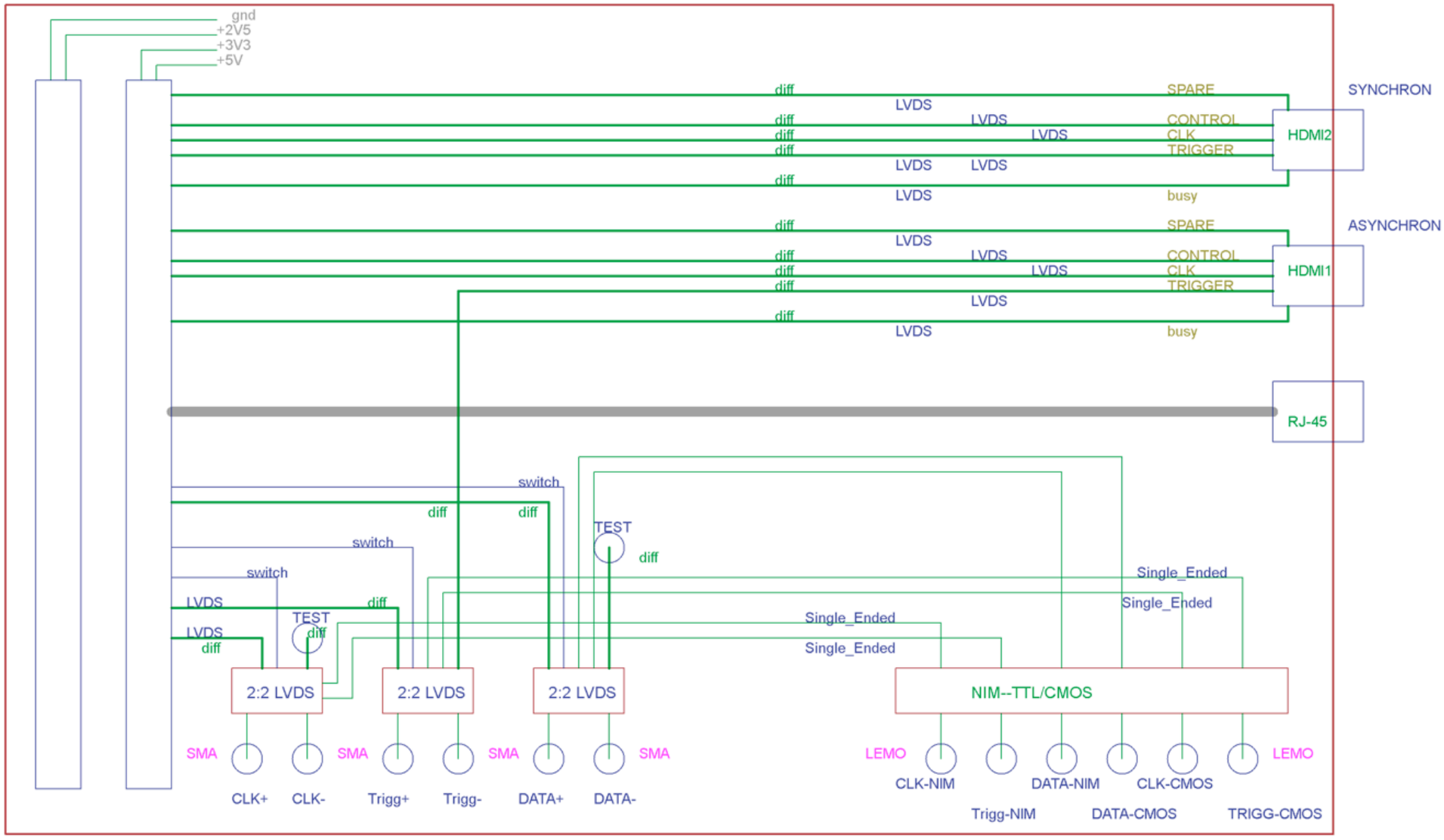
New CCC Board

Xilinx ML507 evaluation board (with Virtex 5, later: Kintex 7)



CCC Daughter Card

- Connects incoming/outgoing lines with FPGA.
- Specific for March test run (to be dumped afterwards).



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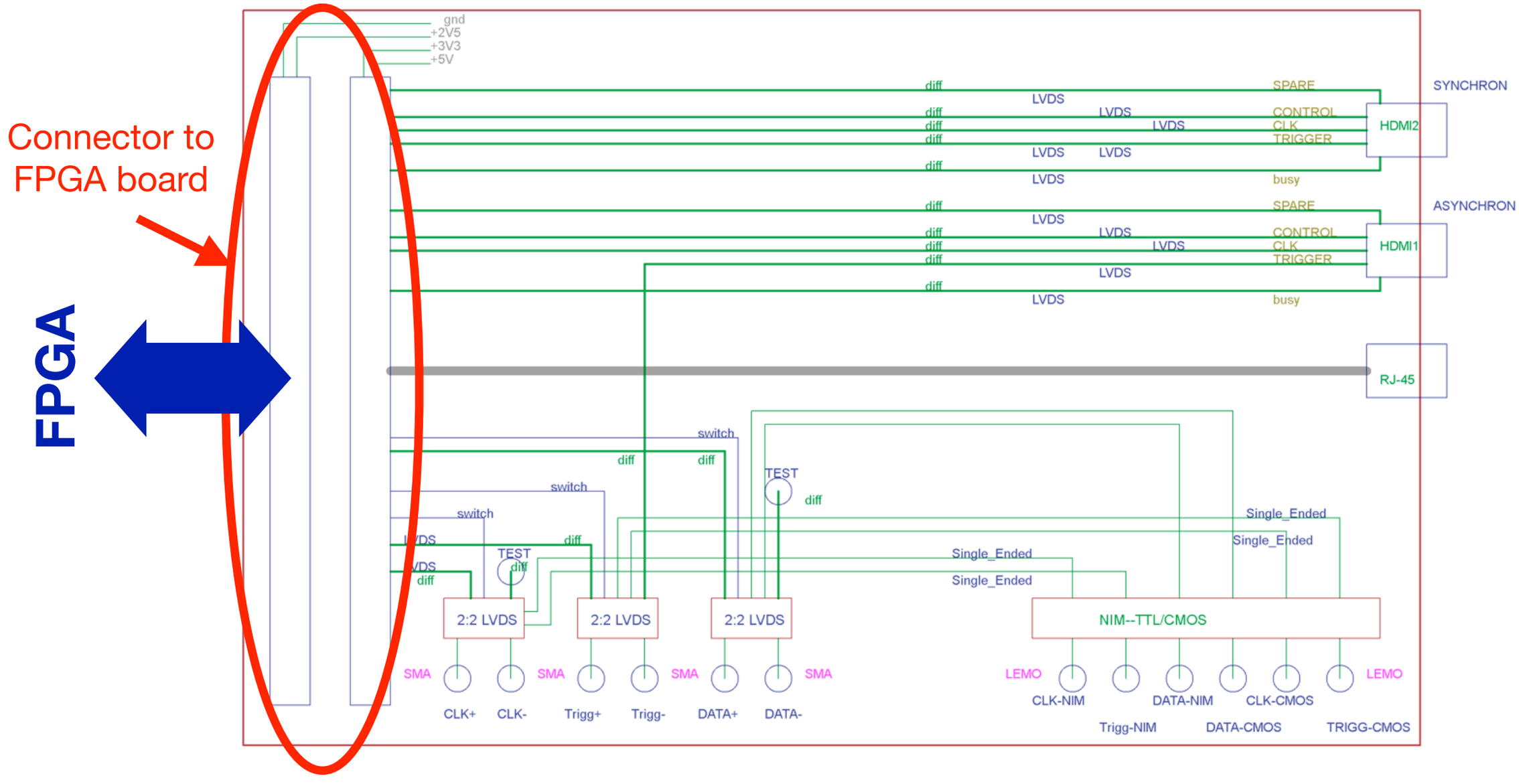

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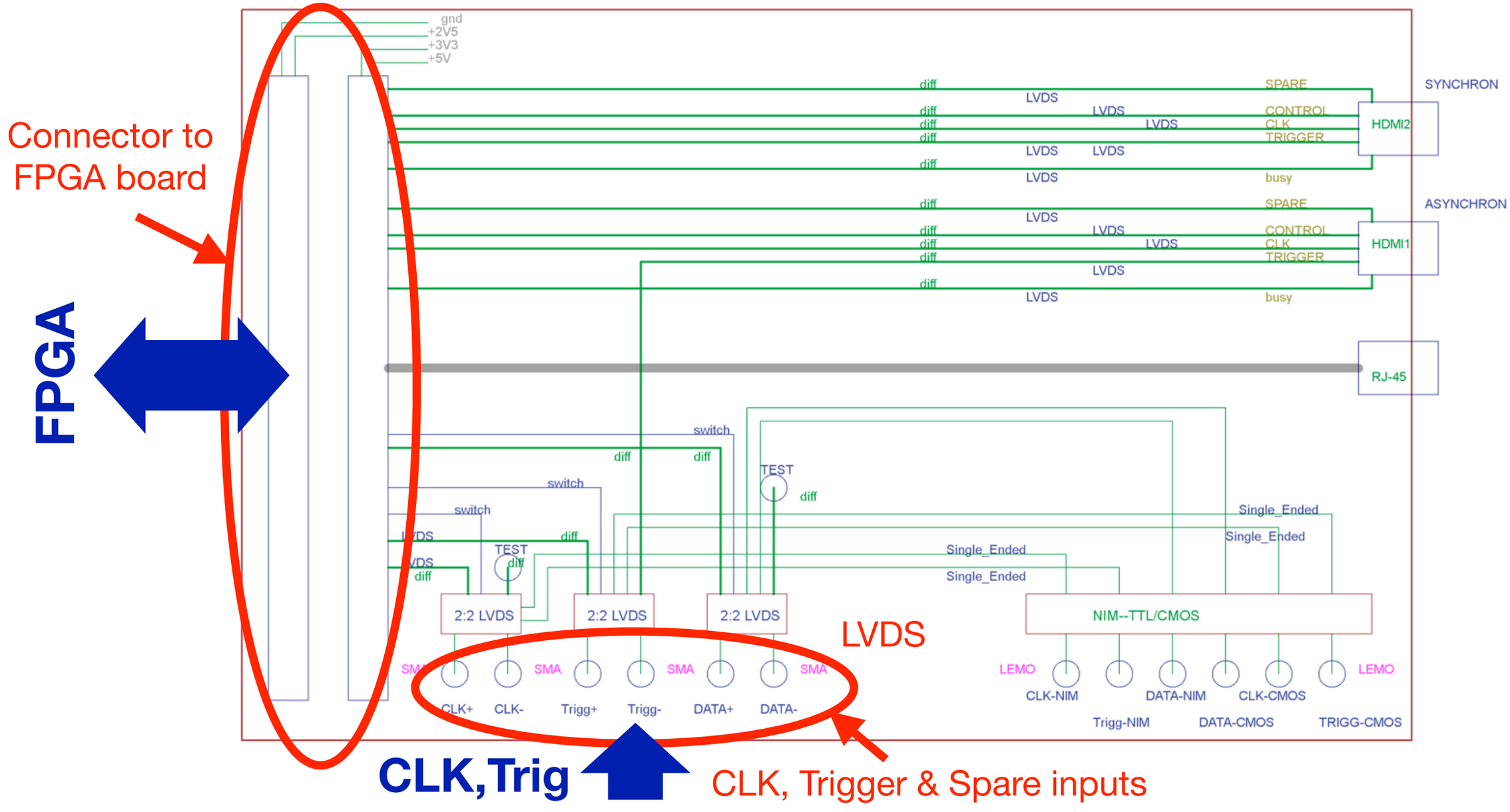

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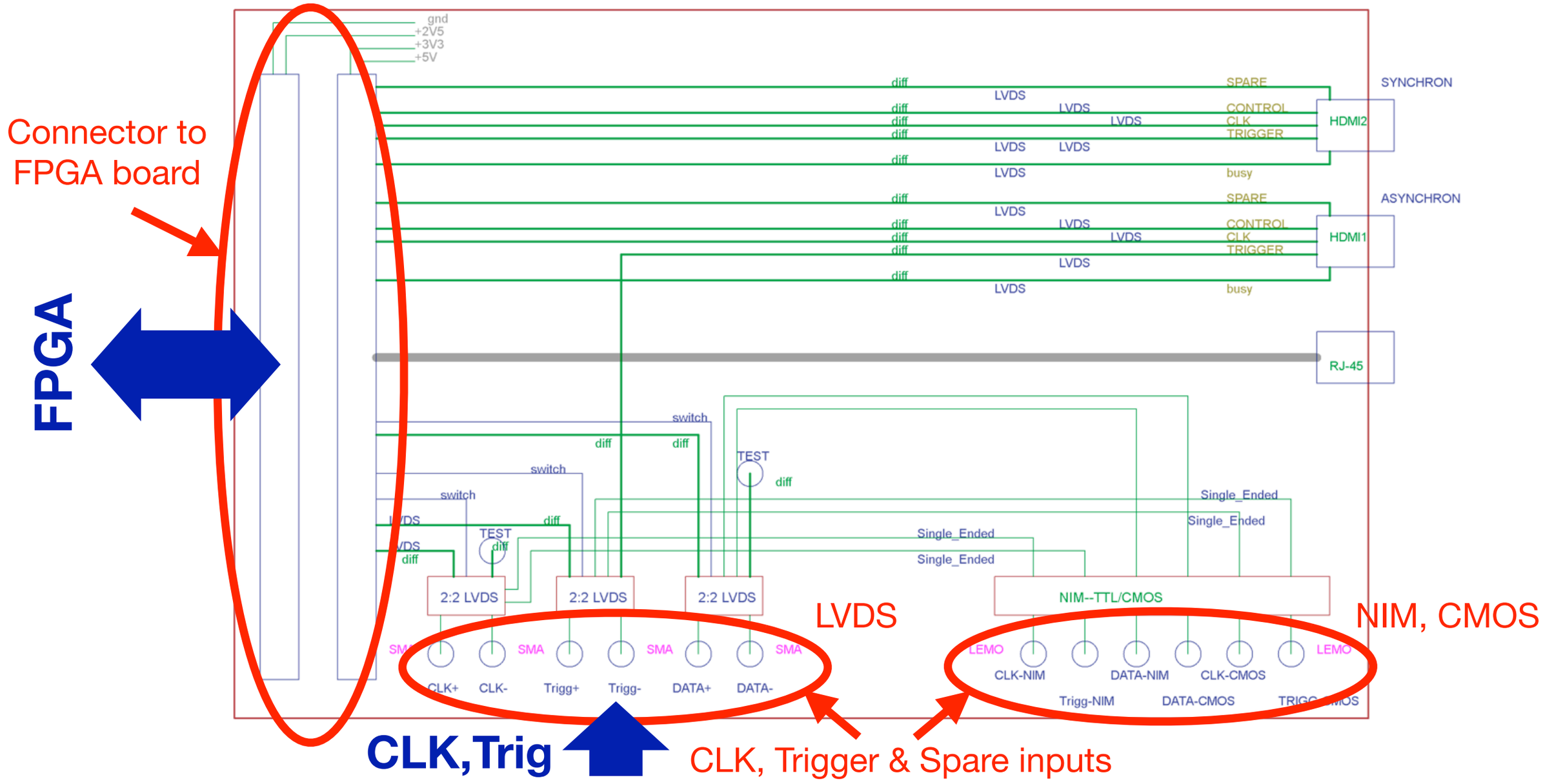

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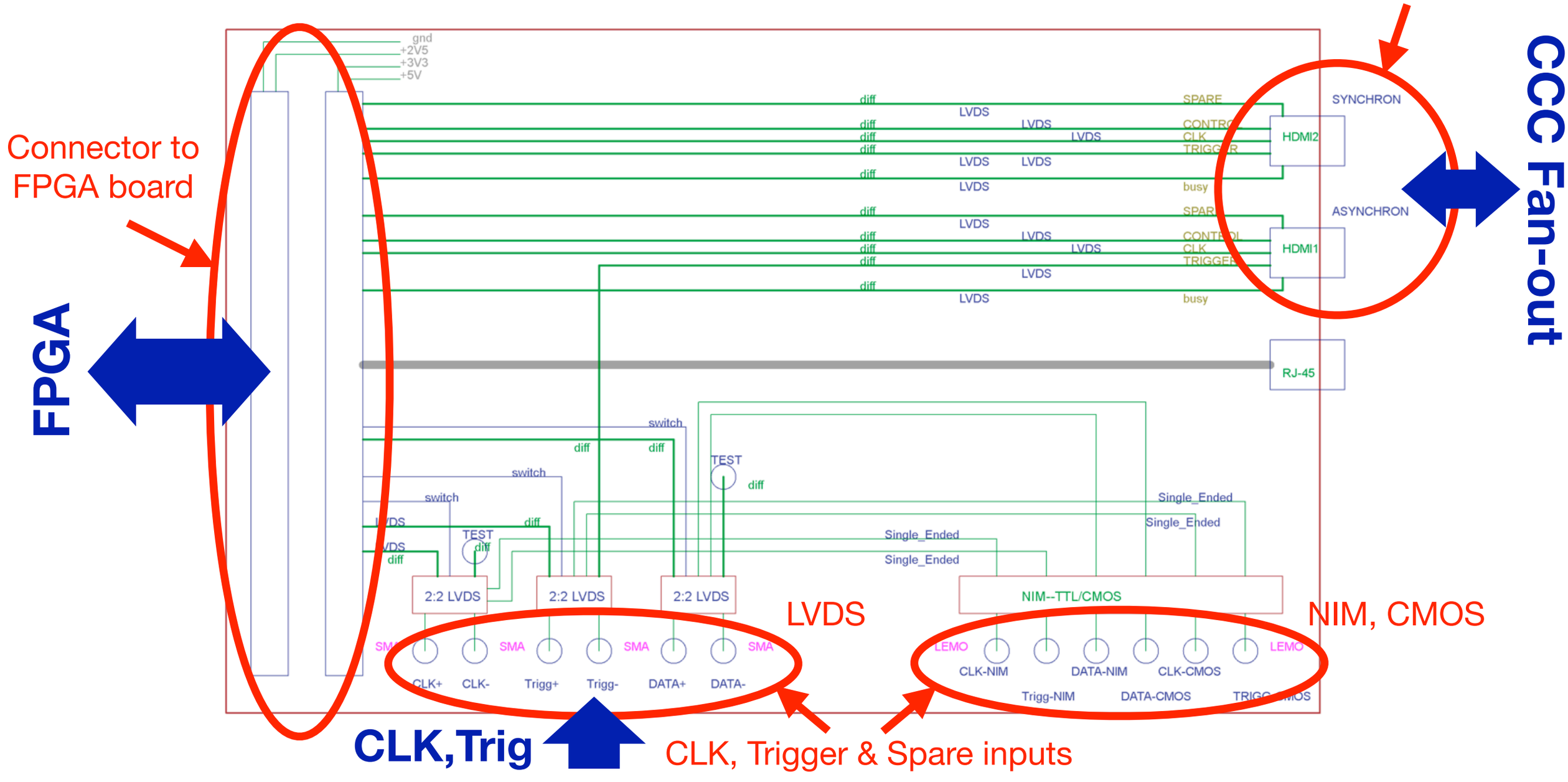

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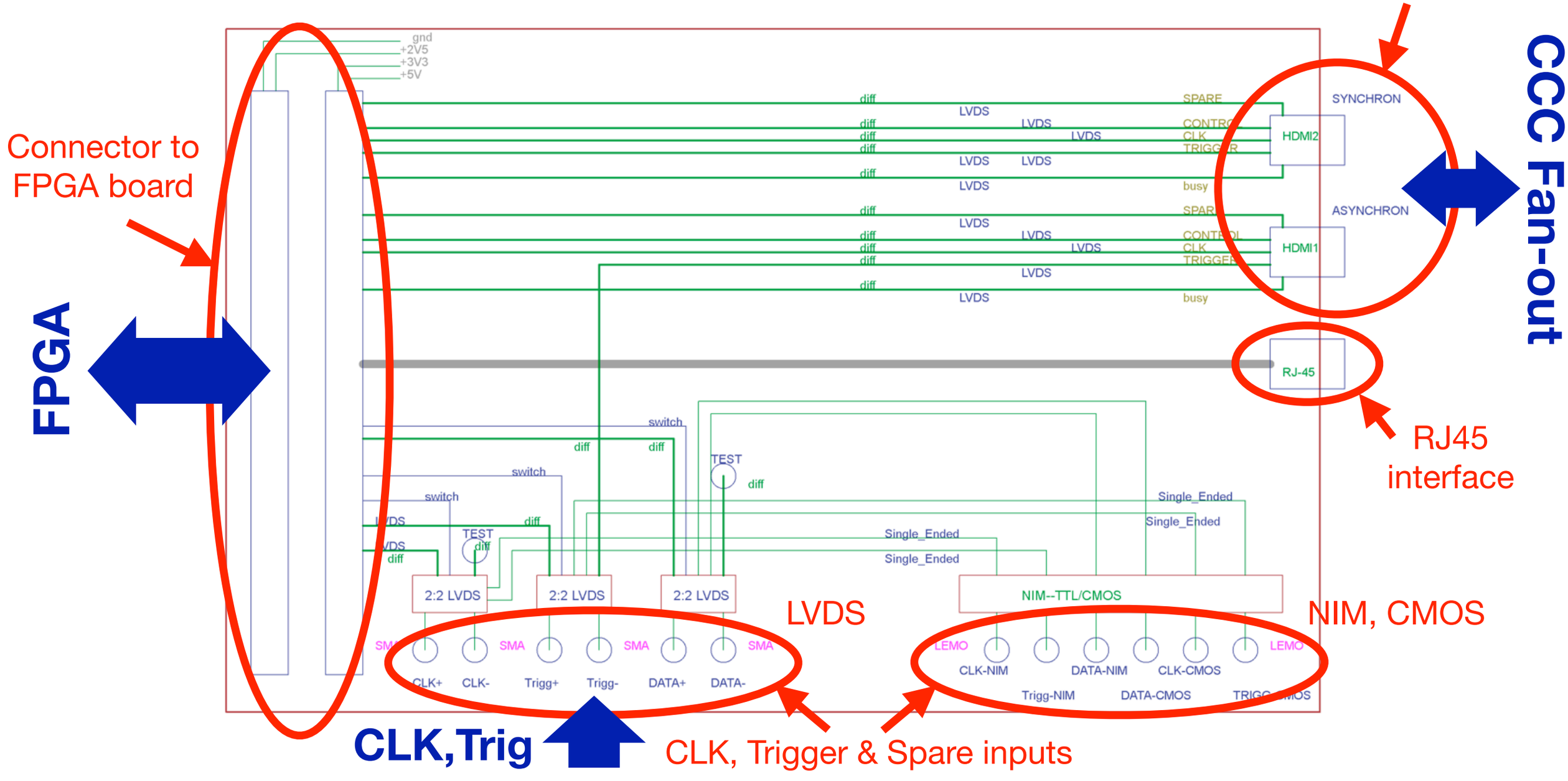
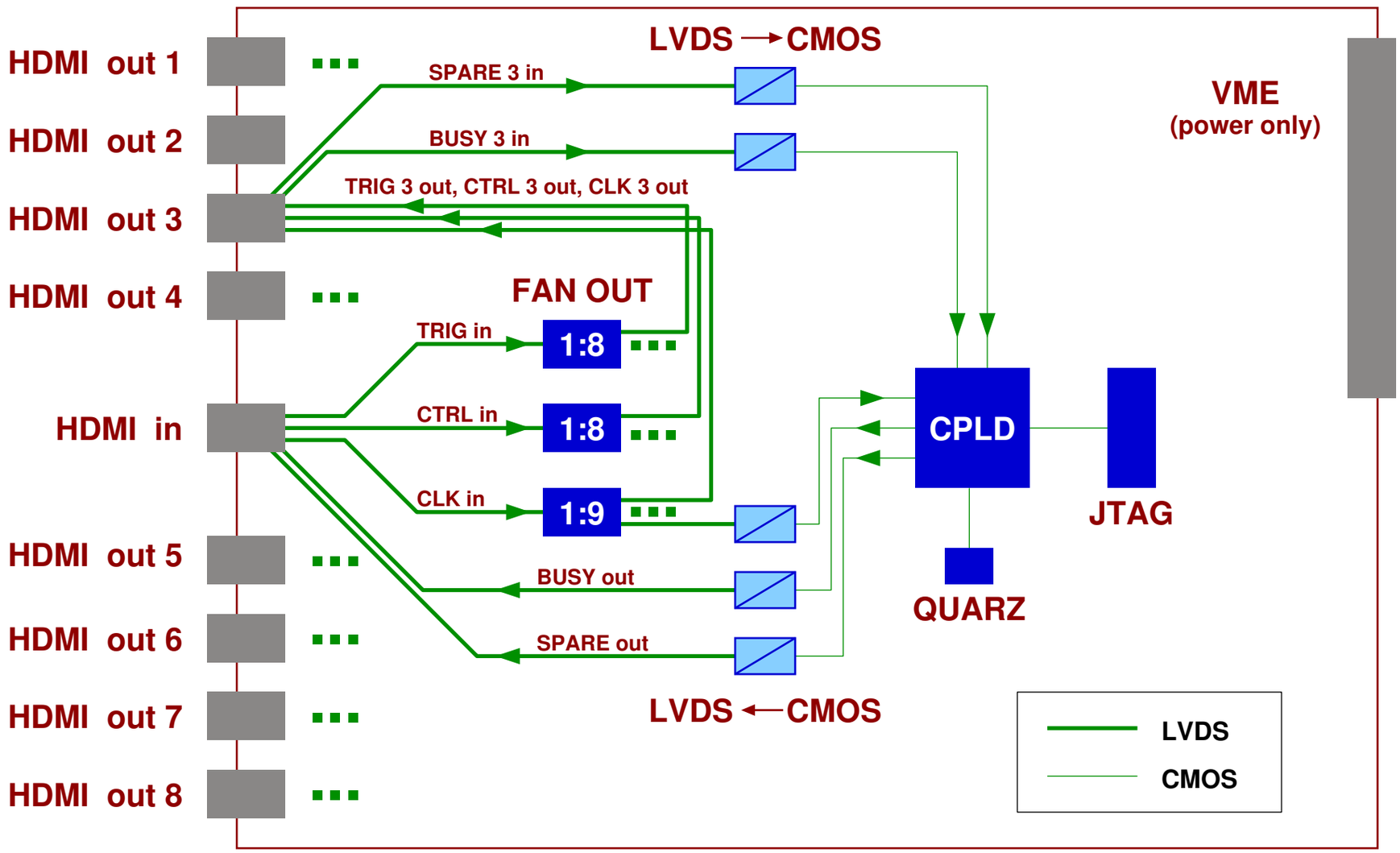


CCC Status

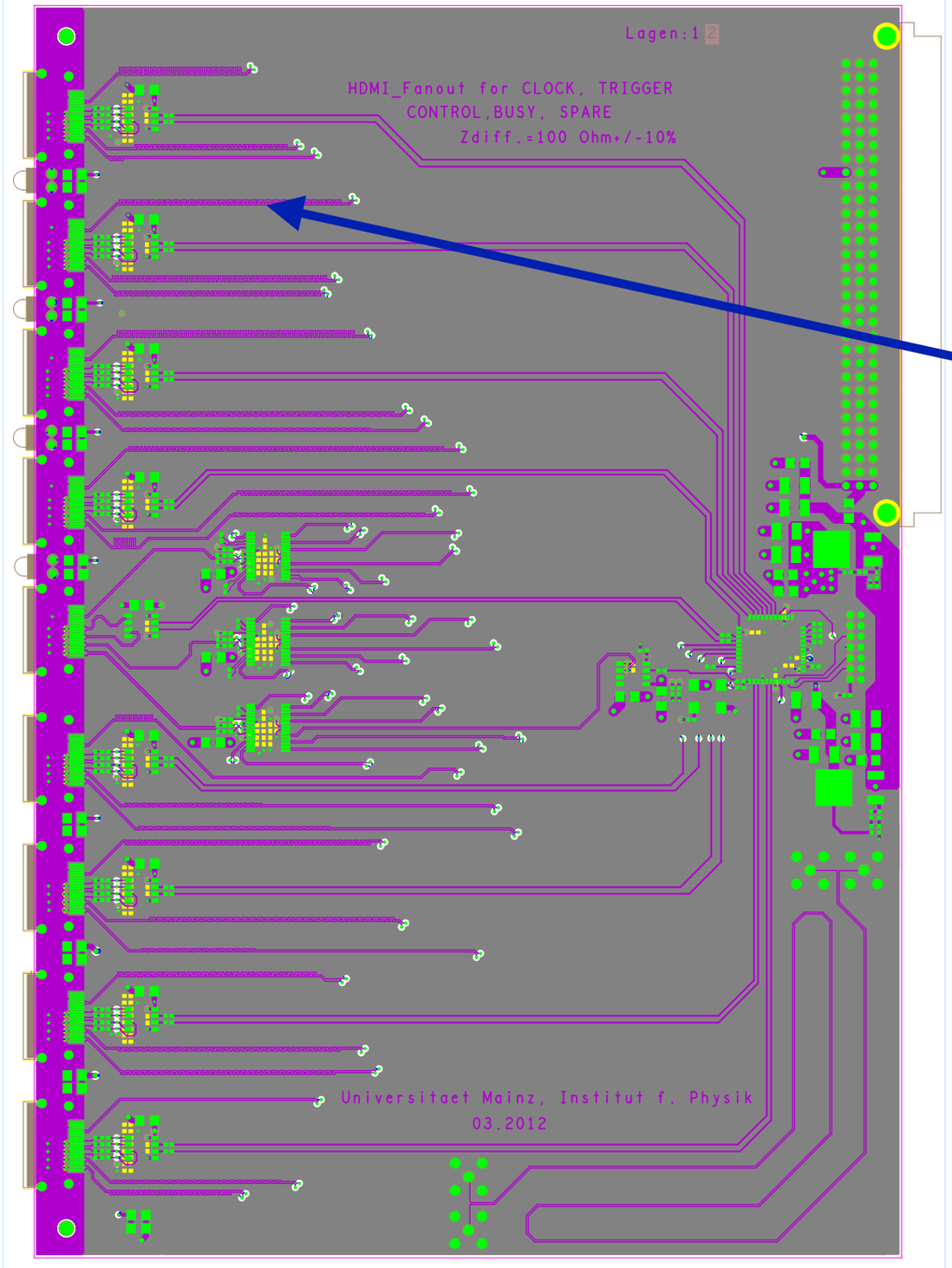
- **Daughter card:** PCB design to be submitted right now.
  - Production ≲ 2 weeks (two boards, not impedance-controlled).
  - Assembly immediately after.
    - ➜ **Ready for DESY test-beam.**
- **CCC FPGA board:** two available in Mainz.
- **Firmware:** (new student: Rouven Spreckels)
  - FPGA able to receive and submit packets.
  - Protocol not entirely clear yet.
- **Online Software:** no new software necessary (should be compatible to existent CCC).

CCC Fan-out Board

- **Distributes Trigger, Control, Clock** via HDMI
- **Receives BUSY** (and a spare line) via HDMI
- Only on-board logic: combination of all BUSYs in a CPLD



Fan-out Board Status



- **PCB board in production** (two ordered).
  - 6U VME board (backplane only for power)
  - Traces adjusted to «1 ns
  - Impedance-controlled
- Will arrive at Mainz this week.
- ~ 1 week for assembly

Ready for ECAL test beam at DESY

Summary

- **New CCC module:**
  - FPGA-based main module.
  - Daughter card for all sorts of input/output signals.
  - HDMI-based fan-out of trigger, clock & control signals and collection of busy signals.
- **Status:**
  - FPGA modules available.
  - Daughter and fan-out cards in or almost in production.
  - Main firmware written.

    ➜ ***Ready to run in the March test-beam!***
- **Further plans:**
  - Design of a long-term CCC solution.