



Laboratoire d'Anney-le-Vieux
de Physique des Particules



m³ Intermediate DAQ

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CALICE DAQ v.2

Status

We had problems with :

- LDA board :

data corruption !/?

CEM instability !/?

No possibility to reset from the control room

Not a classic board format

[...]

- CCC board :

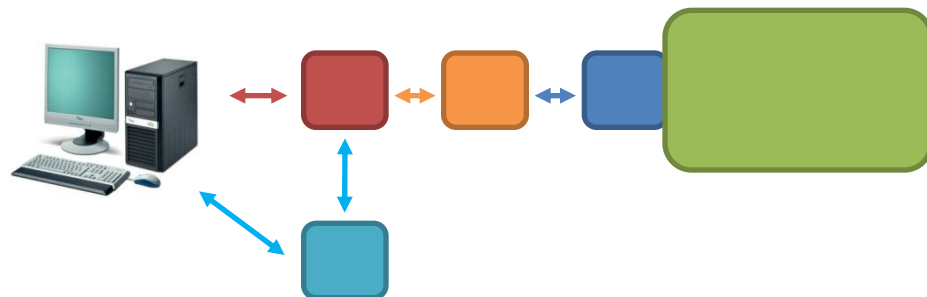
CPLD too small

CEM instability !/?

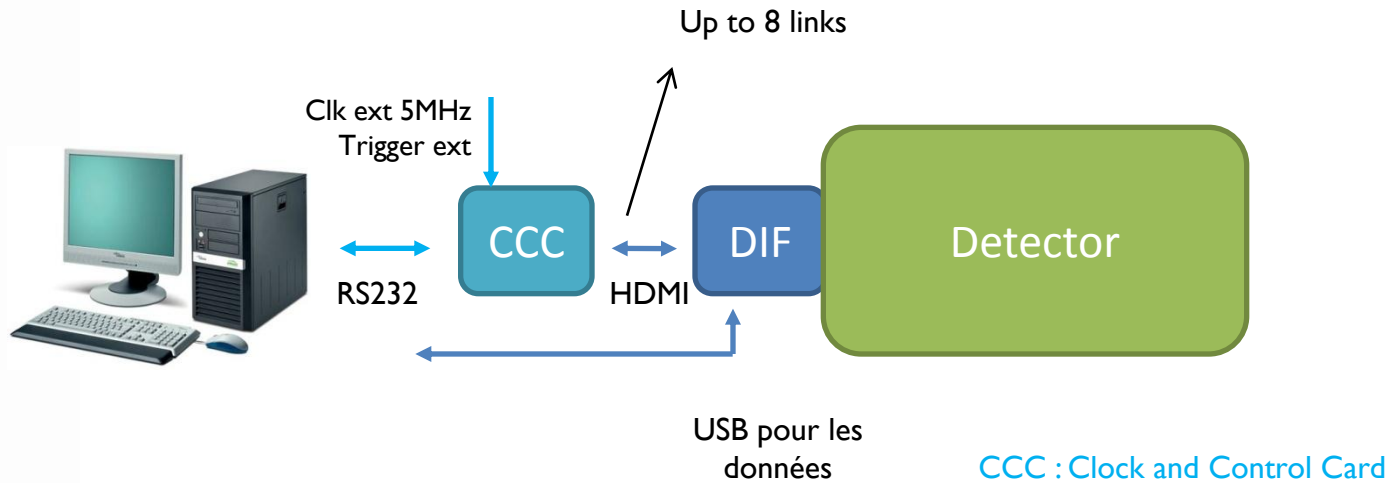
No possibility to reset from the control room

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[...]



m² intermediate μ MEGAS DAQ



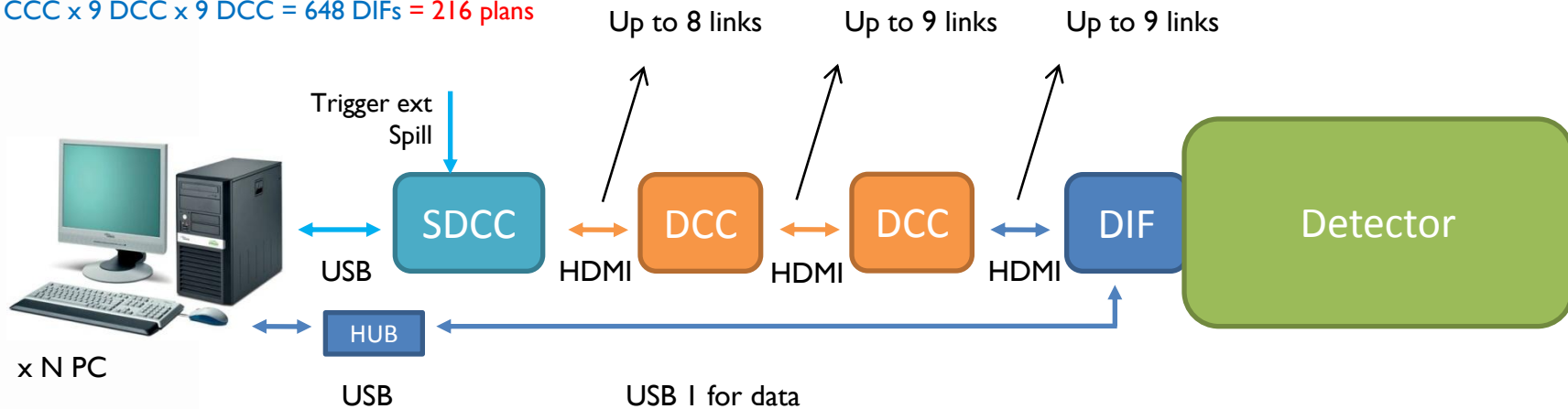
Worked perfectly with a m² MICROMEAS

No bug during 20 days of Beam Test at CERN

m³ intermediate DAQ

8 CCC x 9 DCC = 72 DIFs = 24 plans

8 CCC x 9 DCC x 9 DCC = 648 DIFs = 216 plans



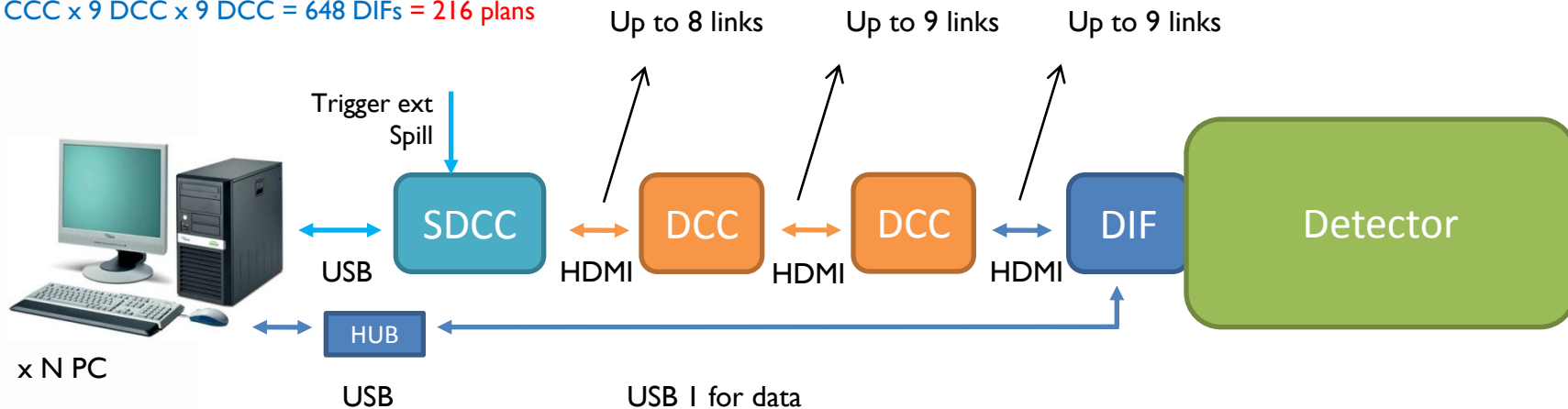
DCC : Data Concentrator Card
SDCC : Synchronous DCC

No LDA or CCC anymore !!

m³ intermediate DAQ

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Things needed to be done :

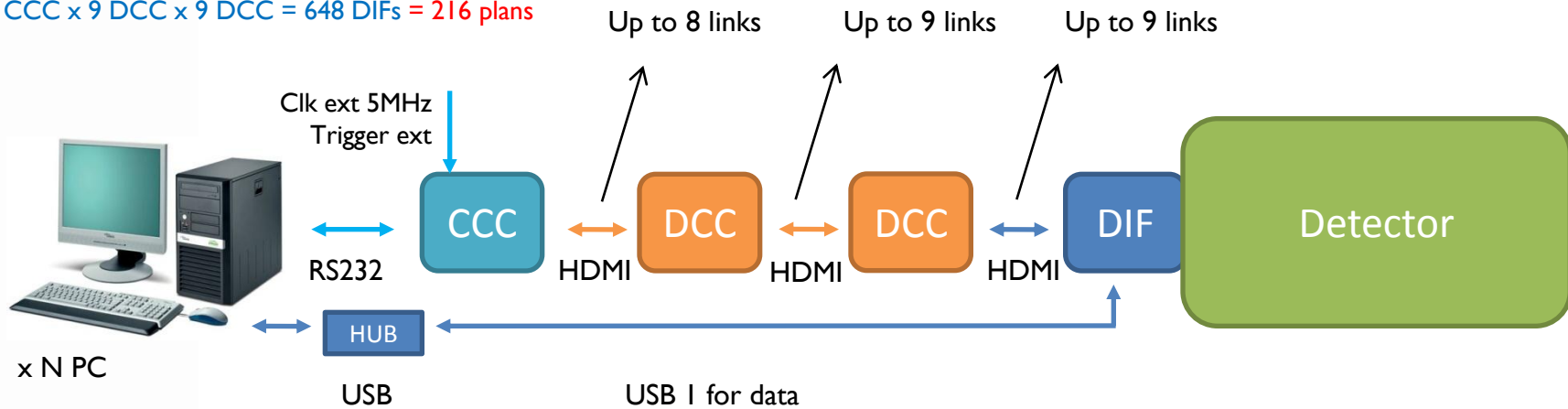
DCC : Data Concentrator Card
SDCC : Synchronous DCC

- Modify the data reception mode on the PC. Ethernet replaced by USB
- Add commands to send through USB
- Do a 2 new FW for the DCC, one for the DCC, one for the SDCC
- Modify the FW on the DIF to deal with Hardrocs for RPCs
- Implement the Power Pulsing feature

m³ intermediate DAQ

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DCC : Data Concentrator Card
CCC : Clock and Control Card

Test done :

- Perform a Slow Control on a μ MEGAS and a RPC detector with XDAQ
- Read a μ MEGAS and a RPC detector in the same time with XDAQ
Data when noise
- Perform a Slow Control on 5 RPC m² with XDAQ(IPLN) (they have tested 13)
- Read up to 13 RPC m² with XDAQ (still stop sometimes)

New CCC : SDCC

CCC problems

- CCC board :

 - CPLD too small

 - CEM instability

 - No possibility to reset from the control room

 - Not a classic size

 - [...]

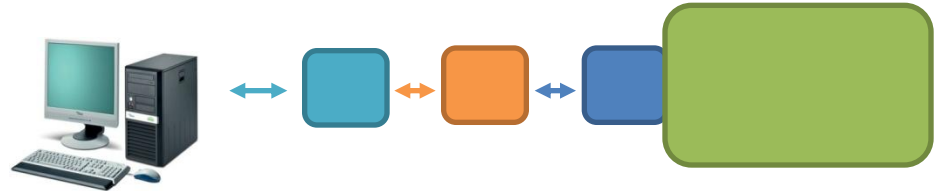
- SDCC (Synchronous DCC):

 - FPGA bigger than the CPLD

 - No CEM instability noted

 - Possibility to reset the board from the control room

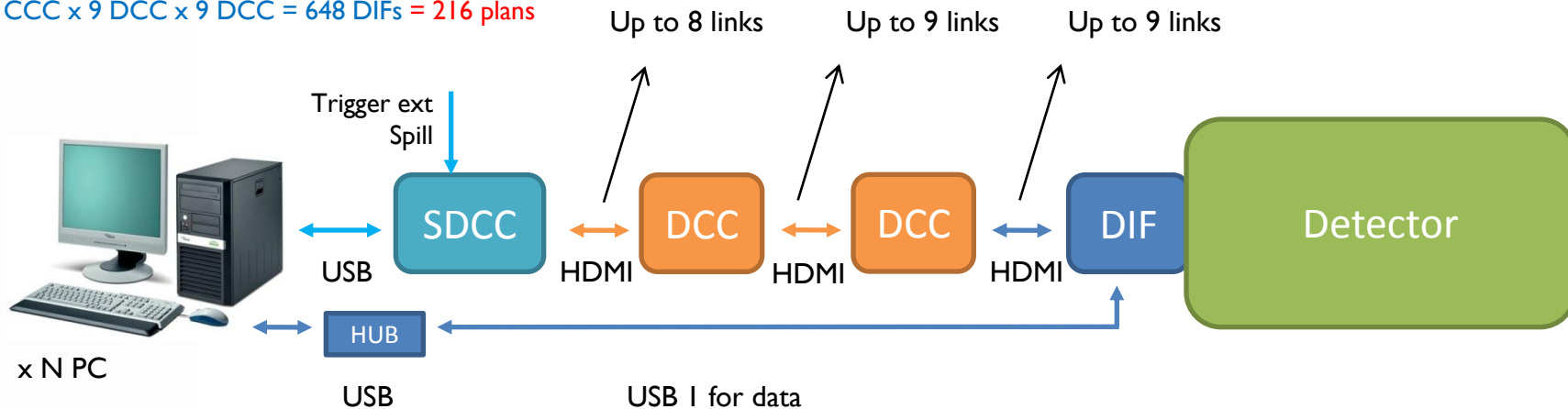
 - Classic VME I6 size.



m³ intermediate DAQ

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DCC : Data Concentrator Card
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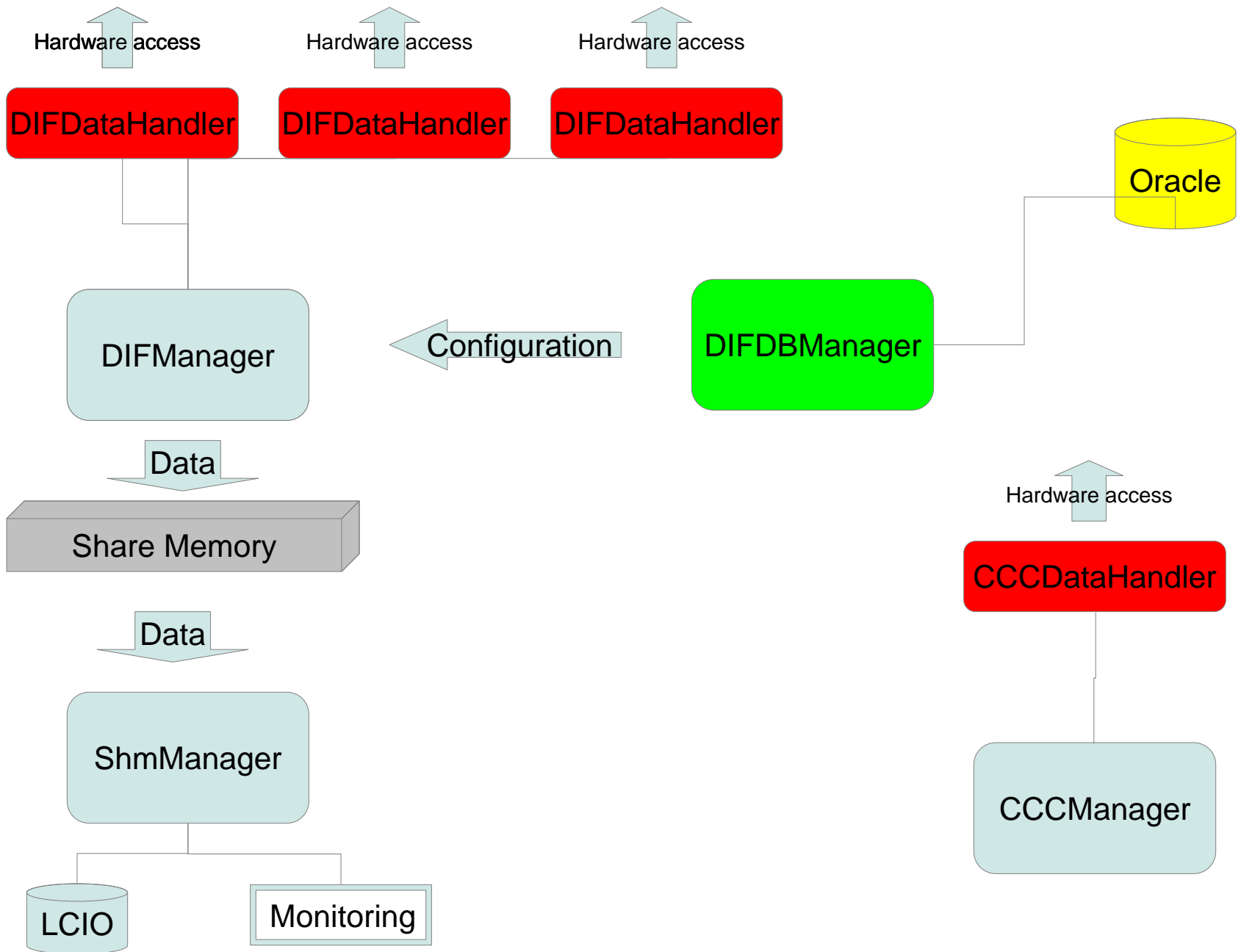
The system is currently working with more than 40 plans of RPC and it's stable. It's also working with one layer of MicroMEGAS Done in Trigger or ILC mode.

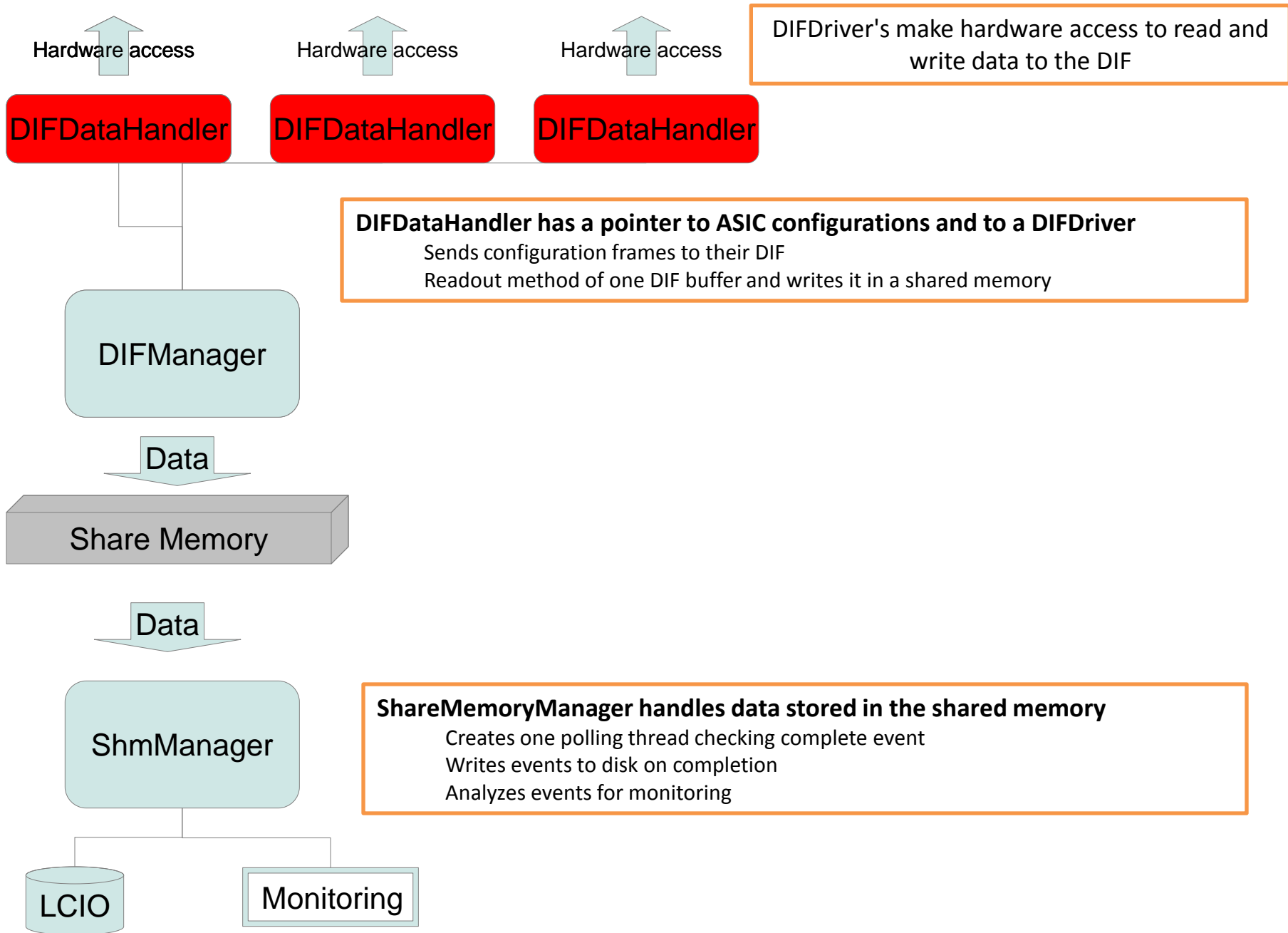
Single PC acquisition

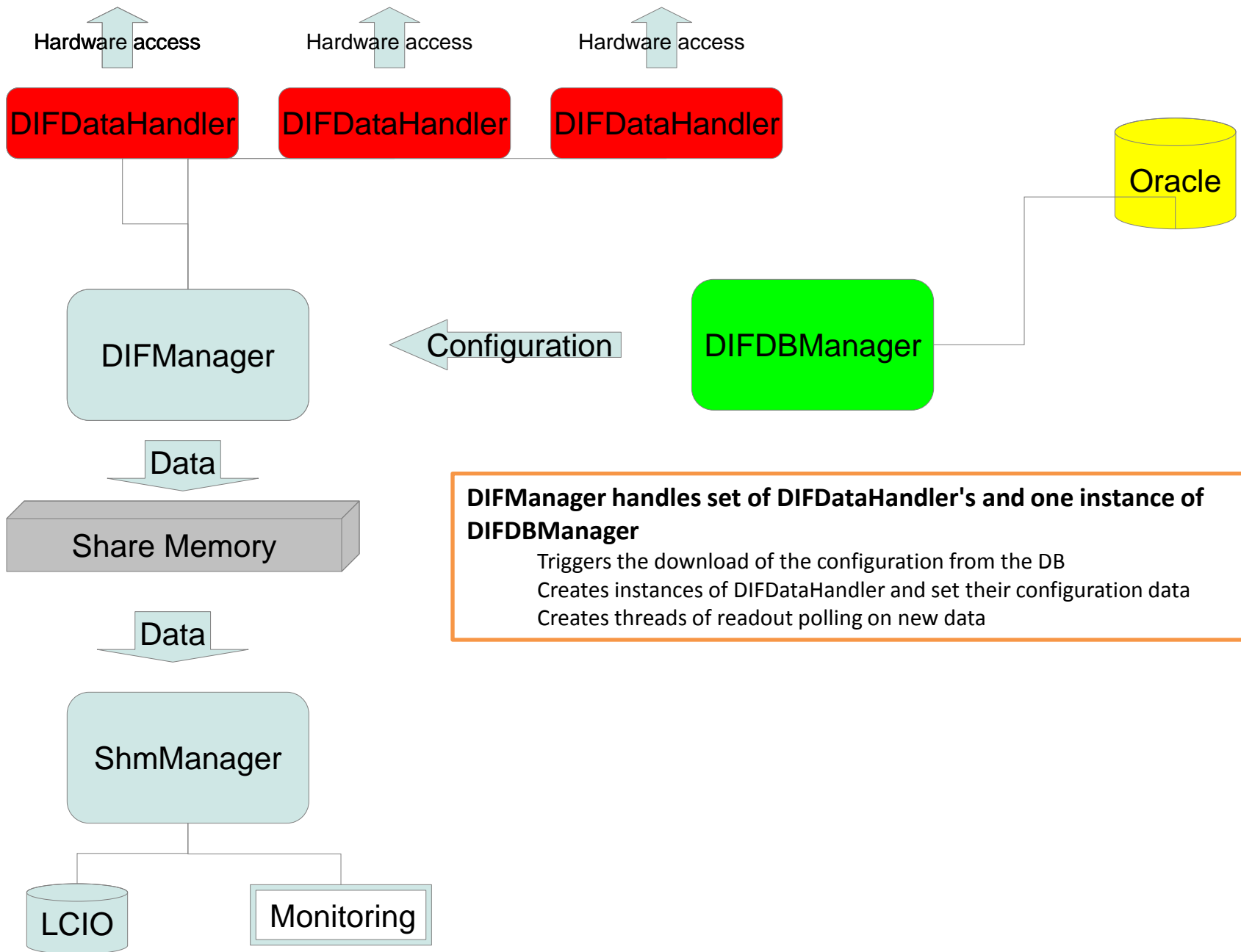
Work done by *Christophe Combaret* and *Laurent Mirabito*

Requirements:

- Storage and history of configuration parameter
 - DB model and interface library (C or C++)
 - ILCCONFDB developed by G.Baulieu
- DBManager to access DB and make appropriate downloads
- DIF/LDAManager to access DIFs via USB or Ethernet to configure ASICs and read data
- CCCManager to control the trigger

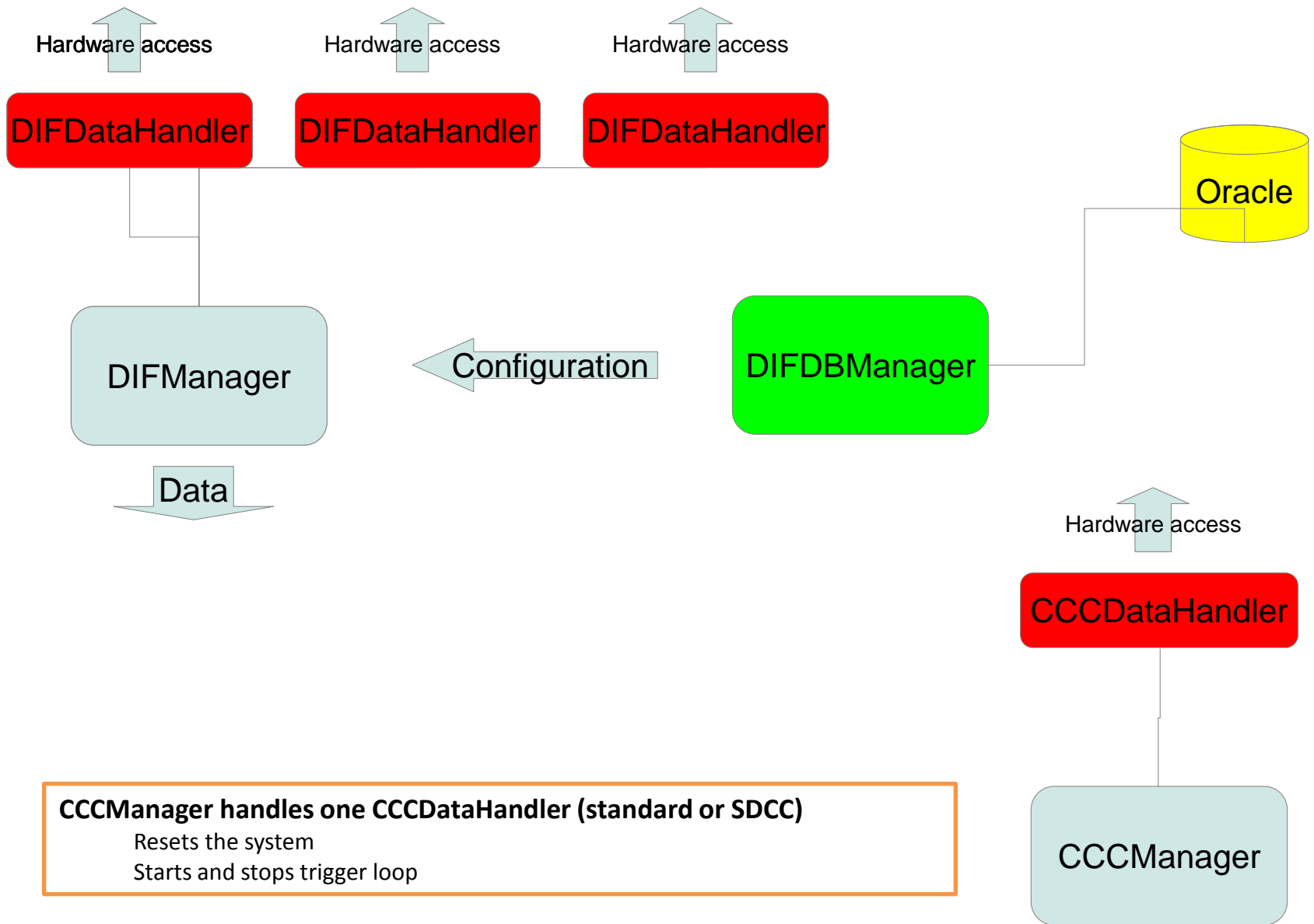






DIFManager handles set of DIFDataHandler's and one instance of DIFDBManager

- Triggers the download of the configuration from the DB
- Creates instances of DIFDataHandler and set their configuration data
- Creates threads of readout polling on new data



CCCManager handles one CCCDataHandler (standard or SDCC)
 Resets the system
 Starts and stops trigger loop

Multi PC's acquisition

Work done by Christophe Combaret and Laurent Mirabito

Requirement

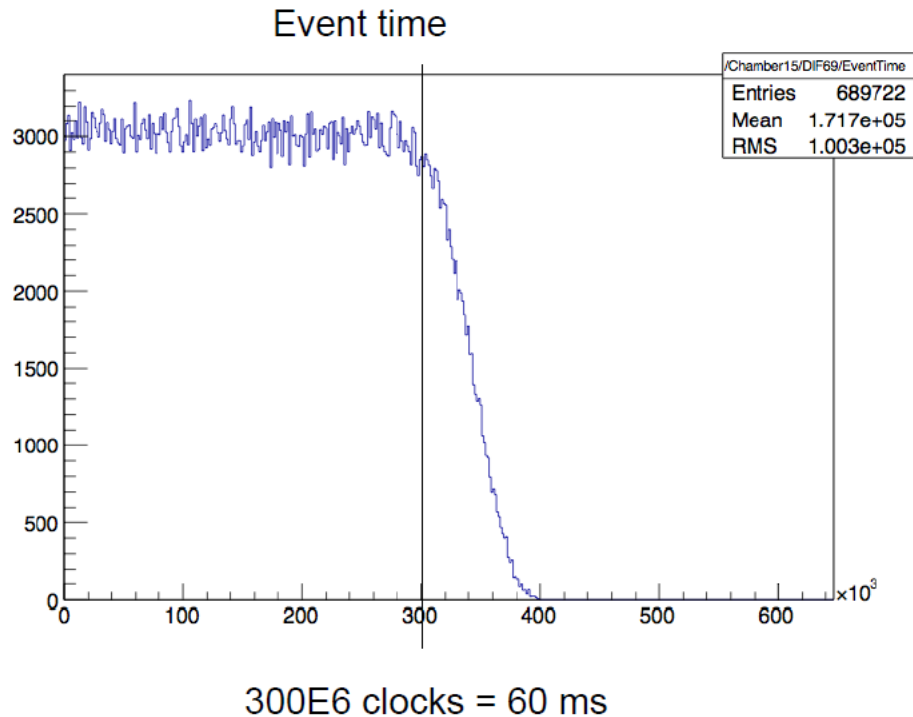
- Communication between PC's
- Event builder
- Global manager

→ XDAQ :

- Communication framework
- CMS Event Builder
- HTTP access to all applications
 - Browser view
 - Web2 (HHTTPRequest/SOAP) access to the applications

Performances

Cosmic data taken in ILC Mode



On 14/02 : memory depth = 60ms

For this run : 7185 readouts in 3314 seconds ie 1 readout each 461ms

And 4434 tracks found according to analysis configuration (5 pts per track)

Perspectives

The current DAQ is performing well enough fo the coming beam tests

Current developments are

- *Software implementation of MicroRoc calibration procedure and analog readout*
- *Power Pulsing*