MICROMEGAS

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CALICE collaboration meeting
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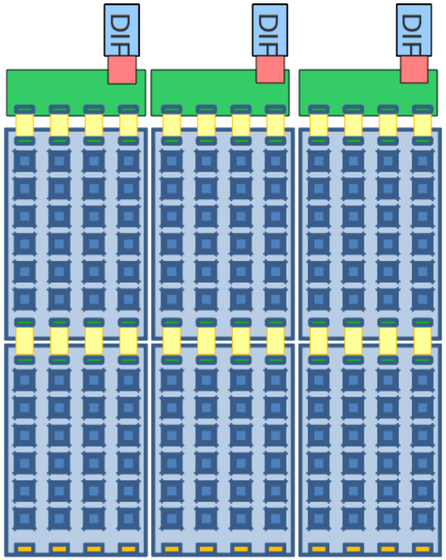
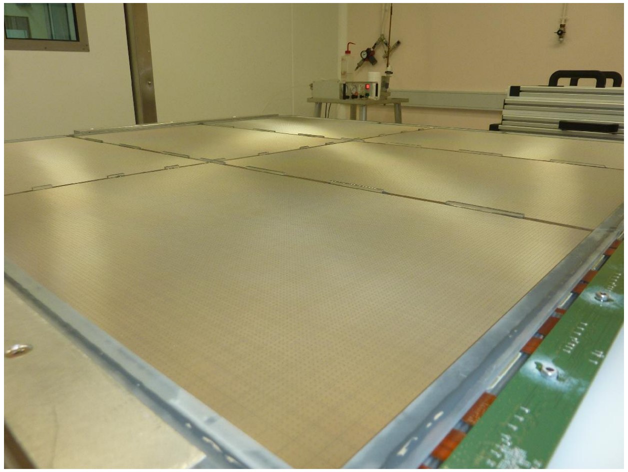
Overview

1. MICROMEGAS : performances, operation
2. Scalability
3. Open R&D issues

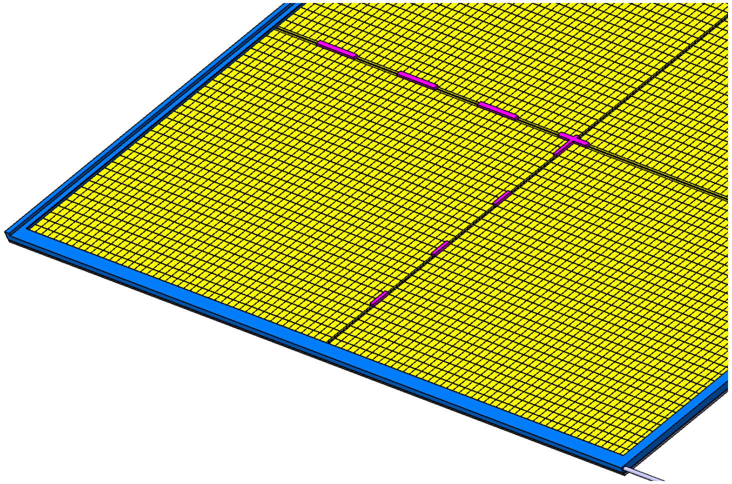
The MICROMEGAS 1 m^2 prototype (1/2)

- Mechanics: 6 ASU with flexible interconnections
  - 96x96 = 9216 pads of 1 cm^2
  - 2% dead areas
  - <1 cm thick chamber, including only one 2 mm Fe top ASIC side is gas tight: active thickness : < 8mm
- Electronics: 144 MICROROC ASIC
  - Noise RMS of 0.25 fC, 50-200 ns shaping, improved spark protections
- At LAPP : 2 large area MICROMEGAS , 4 in fall 2012

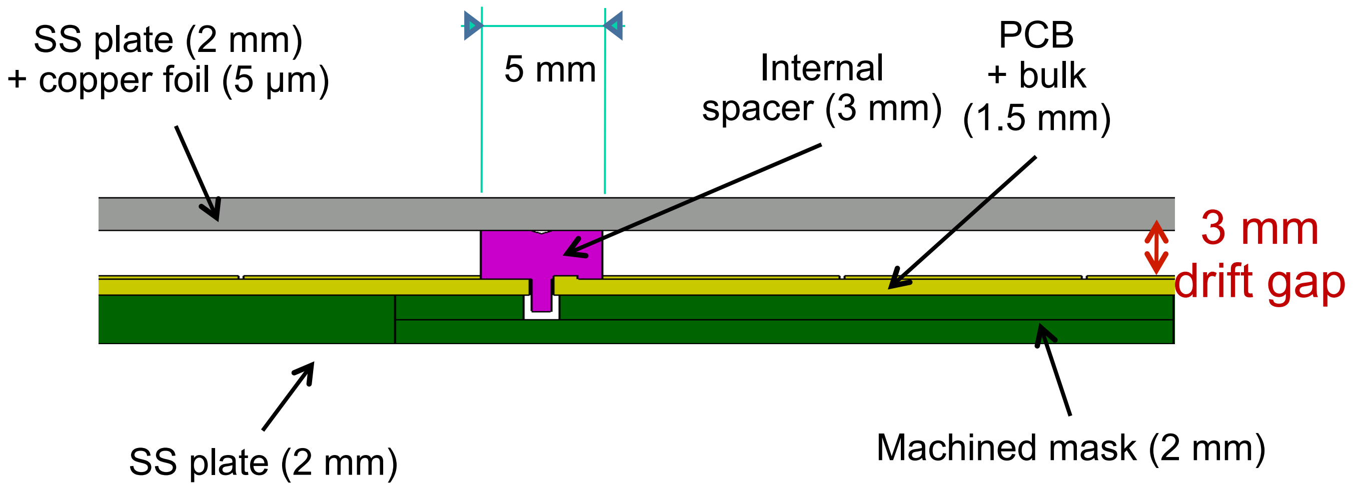




The Micromegas 1 m^2 prototype (2/2)



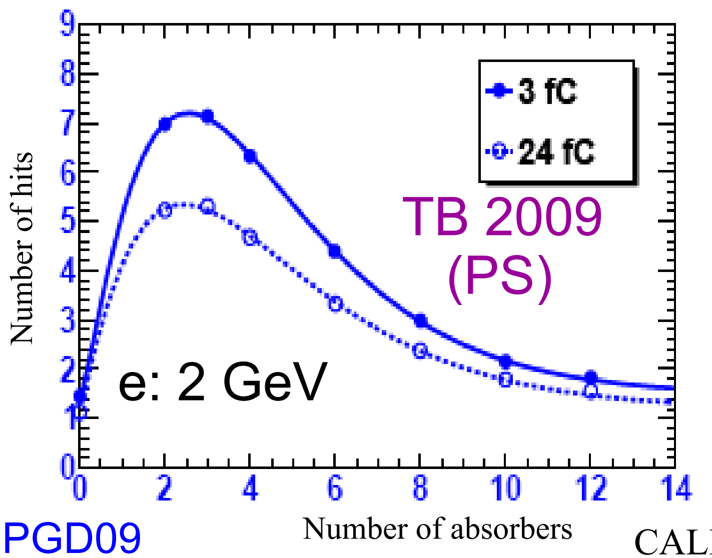
frame + internal spacers
fix the 3 mm drift gap



8.5 mm thickness + glue + tolerance = 9 mm total thickness

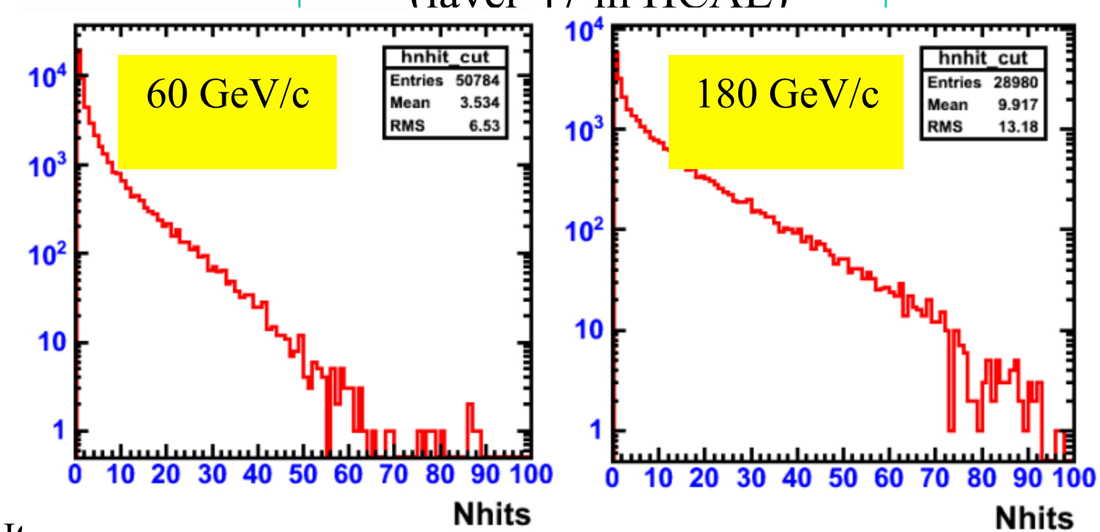
MICROMEGAS Performances

- Large area MICROMEGAS has same performances than mall analog readout prototypes.
- working voltage of 390 V with Ar/CF4/iC4H10 95/3/2
  - gas gain of ~3000, Efficiency = 98 %, hit multiplicity = 1.15
- EM showers in mini calorimeter
- Uniformity : ~ 1% relative variation on the efficiency
- Response in hadronic showers



MPGD09

Pions after ~ 5 λ_{int} of Fe
(layer 47 in HCAL)



Prototype operation

- Non-flammable mixture Ar/CF4/iC4H10 95/3/2
- Very low first threshold and very low noise thanks to MICROROC pedestals offset correction
  - 64 offsets and 3 thresholds per MICROROC are set to get minimum noise hit rate over all 9216 channels
  - Noise = 0.1 Hz on the complete $1m^2$
    aligned rate*Nchannel*threshold_plus_3DACunits
    $= 10^{-2}.10^{4}.10^{-3}$ Hz
- Number of masked channels:
  16 (6 hardware + 10 shoftware) < 0.2 %
- During more than 2 weeks in 2011 TB: less than 10 trips on the m^2 despite high intensity pion beam focused on 2 pads (RD51 users)
- No dead channels! actual spark protections is efficient.
- Pressure and temperature dependency can be removed by online HV correction

Scalability

- Actual 1 m^2 MICROMEGAS can be increase in both directions:
  - Assembly procedure should be defined
  - Drift cathode may be segmented
- ASIC power consumption can be reduced with achieved detector gain, power-pulsing already implemented
- DIF+interDIF area can easily be reduced:
  - DIF design can be easily optimised
  - Merge DIF+interDIF (may be some part on the ASU : HV…)

Open R&D issue

- This year test beam will give us data for comparison with simulation and optimisation of simulation
- Actual SMD for spark protection should be integrated in PCB, ASIC and/or spark energy and rate should be reduced (resistive MICROMEGAS) : ANR SPLAM
- MICROMEGAS bulk technology is using industrial processes :
  main issue for industrialisation is to have one industry being able to do all processes : this is underwork within RD51

Conclusion

- Does not belong to myself!

Acknowledgements

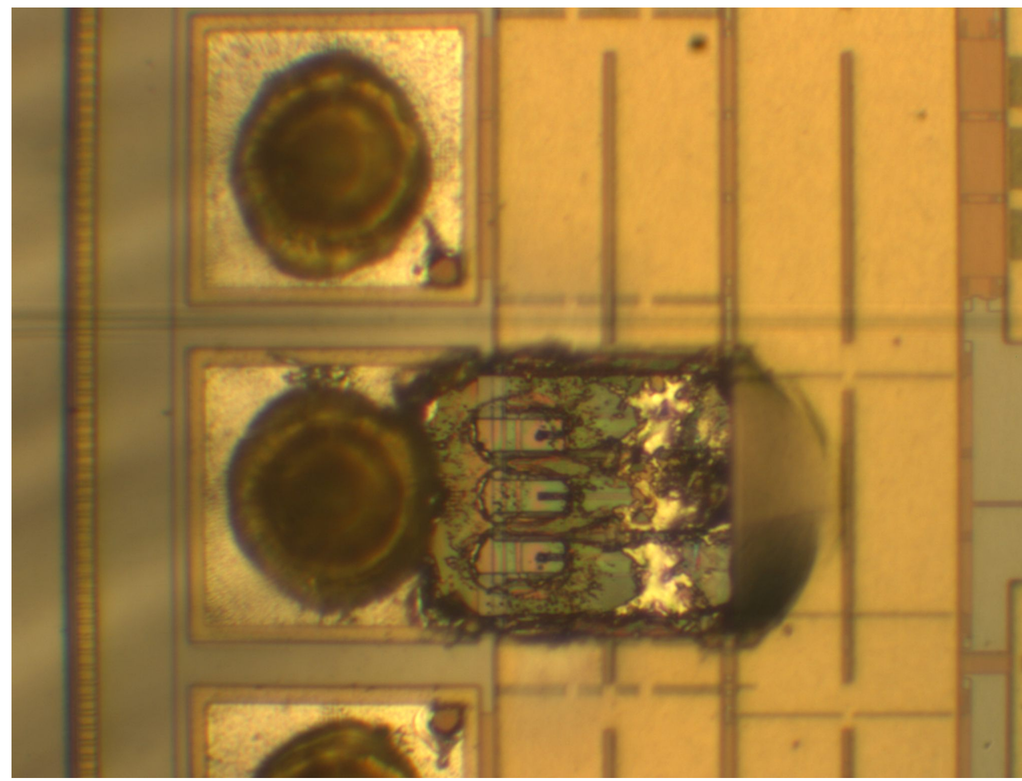
- LAPP
- IRFU
- CERN, TS/DM
- LAL/Omega
- IPNL
- CIEMAT

Discharge studies and protection

Road map against discharges :

1) Quantify discharge parameters (energy released, dead time to recover voltage on the detector...) using well known discharge physical mechanism:
    1) Measure detector electrical characteristics.
    2) Simulate detector behaviour during discharges (mesh PCB)
2) Design and optimise protections
    1) at the detector level : PCB, resistive MICROMEGAS
    2) At the ASIC level

in order to protect against that



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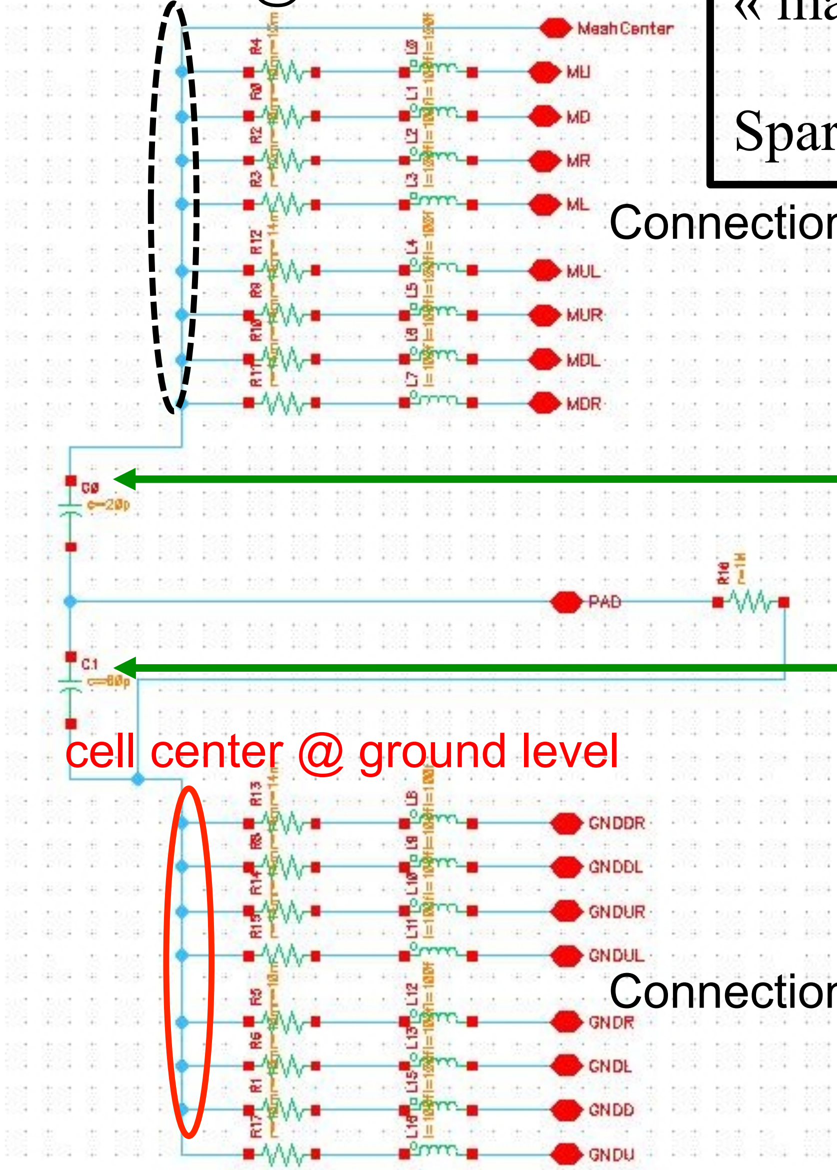
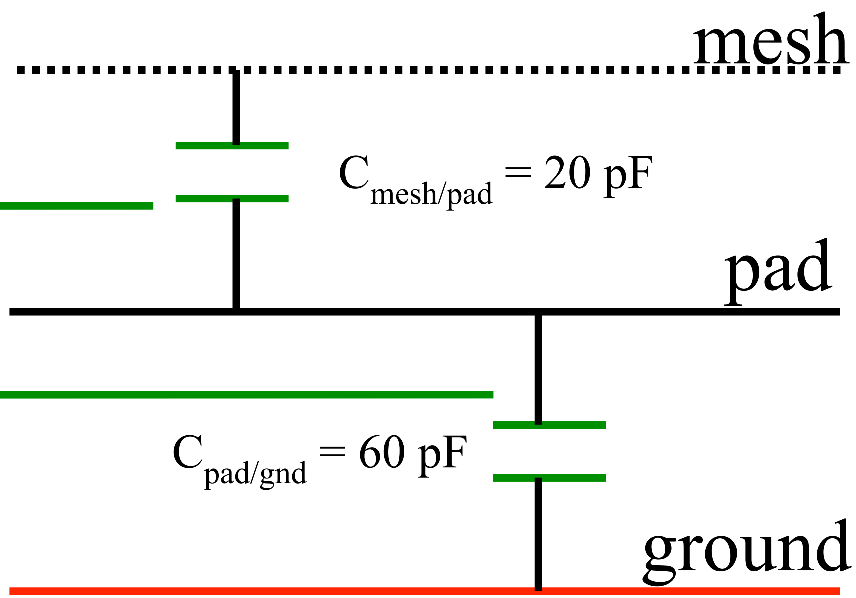
First simulations

Simulations with SPECTRE from CADENCE:
« manual « FEA: elementary cell (1 cm^2) of mesh-pad-ground
Sparks : switch mesh/pad

cell center @ mesh level



Connection to neigbour cell (mesh side)



cell center @ ground level

Connection to neigbour cell (groud side)

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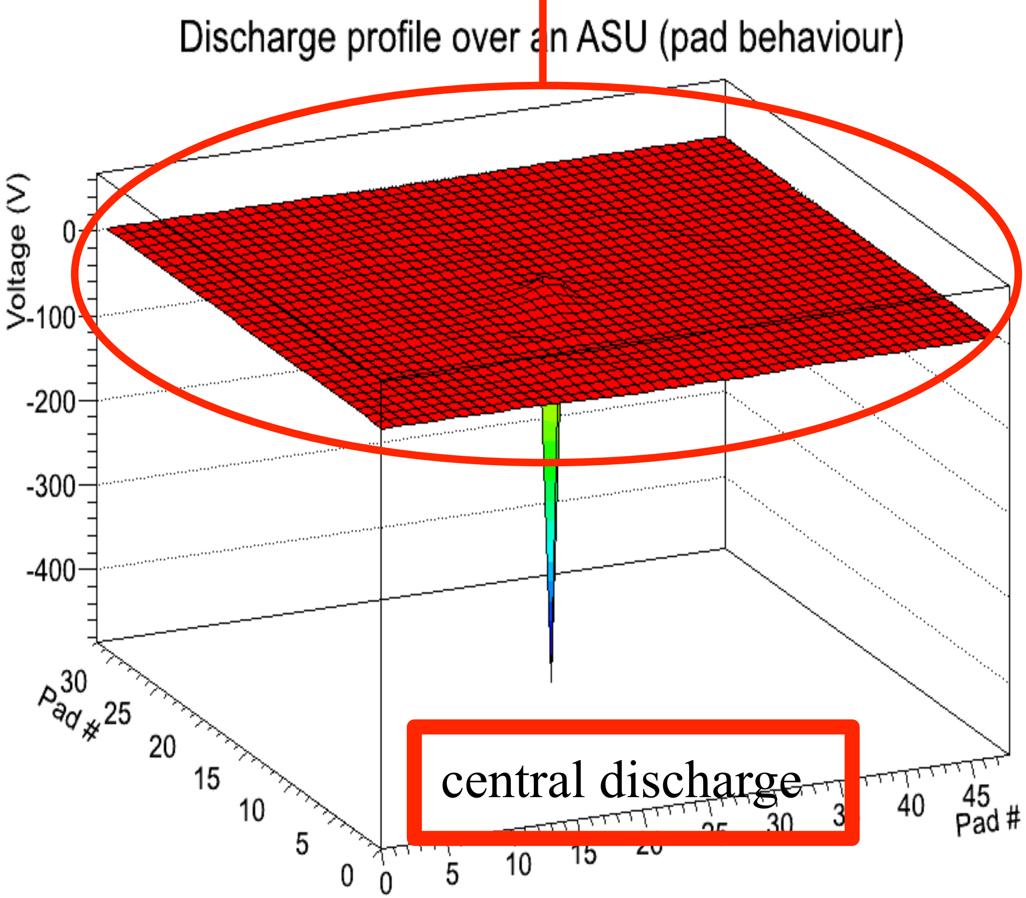
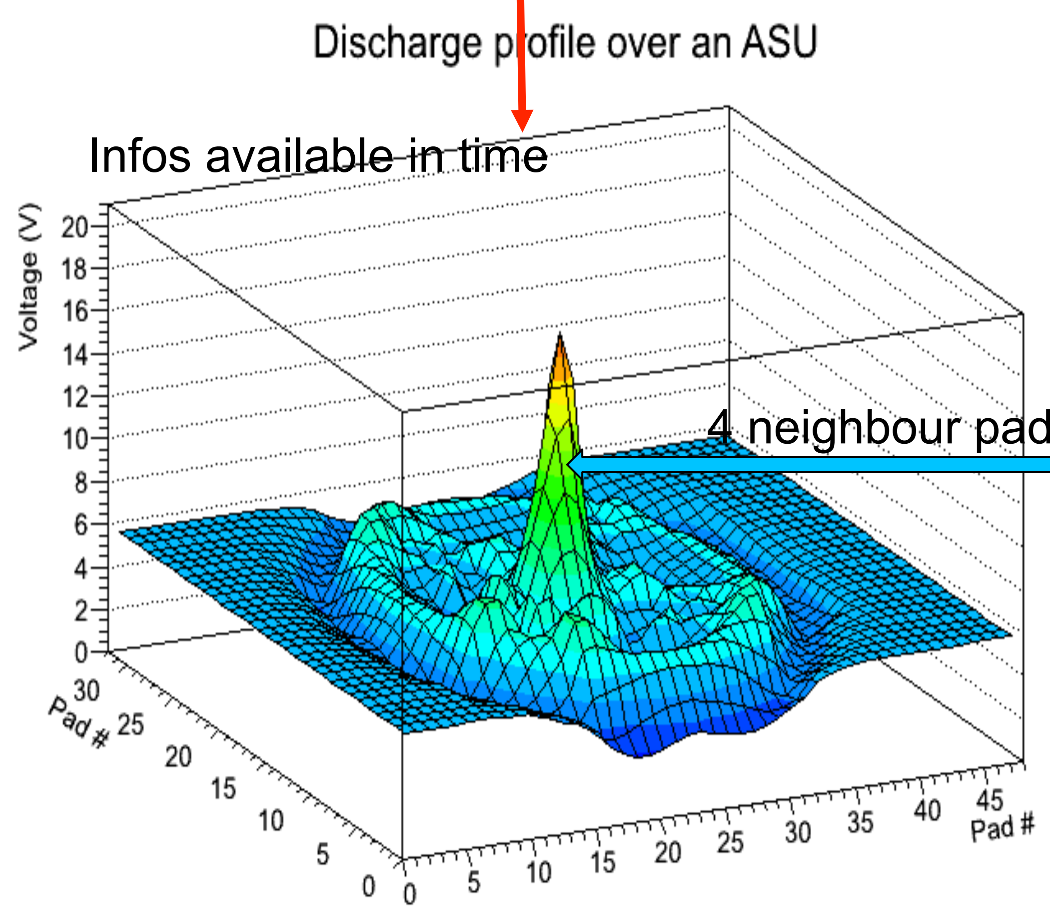
Example : pad maximum voltage value
(32x48 pads plane)





"discharge pad" goes to mesh voltage (-400 V)

Neighbours pads compensate with positive voltage (from 6V for the farer pad to 20 V for the closer ones)

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Status

Simulation with 1 cm^2 cell : ok

Complete ASU simulation without resistif : ok

Simulation with $(11/10\ mm)^2$ cell

Additional layer implemented

Resistive and/or capacitive layers:
comparison possible

Complete ASU simulations with resistive layer :
ongoing