News about DAQ2

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DAQ2 (autumn 2010)

Decision to not change the UK baseline

- No redesign, keep LDA & DIF, connectors
- Coherence with work already made within CALICE
- THIS SHOULD BE CONSIDERED AS AN EXERCISE : going at the end of the work initiated by UK groups

Decision to not use ODR

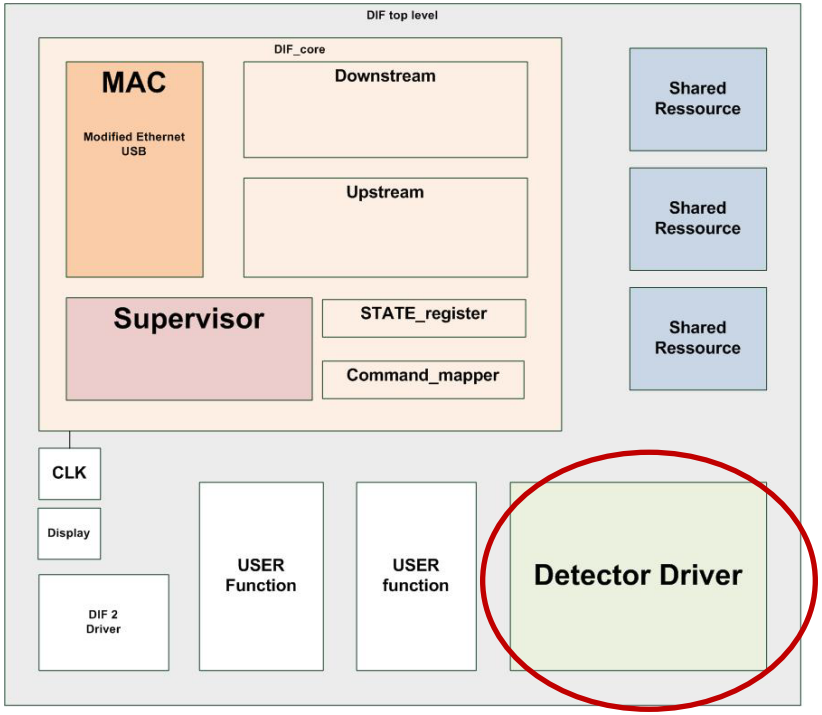
- One less card to understand
- Software « simplification » (standard lib, Ethernet stack of OS kernel)
- Known Limitations on bandwidth & performance (/4 compared to ODR tests)

Set up of a first version of DAQ, TFC & SC LLR & LAPP

- ~success SDHCAL@CERN-PS in **July'11**: in less than 1 yr : 300k channel detector read out (even if the system is not so stable)
- Limits, bugs, improvements to be found & understood
- NEXT STEP : ~free to play and change things

Attempts to understand instabilities of DAQ2.0

- Based on the latest SVN version (July'11, aka V2 as a part of DIF DEV3.0), do not take into account modifications done during/after the move from PS to SPS (SDHCAL@CERN)
- Concentrating on DIF only and on ROC interface in particular



Attempts to understand instabilities of DAQ2.0

- 1st test : start/stop DAQ using CCC orders
  - Equivalent to start/stop SPILL
  - After a stop : random break of FSM cycles : 4 possibilities
    - "error1" flag (I don't know the meaning)
    - Remain in Acquisition state
    - Both
    - Status "C" : rare, not investigated
  - Recovery
    - Reset chips : remove permanent ramfull/chipsat state (Acquisition cannot restart)
    - Reset DIF (need to reconfigure)
  - 4 possibilities after recovery
    - The DIF reset put chips into ramfull/chipsat state (let's try again to recover…)
      - Need to switch off power supplies : firmware reload, sometimes put chips in ramfull/chipsat
    - Resets are ok but the loading of the SlowControl puts chips in ramfull/chipsat state
      - Need to try again or to switch off power supplies (with same risks)
      - Need to stop CCC, unless it will attempt to restart ASAP => may put chips in ramfull/chipsat
    - Resets are ok but the acquisition restart only once
      - Chips remains in ramfull/chipsat after the second startCONV
    - Resets are ok, SC is loaded, everything OK
  - High probability to be UNABLE to recover. It increase with the number of SLAB/ASU/HBU => most probably what we saw during summer'11

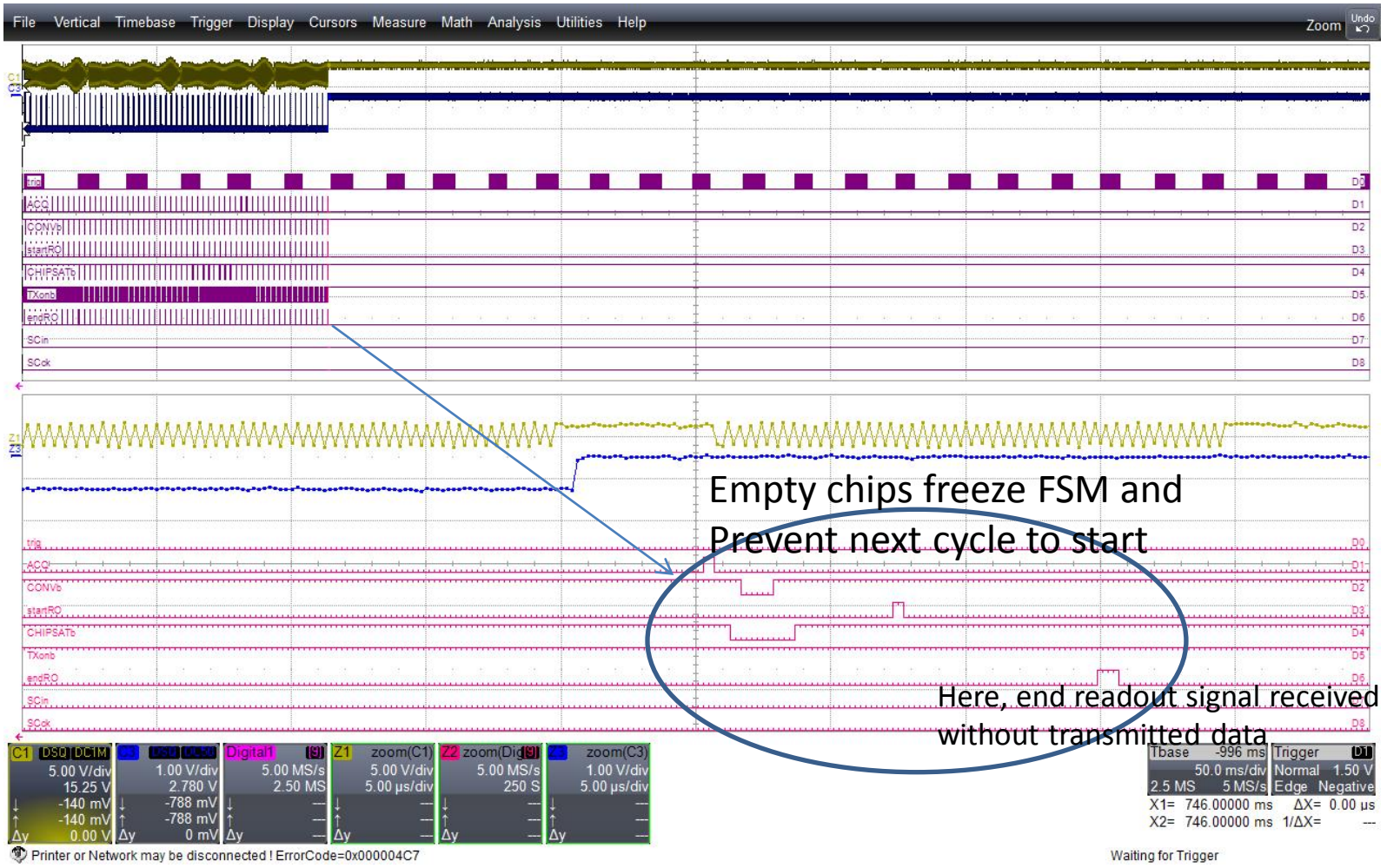
Based on real measurements

Attempts to understand instabilities of DAQ2.0

- 2nd test : stability of DAQ cycle
  - The cycle is driven by CCC with respect to BUSY
    - CCC start cycle at first
    - CCC stop acquisition when BUSY'start (the first busy received)
    - CCC restart when BUSY'stop (the end of last remaining BUSY)
  - After a startCONV, a chip may remain in ramfull/chipsat
    - Permanent BUSY : the cycle never restart
    - Need to reset : see previous slide
    - This ~never occurs in high gain configuration
    - Occurs after 100-1000 cycles in low gain configuration
    - Only solution : power off…(see 1st test…)
    - Not really understood
- CCC AC adaptation outputs non standard LVDS levels, slow transient may cause glitches
- CCC inputs are TTL 5V : triggers can be missed in TTL 3.3V
    - Acquisition stops (test beam mode) with chips empty (see next)

Breaking of DAQ cycles

DAQ cycles



Trying to fix DAQ2.0

- Found major bug
  - Trigger used to stop acquisition in beam test MODE
  - Sometimes it stops FSM before the trigger can be taken into account in the chips
    - Chips empty
    - Read-out FSM frozen
    - Need to reset….
- Fix July'11 version with December'11 version (aka V3, as a part of DIF DEV3.1)
  - Adding timeout and watchdogs
  - "improved" timings (delays, pulse duration)
  - Fix trigger bug in beamtest mode
  - Currently running for weeks without problems on ECAL
    - tests : setup with 1 or 2 SLAB(s) only…
    - Still high complexity of ROC interface : optimization needed

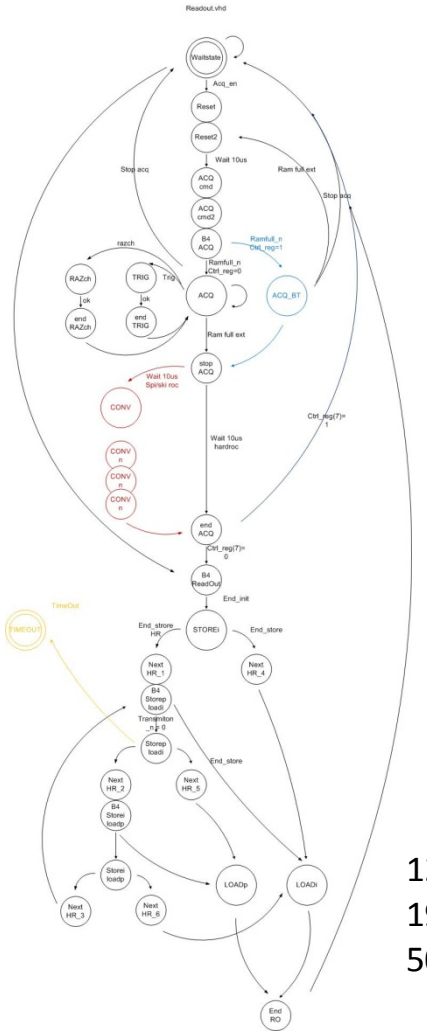
ROC interface rewritten from scratch (aka V4)

- Same time domain as for chips, follow ILC cycle (acquisition-conversion-readout-idle), compliant with datasheet timings
- Simplified FSM (5 states instead of 22)
- Completely new slow-control bloc using shared RAM, saves 15% time for loading chips parameters
- Usage of FPGA logic resources optimized by a factor 6, no specific RAM
- Implements Power pulsing
- Compatibility with most chips
- Initial flavor of V4 is being tested now on ECAL
  - As a part of an improved DIF version (aka DEV4.0)
- DIF DEV4.0 includes monitoring (statistics) and warning messages (in ascii !), new formatting of readout data (ascii tags, readout stats)
  - Advanced features to be debugged, do not prevent this version to be used
  - Baseline for forthcoming SKIROC2 chips for the ECAL.

ROC interface V4

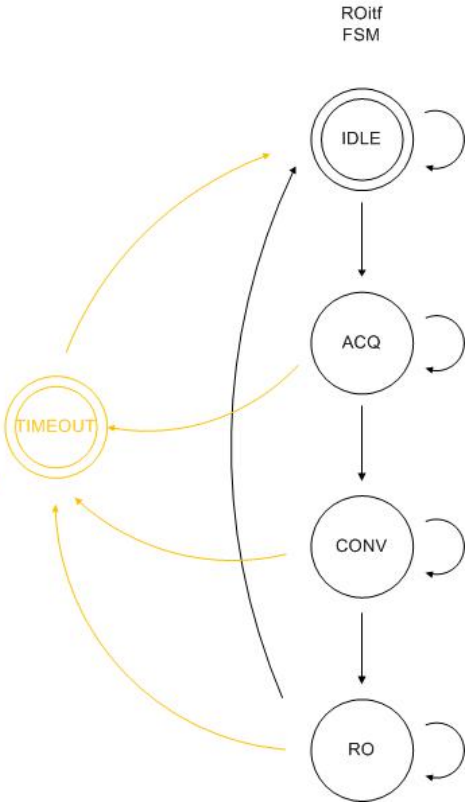
A first step toward simplification and system level optimization

OLD FSM
(V2)



Factor 6 gained
on complexity
(FPGA cells)

NEW FSM
(V4@LLR)



12% of ECAL DIF (RO & SC) :
1900 cells, 1270 FF
50% RAM

2% of ECAL DIF (RO & SC) :
383 cells, 325 FF
0% RAM

Conclusion

System is being improved and CAN be used

- Brainstorm for system level improvements of DAQ2 , started with DIF
  - **No changes in architecture** (may not be optimized for ILD)
  - Will make a proposal soon (discussion started with CCC@Mainz) : new cycle method, …
- With the help of everybody (designers and users)
  - Already have some ideas
- USE it (instead of using something else) and report/diagnose/solve bugs

DAQ2.1 2.2 2.3… ?

- Documentation and specifications…
- New LDA (GDCC)
- New CCC

Poor software (~scripts) need URGENTLY to be improved

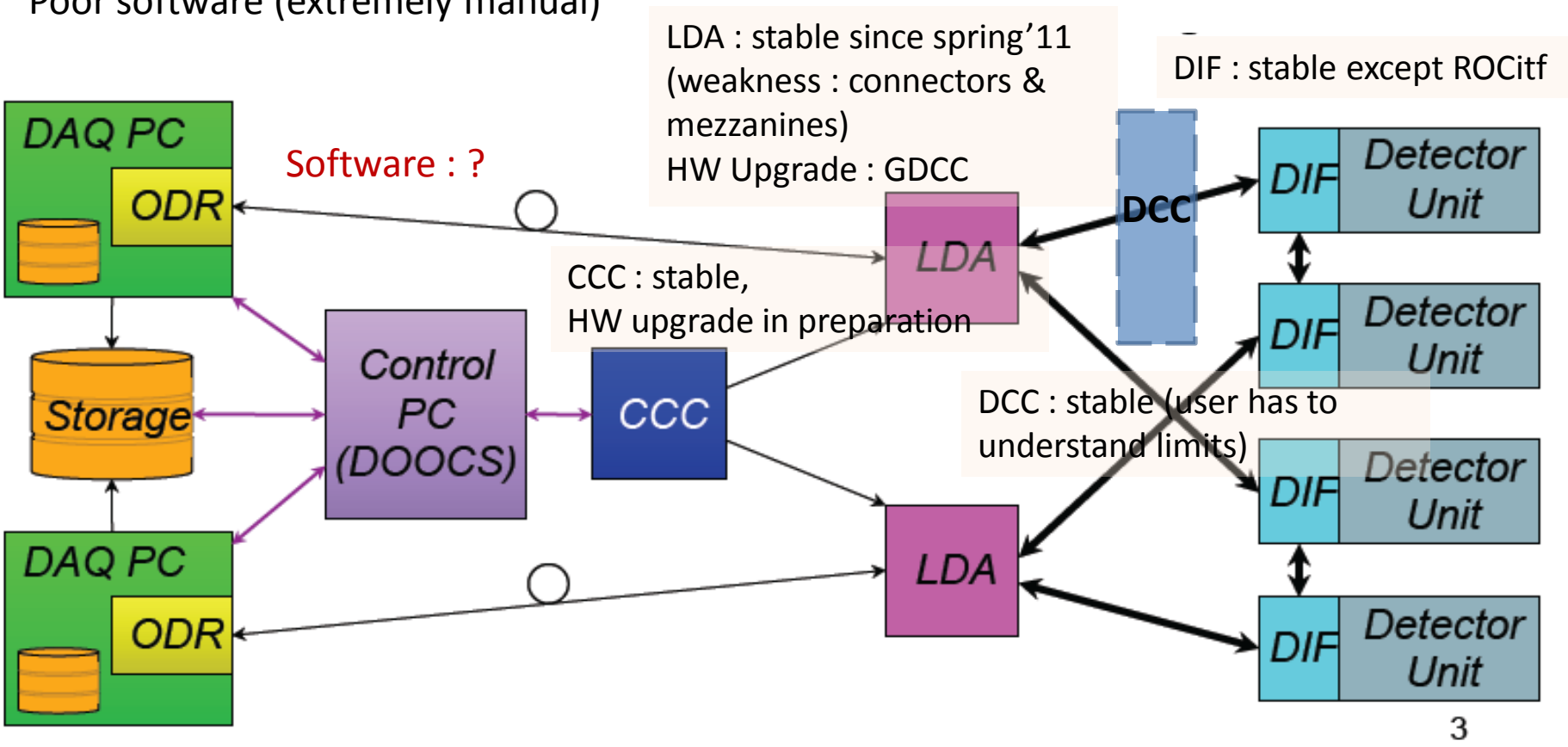
DAQ3 ?

- New architecture ?
- New connectors ?

Conclusion 2/2

Overall system : need a general upgrade (weakness : robustness to errors, sync, buffer saturation)

- Will implement control layer (feedback mechanism) on serial link
- Will redefine functioning principle (DAQ automatic loop, trigger, clock…) : suppress existing correlations among subsystems which should be independent
- We don't have enough detectors to perform tests with large setup
- Poor software (extremely manual)

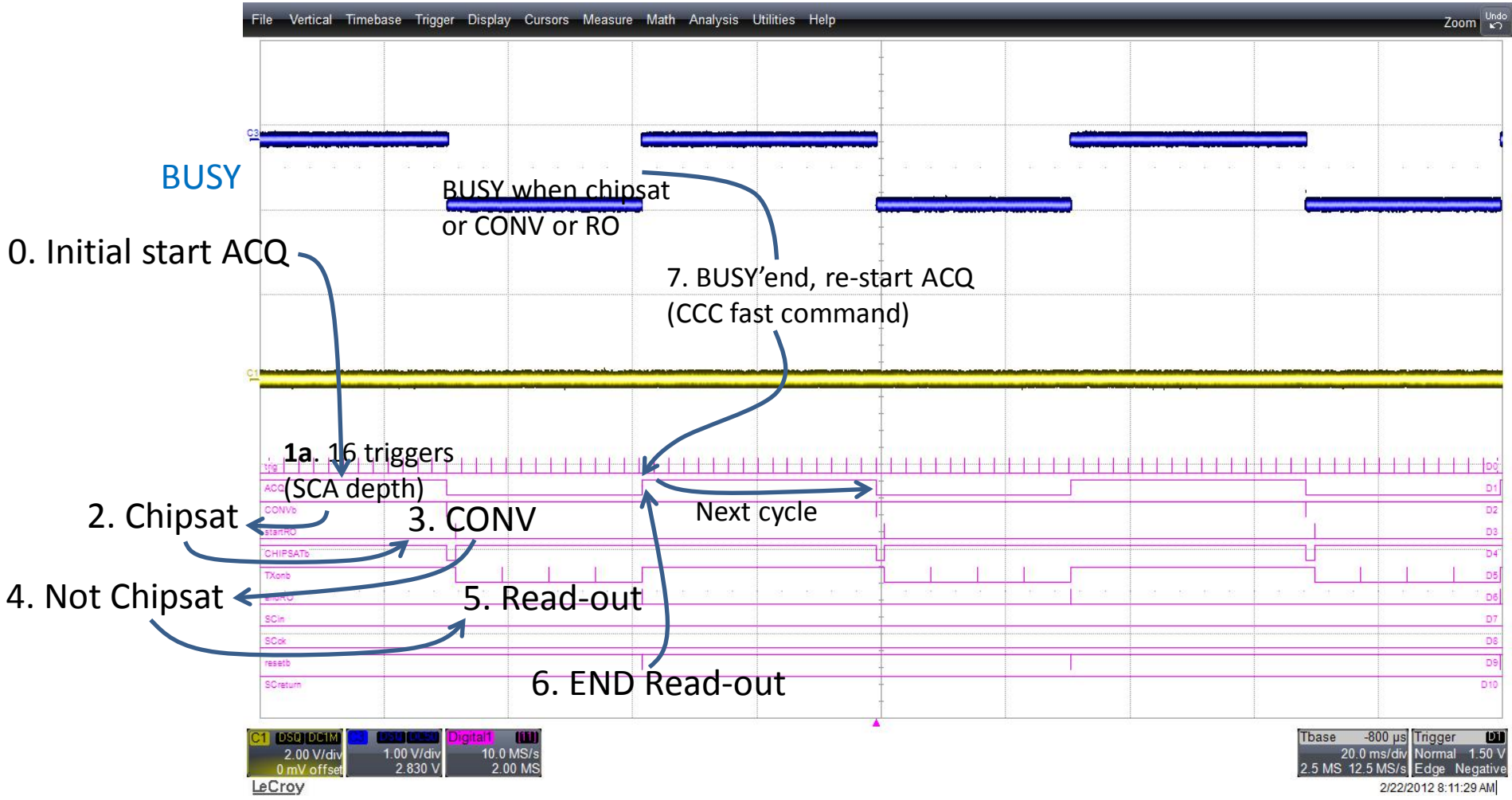


SPARE

How it is working ?

Measured on SPIROC2

- AUTO ILC mode, trigger @ 1MHz and more



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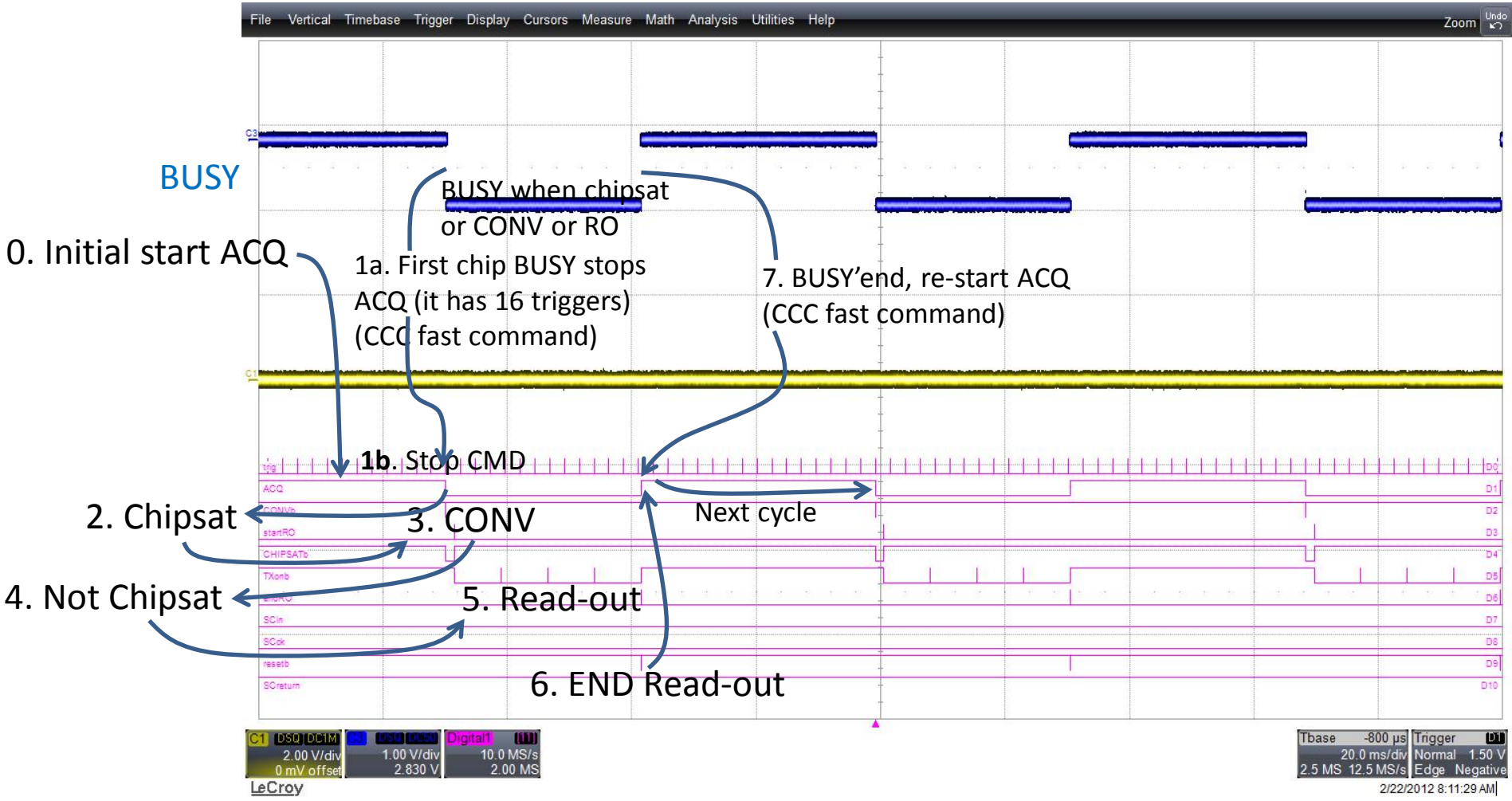

How it is working ?

Measured on SPIROC2

- BEAM TEST MODE , first trigger(local) stops ACQ (@1/ROtime Hz)