Status of the AHCAL engineering prototype - Summary

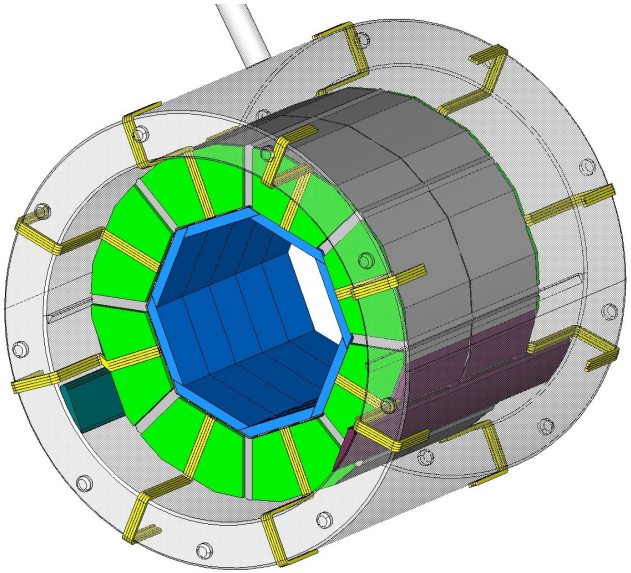
Mark Terwort

CALICE collaboration meeting

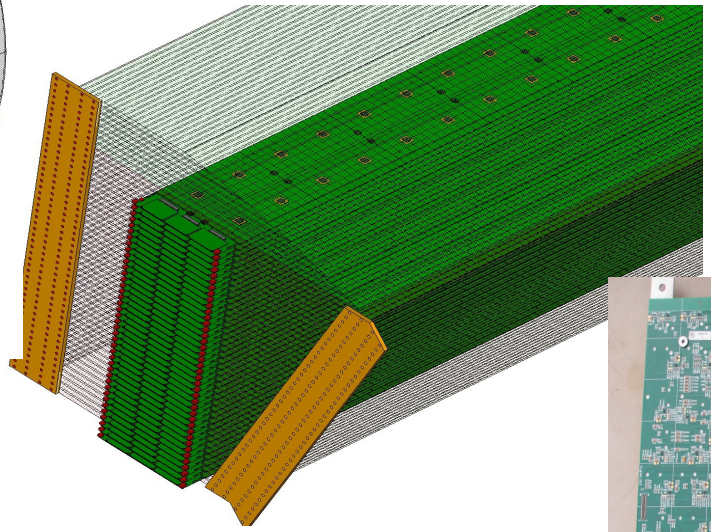
Matsumoto, March 6th, 2012

The engineering AHCAL prototype

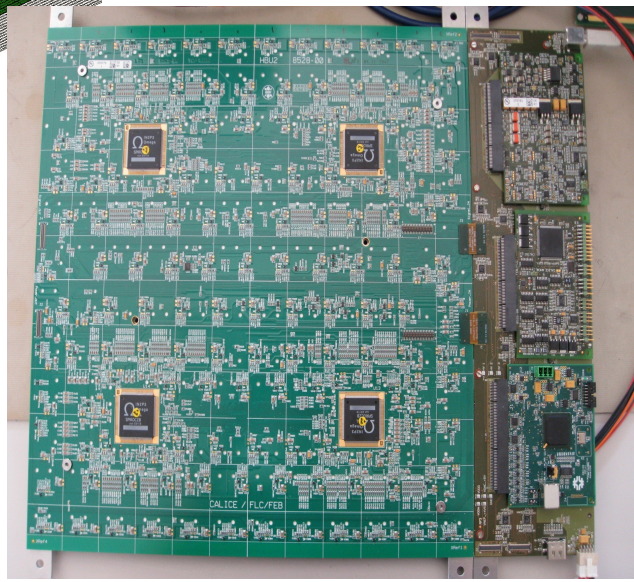
Development of **scalable LC detector** based on successful experience with physics prototype



Octagonal shape, 16 equivalent wedges, segmented in two along z



PCB with 4 ASICs, 144 scintillator tiles, SiPM readout



Challenges:

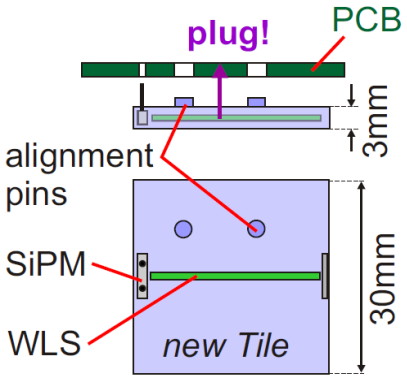
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

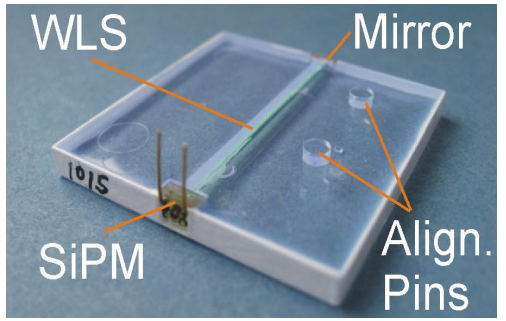
→ Integrated readout electronics

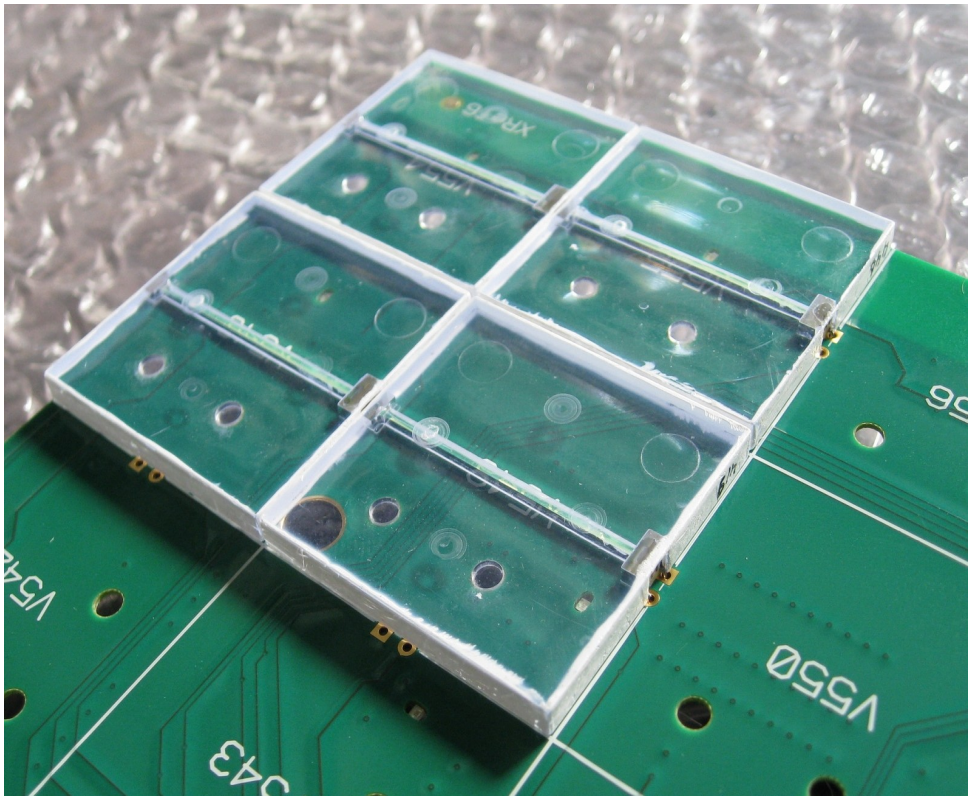
Scintillating tiles

- Signal sampled by scintillating tiles
  → 3x3x0.3cm^3, 2592 tiles per layer
- **450 tiles** from ITEP tested
  - Gain: **500k – 2000k**
  - Light Yield = **15 ± 2**
- Sample of 150 tiles in Heidelberg for characterisation of temperature dependence
- New batch of **470 tiles arrived at DESY last Thursday**
  → Equipment of several new HBUs

→ Important step to multi-HBU-setup now possible!

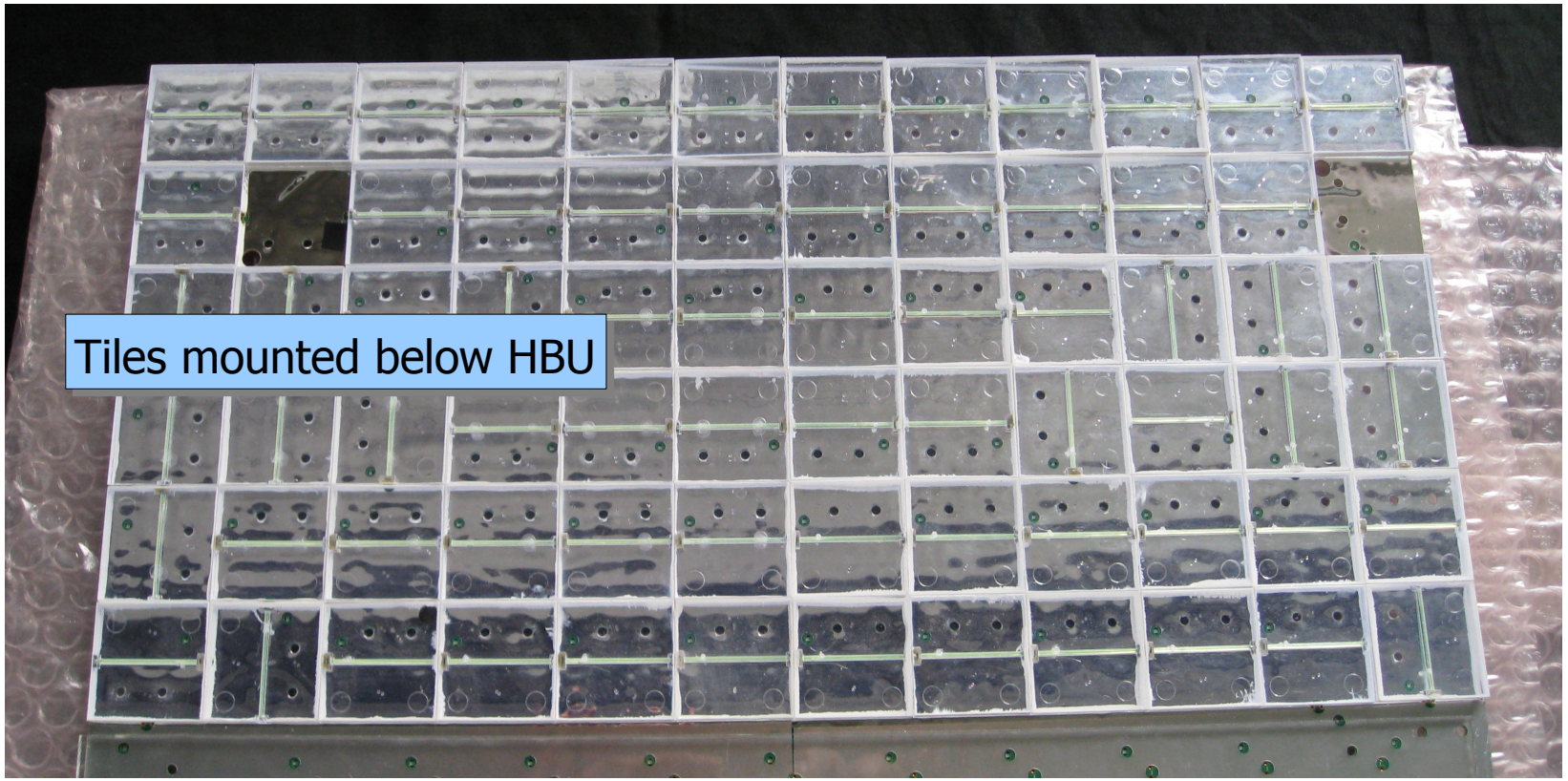






Scintillating tiles

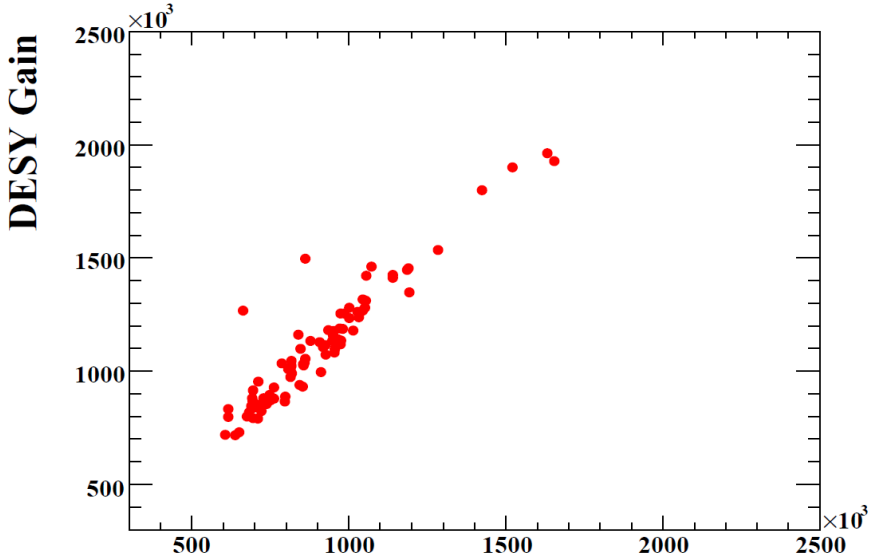
- 70 tiles mounted below new HBU2
  → Larger tests of calibration system and **SiPM gain in HBU2 environment**
  → Test of **light yield** in DESY test beam

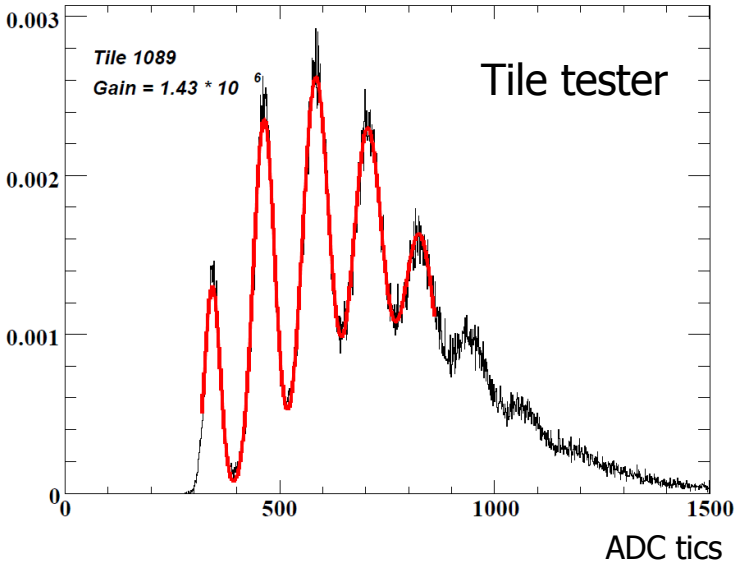


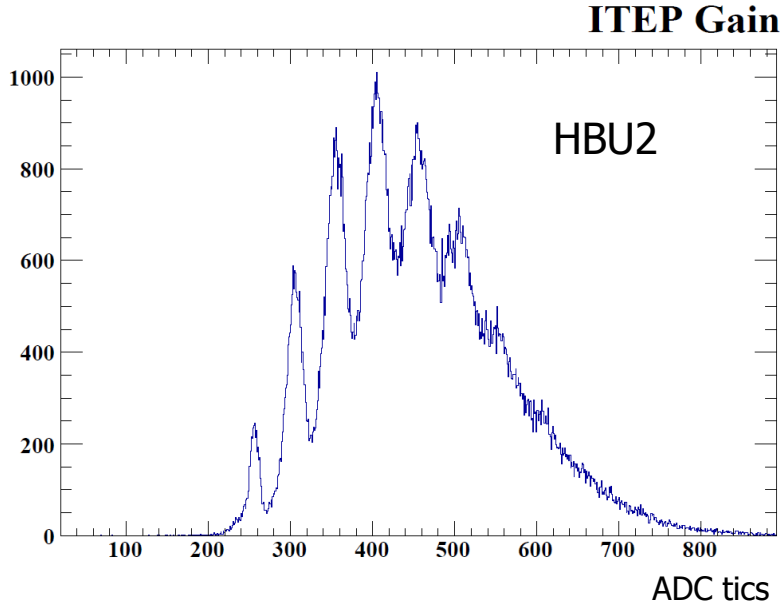
Scintillating tiles

- **Single-pixel-spectra** measured with dedicated tile tester and HBU2

  → Comparable performance!

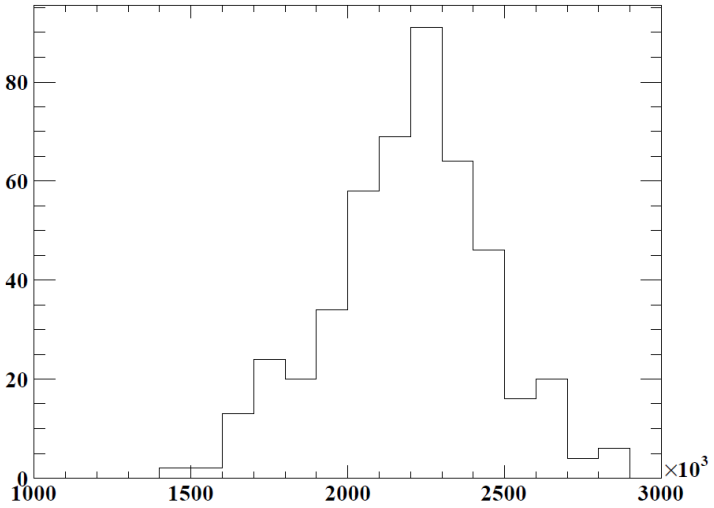




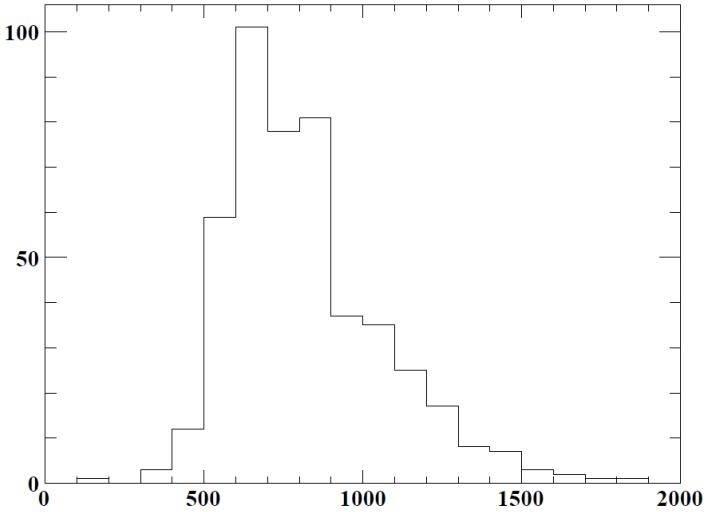


Tiles from last week

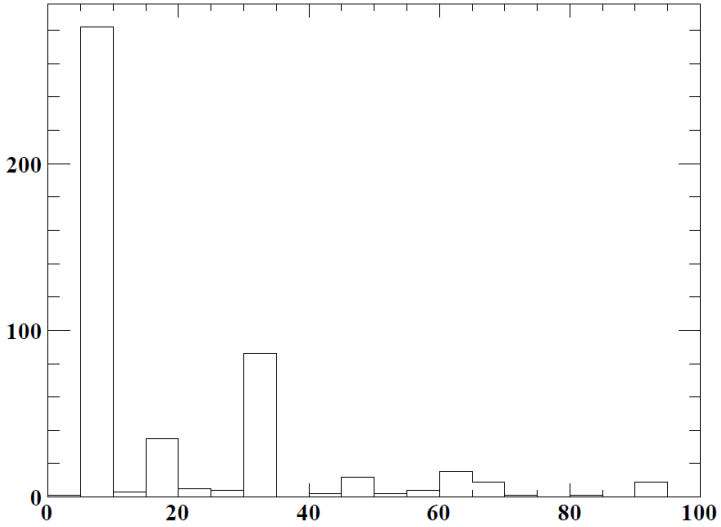
- Bias voltage of latest sample of SiPMs increased to **~47 V**, compared to **~37 V** of the last sample
- Gain increased significantly
- Noise frequency looks ok, have to **wait for single-pixel-spectra**



Gain



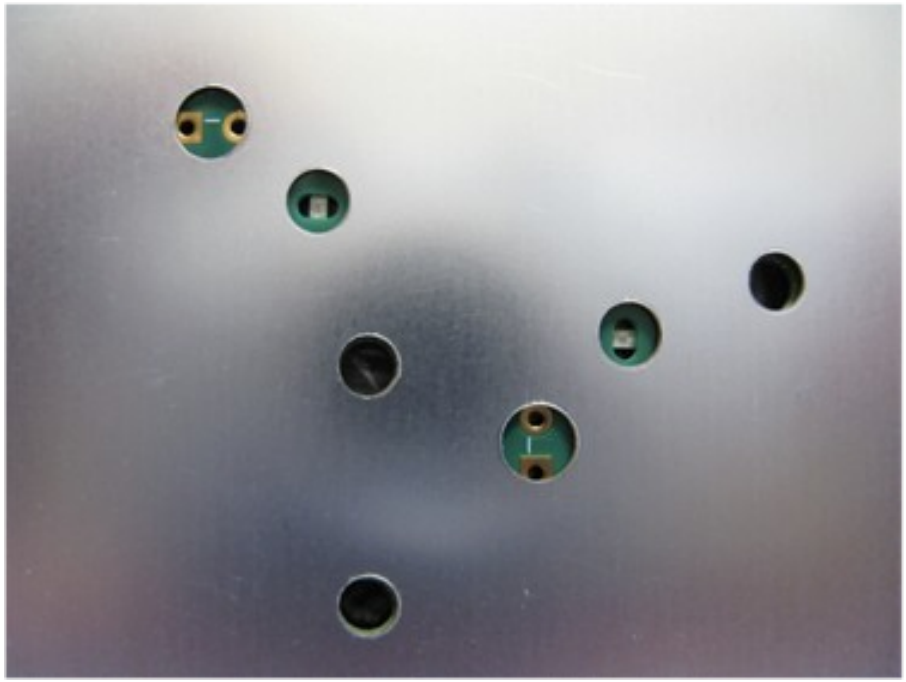
Noise frequency at 0.5 pixel threshold [kHz]

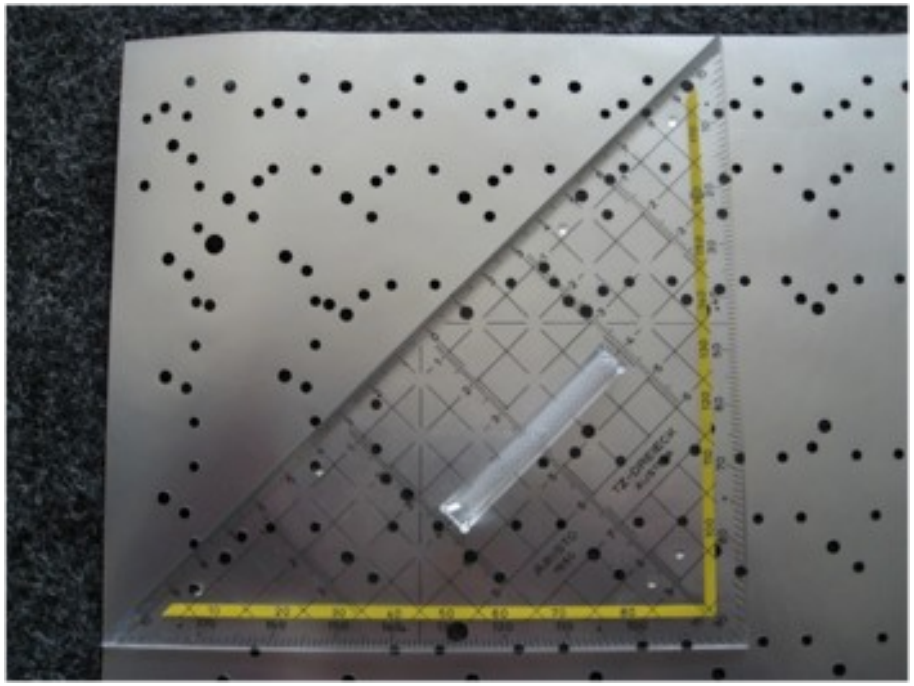


Noise frequency at 0.5 MIP threshold [Hz]

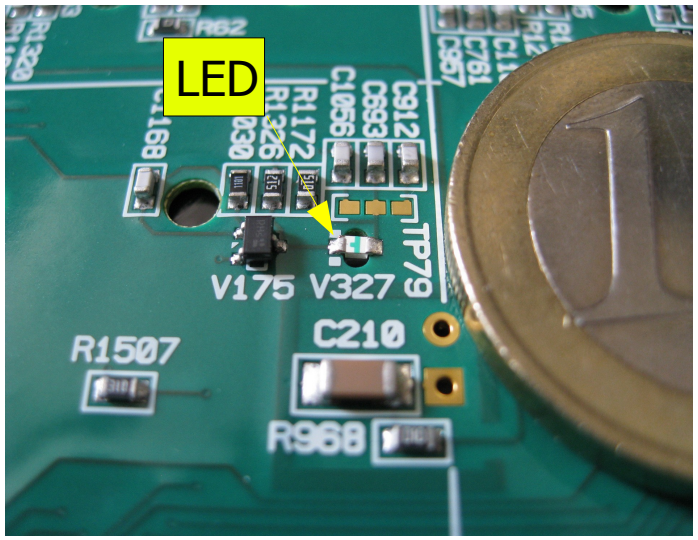
Reflector foils

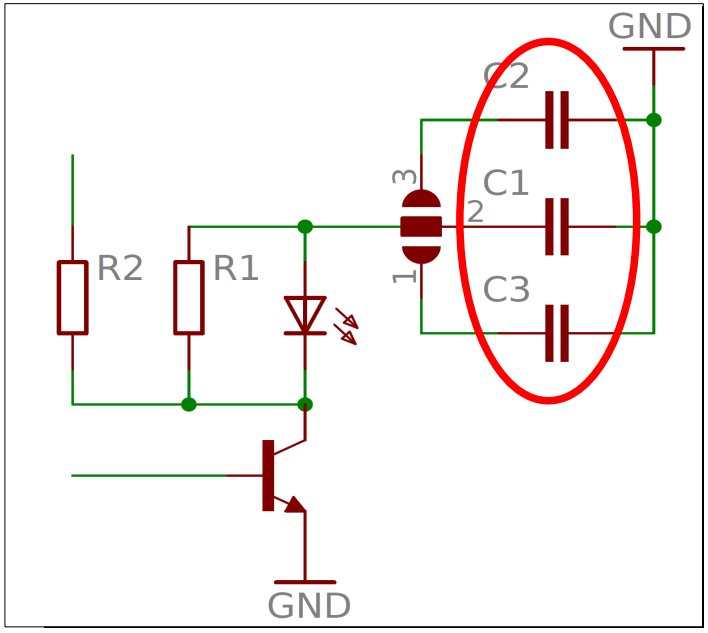
- **New reflector foils realized** (laser cutting), 4x top and bottom types
- Both types look promising:
  → Quality
  → Fit to HBU2





LED calibration system





Wuppertal solution:

- Light directly coupled into tile by 1 integrated LED per channel
- Light output equalization via C1 – C3 (default: 150pF, plus: 22pF, 82pF)
- New design implemented in HBU2 and is currently tested extensively

Prague solution:

- Light coupled into tile by notched fiber
- Mechanical integration difficult

  → First tests performed in DESY lab with new electronics and new tiles

Embedded LED calibration system

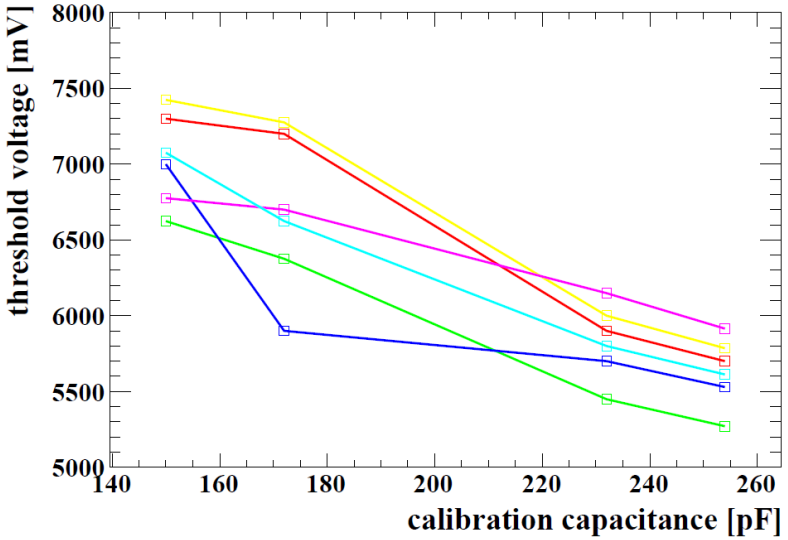
LED light output equalization:

- 4 bias capacitor combinations tested:

  → 150pF, 172pF, 252pF and 254pF

- Measured V_{CALIB} where light output starts

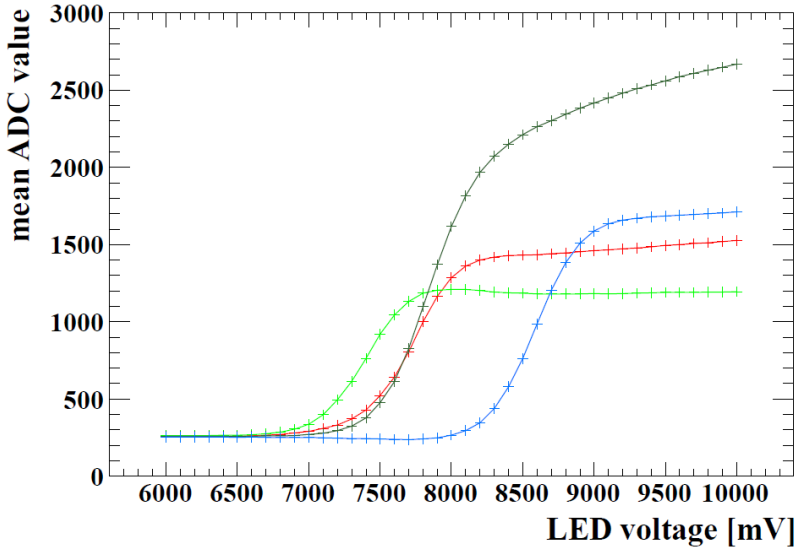
  → Improvement of LED uniformity possible!



SiPM saturation:

- Can the integrated LED system be used for SiPM saturation monitoring?

  → Tests with new DESY electronics prove capability!



The readout chip - SPIROC2b

Specific chip for SiPM readout:

- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

- Power pulsing → 25µW/ch
- Dual-gain setup per channel

  → high gain/low gain ~ 10

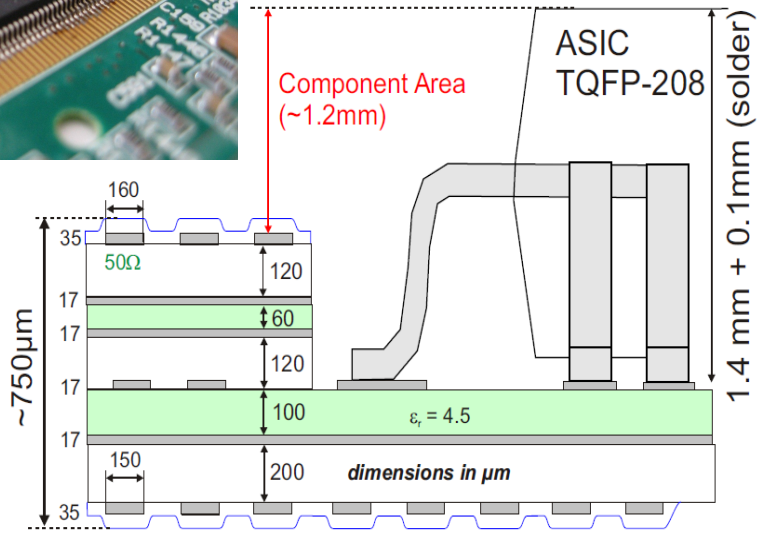
  → 25fF – 1575fF per channel

  (has been used in DESY test beam)
- Auto-trigger mode

  → channel-wise adjustable threshold
- Time stamp (12-bit TDC)
- Many aspects have already been tested and discussed and all (?) issues will be fixed in **SPIROC2c**

  → Still, most probably we will use **SPIROC2b** for next test beam

Designed by OMEGA/IN2P3



Placement of components in PCB cutouts

→ 500µm/layer

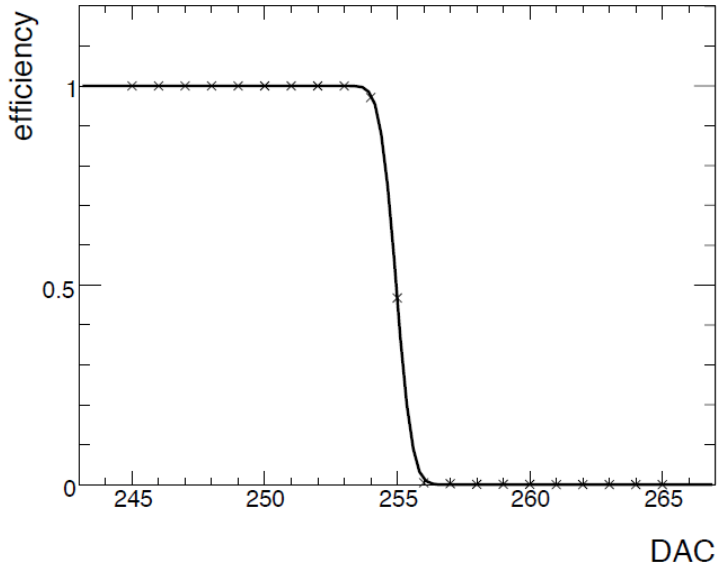
→ 50mm in total!

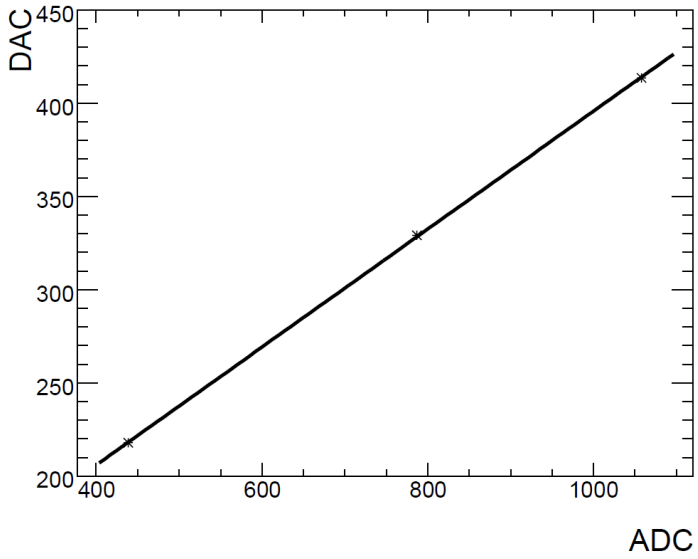
Channel-wise trigger threshold

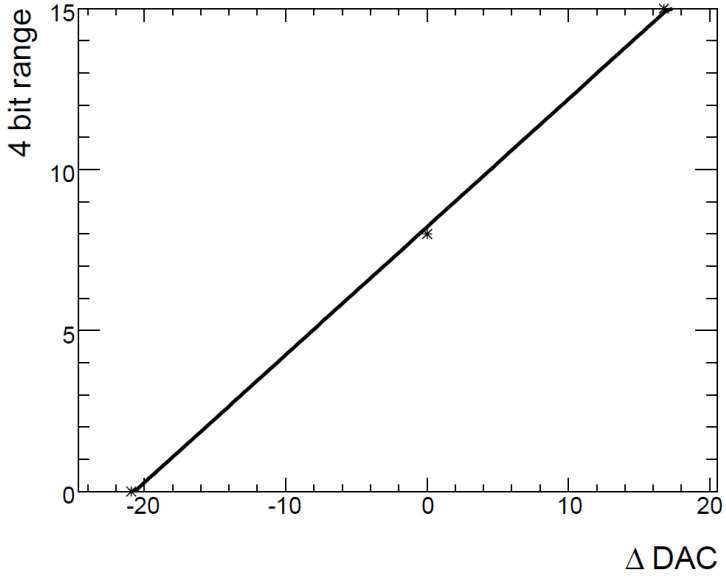
- **How to set online thresholds?**
- Autotrigger threshold in SPIROC2b:
  - 8-bit global threshold
  - 4-bit channel-wise tuning

    → **~1/4 MIP finetuning possible**
- Global threshold depends on finetuning!

  → Effect has to be compensated!







Channel-gain equalization

- **Where to set online thresholds?**

  → New tiles have SiPM gains between 500k and 2000k, with very uniform light yield around 15 pixels/MIP!

  → Channel-wise threshold tuning?

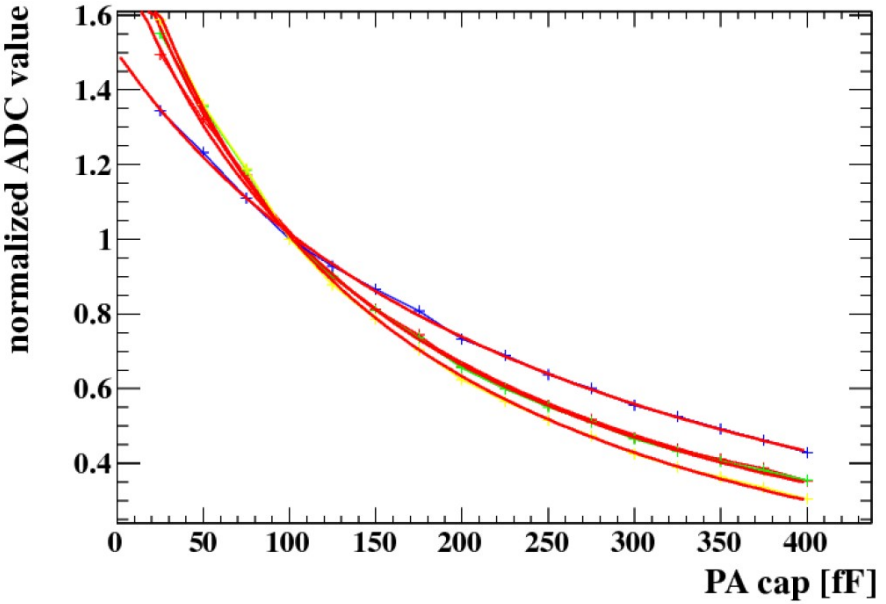
- Channel-gain equalization with pre-amplifier feedback capacitors possible

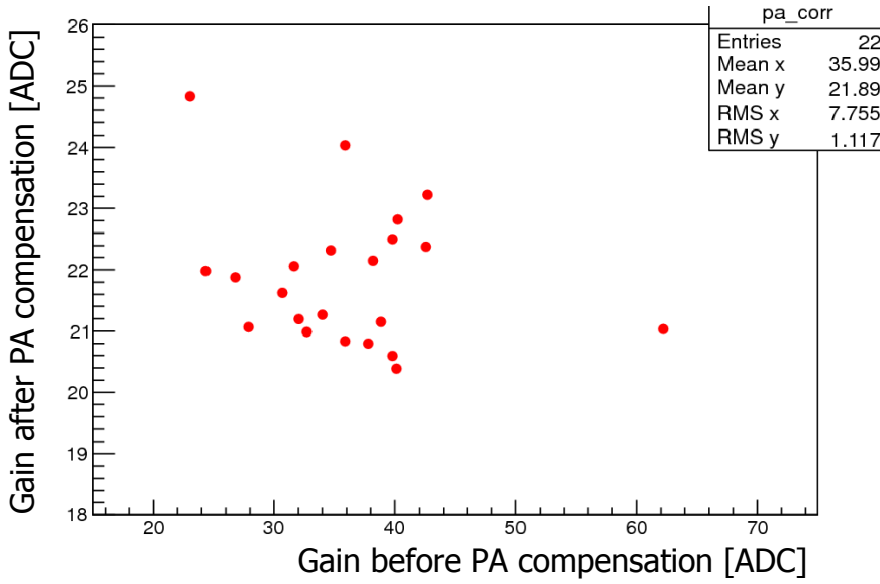
  → Capacity range 25-1575fF in 25fF steps

- Normalize to e.g. 100fF measurement

→ **Factor 4** gain spread can be compensated with SPIROC2b!

→ **Gain spread ~5%** after equalization!





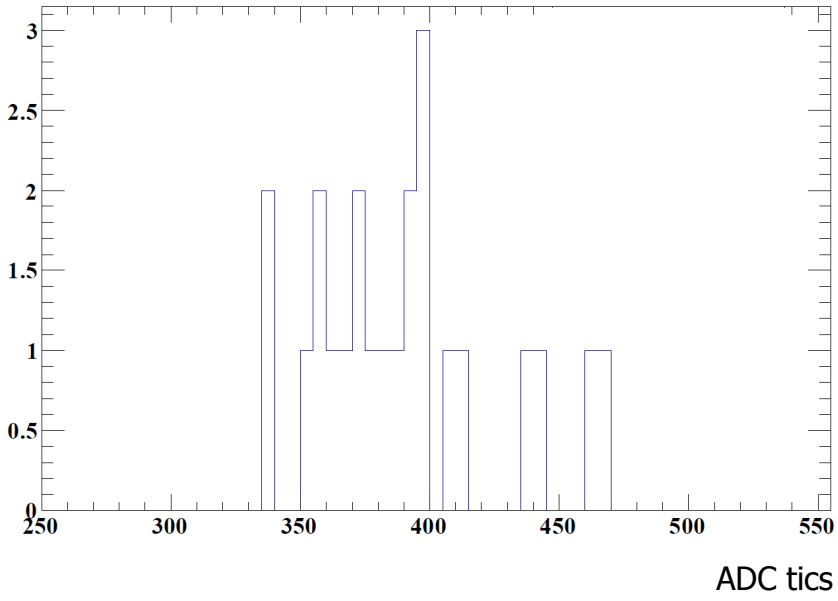
Channel-gain equalization

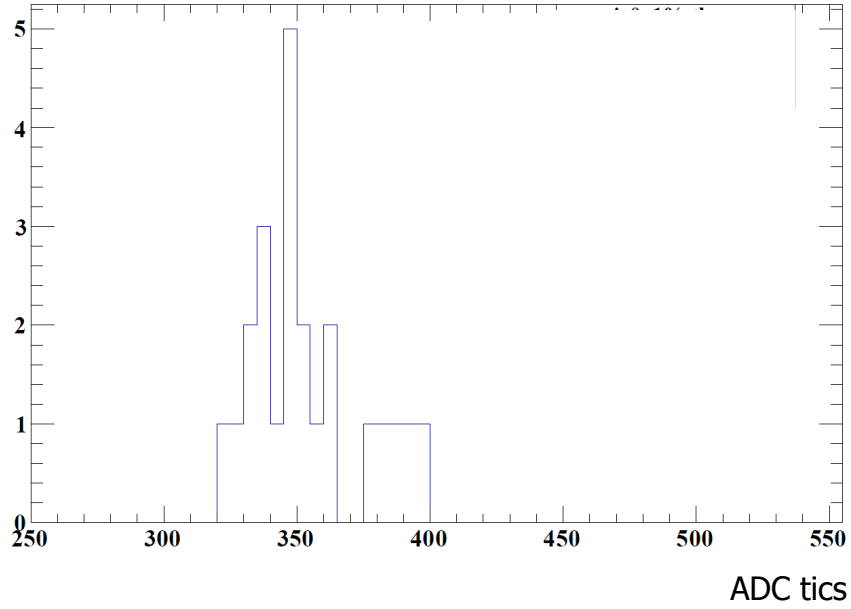
Online threshold setting:

- Is channel-wise threshold setting necessary?

  → Measure pedestal distribution and cut at 10^{-3} ratio

  → After channel-gain equalization very narrow threshold distribution!





New HCAL Base Unit (HBU2)

- 4 **new HBUs** in DESY lab

  → 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs
- 1 HBU2 connected to DAQ modules for first tests

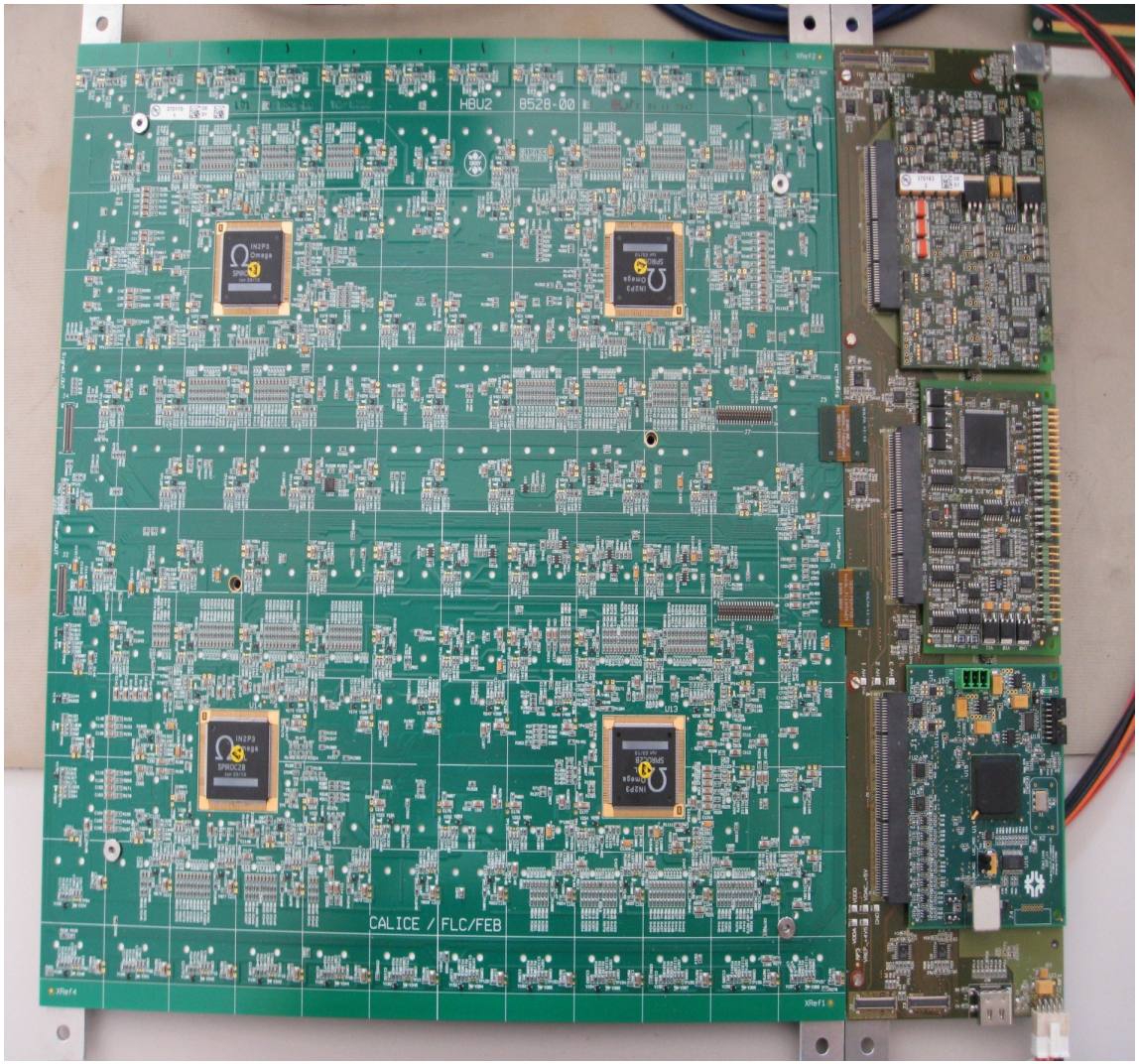
  → so far fully functioning!
- 1 HBU2 in **DESY test beam**
- We ordered 6 new HBU2s for **full slab test**:

  → Quality of electrical signals

  → Mechanics, temperature

  → DAQ

  Build small stack with ~10 layers, 1 HBU each?



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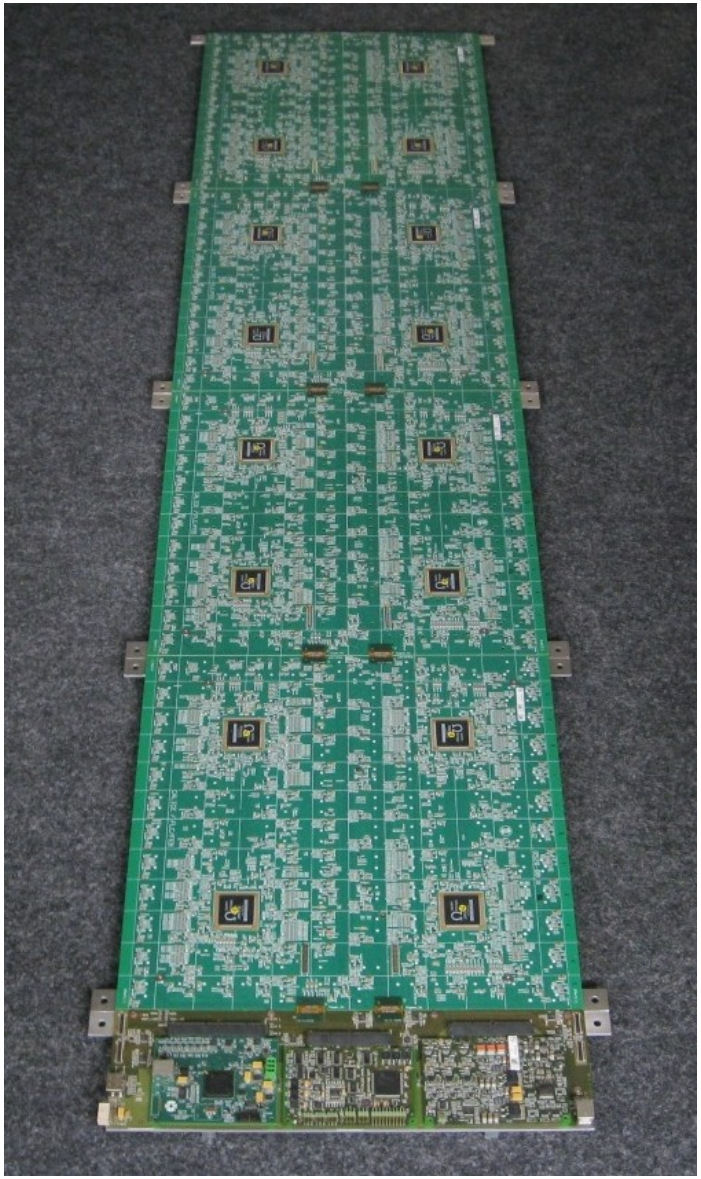

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  → Quality of electrical signals

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  → DAQ

Build small stack with ~10 layers, 1 HBU each?

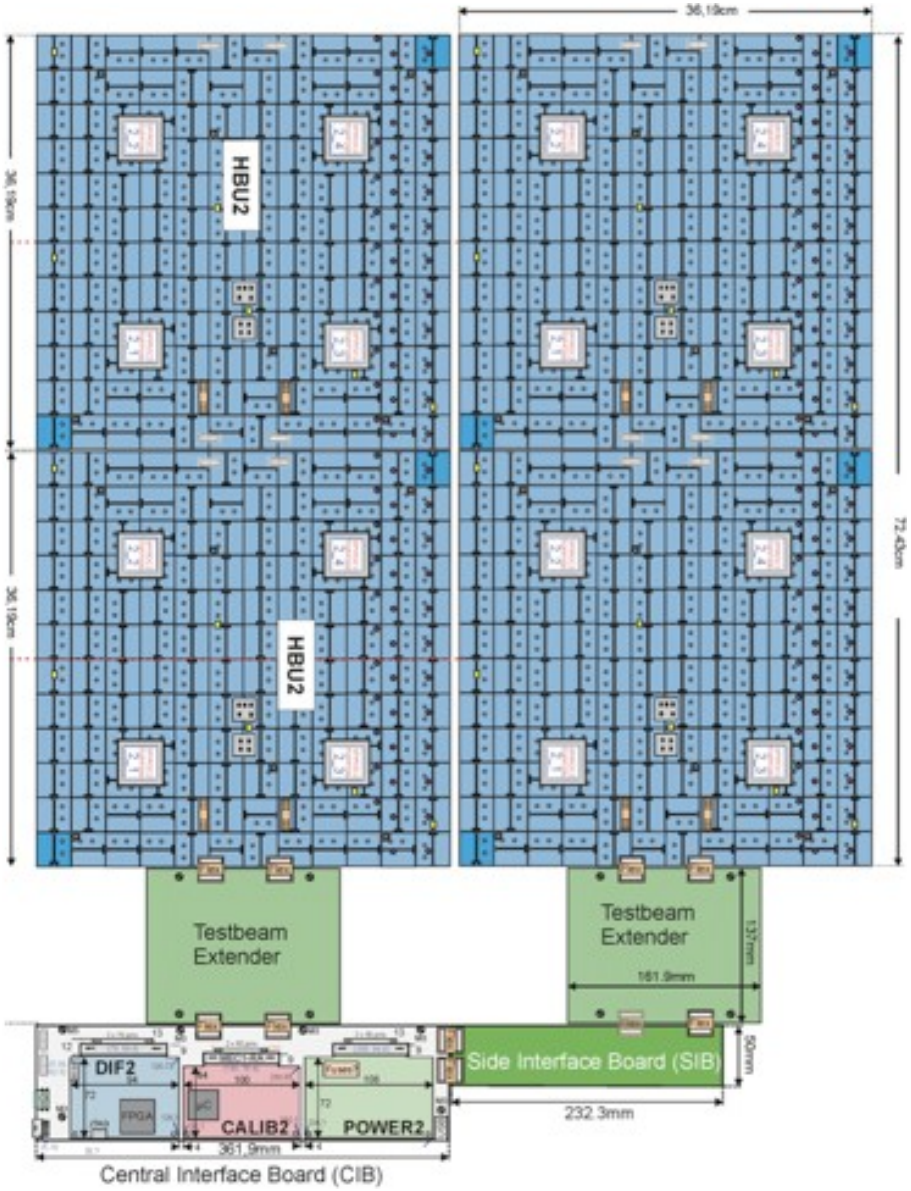
- **Mechanics is in place** since long time

  → Use it to perform temperature tests

  → Use it for small stack

  → Cassettes are being built by Karsten

New mechanics and boards



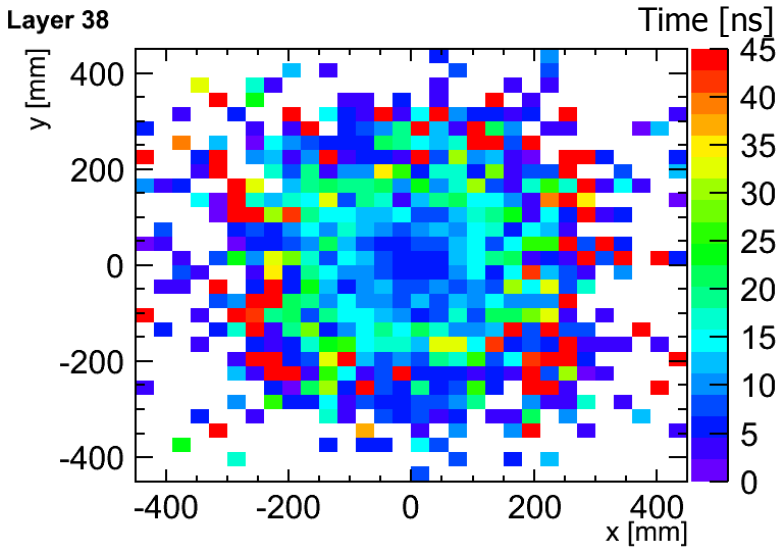
- Preparations for test beam with **4-HBU-layer** started

  → Cassettes in production

  → **Side-Interface-Board** in development

  → **Extender board** in development

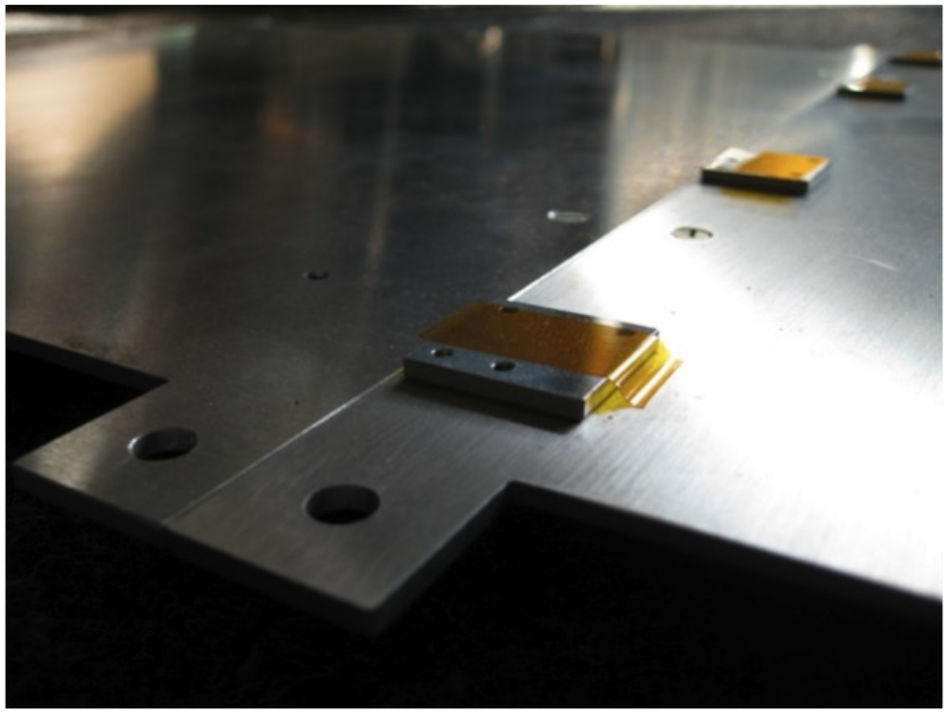
  → **DIF redesign** ongoing

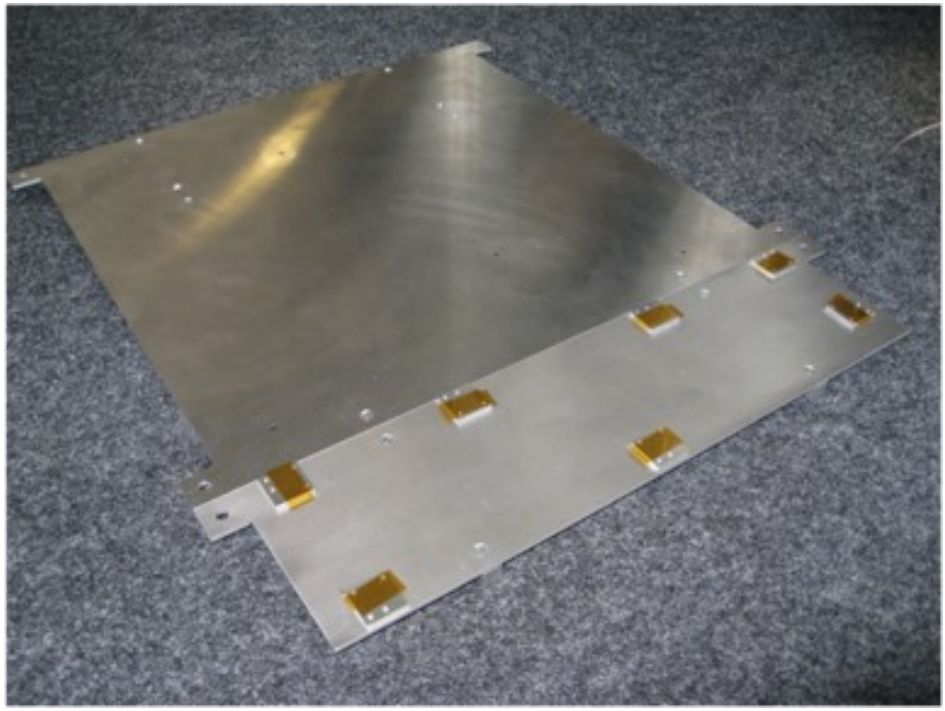


Mechanical support structures

- New mechanical support structure ready

  → 4 sets have been build
- Allows stitching of **up to 6 HBUs to a full slab**

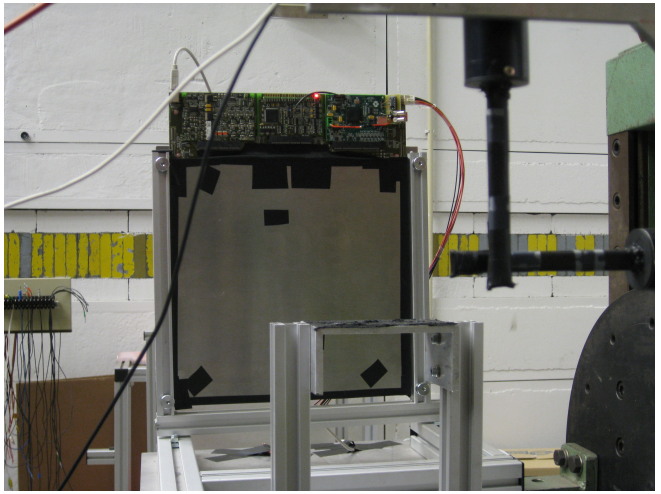


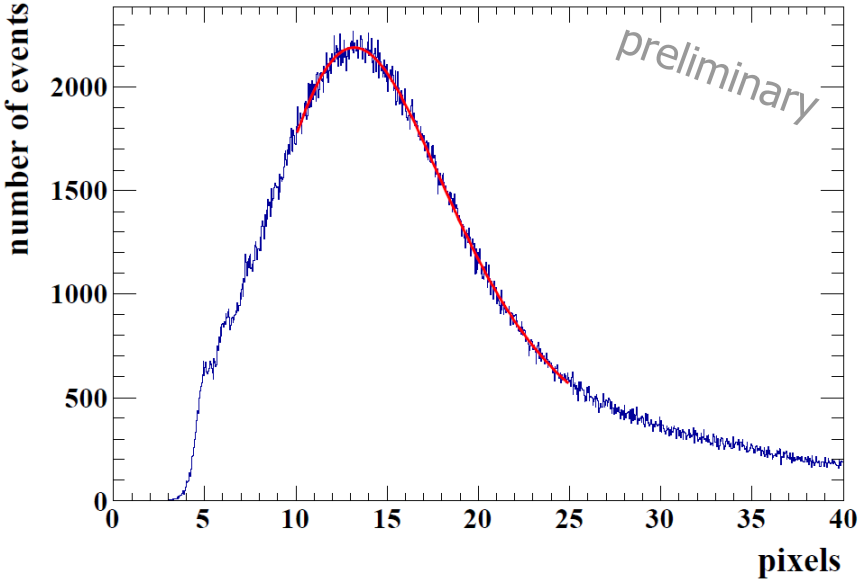


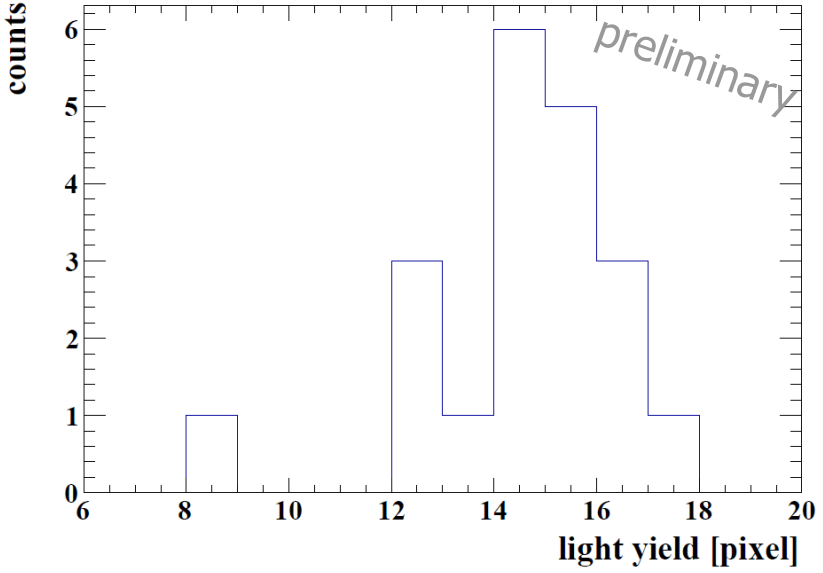
Test beam – First MIP results

- **HBU2 in DESY test beam**
  - Test functionality in test beam environment
  - Measure MIPs with 2 GeV electron beam

    → **~15 pixels per MIP**
  - Test channel-wise gain and autotrigger adjustment and **optimize MIP efficiency**







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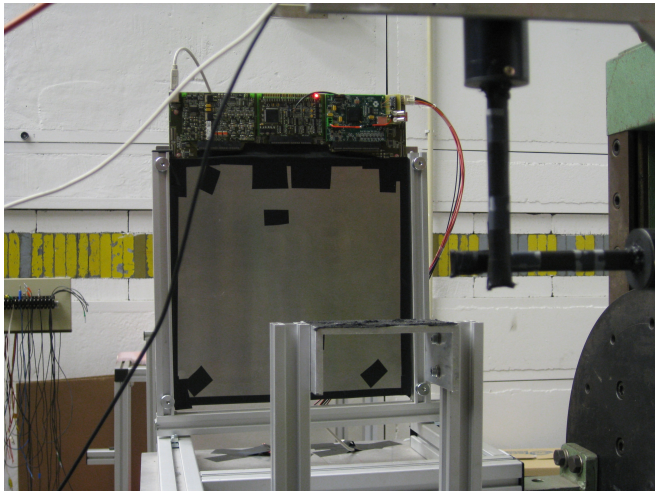
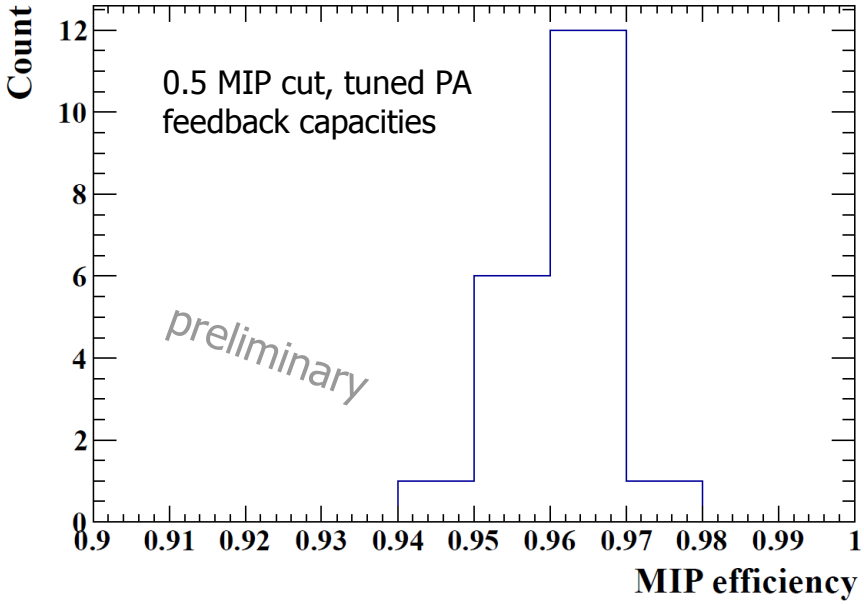
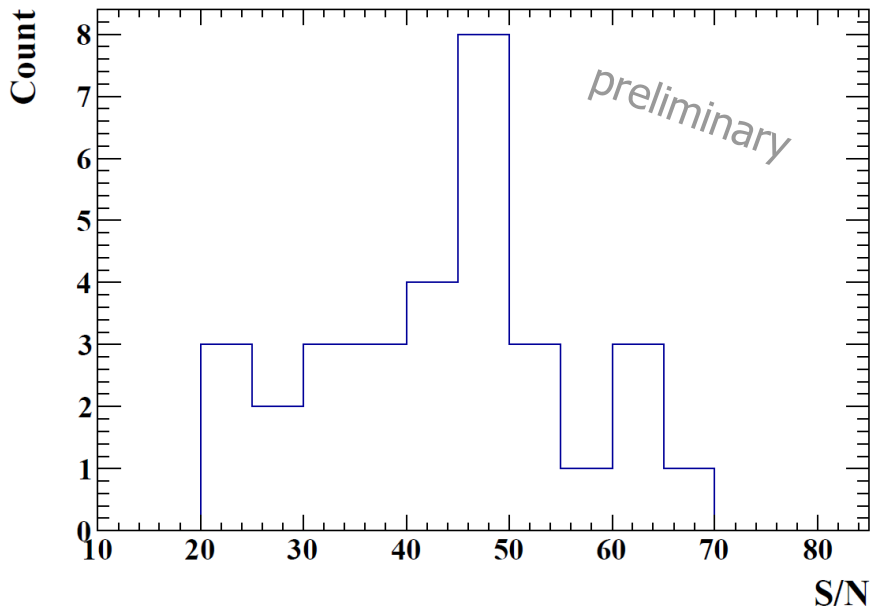






Summary and outlook

Status:

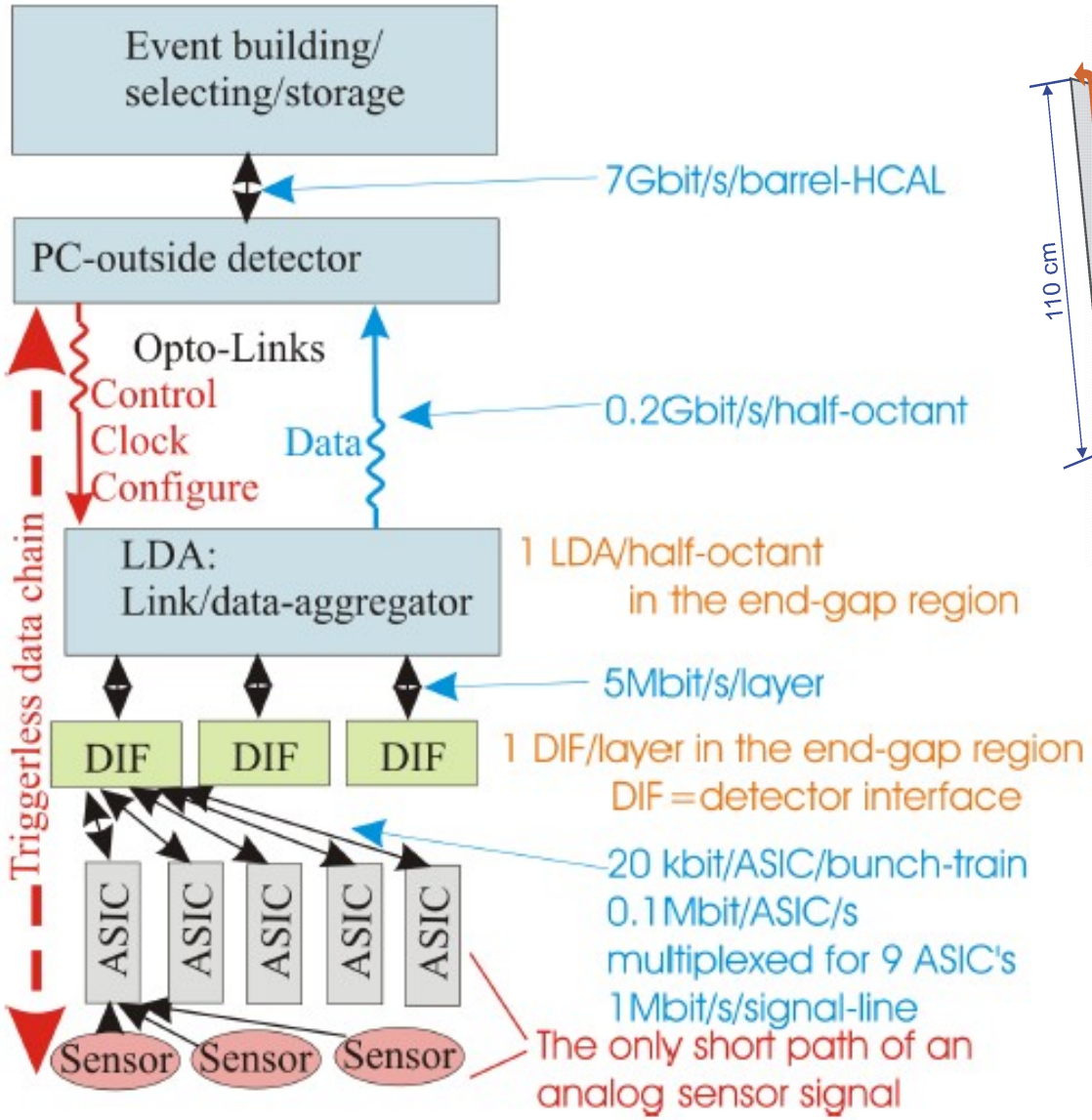
- HBU2 plus SPIROC2b in action and working fine!
- Understanding of SPIROC2b improving
- First tests of new calibration system promising
- New tiles at DESY, plenty of tests ongoing
- HBU2 tested successfully in DESY test beam
- DAQ development ongoing to build multi-HBU setups
- Preparations for simulations have started

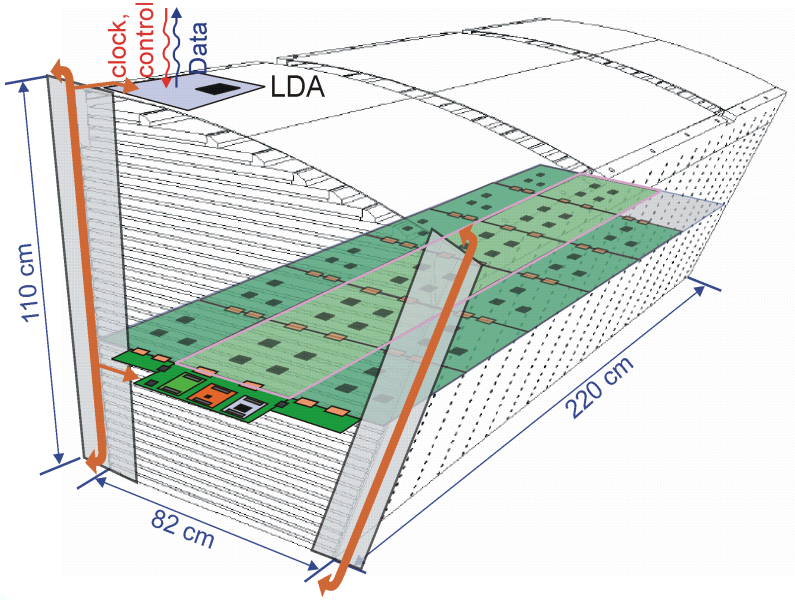
Plans:

- Full slab test (4 or more HBUs)
- Maybe small stack (~10 layers) in the future?
- Large layer in hadron test beam in late fall

  → **Measure shower time development!**

Data acquisition

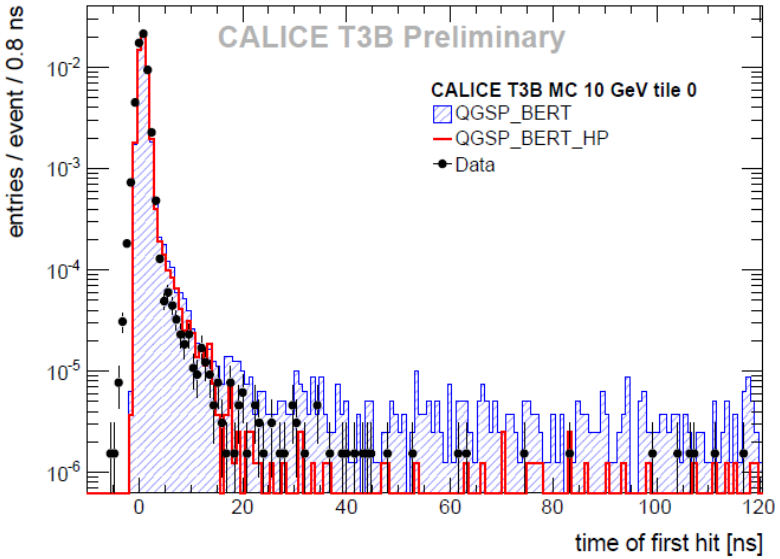


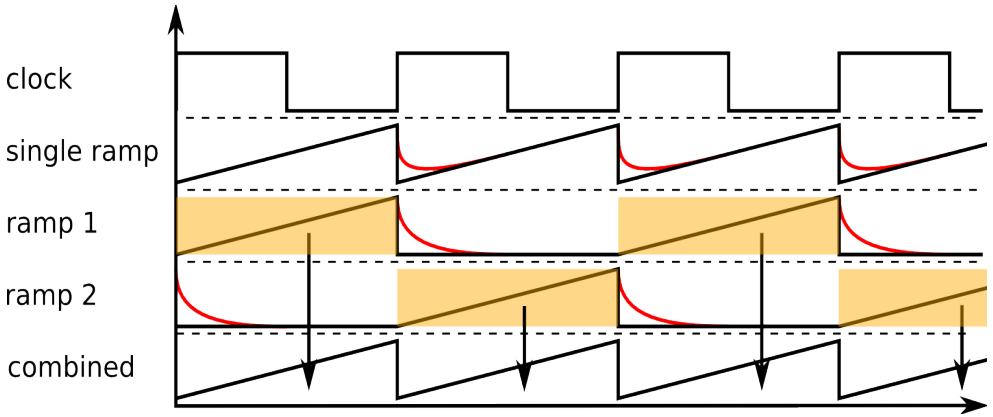


- Moderate data rates using channel-wise self-triggering

  → No need for further front-end event selection

SPIROC2b – Time measurements





- T3B measured radial development of shower in time in one row of last layer

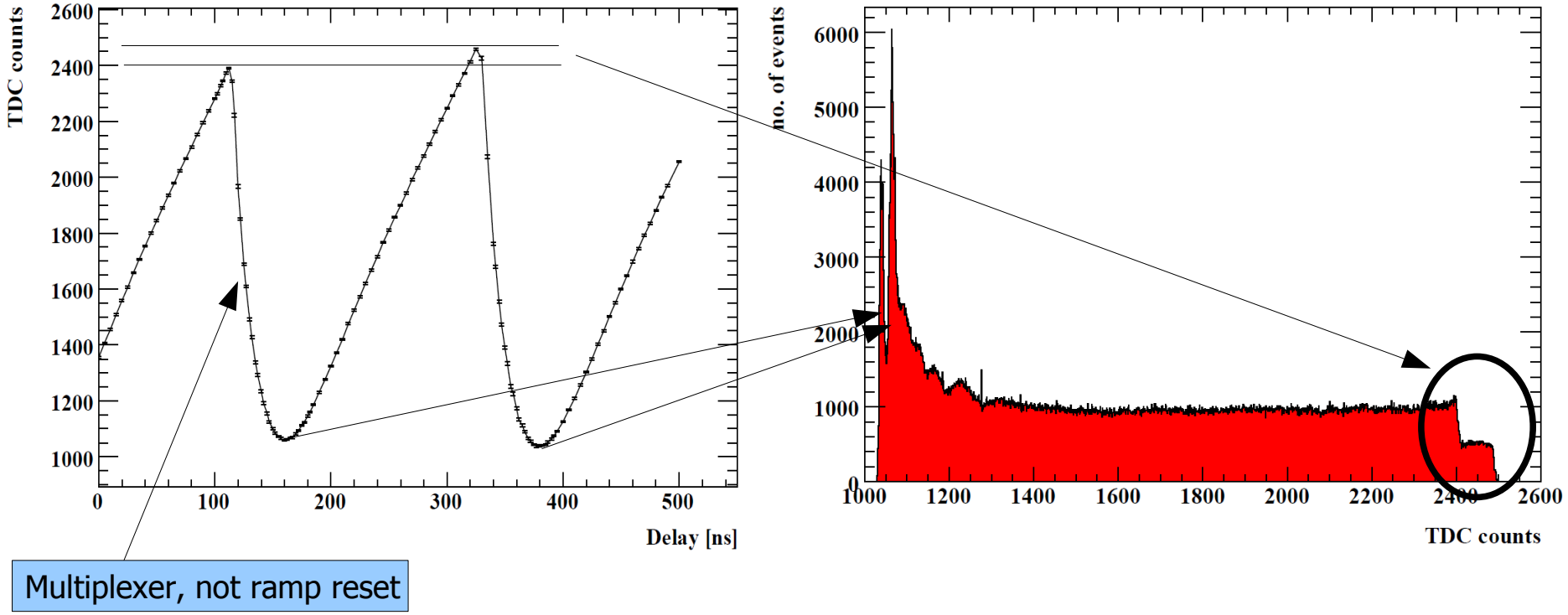
  → Repeat measurement with full layer or even multiple layers
- SPIROC2b measures time in auto-trigger mode relative to bunch clock

  → 2 ramps to reduce deadtime due to ramp reset

  → ILC mode = 200ns ramp, testbeam mode = 5µs ramp (less dead time)

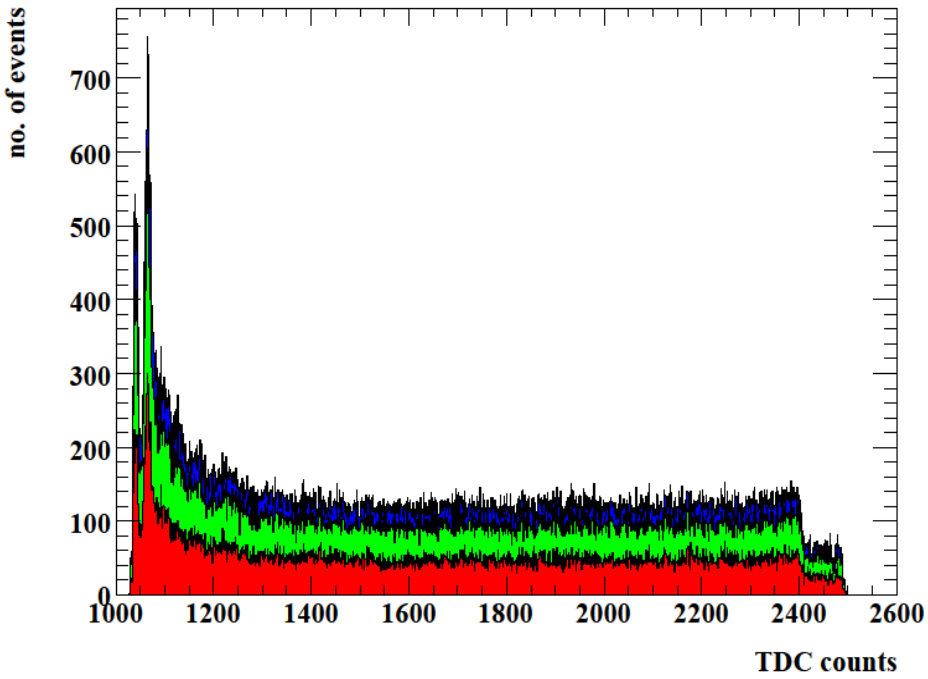
  → Investigate time resolution to optimize ramp slopes (and lengths)

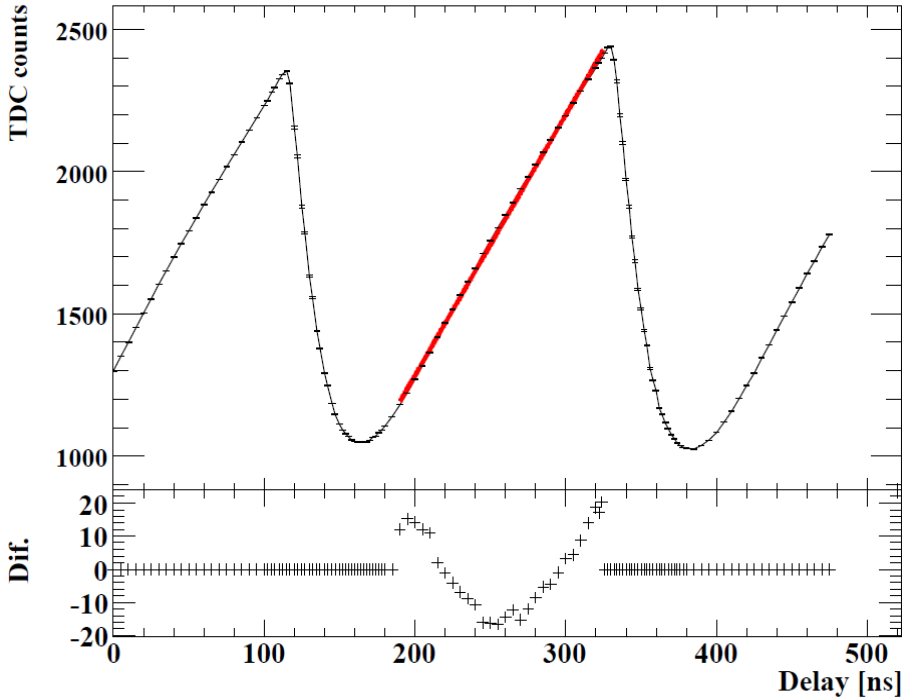
SPIROC2b – TDC (ILC mode)



- First tests of TDC ramps in SPIROC2b show promising results
- Resolution in ILC mode: ~250-350ps (dominated by linearity)
- The 2 ramps have different slopes/heights in ILC mode
- A few aspects will change in SPIROC3, but we have to use SPIROC2b!

SPIROC2b – TDC (ILC mode)





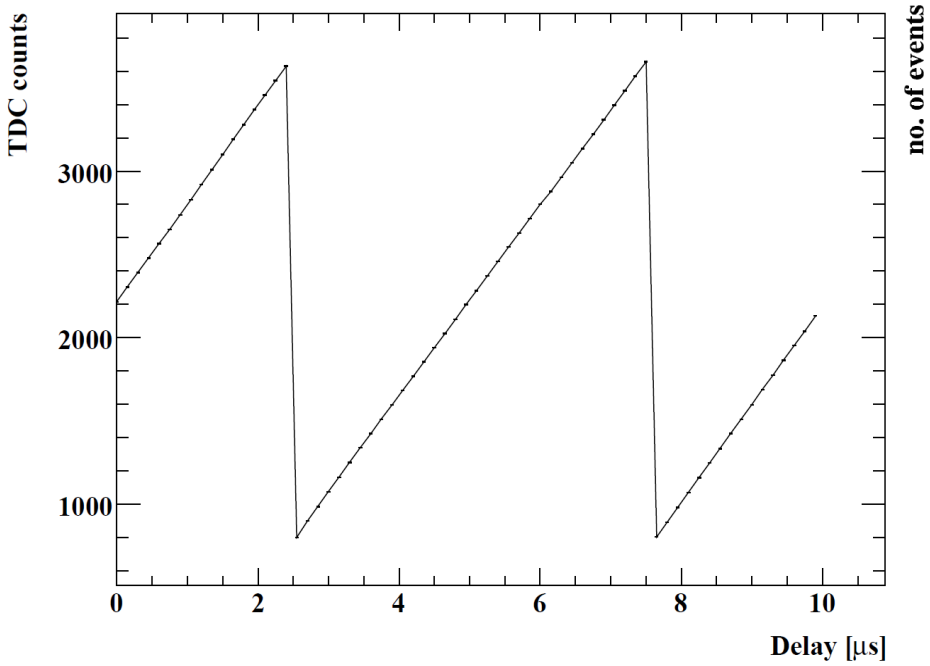
- No correlations visible between ADC and TDC measurements
- Resolution in ILC mode limited by linearity (~1ns)

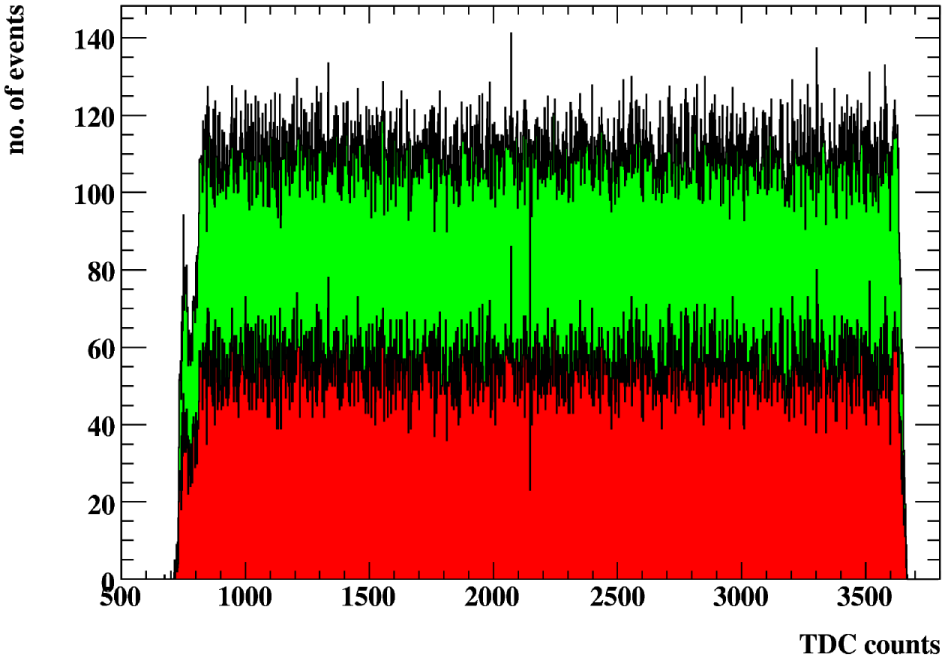
  → Linear fit reveals clear structure

  → Fit of 2 linear functions improves resolution (~300ps)

  → What is the most reasonable measurement/fit strategy?

SPIROC2b – TDC (testbeam mode)

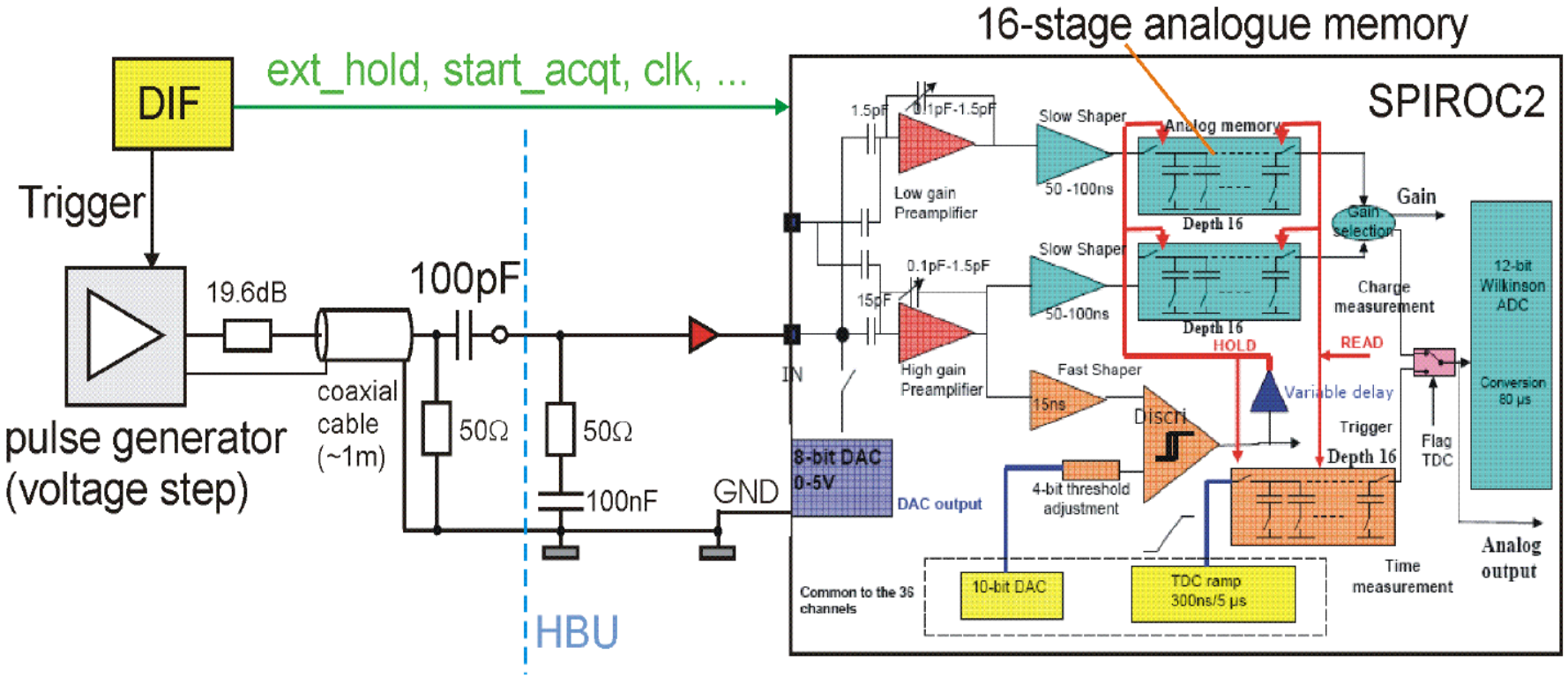




- Multiplexer deadtime very small in testbeam mode (longer ramp)
- Resolution in testbeam mode: ~3ns
- Very small differences for the two ramps in testbeam mode
- Resolution of ~1ns possible by optimizing ramp slopes (and dynamic range)

  → Tests with 1.25µs ramp promising

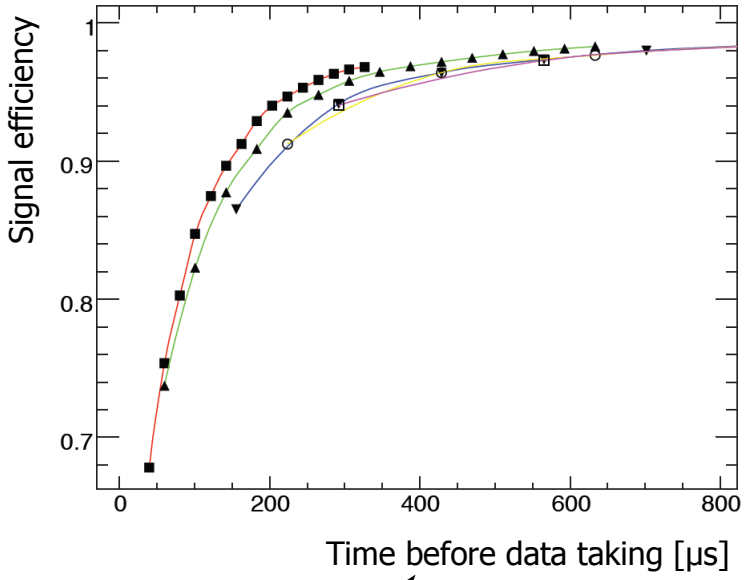
SPIROC2b

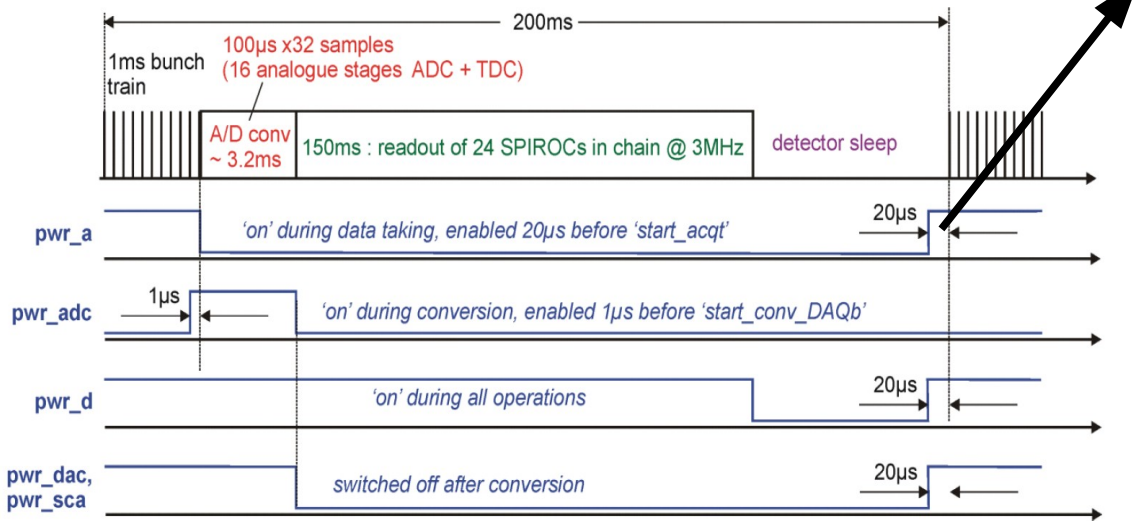

16-stage analogue memory
DIF
ext_hold, start_acqt, clk, ...
Trigger
19.6dB
100pF
coaxial cable (~1m)
pulse generator (voltage step)
50Ω
50Ω
100nF
GND
HBU
IN
SPIROC2
1.5pF
0.1pF-1.5pF
Low gain Preamplifier
Slow Shaper
50 -100ns
Analog memory
Depth 16
Gain selection
Gain
0.1pF-1.5pF
15pF
High gain Preamplifier
Slow Shaper
50-100ns
Depth 16
Charge measurement
HOLD
READ
Fast Shaper
15ns
Discri
Variable delay
Trigger
Depth 16
Flag TDC
12-bit Wilkinson ADC
Conversion 60 µs
8-bit DAC 0-5V
DAC output
4-bit threshold adjustment
Common to the 36 channels
10-bit DAC
TDC ramp 300ns/5 µs
Time measurement
Analog output

Power Pulsing

How to switch on the different SPIROC2b parts?

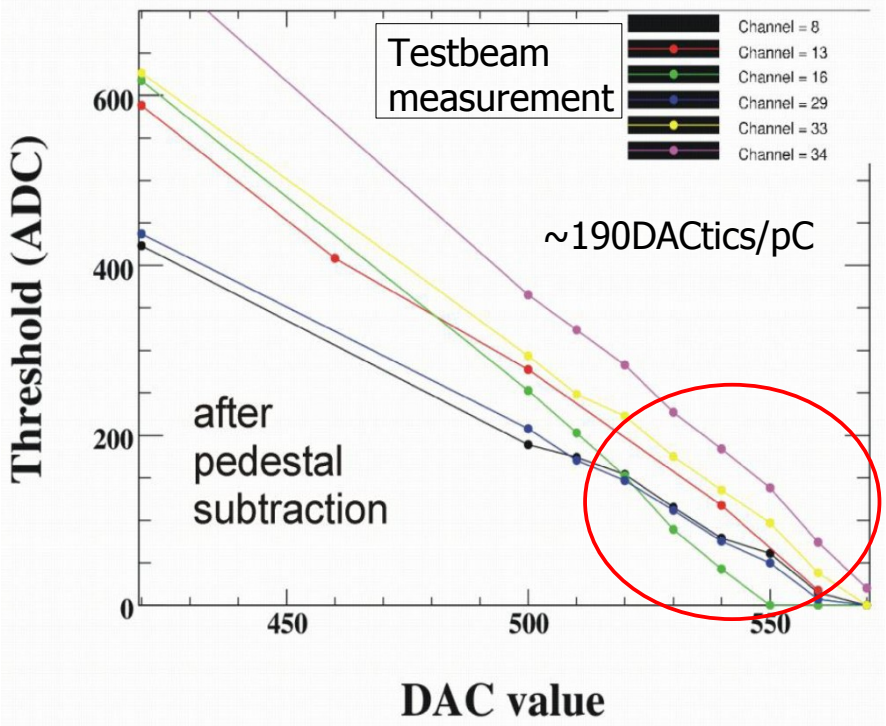
- Test efficiency of signal collection as function of time before first trigger
  - → 250µs required for 95% efficiency
  - → Has to be improved! SPIROC2c?

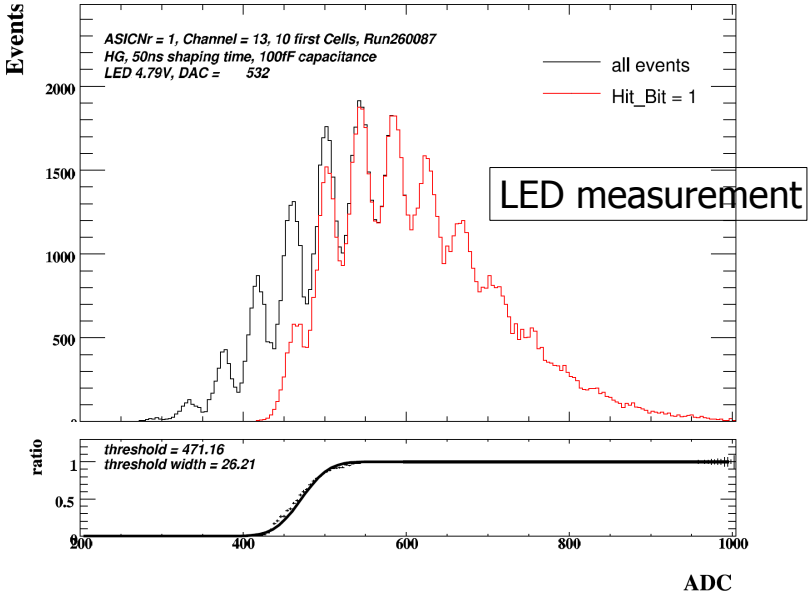


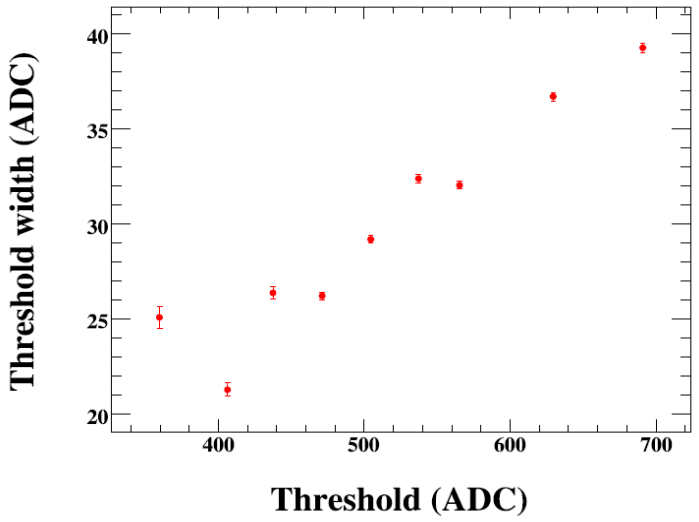


Autotrigger performance

- Autotrigger: mode of ILC operation
- Compare fast shaped signal with predefined (10 bit) DAC threshold
- Set threshold to minimize noise hits and maximize MIP efficiency

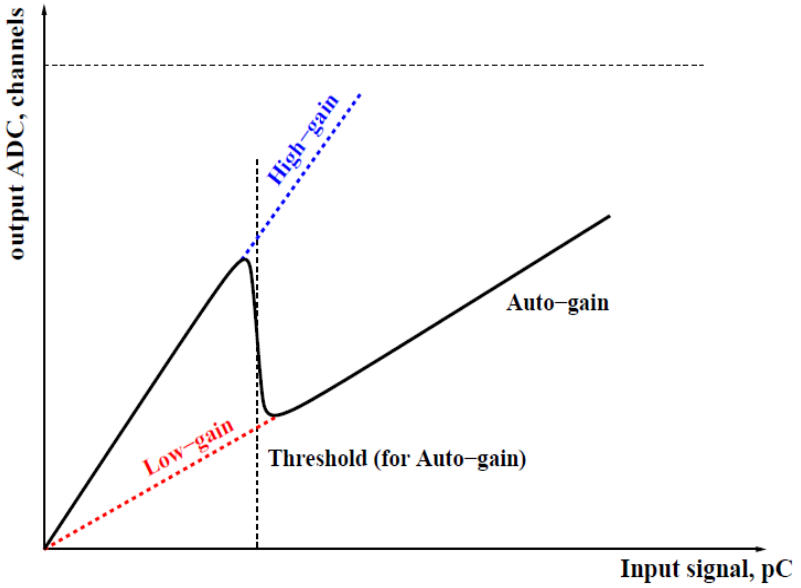


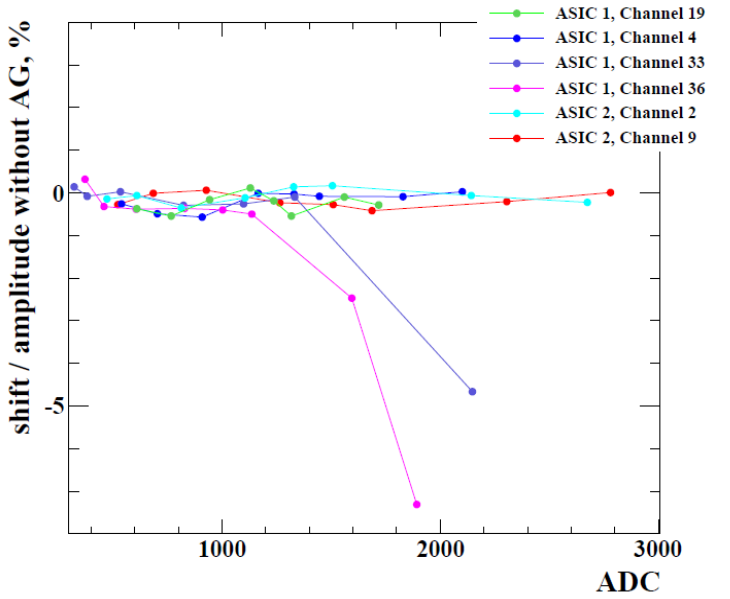


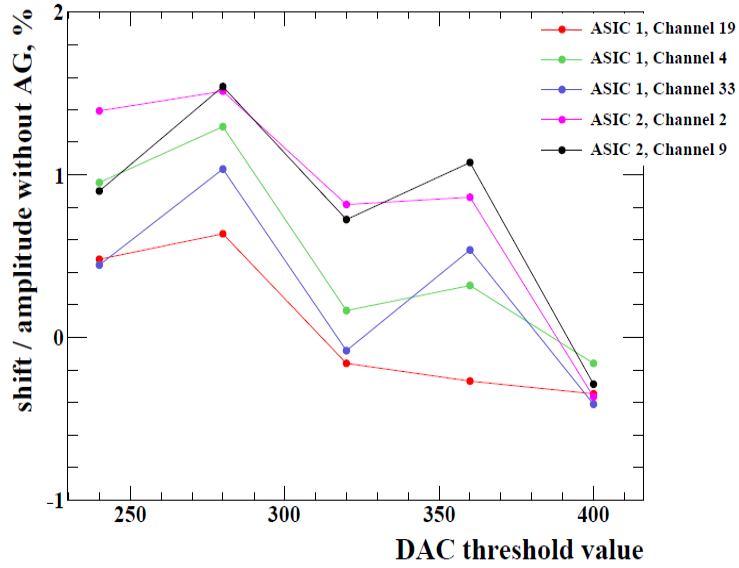


Autogain performance - Linearity

- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Good linearity, but still slightly depends on:
  - Amplitude
  - Distance to threshold

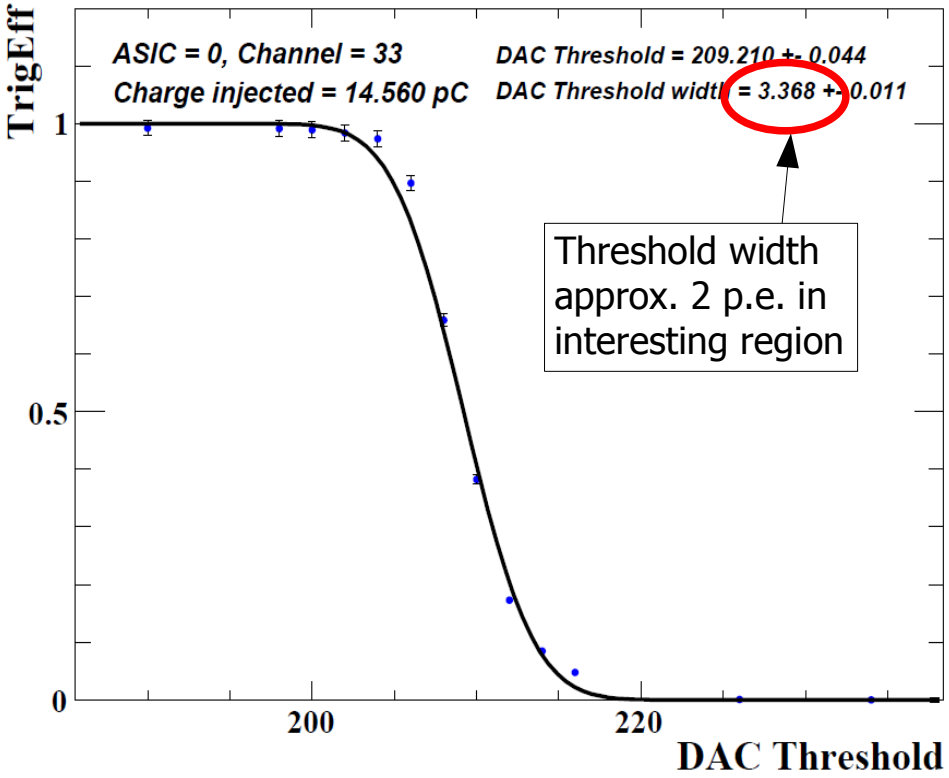


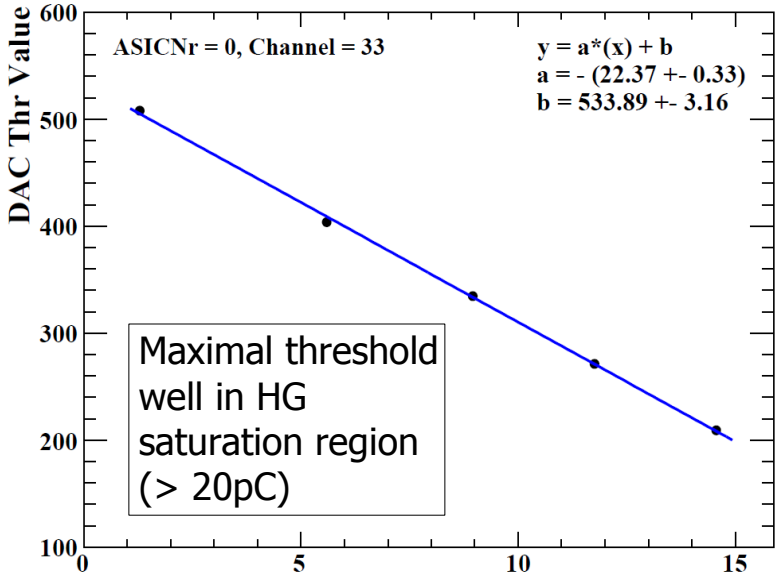


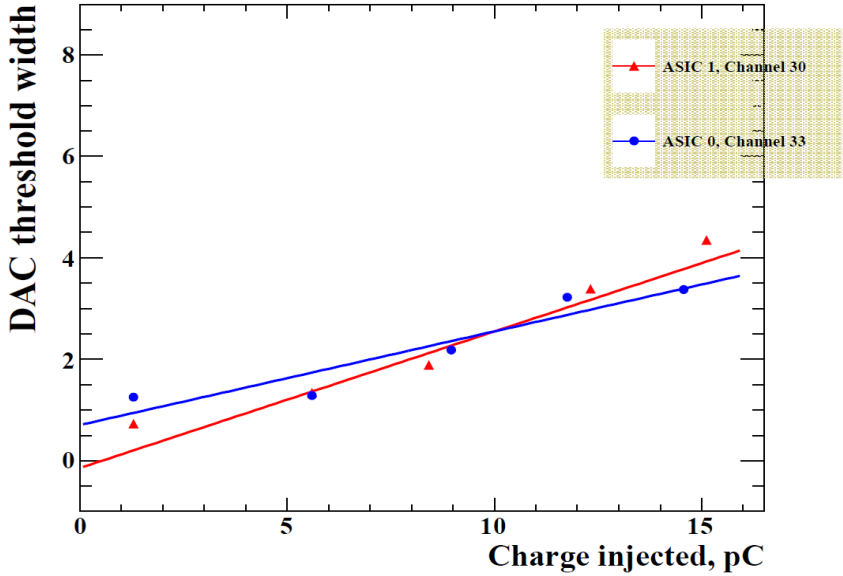


Autogain performance - Thresholds

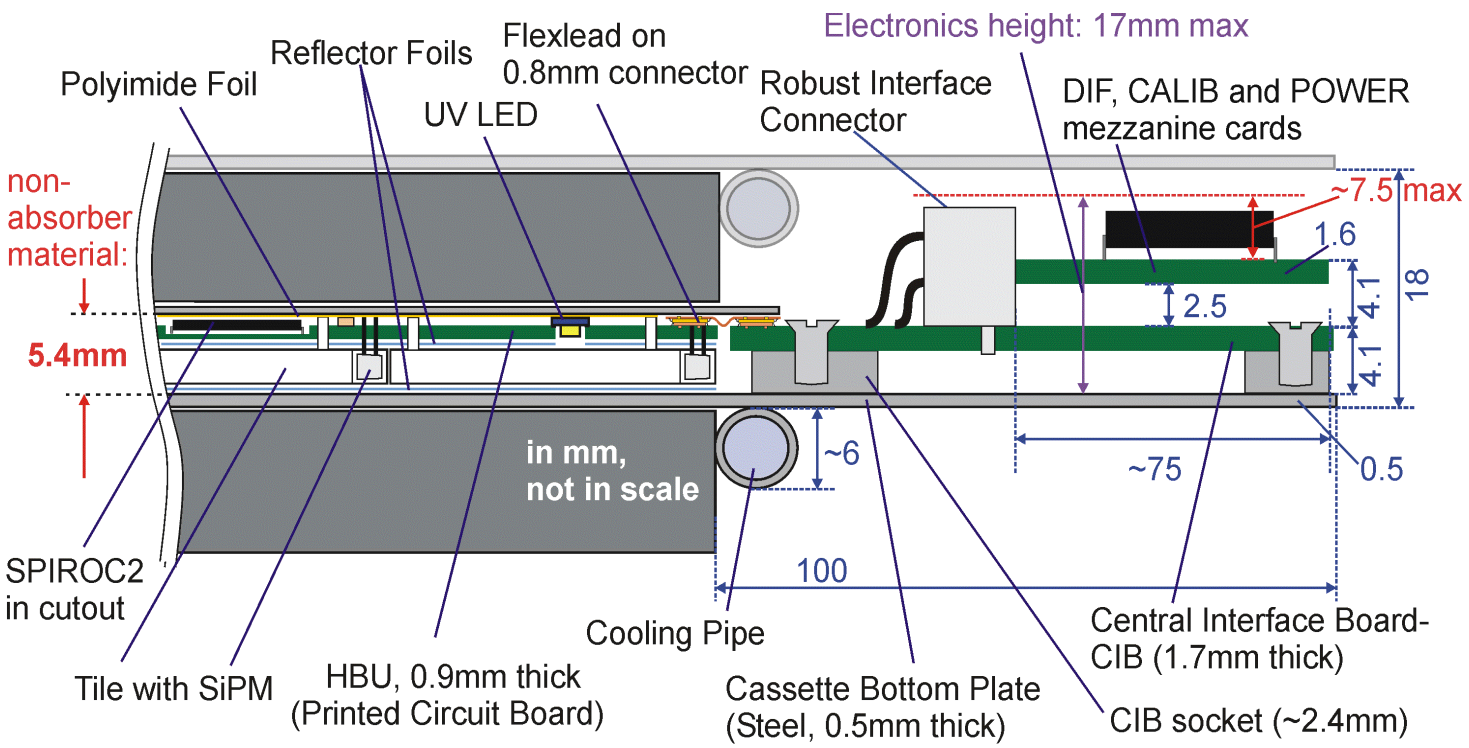
- Autogain: automatically switch between high gain and low gain mode
- Compare signal with predefined (10 bit) DAC threshold
- Similar performance as for autotrigger

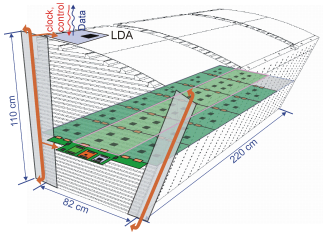






AHCAL layer – cross section





Abbr.	Name
DIF	Detector Interface Board
CALIB	Steering for LED calibration
CIB	Central Interface Board
HBU	Front-end board