DEPFET Status

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Munich, Germany

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DEPFET
Active Pixel Detector

Excellence Cluster
Universe

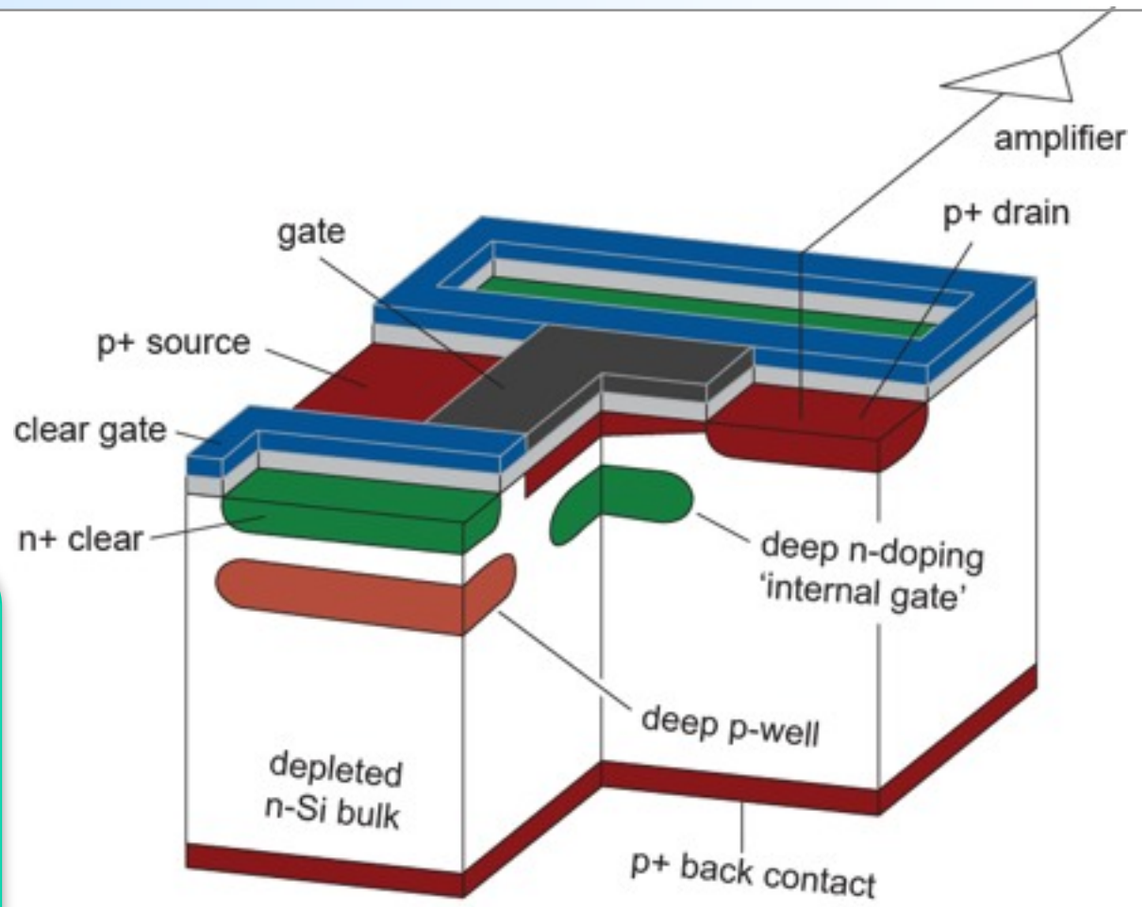
Outline

- DEPFET - ILC and Belle II
- DEPFET Vertex Detectors - Design and Electronics
- Test Beam Results
- Simulation Status

Reminder - DEPFET Technology

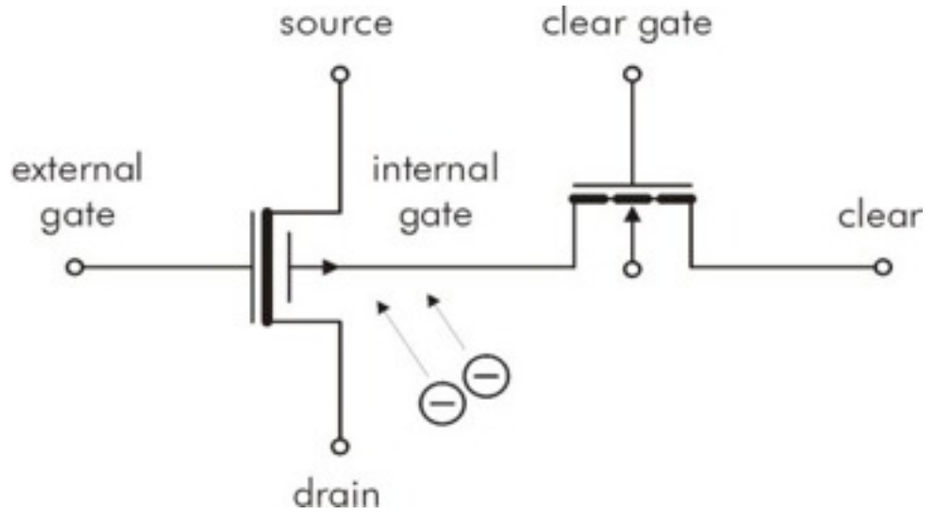
- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 400$ pA/e^-)
- Rolling shutter row-wise readout
- Accumulated charge can be removed by a clear contact



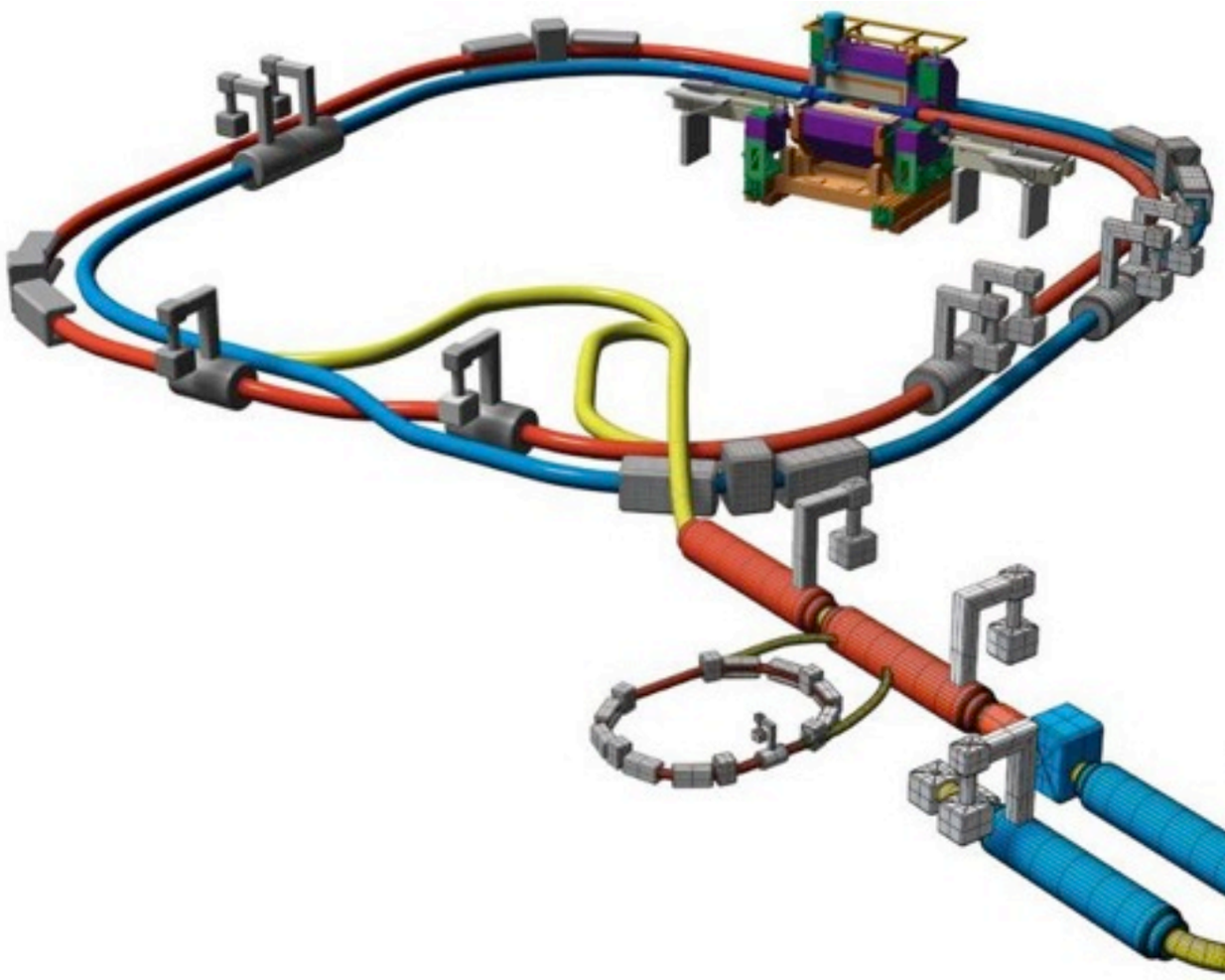
- Detection, fast charge collection and internal amplification
- Excellent signal-to-noise ratio
- Low power consumption
- Thin detectors

Features



Belle II PXD: A Boost in Development

- DEPFET pixel sensors used for the vertex detector of Belle II (2 pixel layers)
  - To be operated at SuperKEK B, Y(4s) resonance, luminosity 8 x 10^{35} $cm^{-2}s^{-1}$



- Installation foreseen for 2015: Accelerated development

DEPFET Design - ILC vs Belle II

- Experimental conditions - ILC vs Belle II

	ILC	Belle II
Occupancy	0.13 hits/μm²/s	0.1 hits/μm²/s
Radiation	< 100 krad/year	< 2 Mrad/year
Duty cycle	1/200	1
Frame time	25-100 μs	20 μs
Momentum range	All momenta	Low momentum (< 1 GeV)
Acceptance	6°-174°	17°-155°

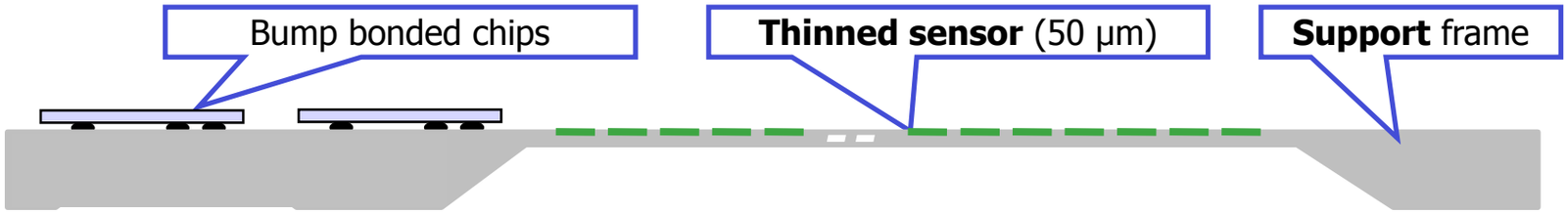
In several aspect Belle II more challenging than ILC

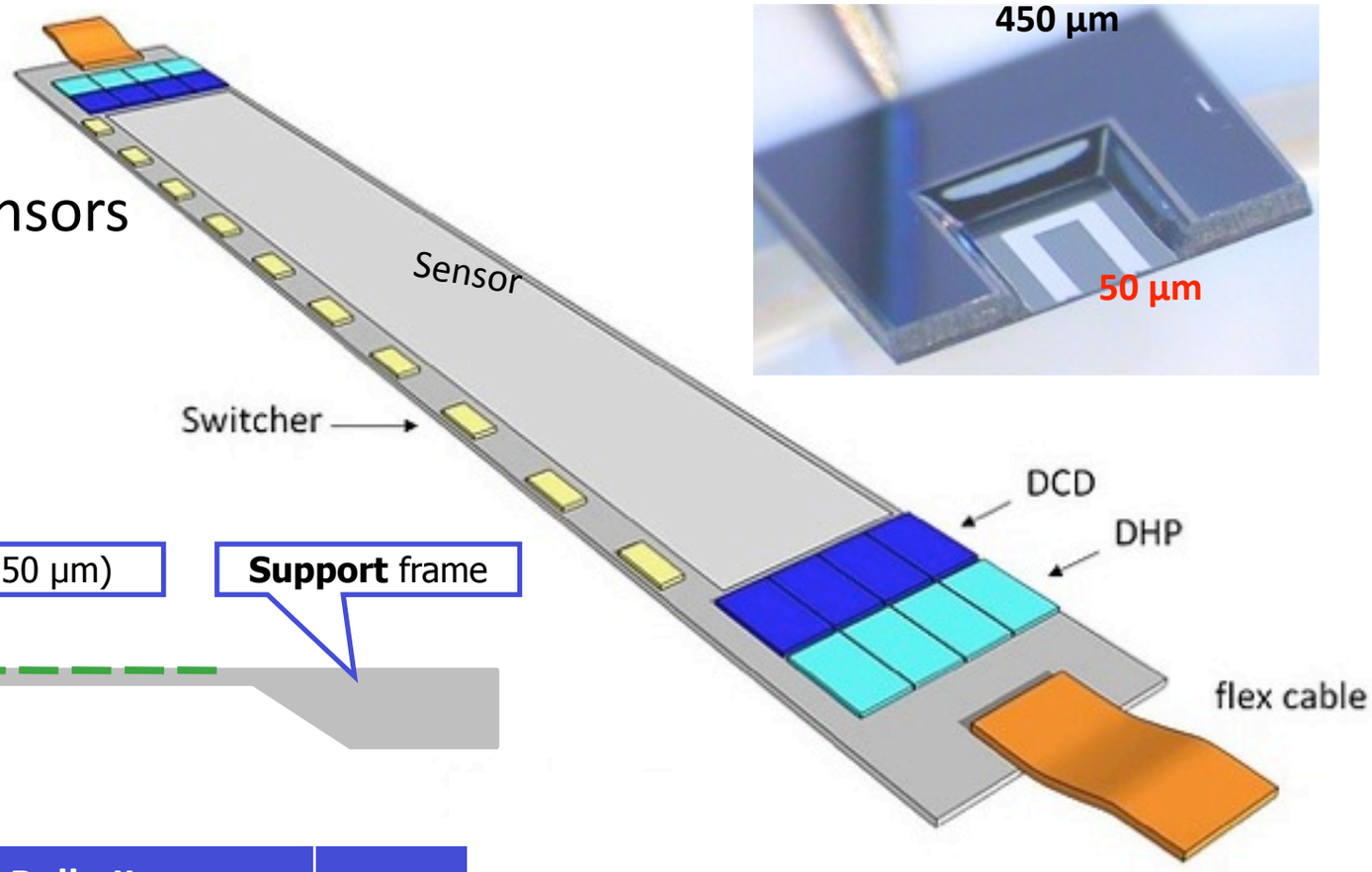
at ILC: focus on best possible spatial resolution - small pixels, thinnest possible layers

at Belle II: Less stringent requirements (limits from multiple scattering at low momentum), number of pixels constrained due to continuous readout

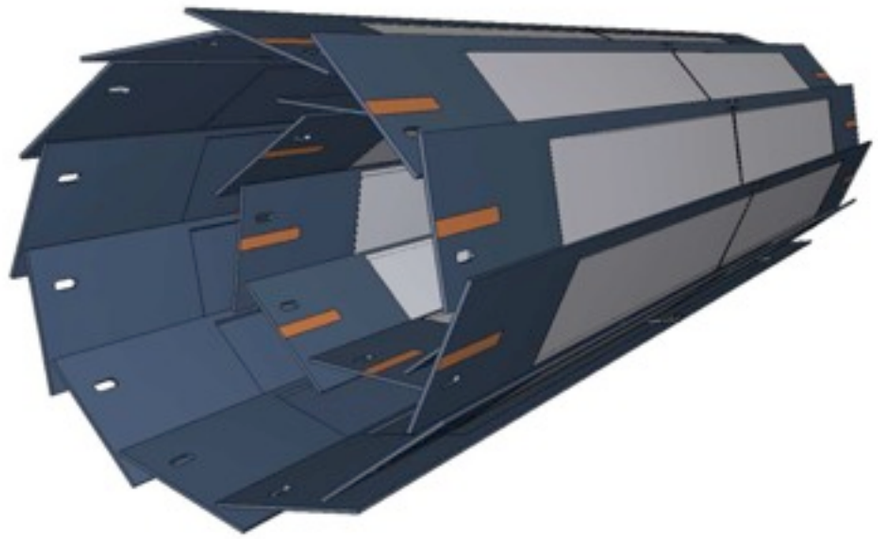
DEPFET Vertex Detectors

- The basic unit is the DEPFET ladder
  - Central region covered with thin sensors
  - Switchers on the lateral balcony
  - Front end at both ends



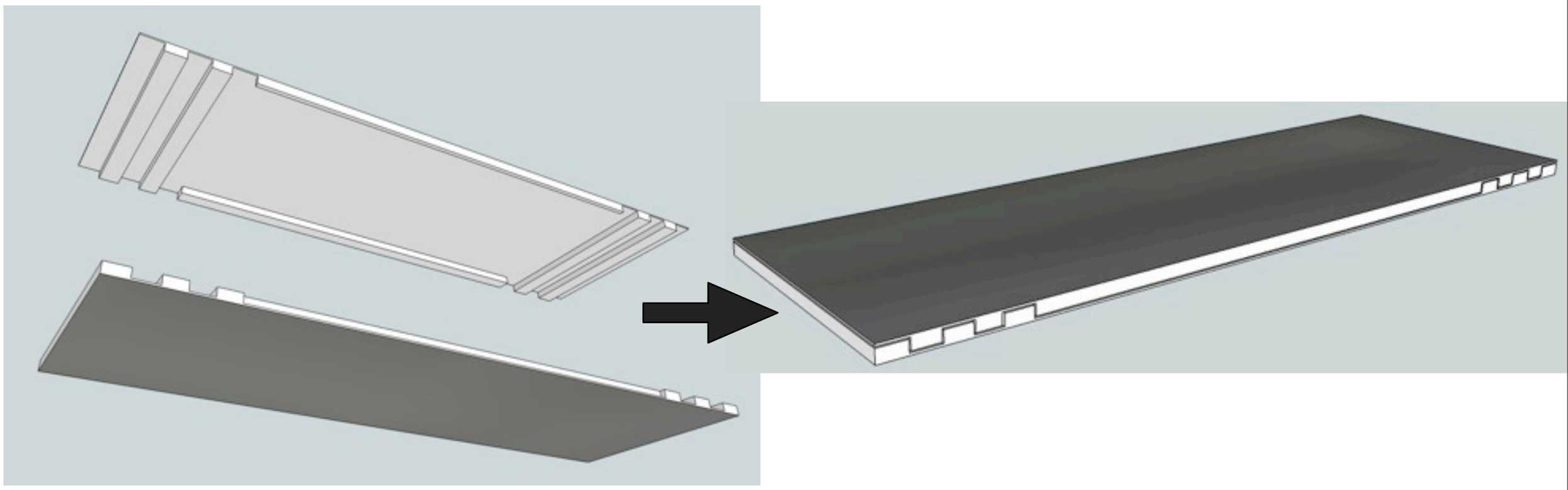


	Old ILD 5-layer layout	Belle II	
Radii	15.5, 26, 38, 49, 60	14, 22	mm
Ladder length	100 (L0), 250 (L1-L4)	136 (L0), 169 (L1)	mm
Sensitive width	13 (L0), 22 (L1-L4)	12.5 (L0-L1)	mm
Number of ladders	8, 8, 12, 16, 20	8, 12	
Pixel size	25x25 (L0-L4)	50x50 (L0), 50x75 (L1)	μm^2
Row rate	40	10	MHz
Number of pixels	800	8	Mpix



DEPFETs: Mechanical concepts

- DEPFET technology compatible with 5 individual layers (original concept)
  or 3 double layers
  First ideas for silicon-only double layers:



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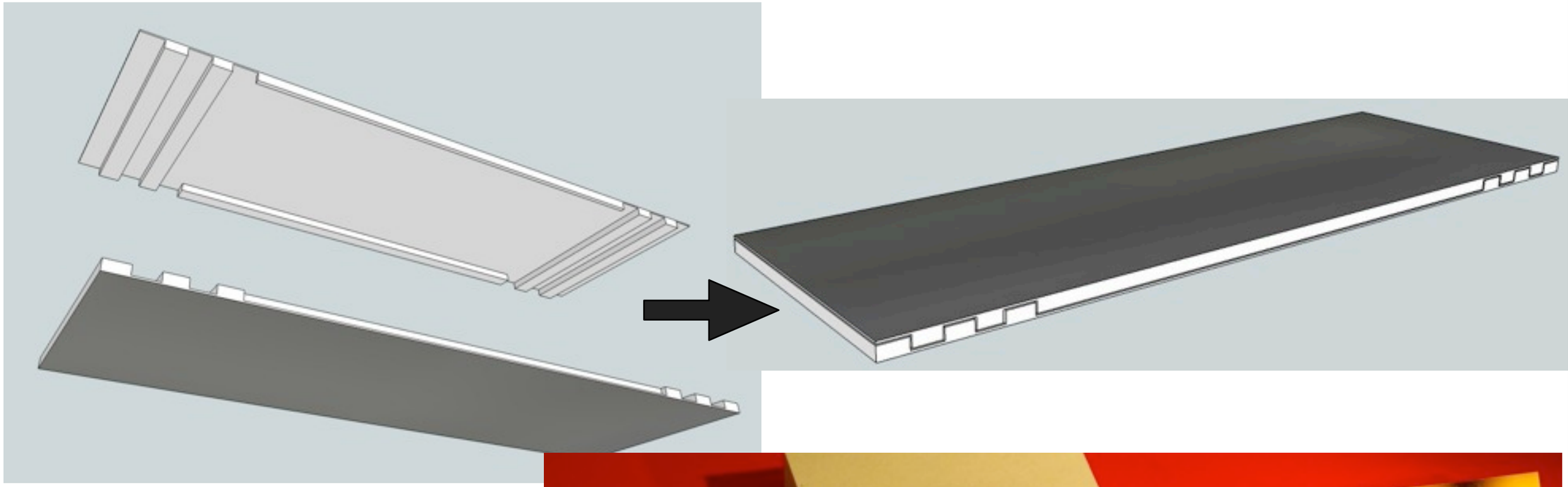
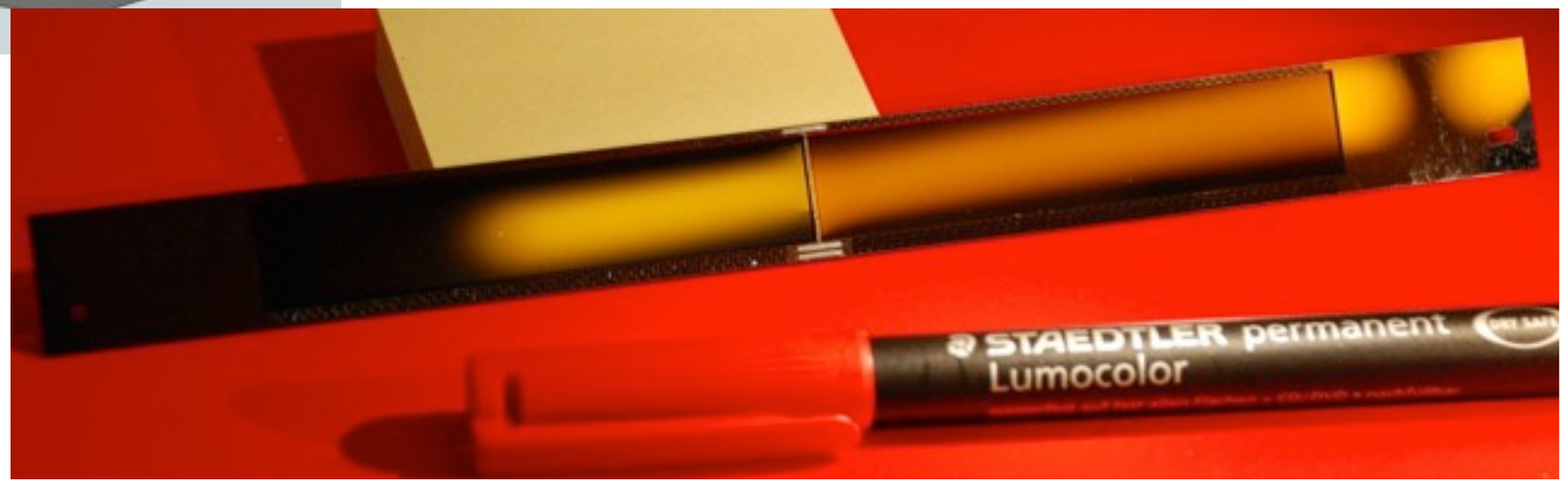
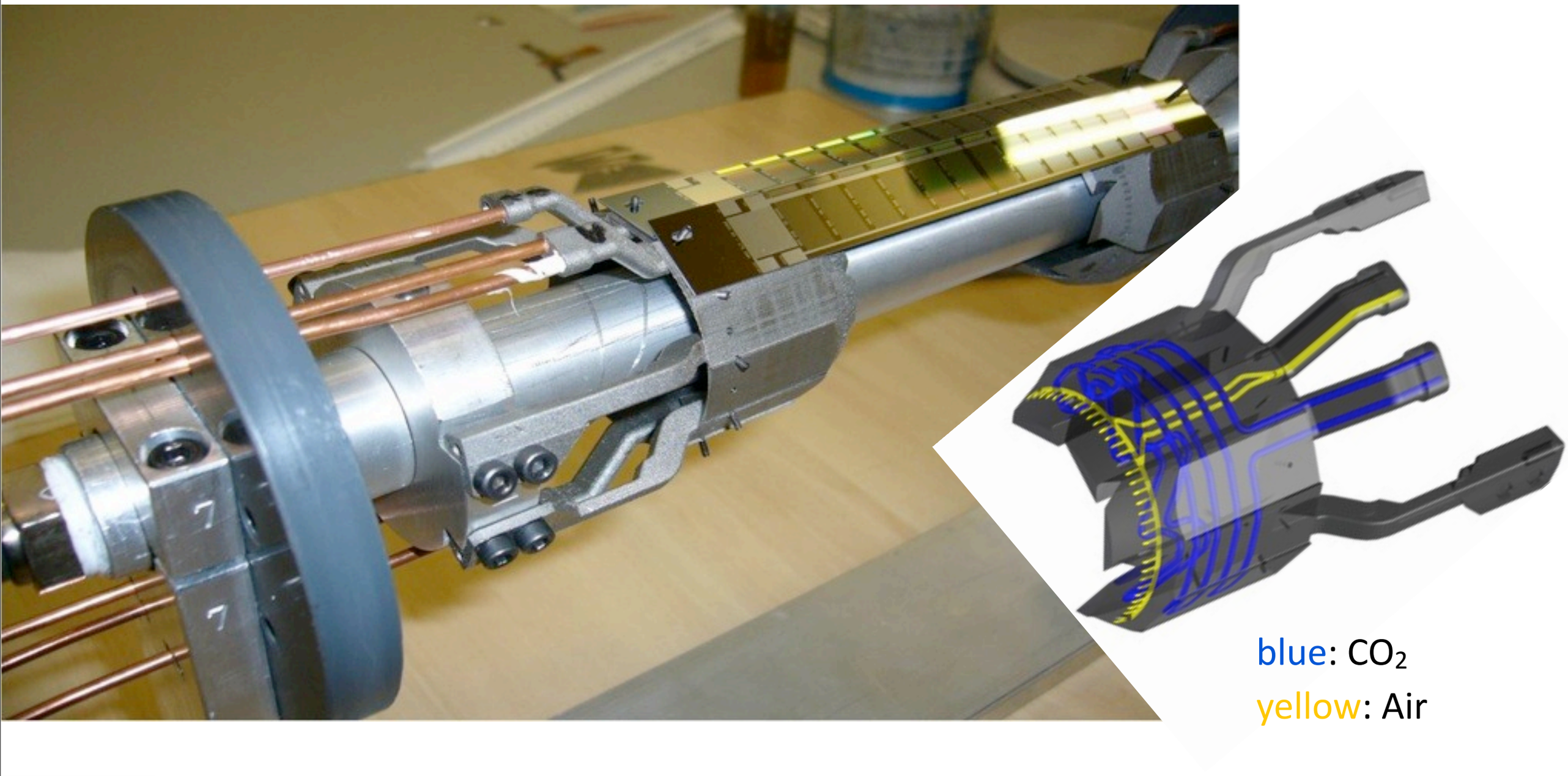


Fully tested low-mass ceramic micro-joint connections of silicon modules



DEPFETs: Mechanical Concepts

- Fully developed mechanical design for Belle-II
  - includes CO_2 cooling of support structure and air cooling of sensors

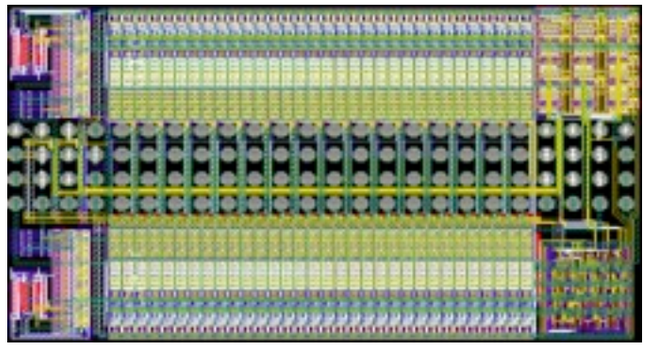


On Detector Electronics - Status

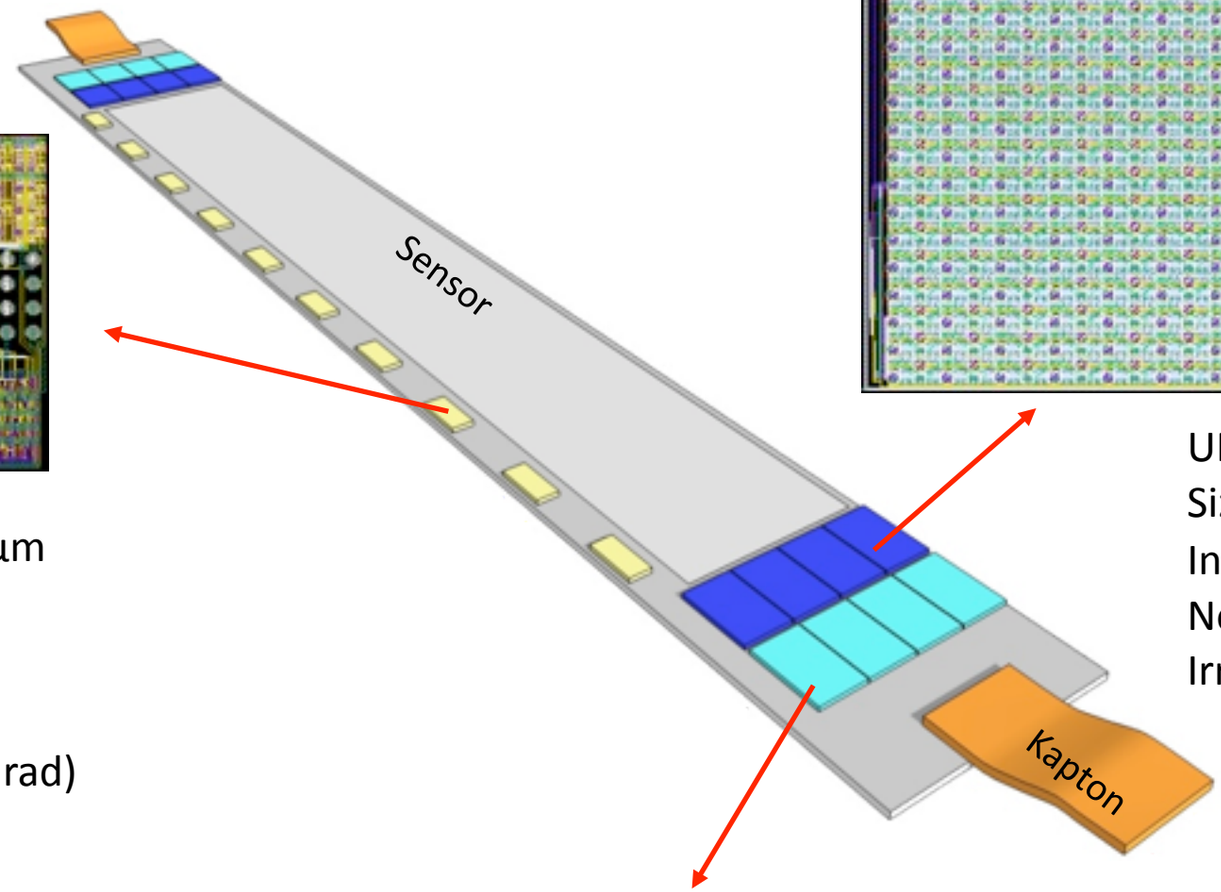
The full-size close to final versions of the ASICs are designed, produced and found to work

SwitcherB

Row control

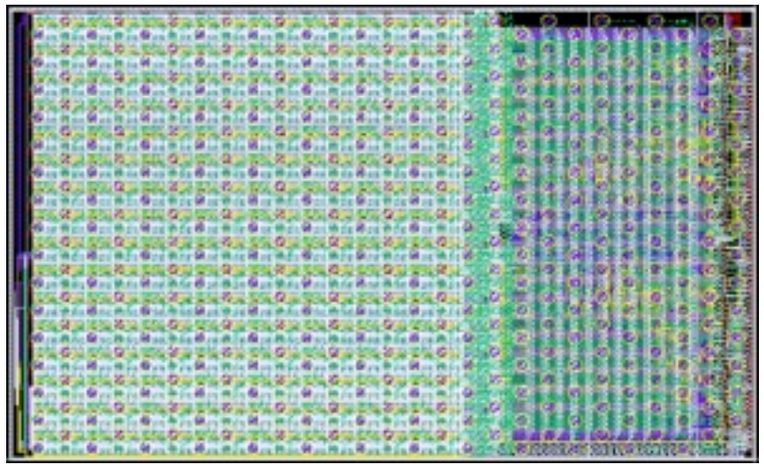


AMS high voltage 0.35 µm
Size 3.6 × 2.1 mm²
Gate and Clear signal
Fast HV up to 30V
Rad. Hard proved (36 Mrad)



DCDB (Drain Current Digitizer)

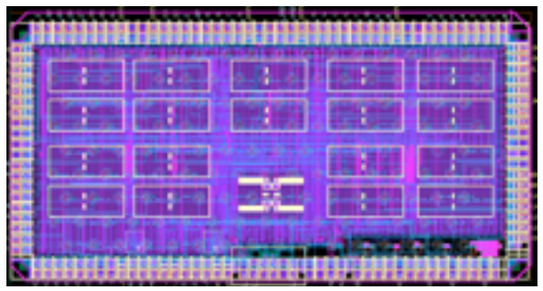
Analog frontend



UMC 180 nm
Size 3.3 × 5.0 mm²
Integrated ADC
Noise 40 nA
Irradiation up to 7Mrad

DHP (Data Handling Processor)

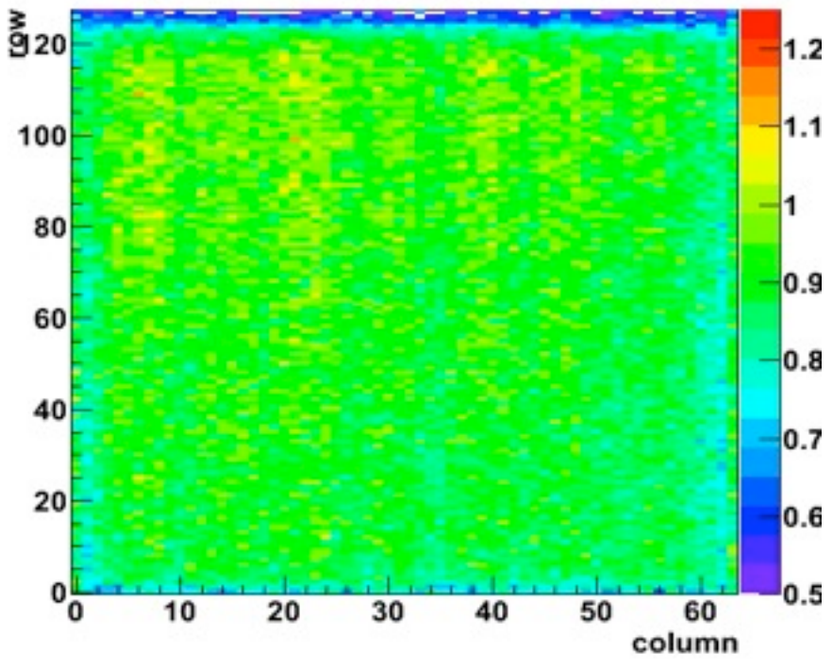
The layout of the module periphery is ready as well

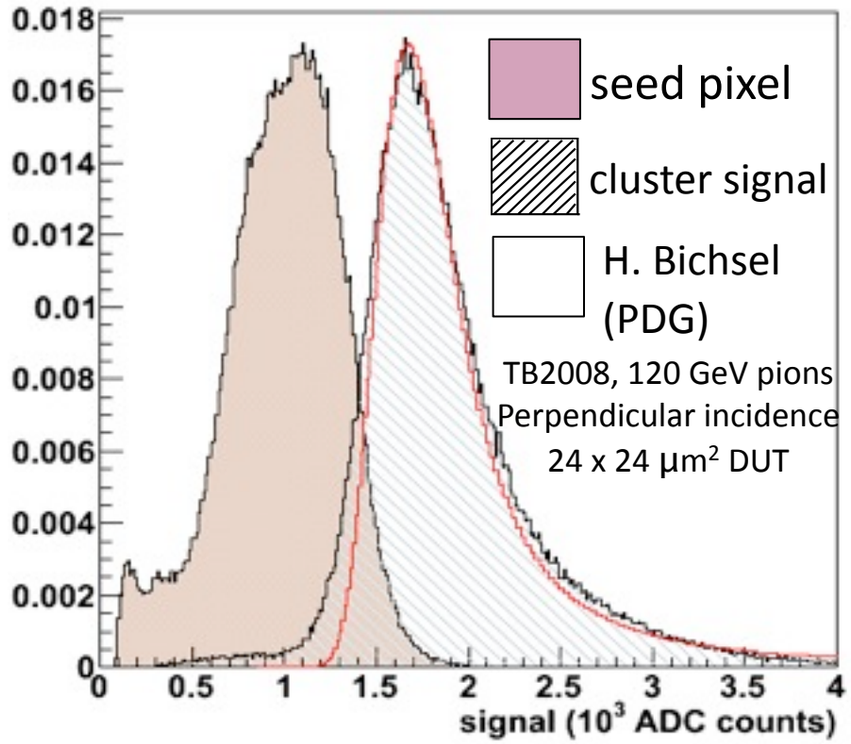


IBM CMOS 90 nm (TSMC 65 nm)
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation

Testbeam Results - ILC Prototypes

Gain map: Deviation from average seed signal



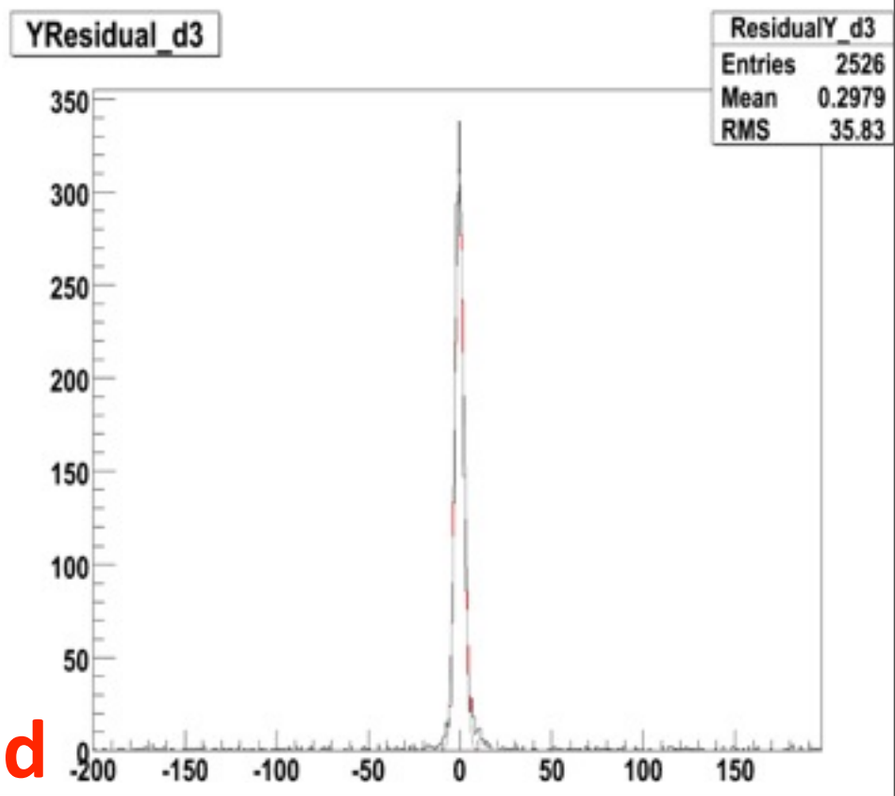


- 64x128, 24x24x450 µm³ CCG, 6 µm (TB2008)
  g_q=363pA/e⁻

- 64x256, 20x20x**450** µm³ CCG, 5 µm (TB2009)
  g_q~650 pA/e⁻

- Resolution **σ~1 µm**, 20x20x**450** µm³, analog readout with charge interpolation **ILC Design**

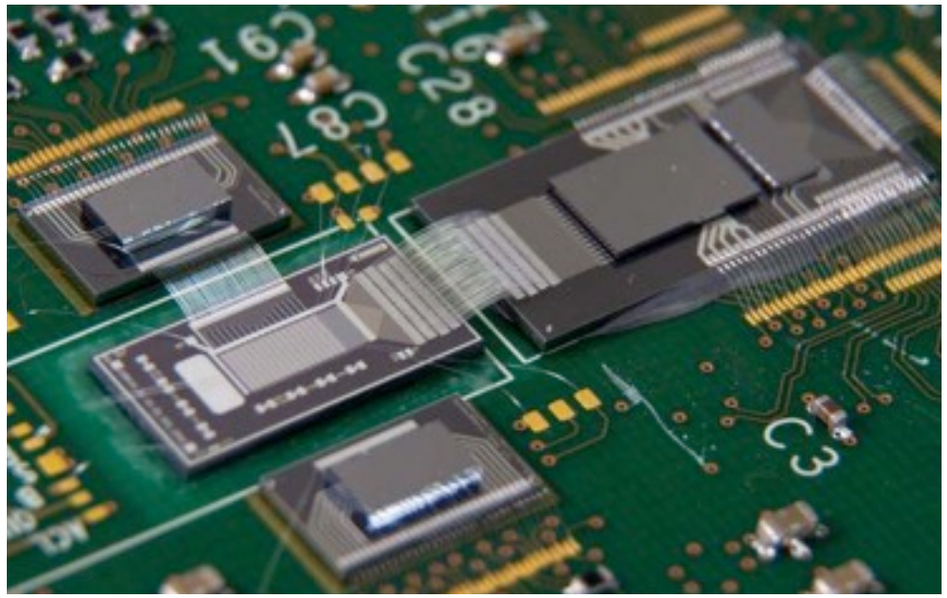
→ Extensively tested

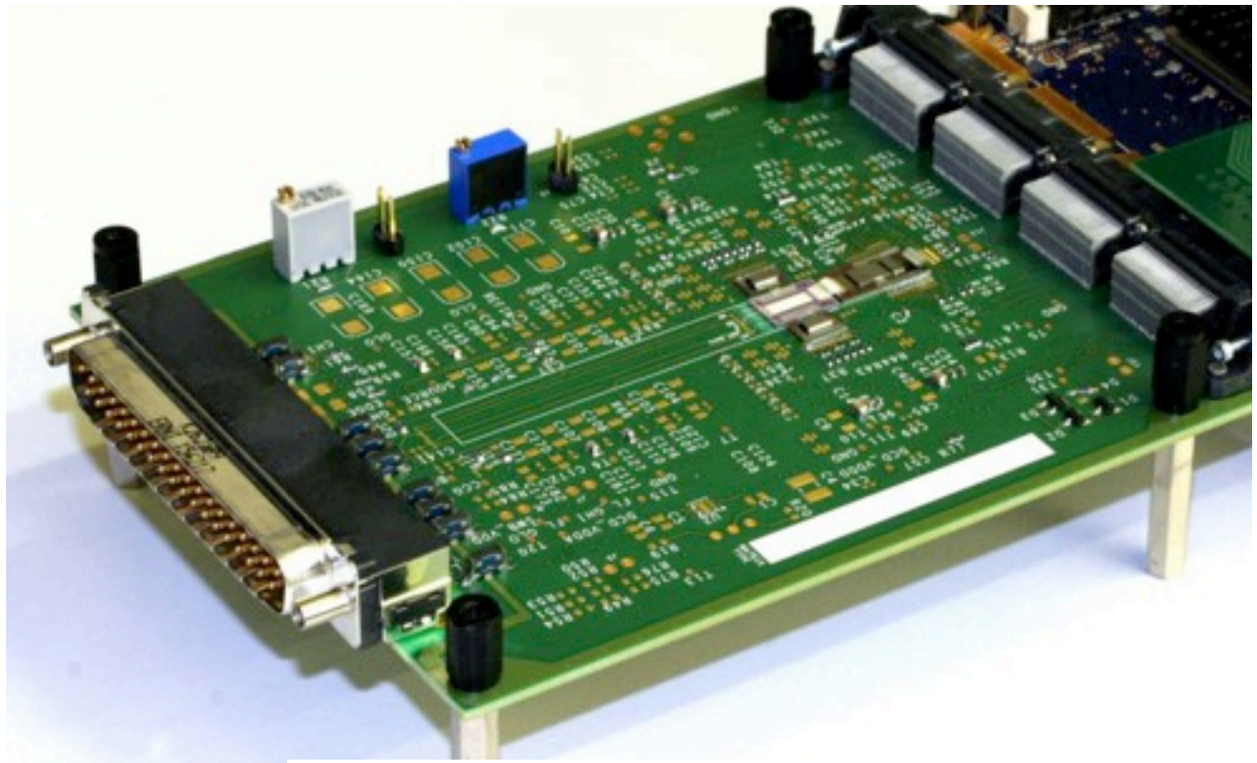


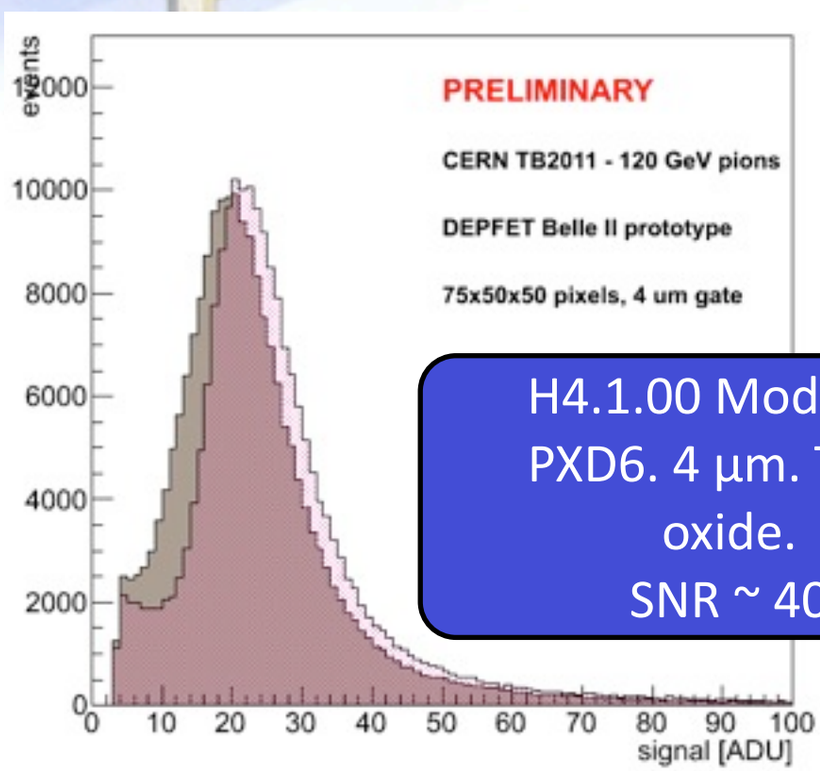
Testbeam Results: Belle II Thinned Prototypes

Belle II design
Sensor 32x64 pixels
50x75x**50** μm^3
SwitcherB and DCDB at full speed
DCDB readout at 320MHz
100 ns row time

Close to final specs!





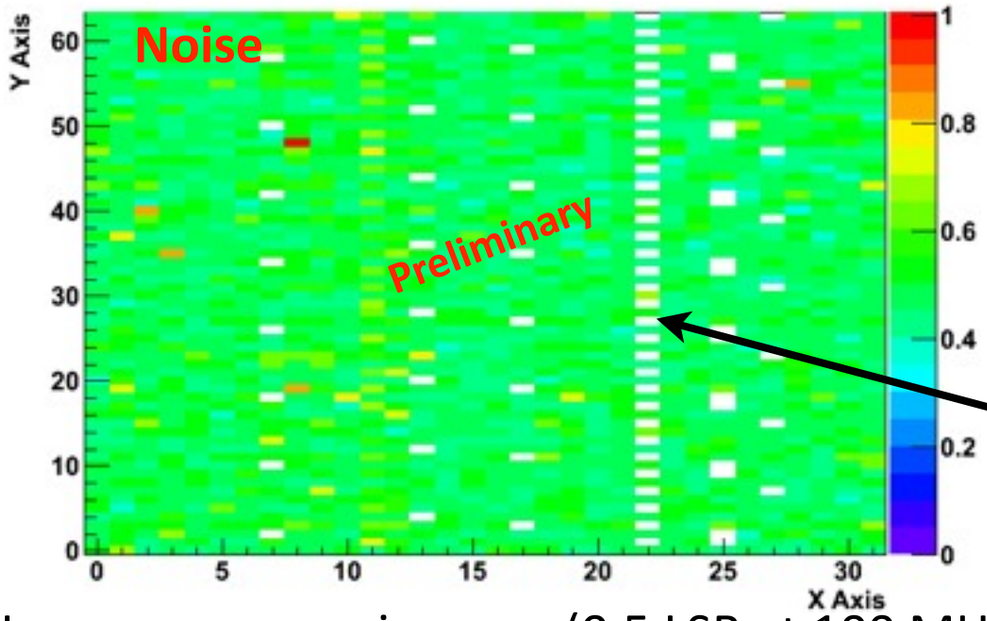


H4.1.00 Module B
PXD6. 4 µm. Thick oxide.
SNR ~ 40

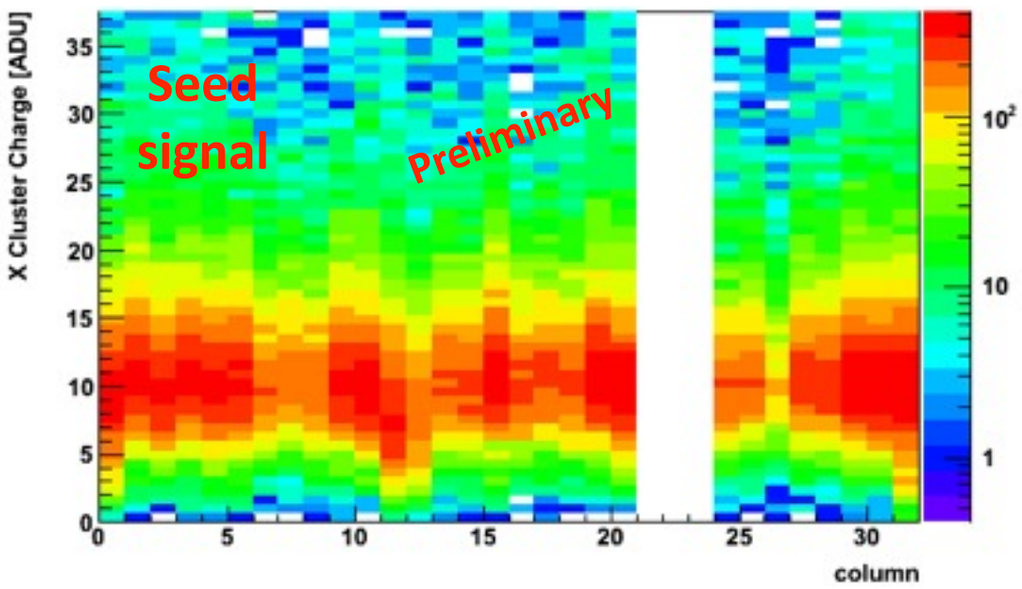
Based on the valuable information obtained with the PXD6, the final Belle II production (PXD9) is already launched

Testbeam Results: Belle II Thinned Prototypes

- Homogeneous behavior observed in noise and gain



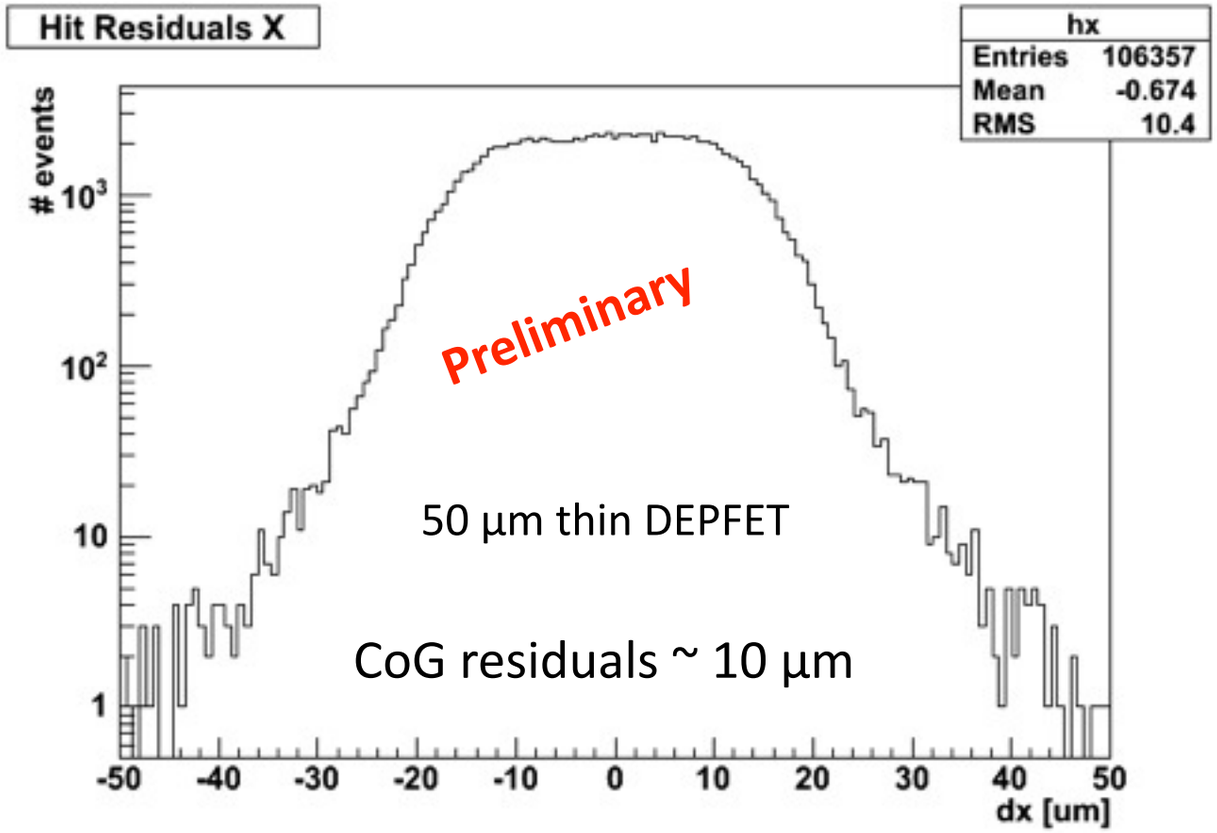
Homogeneous noise map (0.5 LSB at 100 MHz)



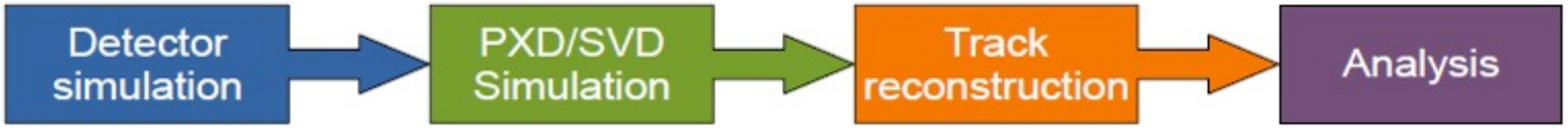
Column wise variations in the order 10%

some dead channels due to a few non-working ADC channels

spatial resolution ~ 10 µm



A Full Simulation Chain

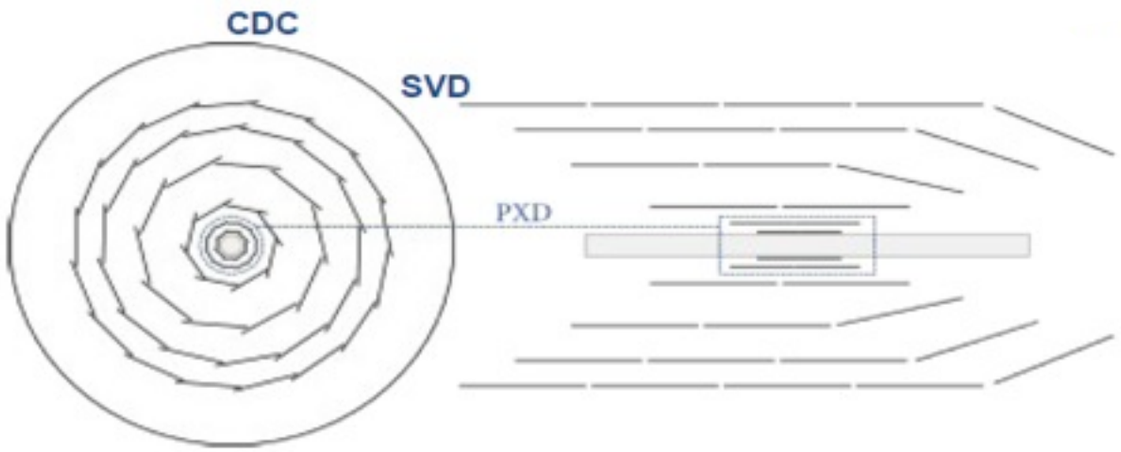


Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

Marlin tracking
PXD+SVD+CDC

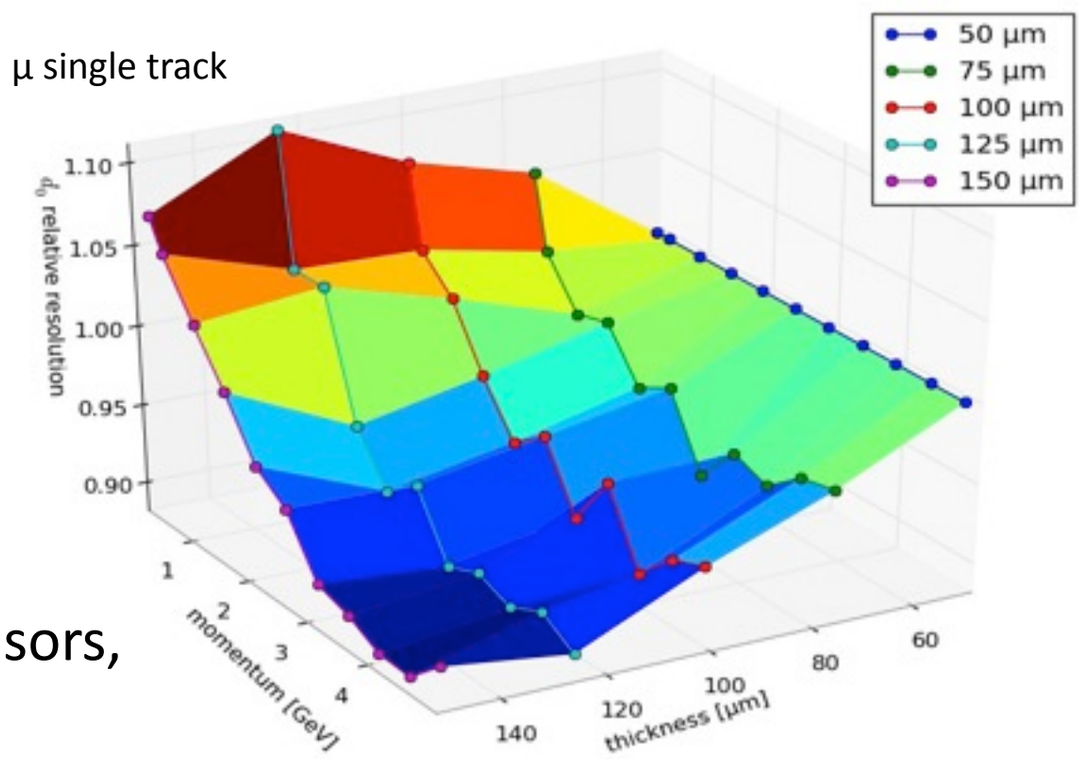
Physics channels



- Digitizer (Geant4) tuned with TBeam data:
  - Electric noise
  - Electric field in Si (charge collection time)
  - Lorentz angle in magnetic fields

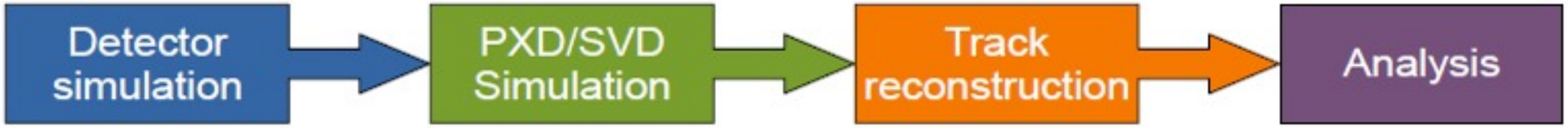
Optimization studies:
- Sensor thickness
- Pixel size
- Inner layer radius

μ single track



Best performance for Belle-II with 75 μm thick sensors, up from originally studied 50 μm

A Full Simulation Chain



Particle gun (single event)
EvtGen (physics event)
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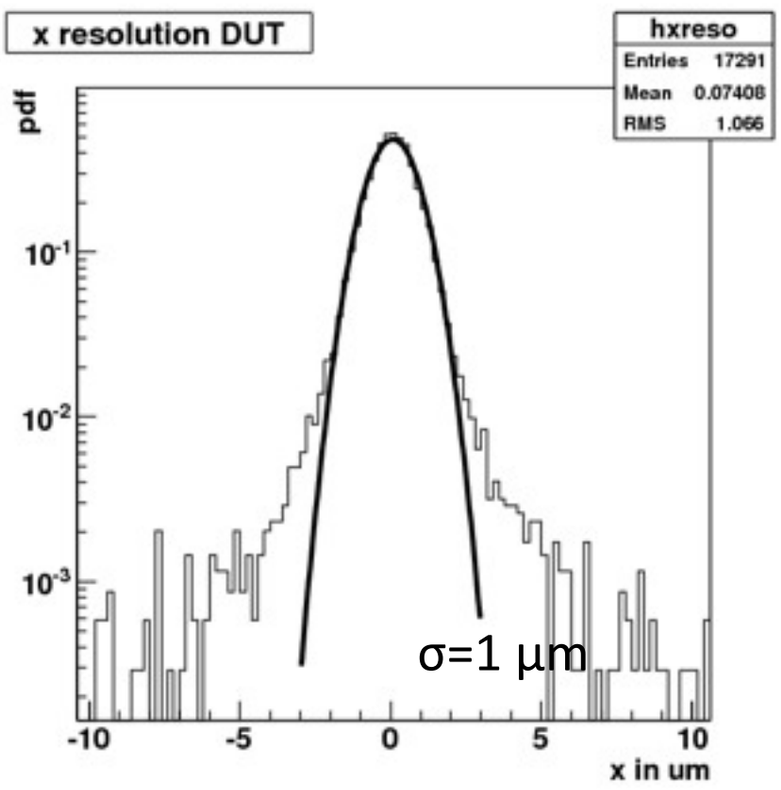
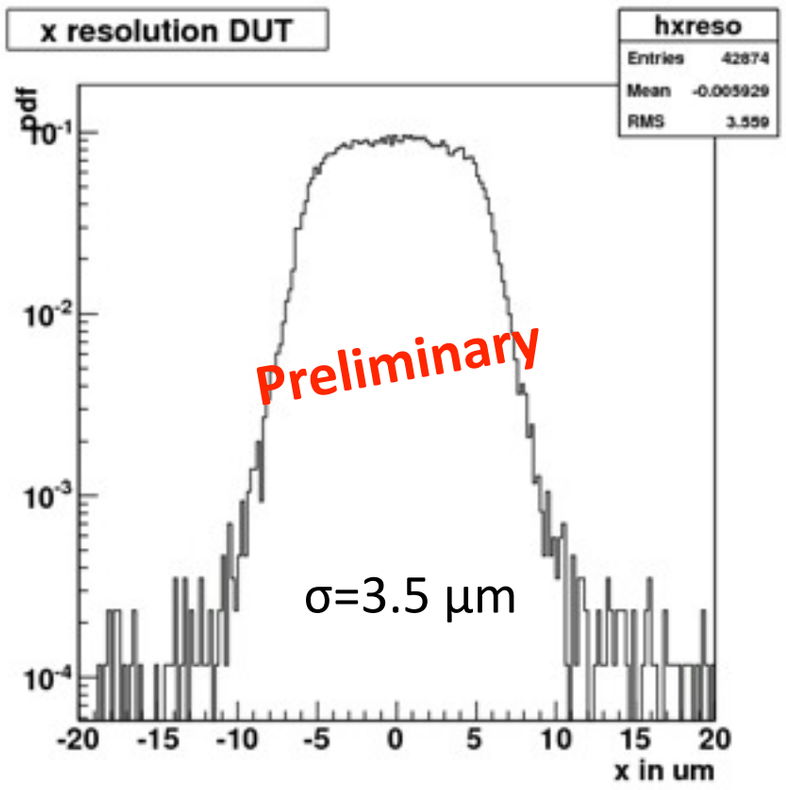
Physics channels

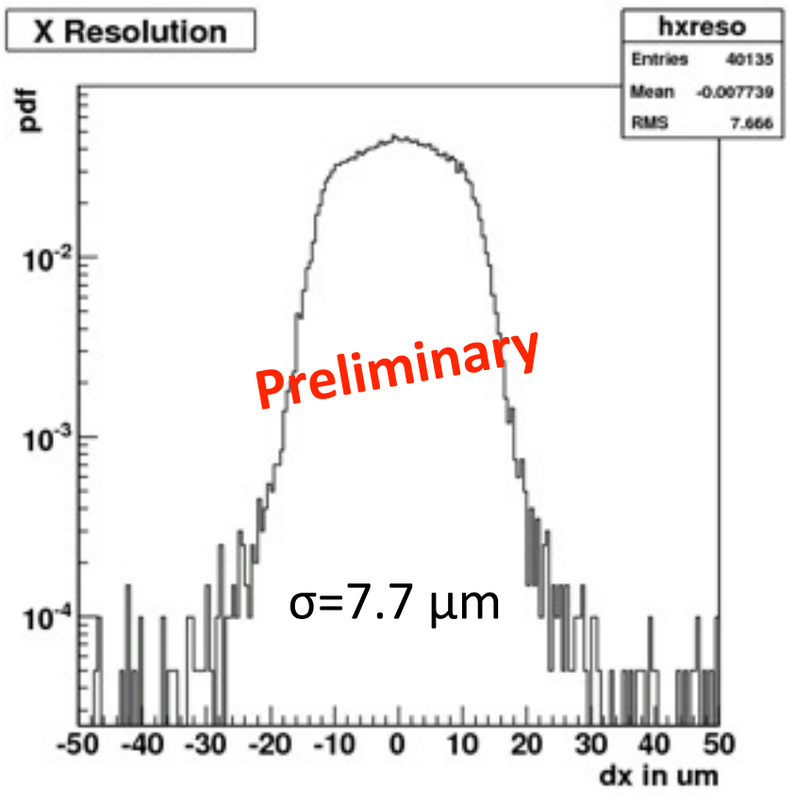
Test Beam Data
20x20x450 µm^3
Single point resolution: 1 µm

ILC (Simulation)
20x20x50 µm^3
Single point resolution: 3.5 µm

Belle II (Simulation)
50x50x75 µm^3
Single point resolution: 7.7 µm







→ Compare to ~ 10 µm seen in TB, with thinner sensors and wider pixel pitch in one dimension

Summary

- DEPFET by now is a mature technology for high-resolution, low mass pixel detectors
- Accelerated development for the Belle II pixel detector
- Full electronic chain established, ASICS designed
- Mechanical concepts established: All silicon solution with micro-joints used for Belle II PXD, CO_2 and air cooling
- Thin sensors successfully operated in test beams: signal/noise ~ 40 achieved
- Design for ILD profits substantially from Belle II experience