WORKSHOP 2012

Status of the SIT SET and ETD Silicon components for the ILD concept

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Outline: following the DBD plan

- Introductory remarks
- Barrel Silicon Tracking
  - The Silicon sensors improved technological aspects
  - The large mechanical design structure
  - The alignment and integration issues & studied solutions
  - Time stamping
  - Possible alternatives and new developments
- End Cap Silicon Tracking
  - The End Cap Silicon ladders
  - The ETD large mechanical integration challenges & studied solutions

Strategy: exploit the LHC <-> LC synergy

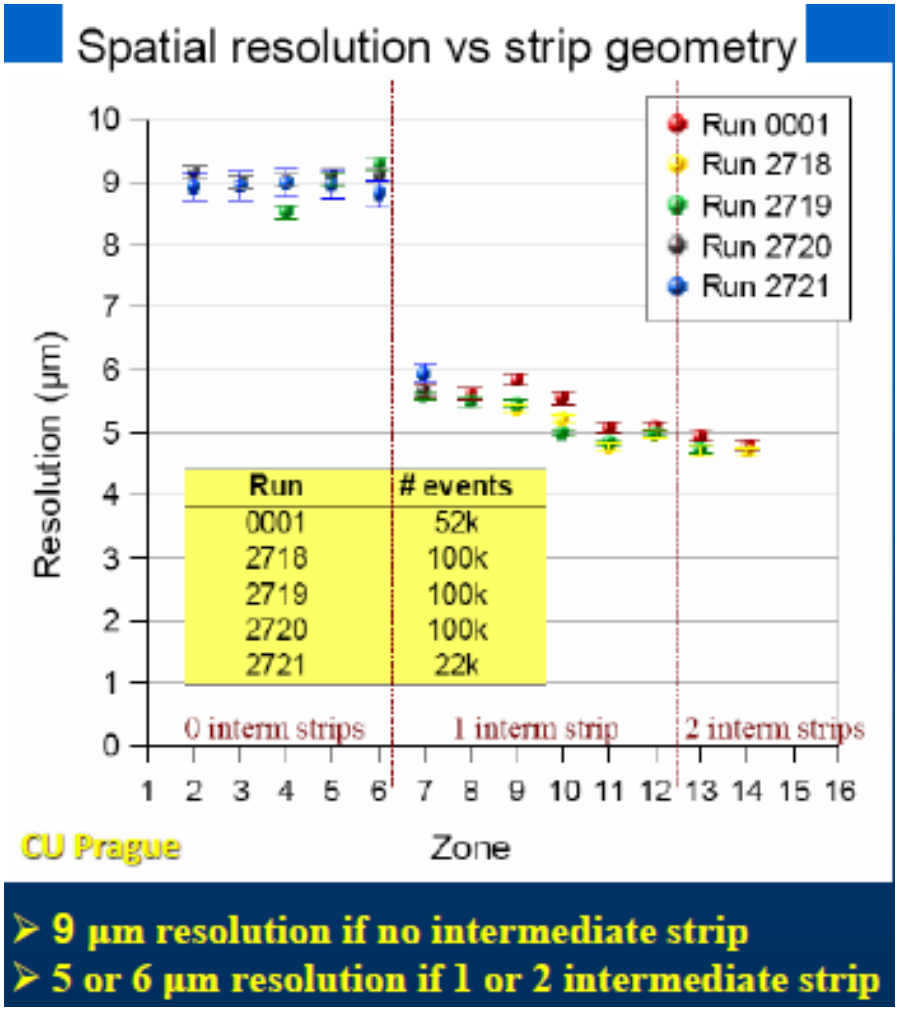
- ***Since the start, the R&D on large area Silicon tracking for LC has been closely related to the synergy between LC and LHC*** especially strong in case of the R&D for this detector technology.
- Since the last 2 years (after the LoI submission), the overall evolution of the HEP context: LC decision pending for LHC discovery (=> drastic decrease in support) and LHC upgrades for Phase 2 (2020 horizon) the R&D lines moved in favour of LHC in terms of support.
- Taking this evolution into account, the R&D on large area Si tracking especially in the ILD case is pursuing by ***fully exploiting the LCxLHC*** strong synergy on all the needed developments => see next slides.

New advances are undergoing on the main R&D topics:

- New advances on Sensors R&D
- Electronics: FEE & full data processing (intelligent devices)
- Mechanics and integration
- Test beams (together with LHC or other experiments)
- Developed new/maintain collaborations with highly expert groups and relevant industrial partners
- Developing the software reconstruction expertise

New developments on Sensors R&D

Goal 1: decrease %X0 and higher performances (spatial resolution)

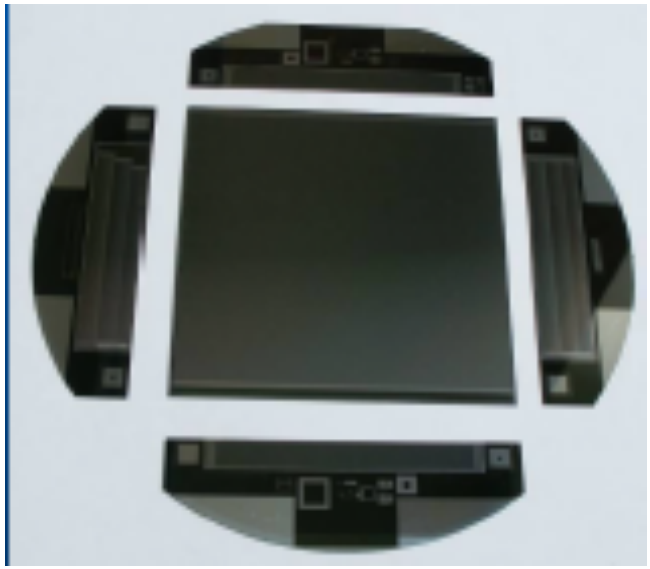


LHC-LC synergy, phase 1

- ILC R&D inherited the use of test structures for optimizing the sensor mask design.

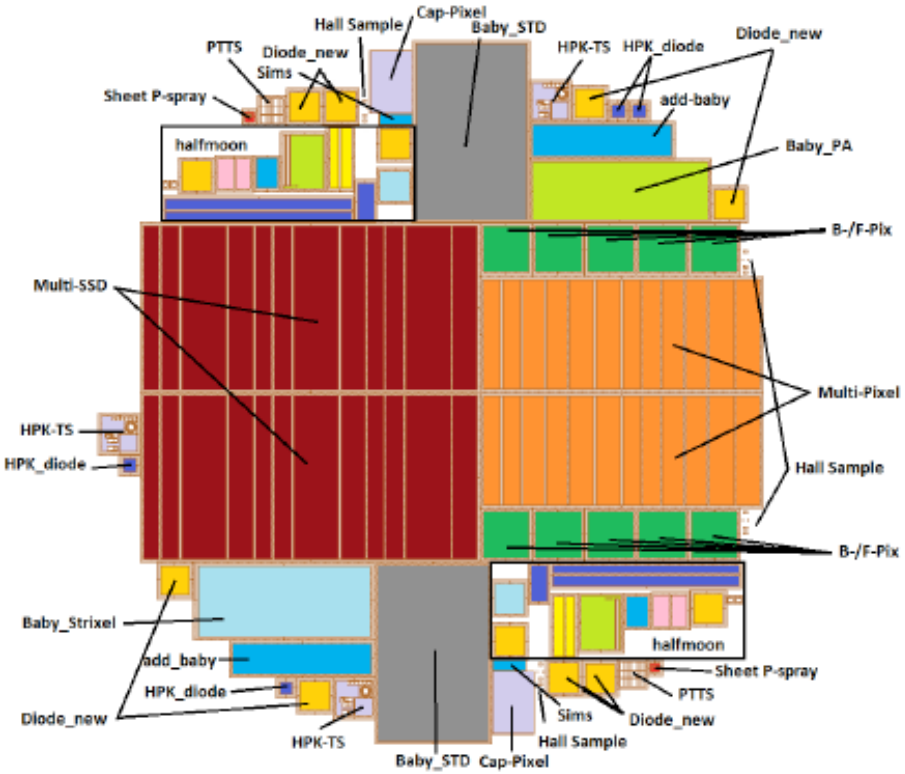
=> New developments where studied with large area strip sensors (HPK 9,45x9,45 cm2)

To still increase spatial resolution and less %X0: smaller pitch (50 µm pitch) inter-strips (not connected) and decrease in sensor thickness (300 µm instead of 500 µm for large sensors)



New developments on Sensors R&D (cont'd)

Goal 1: decrease %X0 and higher performances (spatial resolution)



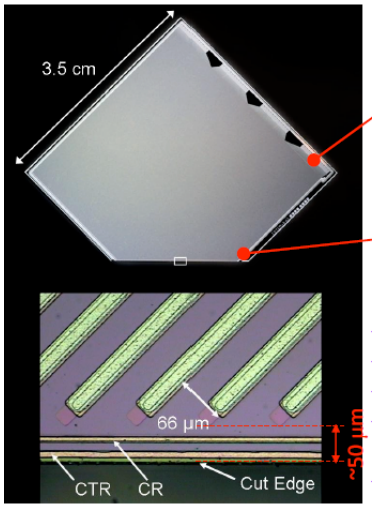
LC-LHC synergy, phase 2

LHC experiments pursue a campaign to identify the future sensor technology for building new Si tracking system =>

Extensive use of test structure with different materials, different thicknesses (300, 200, and 120 μm), different strip sizes and pitch dimension (smaller as compared to actually installed LHC sensors and test of new sensor designs: strixels (short strip) and sensors with integrated pitch adapters.

All these various features are relevant for LC as well and are developed and produced in collaboration with HPK.

New Sensors R&D and integrated pitch adapters



Only 50µm from end of strip to end of sensor!!!

Goal 2: "flat" Si trackers

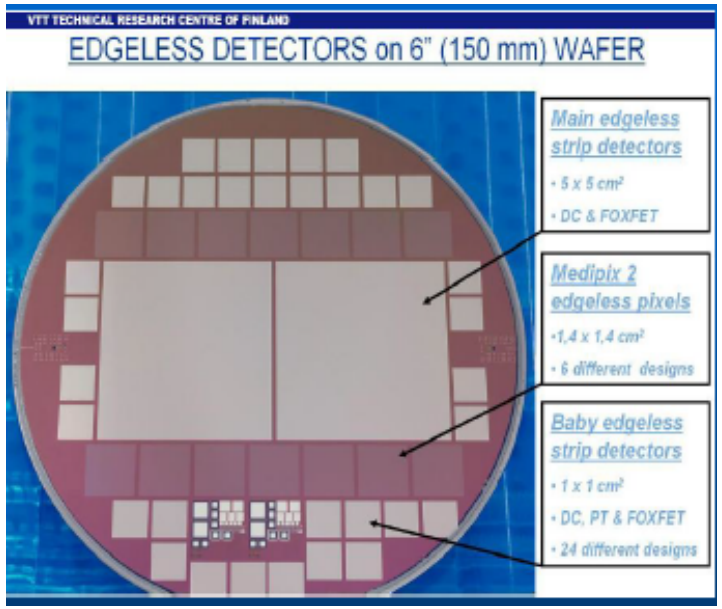
Flat Si trackers are based on

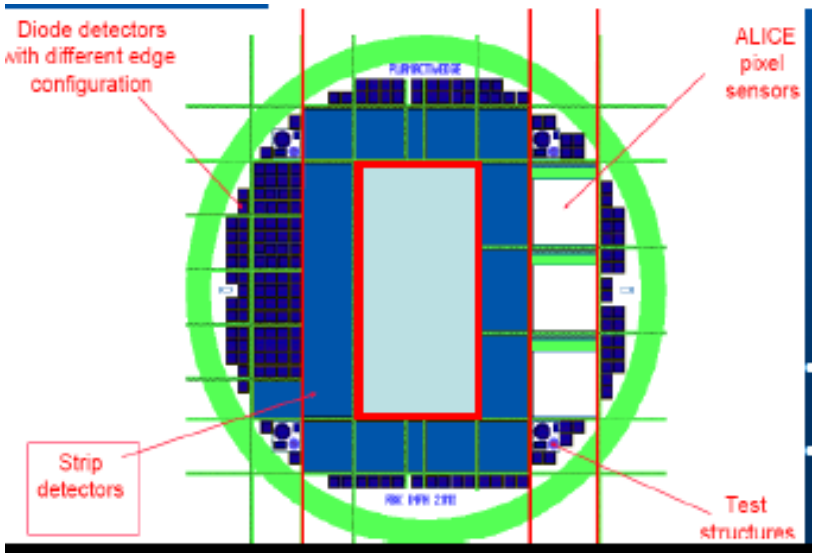
1) edgeless sensors (
2) integrated pitch adapters

=> Pioneering work on " flat trackers" achieved by the ILC R&D:

LHC-LC synergy, phase 1

ILC R&D promoted the use of ***edgeless sensors*** (also used at LHC (TOTEM) with VTT & IRST





New Sensors R&D: edgeless Si sensors

Goal 2: "flat" Si trackers

LC-LHC synergy, phase 2

LHC is experiencing the edgeless technique for all the sensor types: pixels, strixels and long strips.

Ex: **Outer tracking Trigger components R&D for CMS upgrade**

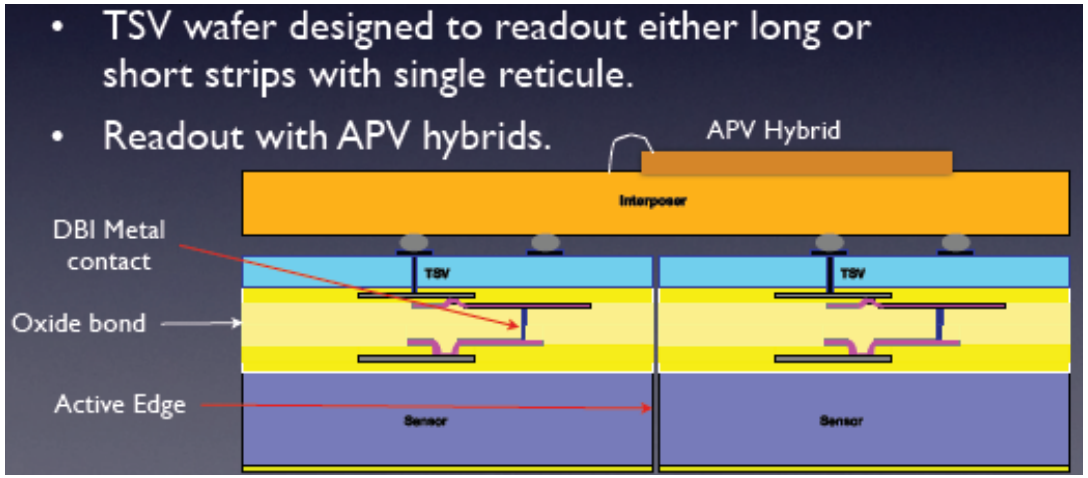
(US-made option: R. Lipton et al.)

Started with VTT, now using US firms (see next slides: courtesy R. Lipton et al) presentation at the WIT 2012 Workshop

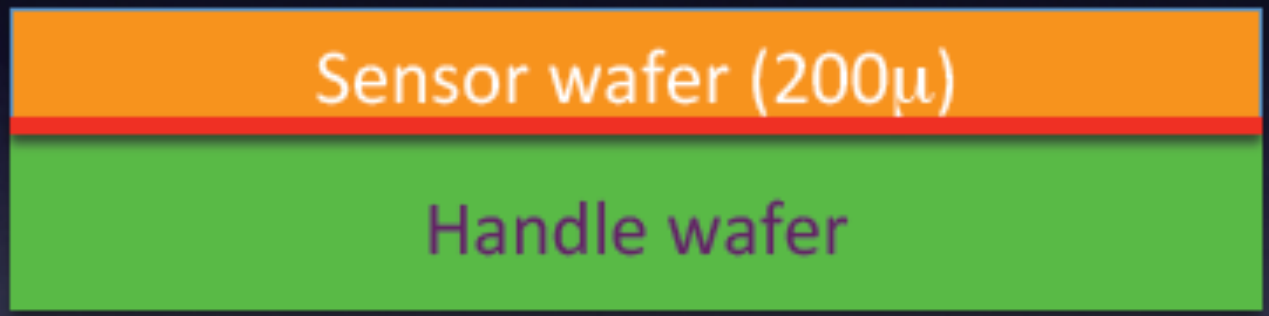
It combines 3D /SOI technology with TSV for Direct Bonding Interconnect (DBI) and thus getting Read Out Integrated Circuits (ROIC's) and pushing as well for 8'' wafers.

VERY challenging R&D going on (EdgelessTechno developed by UCSC, Stanford et al. see next slides)

R. Lipton et al are building a demonstrator with active edge Sensors, oxide bonded wafers And TSV dummy readout wafers (to start with)



3D Active Edge Fabrication Process



3D Active Edge Fabrication Process

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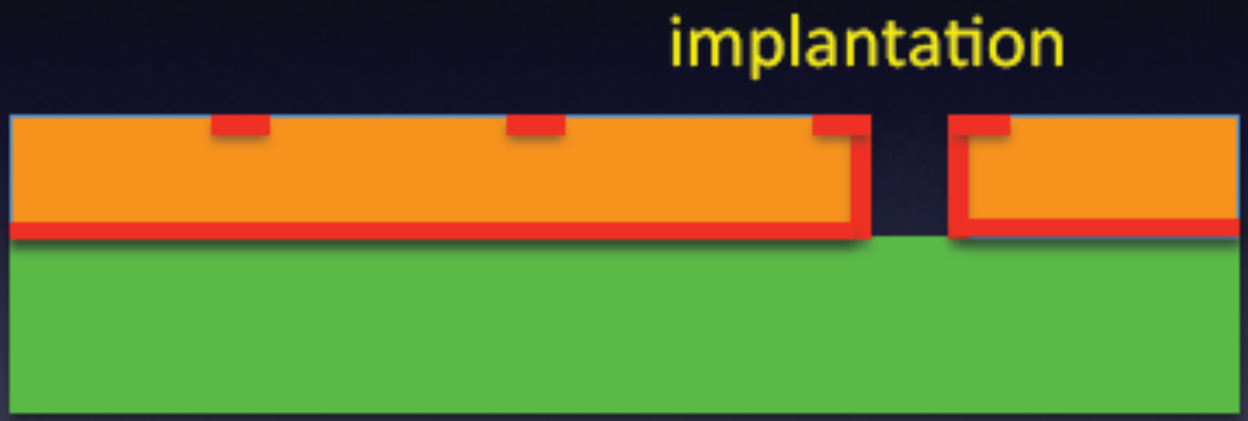
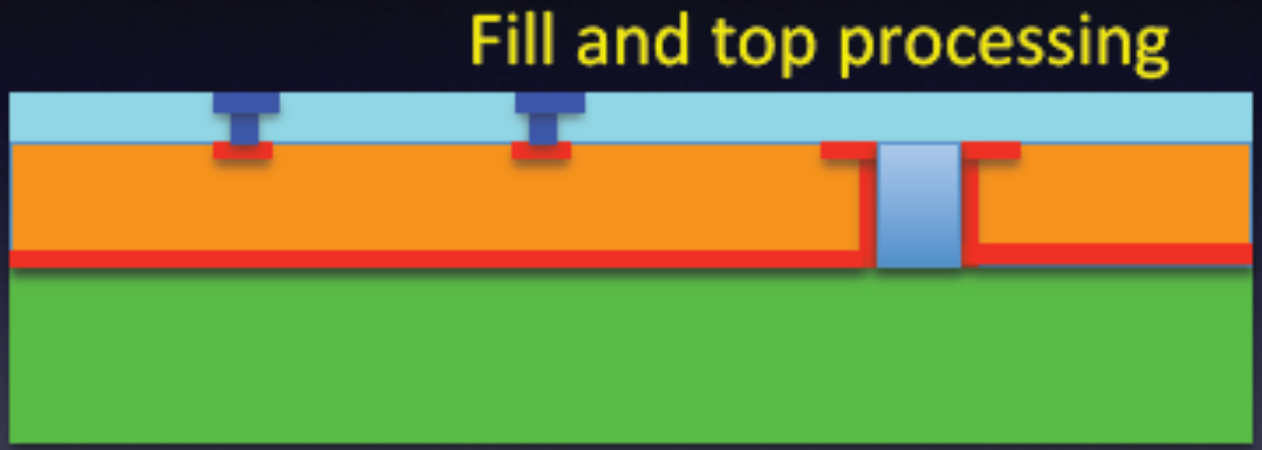
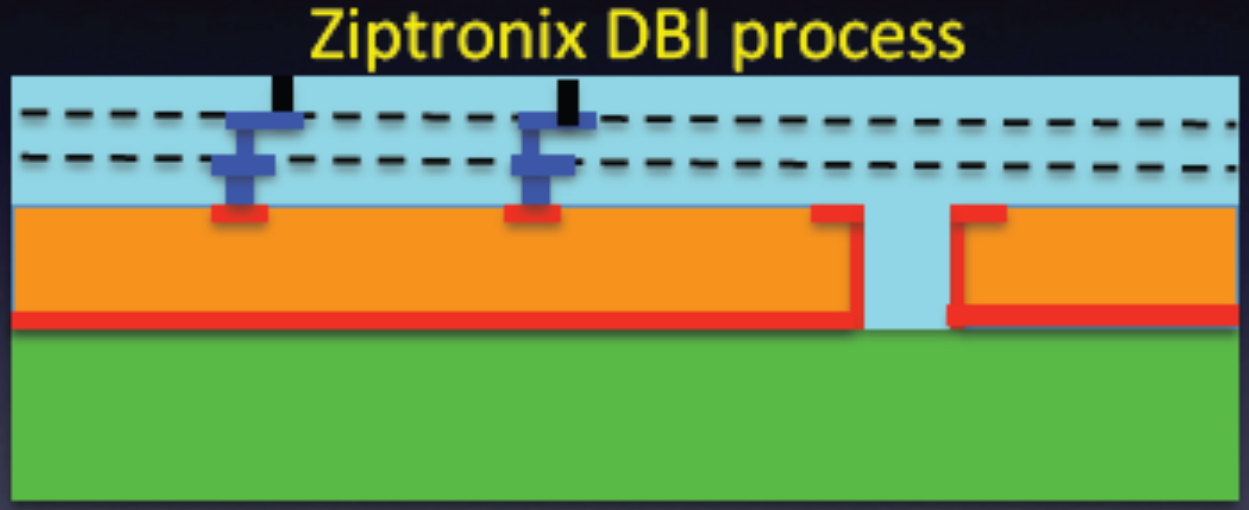


3D Active Edge Fabrication Process

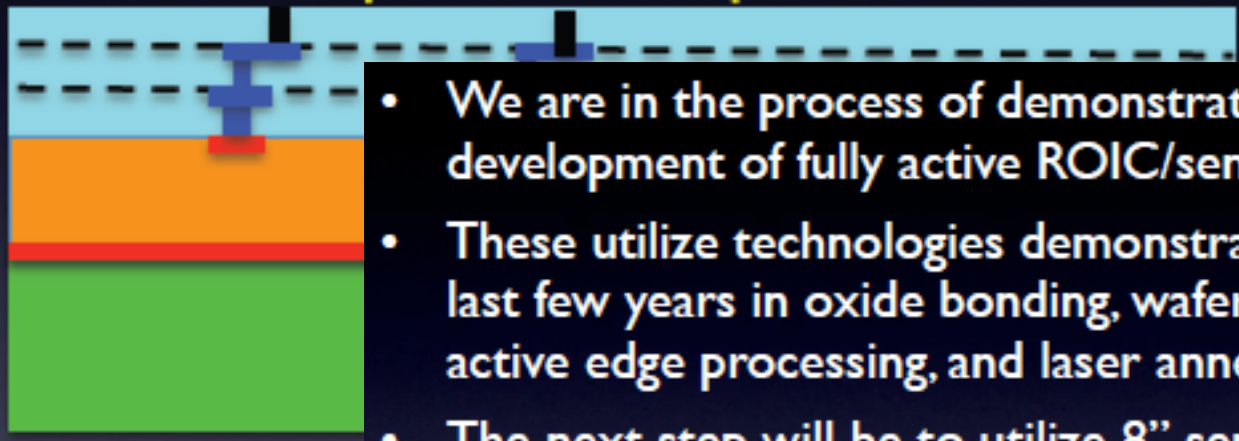


3D Active Edge Fabrication Process



3D Active Edge Fabrication Process

Ziptronix DBI process

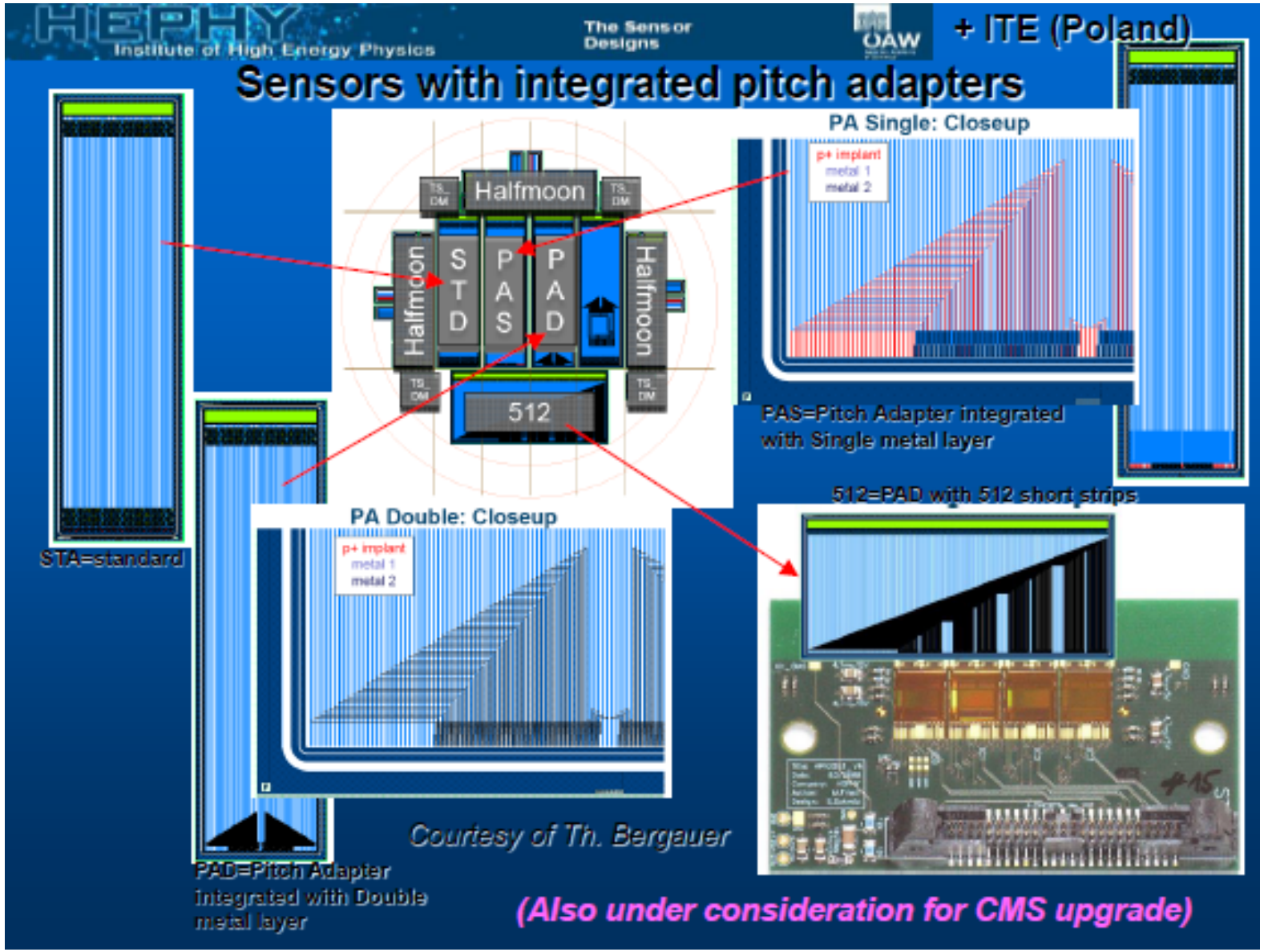


- We are in the process of demonstrating the development of fully active ROIC/sensor tiles
- These utilize technologies demonstrated over the last few years in oxide bonding, wafer thinning, active edge processing, and laser annealing.
- The next step will be to utilize 8" sensor wafers with spare TSV ROIC wafers

- This work is being driven by CMS upgrade track trigger needs - but clearly has wider application. It is an outcome of earlier R&D on detectors and electronics for the linear collider.

New Sensors R&D and integrated pitch adapters

Goal 2: "flat" Si trackers => IPA's

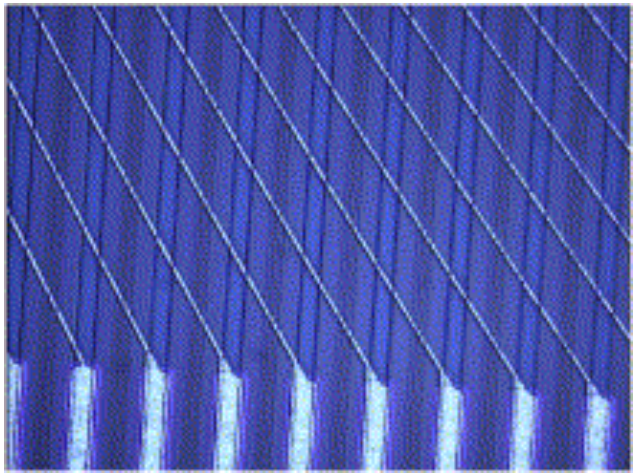


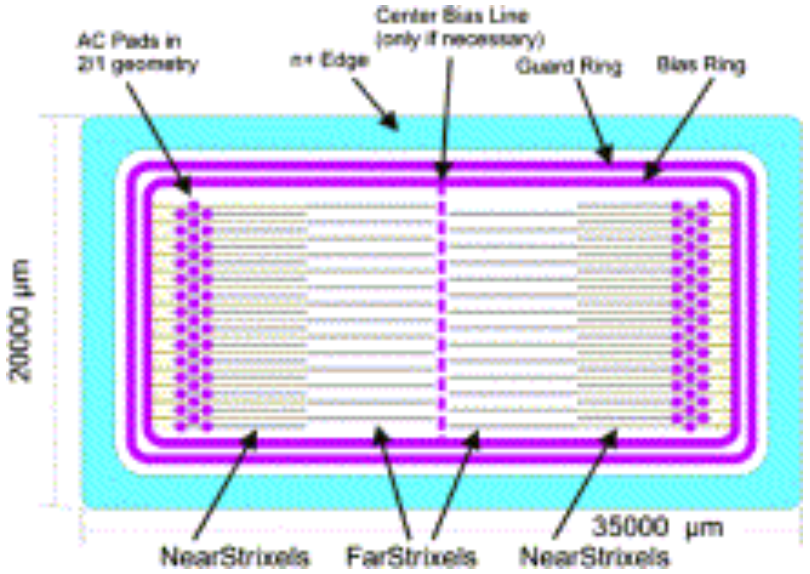
New Sensors R&D and integrated pitch adapters

Goal 2: "flat" Si trackers

LHC is including the development of integrated pitch adapter (IPA) as well in the design of strip sensors:

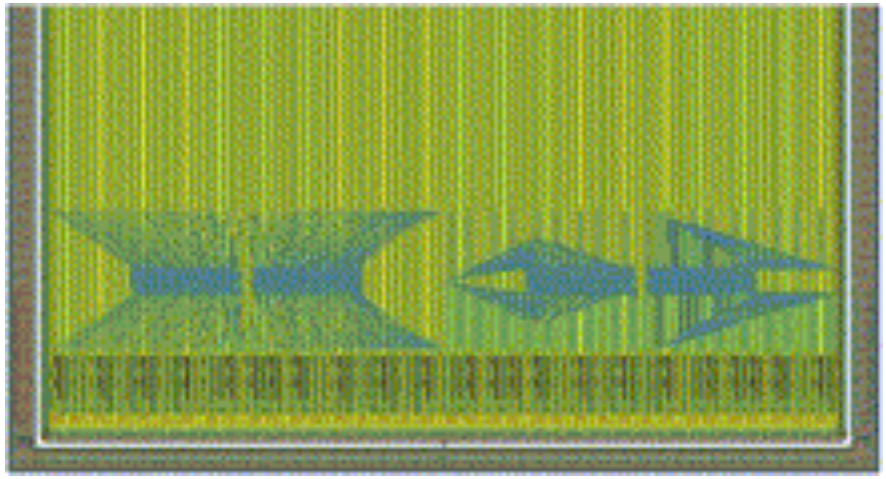
Details of routing fitting with bond pads





Strixels with IPA

Test of various IPA routines => impact on cross-talk, noise & other sensor characteristics



IPA in a second metal layer

REMINDER: THE SENSOR R&D ROADMAP

Conclusion on sensors for the DBD:

The baseline (see ILWC2010) on Si sensors for SIT/SET/ETD is confirmed with the latest R&D progress as quite feasible, namely:
A unique SSD strip sensor type (min 6" wafers), 9.5x9.5 cm^2, 200 µm thick, 50 pitch and integrated pitch adapter.
it will be briefly described as such in the DBD for SIT/SET and ETD components, pointing out the latest advances and results in this topic.
The provider is HPK at the present time.

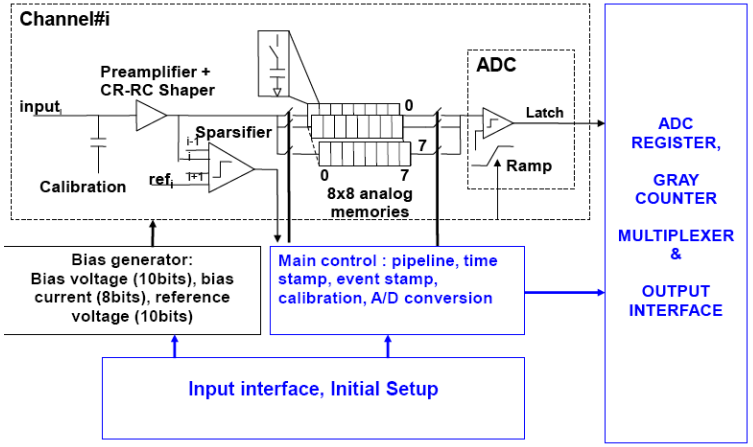
Just one (interesting) remark/issue
By 2020, ATLAS & CMS are building/rebuilding their Si tracking system
=> About 200 m^2 for each experiment.
If ILD (SiD) join the game at the same time, it would mean additional 2x 200 m^2
⇒About 4 Football (soccer) camps in SSD's...
⇒ HPK should at least find subcontractor(s) or else other firms should participate to the Market (let's see how HPK and LHC experiments handle this point).

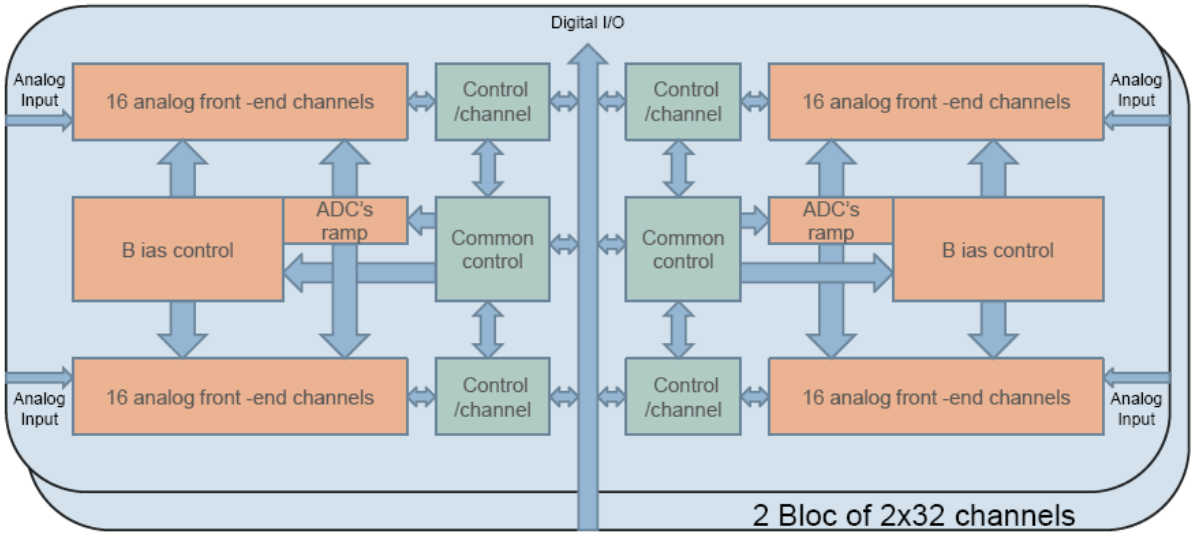
Advances on FEE & full processing of Si tracking signals

New advances are undergoing on:

- The use of 130 nm CMOS technology for mixed mode analogue-digital FEE readout design is now well established and actively developed by several LHC experiments for their upgrades. The use of 65nm technology is also under active developments (ex: timepix or FEI4).

- The preliminary version of the FEE , mixed mode design developed and tested in CMOS130 nm technology will be revisited by 2013, taking advantage of advances on the FEE of the Si trackers (for the LHC upgrade) and once the LC project is hopefully launched (thus the machine to be built is decided).





Advances on FEE & full processing of Si tracking signals

- Lot of advances are underway on the on-detector cabling and the long distance connections between the on-detector electronics and the full DAQ system architecture, based on the development of “intelligent devices”.

- The ongoing R&D on real time processing of Si tracking information (tracking–based trigger architectures) for LHC upgrades is inspiring from several points of view:
  FEE readout & several advanced related technology (VDSM, TSV/DBI, 3D packaging techno) and High Level processing.

For the DBD, the ILD detector concept will include new perspectives for an improved FEE-readout design and of the overall DAQ signal processing architecture.
New collaborations on these aspects have just been launched.

Time stamping and Time tagging

Very important issue especially for the Fast LC case
At ILC or CLIC, because a relatively very low occupancy,
a ***time stamping of order:***

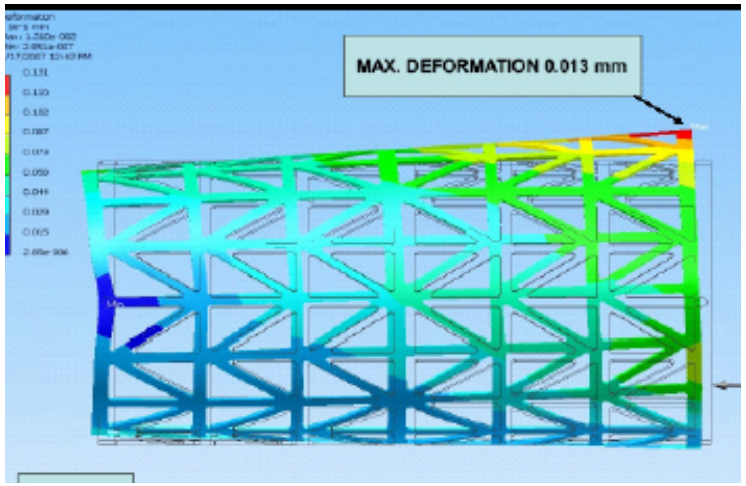
- 10 ns in the CLIC case (remind BX (CLIC): 0.65 ns)
- 100 ns for ILC, slower machine (300 ns BX)

Implementing an adequate time stamping relates both to the sensor and to the associated FEE. It may lead to additional power dissipation and material budget => the idea to install dedicated Time stamping layers at the outmost part of the tracking system just before the e.m. calorimeter
(=> even if more %X0 it acts as a preshower device)

To be reminded:
The interesting feature of the hybrid tracking as in ILD, i.e TPC x SET demonstrated by M. Hautschild's simulation study:
By combining the TPC and SET with 50μm pitch => a time stamping of 2.8 bunch crossing is achieved.

NA62 Gigatracker prototype: a low mass & sub ns time resolution silicon pixel detector

New R&D on mechanical design, fabrication-line, integration



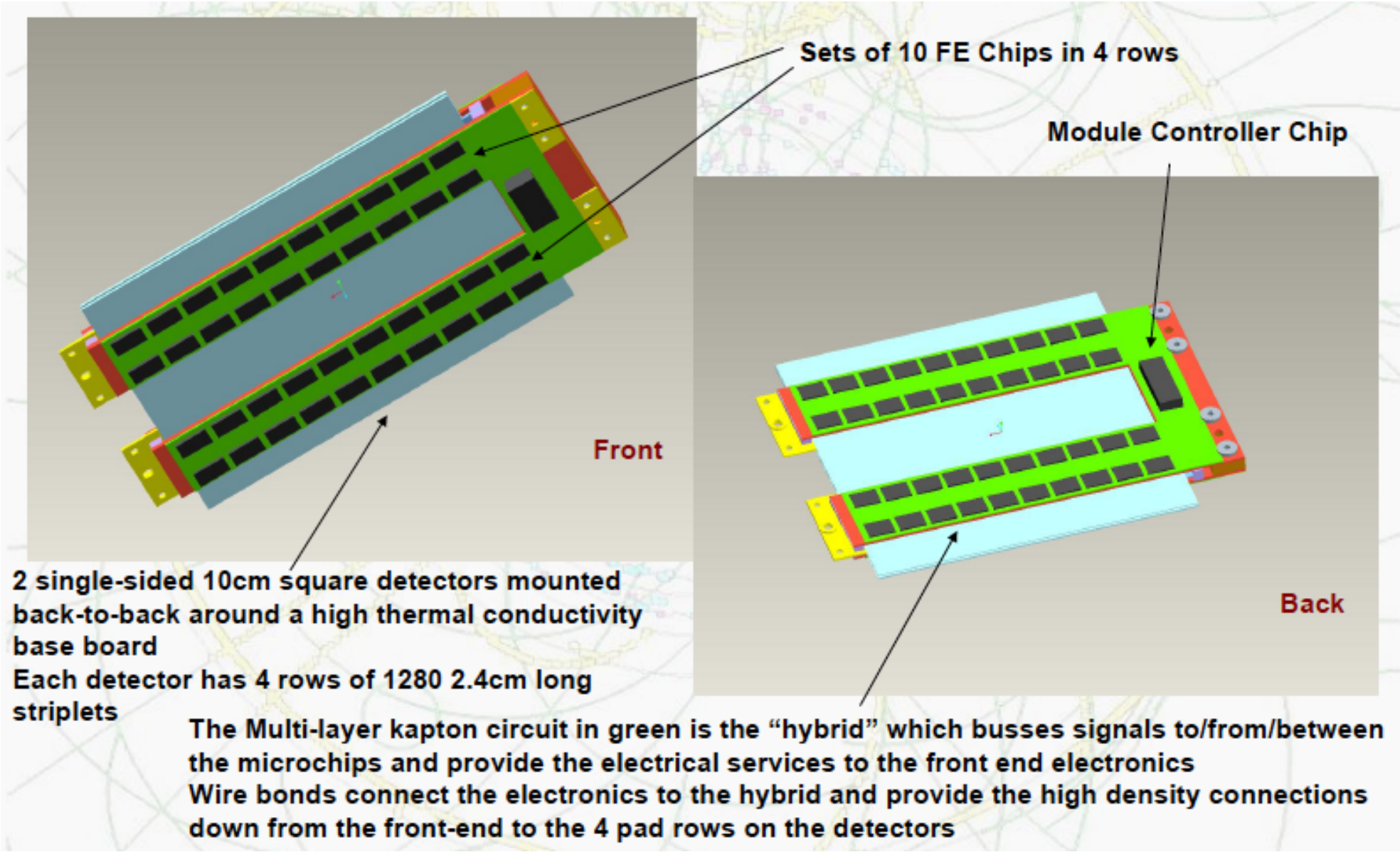
LC x LHC have similar goals:

- Decrease %X0
- Simplification of mechanical design of large area Si trackers of the fabrication-line and of the integration (installation & push-pull)

Important new feature:
*"**intelligent structures**" = structures that do not act only as support structure, but also include other functions:*
cooling, cabling, services, positioning =>
*a lot of interesting developments in many different locations & applications including **novel materials***

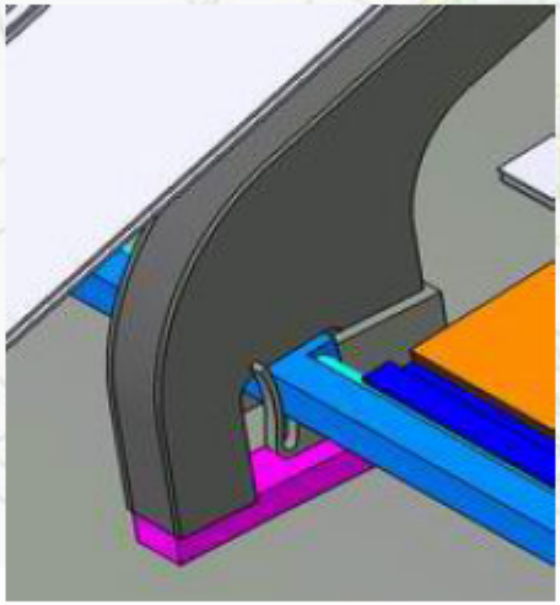
Ex: SuperB is developing novel micro-tubes techno embedded in the Carbon Fiber Reinforced Polymer (CFRP) support structure.

Ex: Modules for LHC upgrades



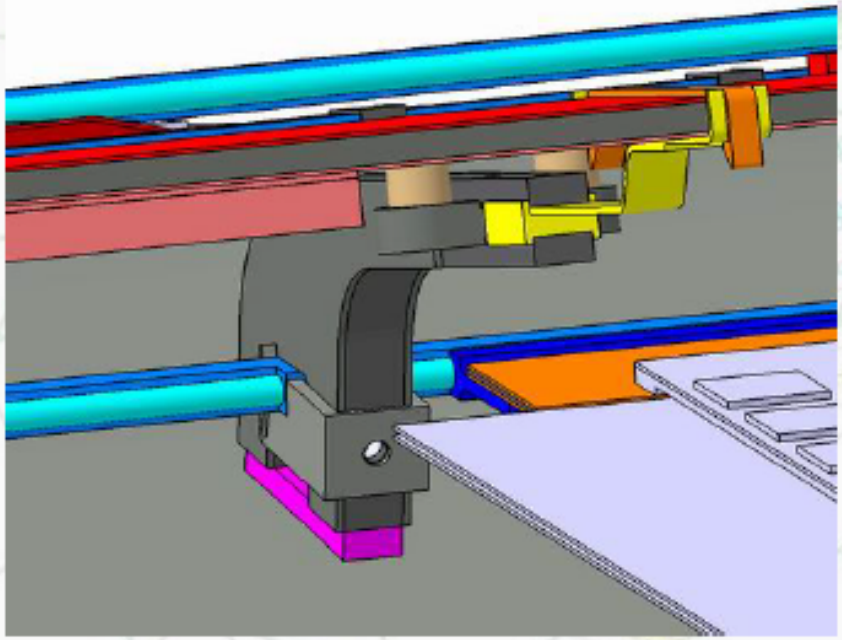
Individual Module - Direct Mounting

ATLAS

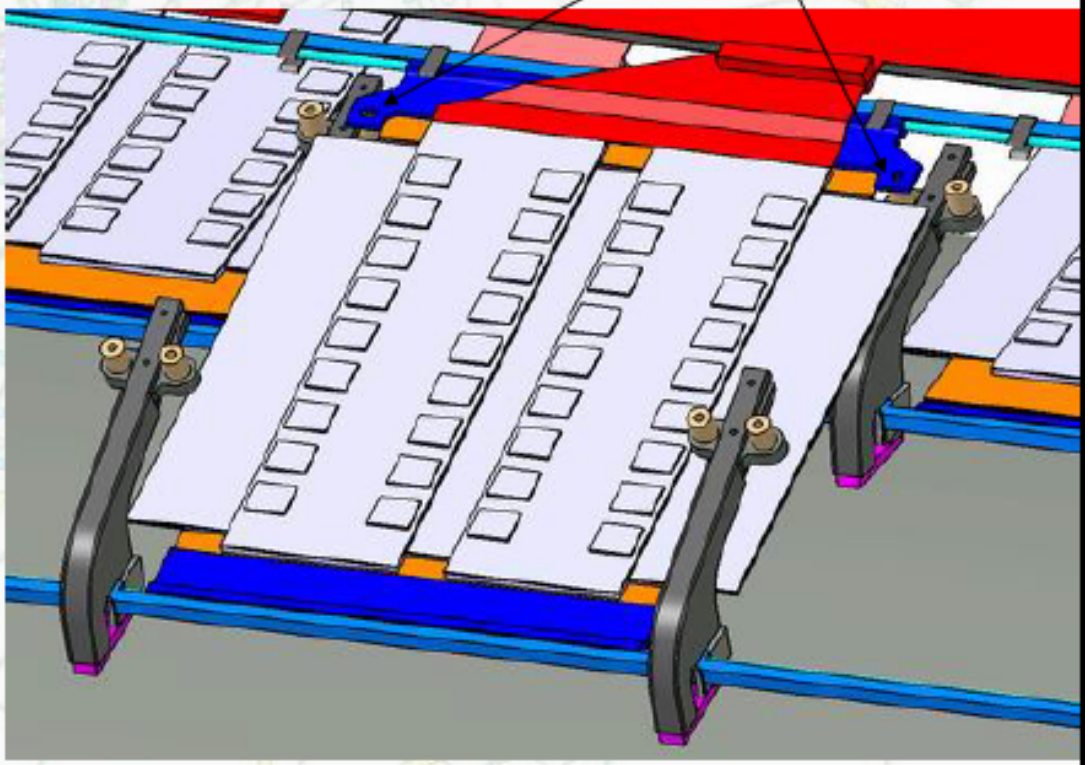


- 3rd “point” is defined by the pipe
- Cooling block is set with 2 fixation points on the pig-tail side
- 1 bracket is holding 2 neighboring modules
- The bottom left pipe is embedded in the brackets and must be assembled before the module.

Y. Unno



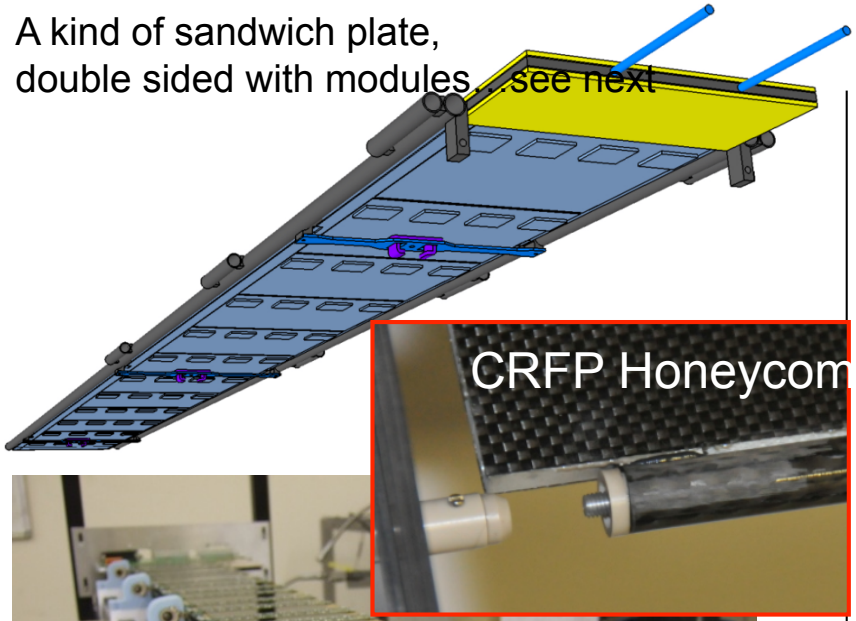
2 fixed mounting points

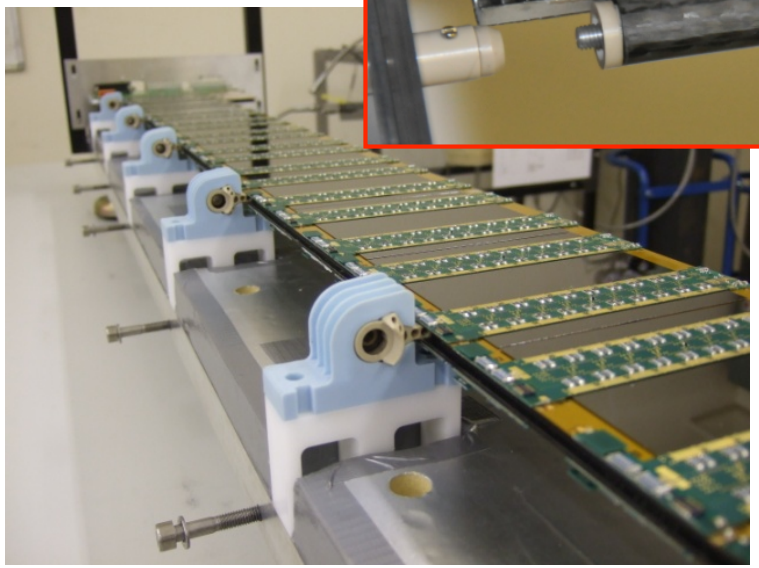


Ex: ATLAS => 2 approaches in parallel to hold 12 modules (or more…): **Staves** & **SuperModules**

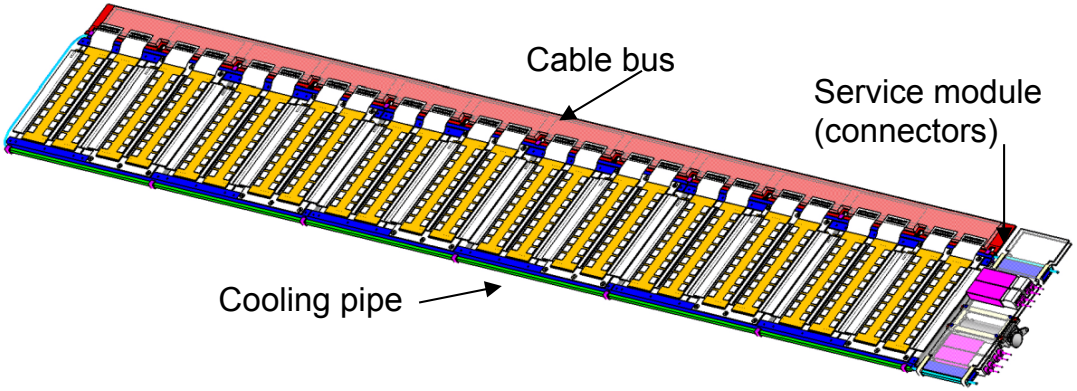
- Self supporting, light and robust structure
- Independent part including Modules, Services, and its own Cooling
- to be assembled after barrel assembly
- Replacement at any moment (thanks to End Insertion)

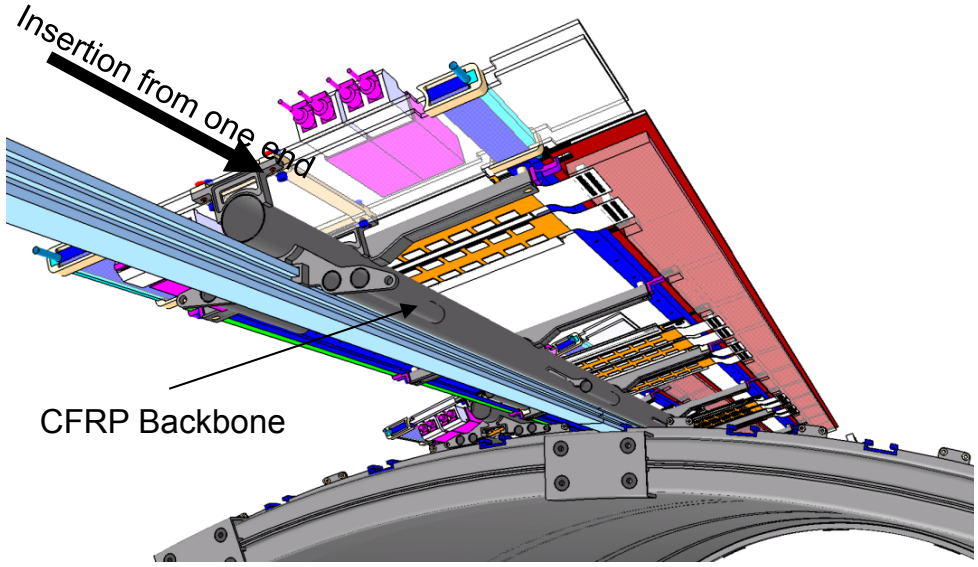
A kind of sandwich plate,
double sided with modules…see next





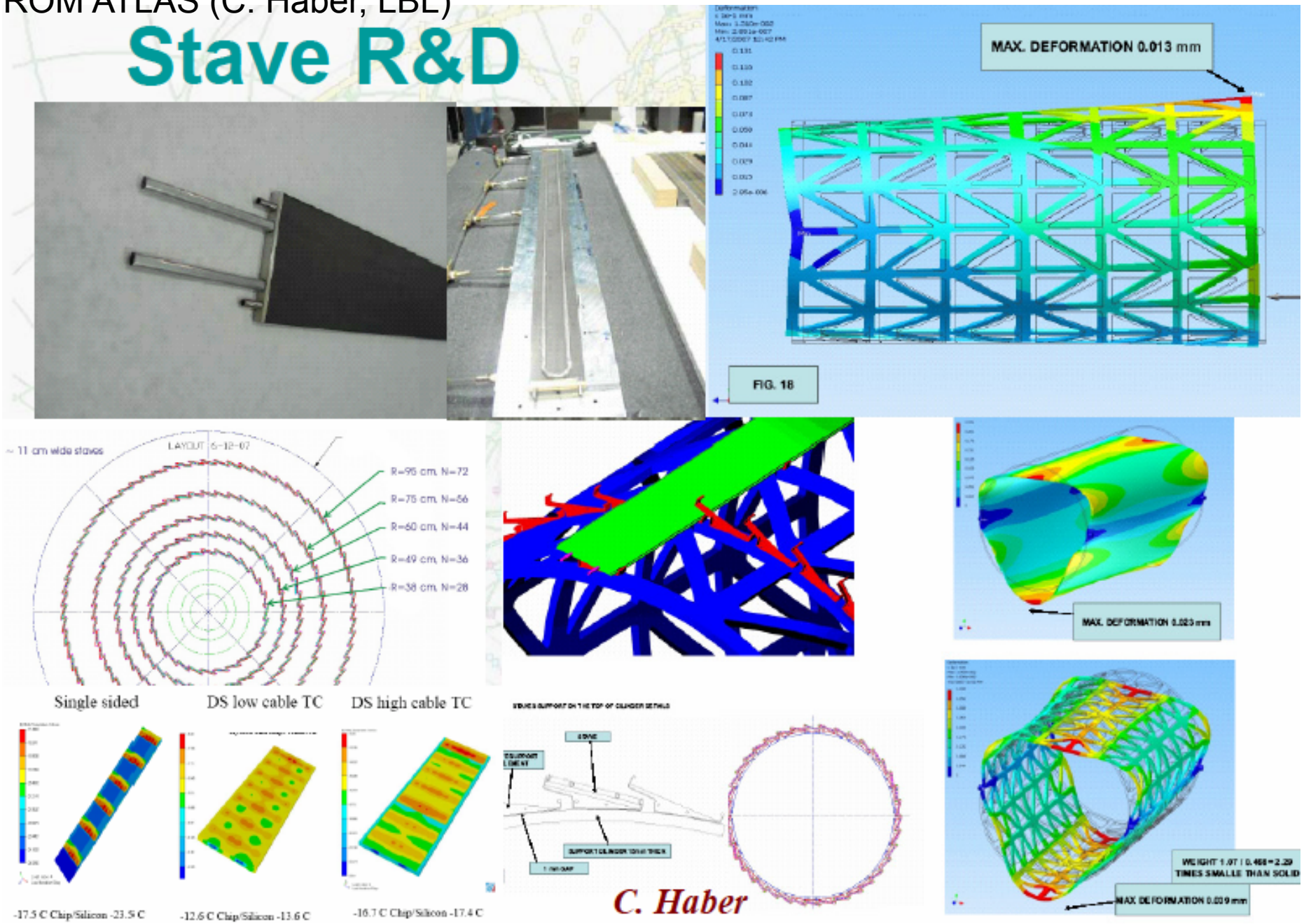
Stave approach



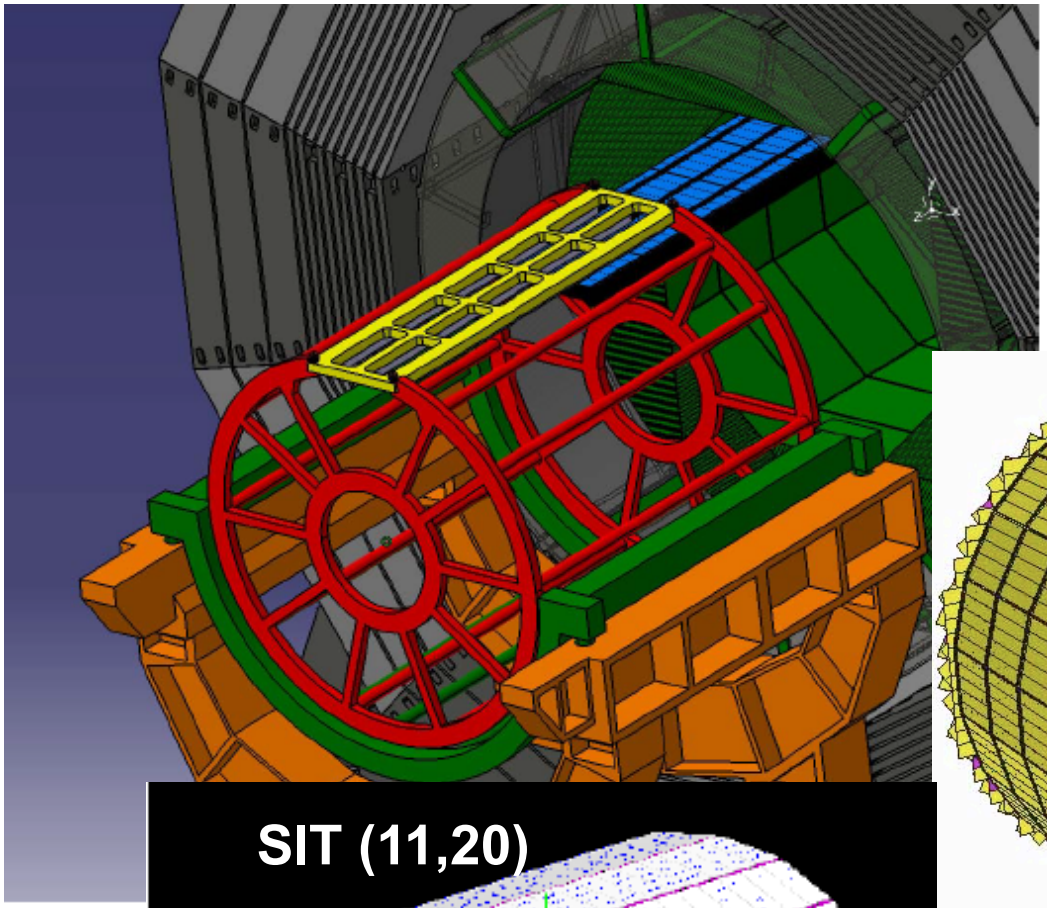


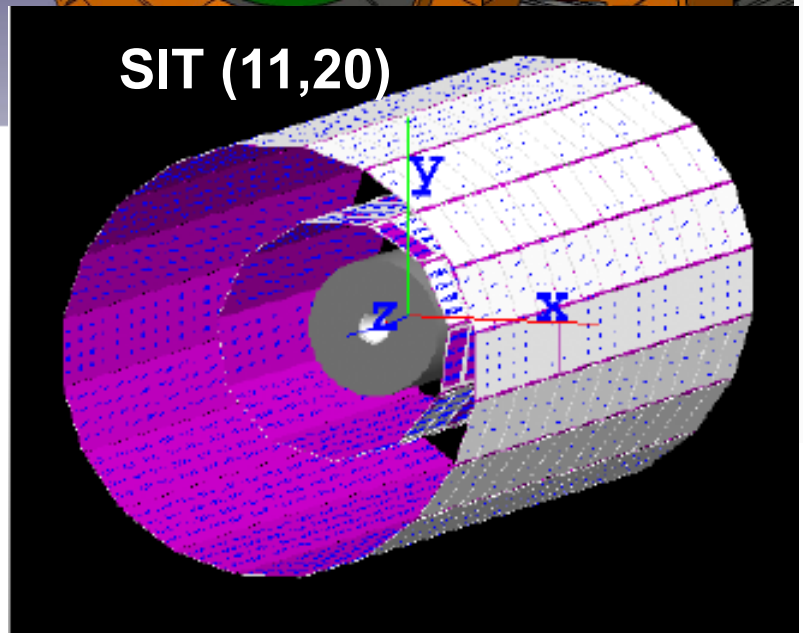
SuperModule approach

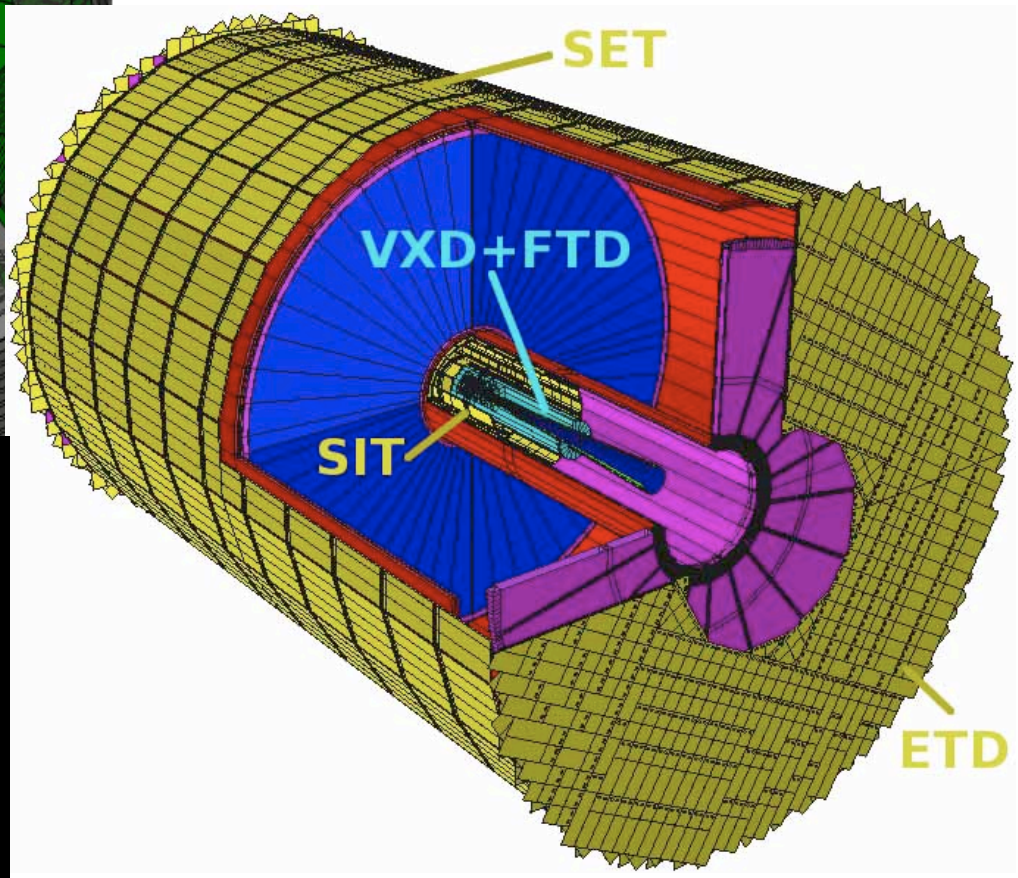
FROM ATLAS (C. Haber, LBL)



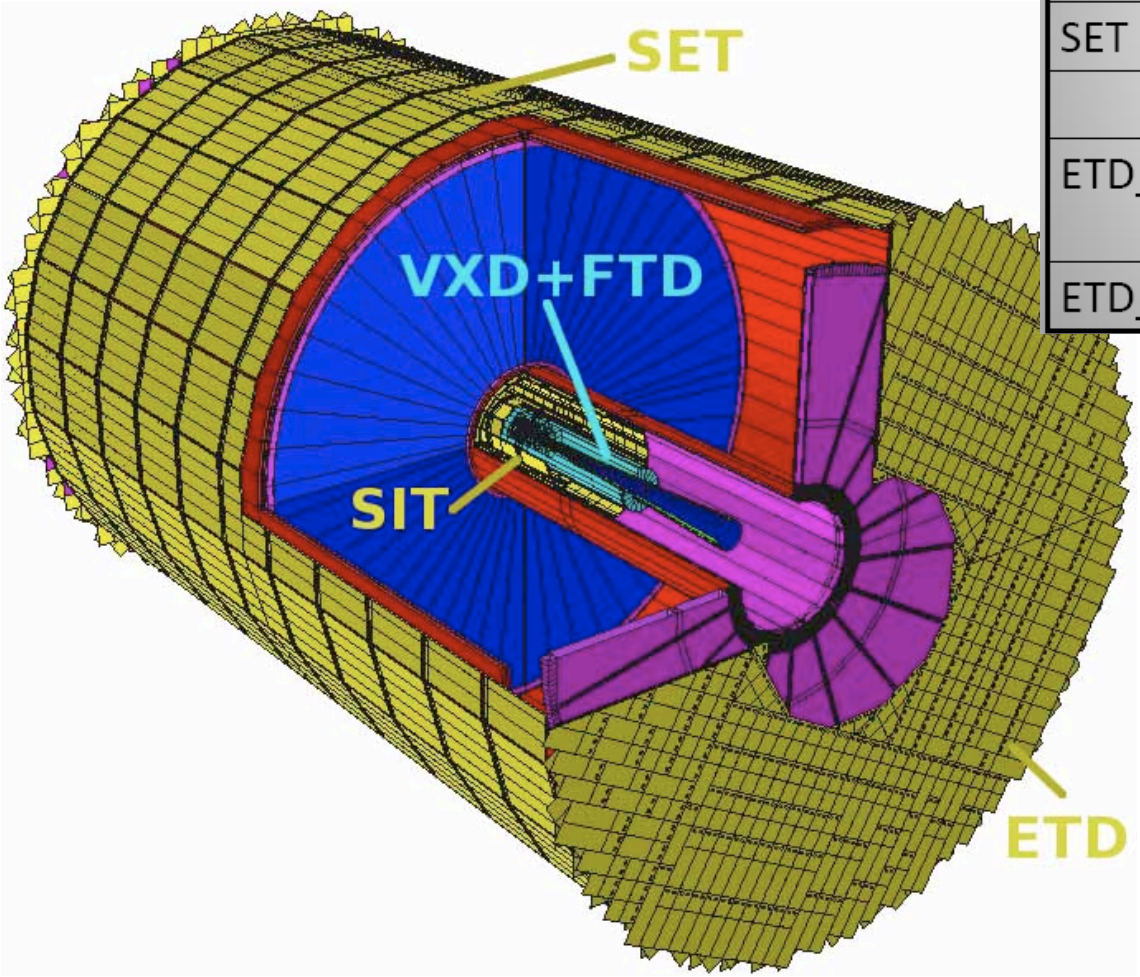
Integration of the Silicon tracking components







ILD Hybrid tracking:
The Silicon Envelope
(in numbers as in the ILD LOI)

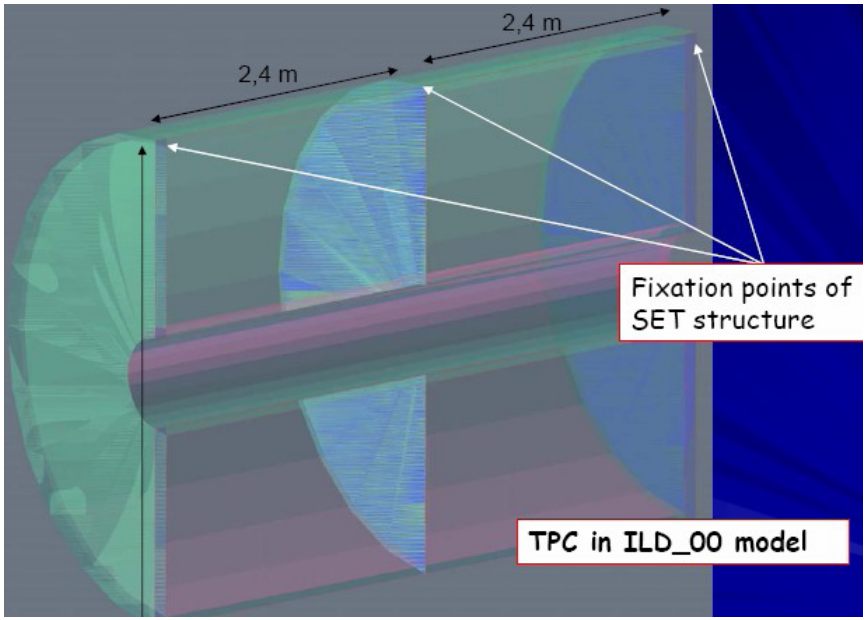


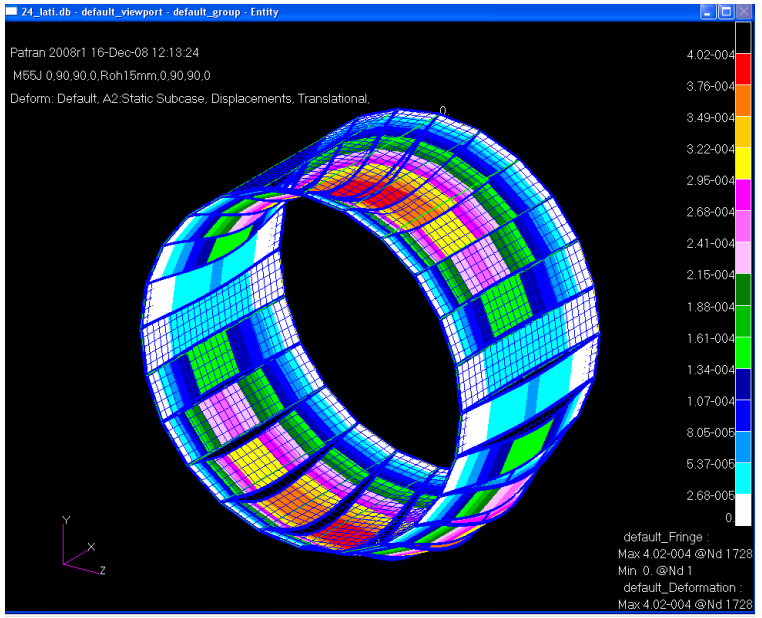
Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

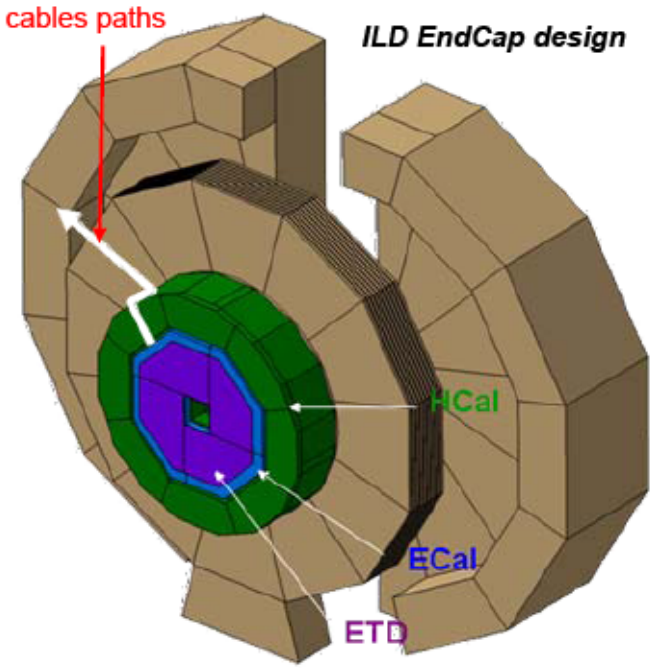
Total number of channels:
10^6 (SIT) + $5x10^6$ (SET) + $4x10^6$ (2 ETD)
= **$10 x10^6$ channels**

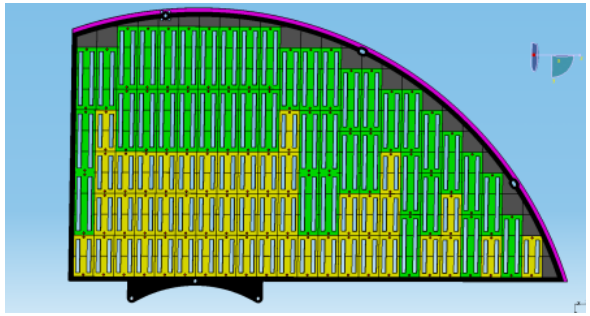
Total area:
7 (SIT)+110 (SET) +2x30(ETDs) = **180 m^2**

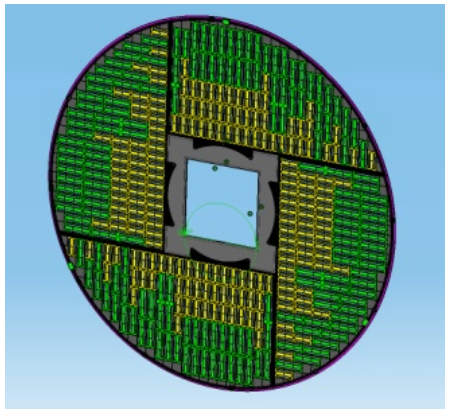
Total number of modules:
500 (SIT) + 2500 (SET) + 2000 (ETDs)=
5000 modules with unique sensor type
but ***variable strip length***
(10-30 cm) depending module location.



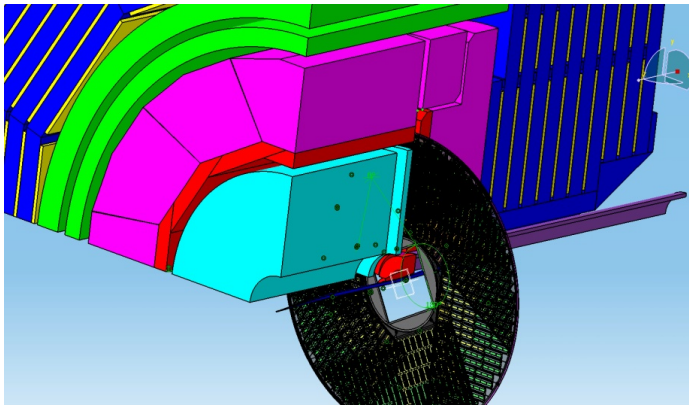


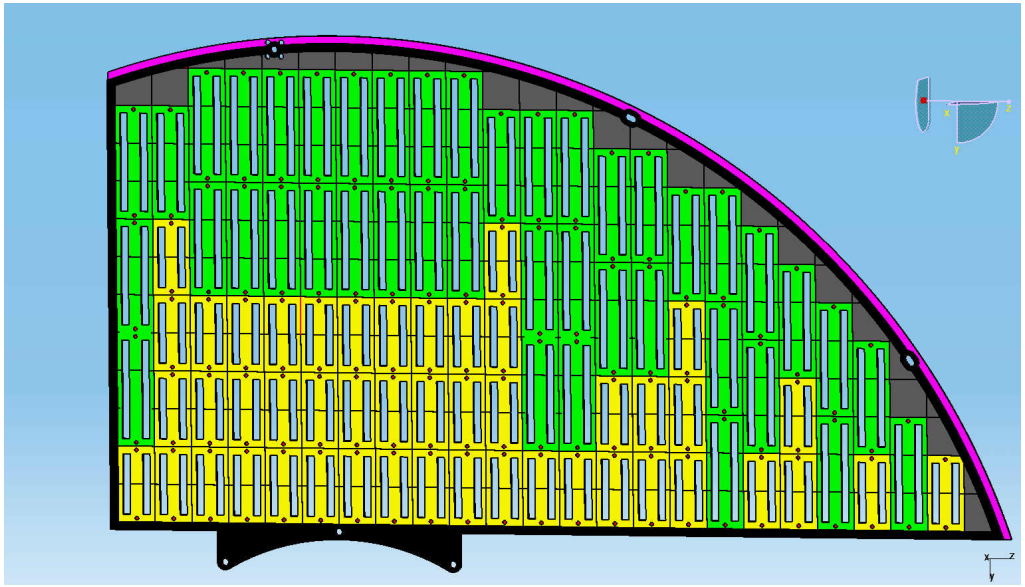


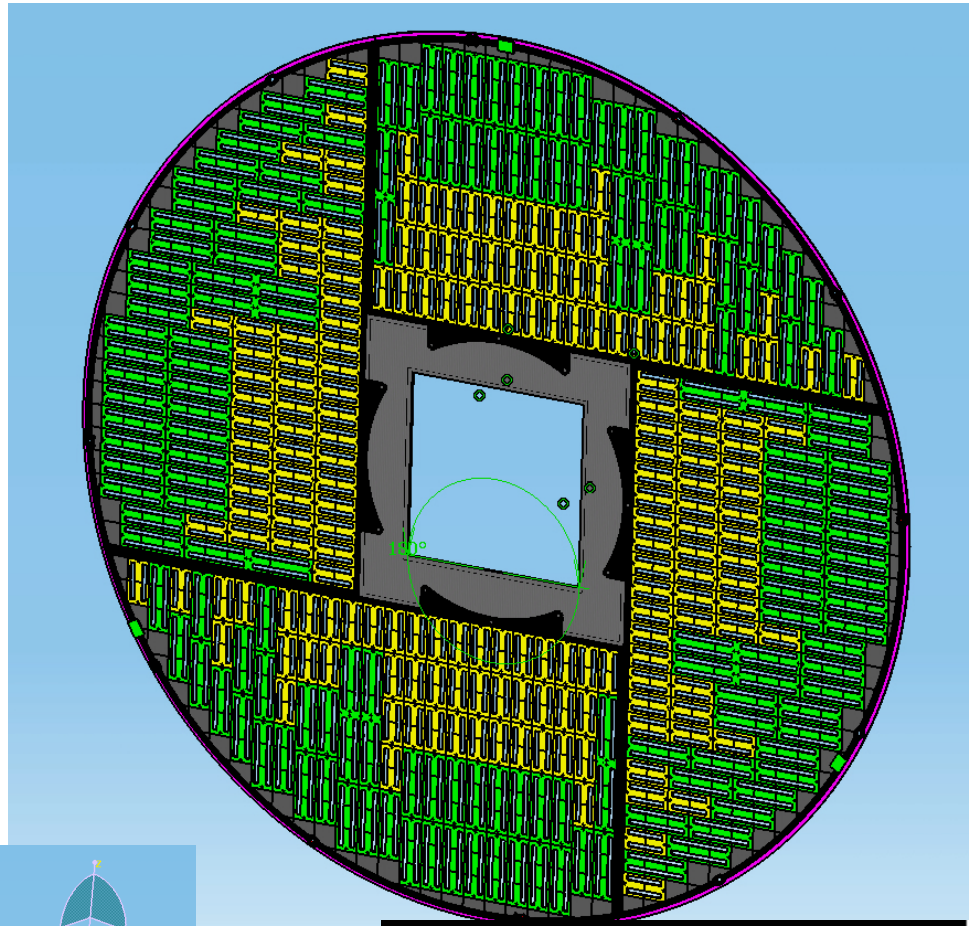




SET/ETD: INTEGRATION



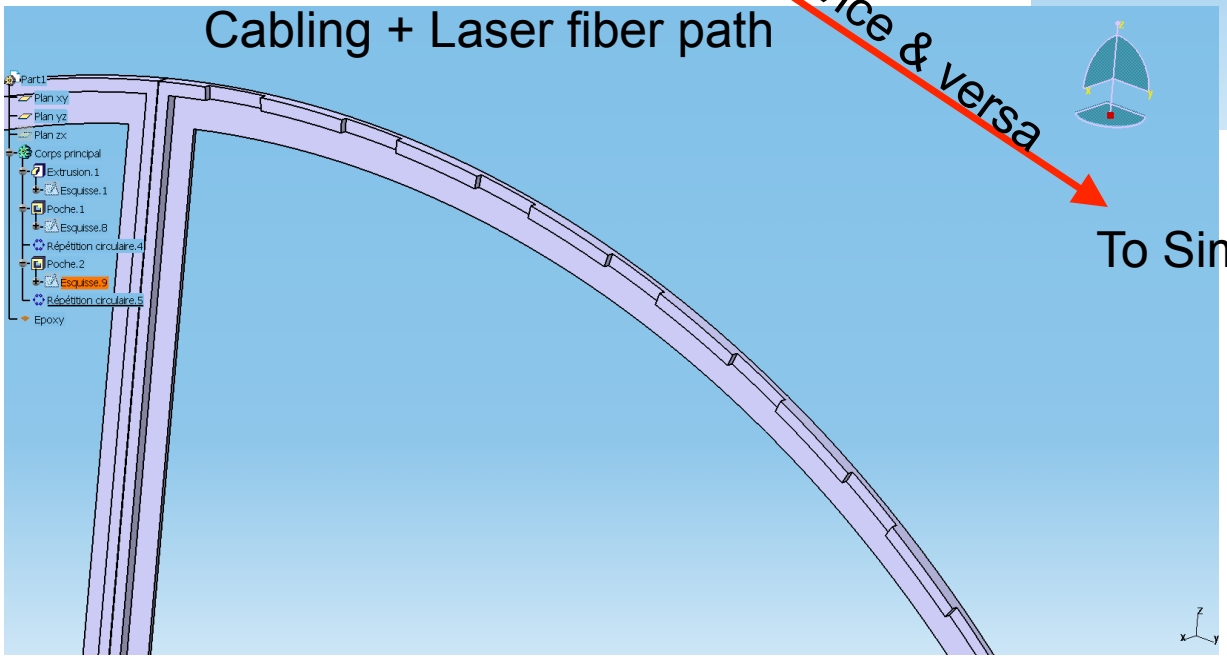




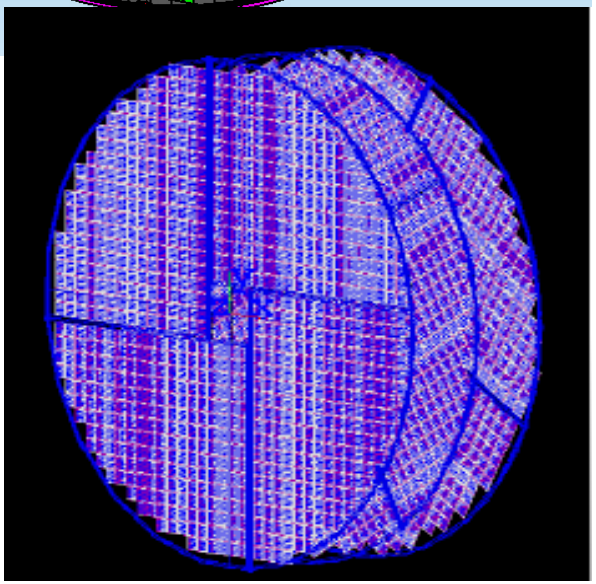
From CATIA

And vice & versa

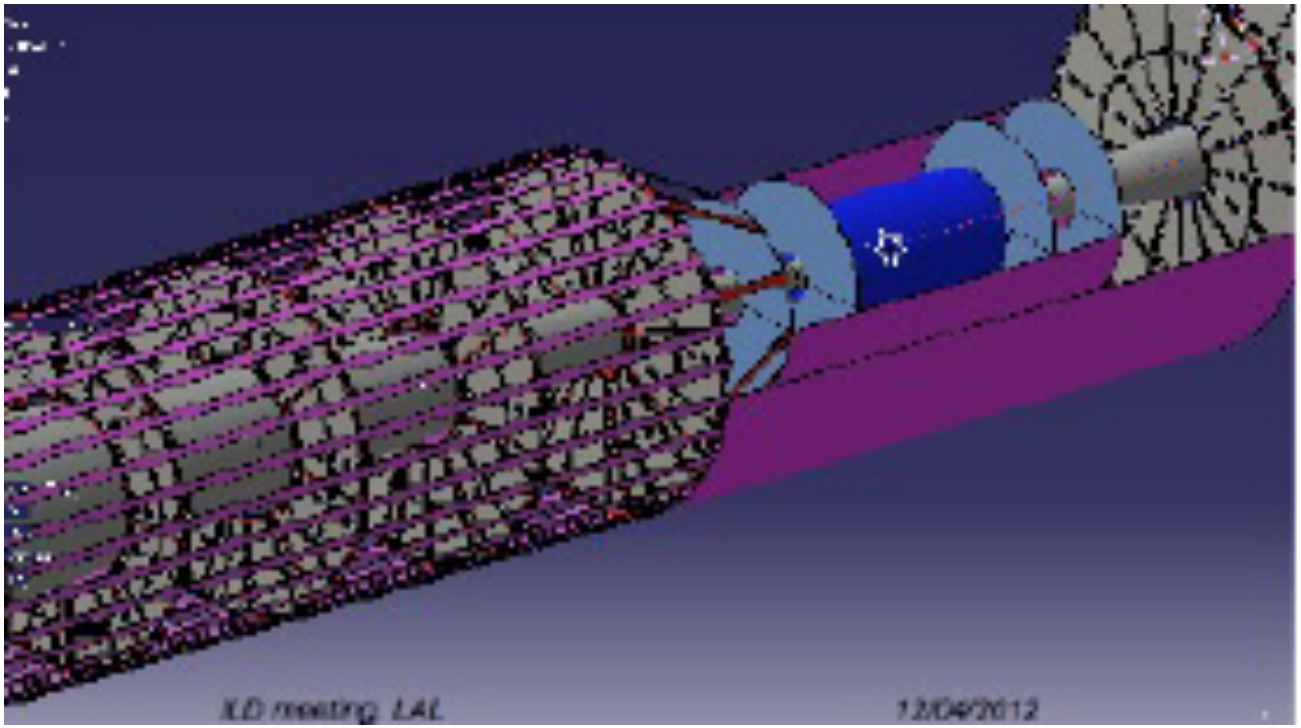
Cabling + Laser fiber path



To Simulation



Cables routing SIT/SET



Our preferred solution is that the SIT cables run along the inner radius of the TPC;
Because it reduces

- the amount of material around the beam pipe
- and wrt the FTD's

Will be further discussed with Catherine

For the SET component: cabling is being studied applying similar solutions as those developed for outer HL-LHC Si trackers upgrade (see ladder description).

Simulation & tracking reconstruction

(*following Frank's presentation at this meeting*)

- very detailed new simulation models had been developed for SIT/SET as well as for the FTD (ETD is not in simulation models)
- these models did not quite reach the level of maturity one would need for the DBD mass production
- slightly simplified have been developed in parallel in order to proceed with new C++ tracking code
- these models have planar wafers, ~realistic support material and work with new tracking
- have now been validated by R&D groups

=>SIT/SET validated

Konstantin Androsov did a lot of work towards developing the new models for SIT,SET &ETD
1) in collab with A. Charpy
2) then taking over last 6-8 months of 2011
Acquired expertise remains available. Being still further developed with LHC

Indeed "planar wafers" are the way to go!

Simulation & tracking reconstruction

(*following Frank's presentation at this meeting*)

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=>SIT/SET validated

Konstantin will remain the SIT/SET/FTD contact & keep in touch with Frank+Steve.

N.B. Maintaining collaborative contacts with HEPHY Vienna on this topic. (W. Mitarof, R. Fruwirth).

detector	person	status
VXD	G.Voutsinas	done
SIT/SET	K.Androsov	done
FTD	J.Duarte	done
TPC	S.Aplin	done
ECal	D.Jeans	done
AHCal	Sh.Lu	done
SDHcal	G.Grenier	to be done
FCal	A.Rosca,	done

Some remarks:

- Since the early start of R&D on large area Si tracking for LC, the strong synergy with LHC is fully/successfully exploited by both parties.
- Taking into account the drastic decrease in support (financial/people) and the strong attraction of expert people/teams by LHC upgrades over these last 2 years, this R&D for LC pursues the synergy by integrating/participating to the advances underway on LHC upgrades.
- This allows pursuing the R&D advances we performed and some time even pioneered (see some examples in previous slides), on all the needed R&D aspects for building the large area Si components of ILD (SIT, SET and ETD).
- It allows furthermore maintaining & developing new collaborative contacts with expert teams, relevant industrial partners
- staying at the forefront of the R&D on this area. Allowing interesting beam test active participation, Keep training young people.
- The DBD will reflect all these advances and new features wrt LoI.

Because of the strong expertise acquired with the Si tracking technology, LC X LHC
And the ongoing R&D advances of this already mature tracking technique, even for confronting high performance challenges

Strong teams are prepared to join & build a highly performing Si tracking for the future LC experiment: this is not really the issue!

Only thing needed:
the GREEN LIGHT for the Linear Collider!!