Status of CMOS Pixel Sensor Development for the VXD at 500 GeV and 1 TeV

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- Sensor design : coll. with IRFU-Saclay -

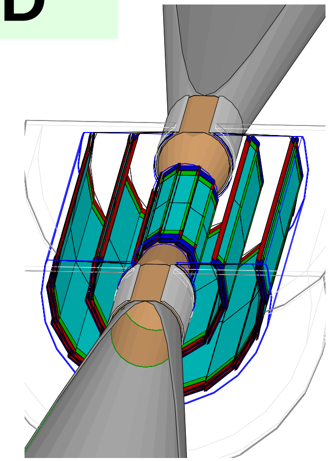
- Ladder design : PLUME coll. - STAR coll. - ALICE coll. - CBM coll.

Kyushu Univ./Fukuoka – 23 May 2012

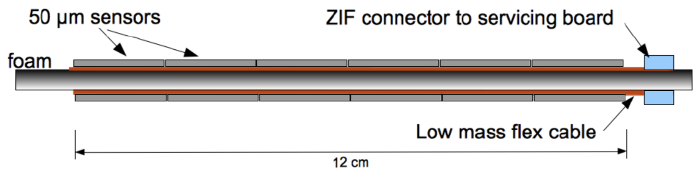
Contents

- *VXD concept based on CMOS Pixel Sensors (CPS)*
- *Status of CPS and ladder developments (500 GeV running)*
- *Developments for 1 TeV running*
  - ↪ *fast CMOS sensor (AROM) with μs level timestamping*
- *Plans until 2015*
- *Summary*

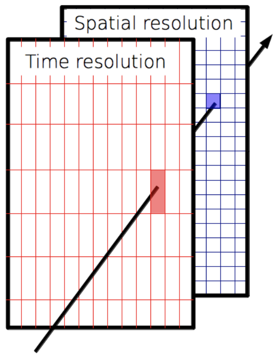
CMOS Pixel Sensors for the ILD-VXD



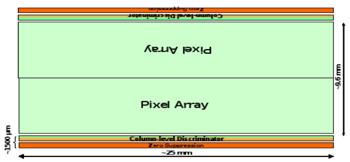
- **Two types of CMOS Pixel Sensors (CPS):**
  - ⋇ **Inner layers** ($\lesssim$ 300 cm^2) : priority to read-out speed & spatial resolution
    - ↪ small pixels (16×16 / 80 μm^2) with binary charge encoding
      - ↪ $t_{r.o.} \sim$ 50 / 10 μs; $\sigma_{sp} \lesssim$ 3 / 6 μm
  - ⋇ **Outer layers** ($\sim$ 3000 cm^2) : priority to power consumption and good resolution
    - ↪ large pixels (35×35 μm^2) with 3-4 bits charge encoding
      - ↪ $t_{r.o.} \sim$ 100 μs; $\sigma_{sp} \lesssim$ 4 μm
  - ⋇ Total VXD instantaneous/average power $<$ 700/15 W (0.35 μm process)
    - ↪ $<$ 600/12 W (0.18 μm process)

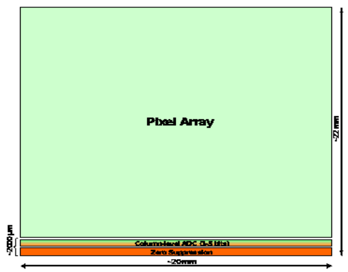


- **2-sided ladder concept for inner layer :**
  - ⋇ *S*quare pixels (16×16 μm^2) on internal ladder face ($\sigma_{sp} <$ 3 μm)
    & *E*longated pixels (16×64/80 μm^2) on external ladder face ($t_{r.o.} \sim$ 10 μs)



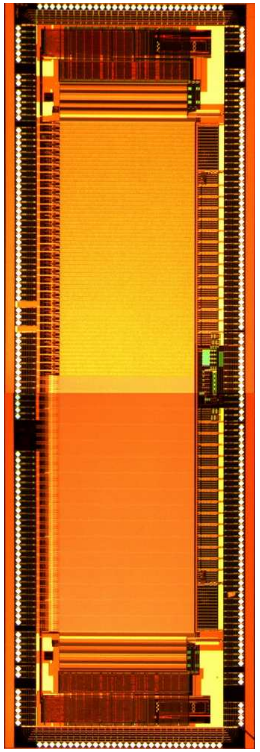
- **Sensor final prototypes :** fabricated in Q4/2011
  - ⋇ **MIMOSA-30:** inner layer prototype with 2-sided read-out ▷ ▷ ▷
    - ↪ one side : 256 pixels (16×16 μm^2)
      other side : 64 pixels (16×64 μm^2)
  - ⋇ **MIMOSA-31:** outer layer prototype ▷ ▷ ▷
    - ↪ 48 col. of 64 pixels (35×35 μm^2) ended with 4-bit ADC





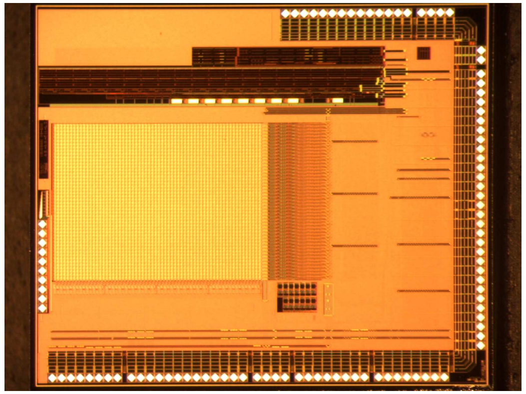
CMOS Pixel Sensors: Status of Baseline Devt

- **MIMOSA-30: prototype for ILD-VXD innermost layer** ▷ ▷ ▷
  - ⋇ 0.35 CMOS μm process with high-resistivity epitaxy
  - ⋇ in-pixel CDS, rolling shutter read-out, binary sparsified output
  - ⋇ columns scale $\simeq$ final sensor (4-5 mm long)
  - ⋇ **high resolution side : pixels of 16$\times$16 μm^2 $\Rrightarrow$ expect σ_{sp} $<$ 3 μm**
    - 128 columns (discri) & 8 col. (analog) of 256 rows
    - read-out time $\lesssim$ 50 μs
  - ⋇ **time stamping side : pixels of 16$\times$64 μm^2 $\Rrightarrow$ $t_{r.o.} \sim$ 10 μs**
    - (expect $\sigma_{sp} \sim$ 6 μm)
    - 128 columns (discri) and 8 col. (analog) of 64 rows
    - lab tests positive : N $\sim$ 15 e$^-$ ENC & discri. all OK for $t_{r.o.} = 10\ \mu s$
  - ⋇ beam tests (CERN-SPS) in June/July '12 $\Rrightarrow$ σ_{sp}, ϵ_{det}, fake rate



- **MIMOSA-31: prototype for ILD-VXD outer layers** ▷ ▷ ▷
  - ⋇ pixels of 35$\times$35 μm^2 (power saving)
  - ⋇ 48 columns of 64 pixels ended with 4-bit ADC (1/10 of full scale chip)

    $\hookrightarrow$ expect $\sigma_{sp} \lesssim$ 3.5 μm
  - ⋇ $t_{r.o.} \sim$ 10 μs (1/10 of full scale chip $\rightarrowtail$ $\sim$ 100 μs)
  - ⋇ beam tests (DESY) in Q1/2013 $\Rrightarrow$ σ_{sp}, ϵ_{det}, fake rate



Status of Ladder Developments

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**

  ⋇ *1st PLUME ladder prototype (0.6 % X_0)*

  ↪ *6 MIMO-26 (50 μm) on each side (8 Mpix, 2 Gb/s)*

  ⋇ *Preliminary results : no X-talk observed*

  ↪ *combined impact res. (20 % improvmt) & pointing resolution (2 mrad)*

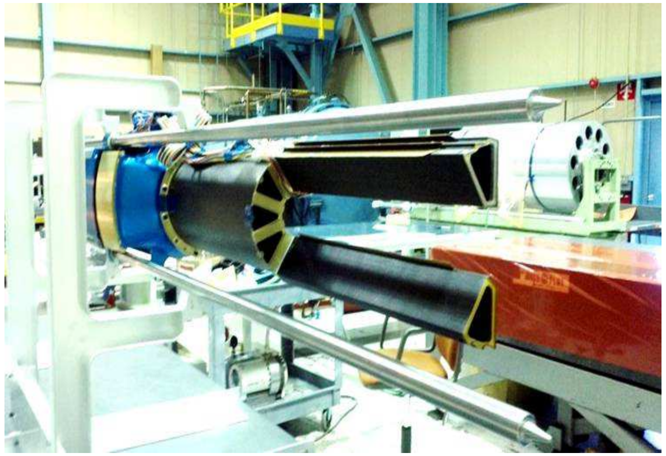
- **New PLUME proto. being fabricated with 0.35% X0** (X-section) ⟼ **beam tests in Q4/2012**

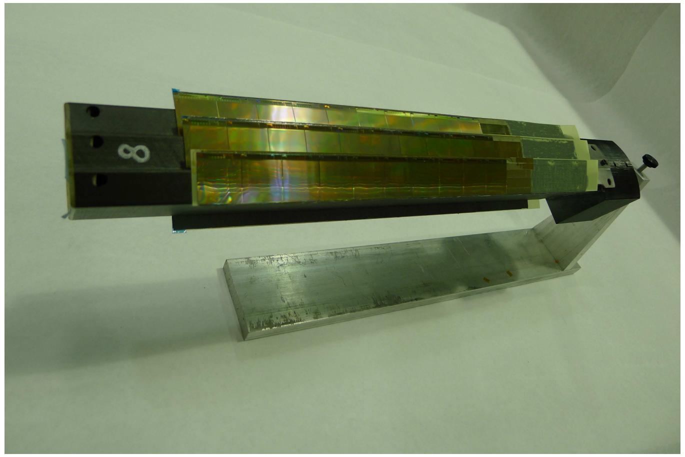
- **Other developments :**

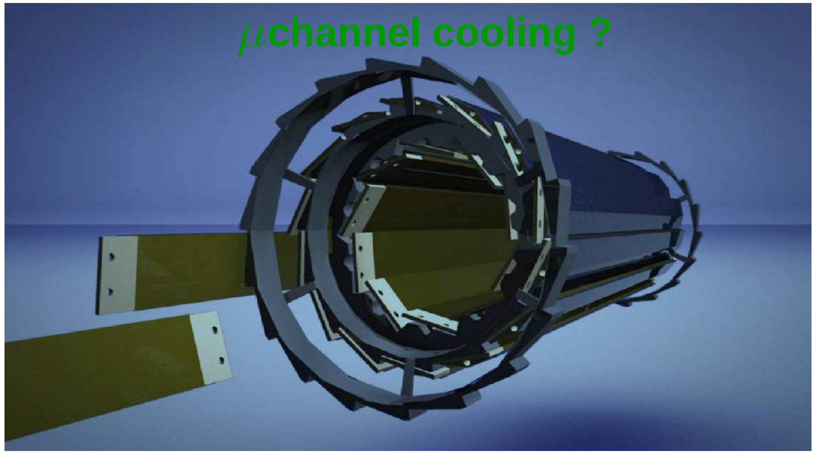
  ⋇ *SERNWIETE : unsupported ladder with $\lesssim$ 0.15 % X_0 ⟼ operational prototype under evaluation*

  ⋇ *STAR-PXL : under construction*

  ⋇ *ALICE-ITS: CDR option*

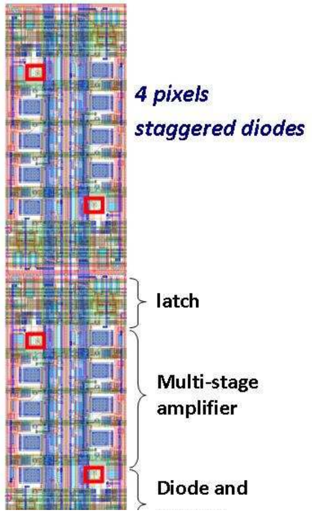




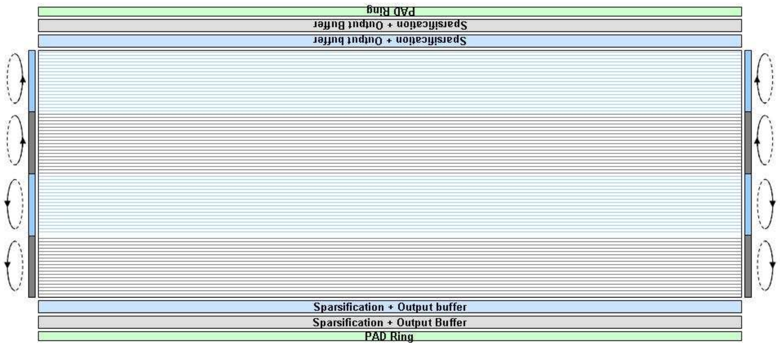


Read-Out Acceleration

- **Motivations**
  - ⋇ robustness w.r.t. predicted 500 GeV BG rate (keep small inner radius, no Anti-DID, ..)
  - ⋇ standalone inner tracking capability (e.g. soft tracks)
  - ⋇ compatibility with high-energy running: beam BG at $\sqrt{s} \gtrsim$ 1 TeV
    - $\hookrightarrow$ beam BG ($\gtrsim$ 1 TeV) 5$\times$BG (500 GeV) ?

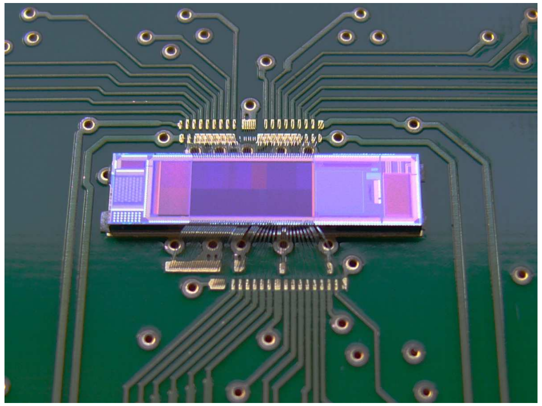


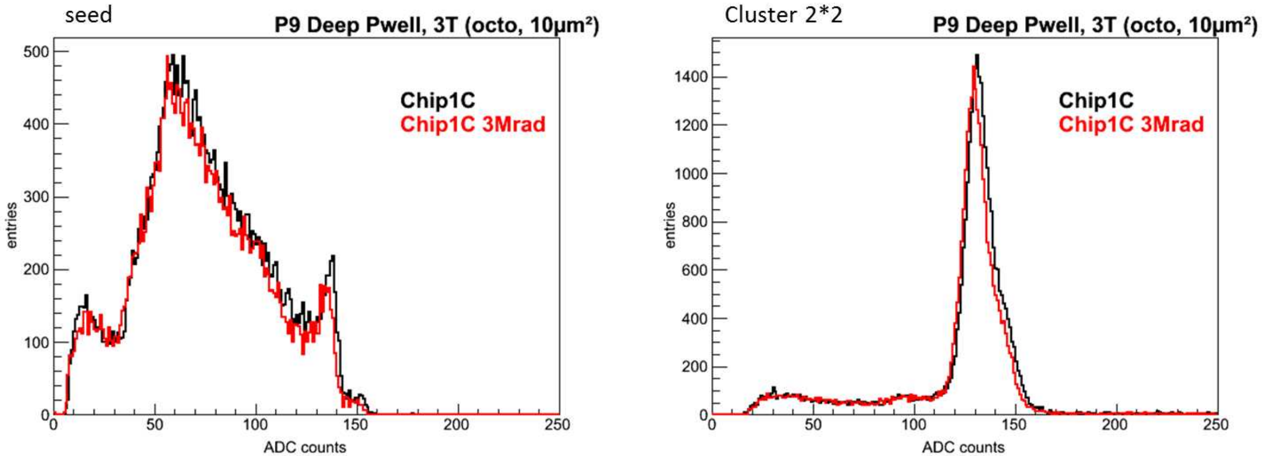
- **How to accelerate the elongated pixel read-out**
  - ⋇ elongated pixel dimensions allow for in-pixel discriminators $\Rrightarrow$ $\geq$ 2 faster r.o. ▷ ▷
  - ⋇ read out simultaneously 2 or 4 rows $\Rrightarrow$ 2-4 faster r.o./side
  - ⋇ subdivide pixel area in 4-8 sub-arrays read out in // $\Rrightarrow$ 2-4 faster r.o./side
  - ▷ 0.18 μm CMOS process needed
    - $\hookrightarrow$ 6-7 ML,, design compactness, in-pixel CMOS T, ...
  - ⋇ conservative step: 2 discri./column **end** (22 μm wide)
    - $\Rrightarrow$ read out 2 rows simultaneously
    - $\hookrightarrow$ 1st stage improvement: 50/10 $\mu s \rightarrowtail$ 25/5 μs
    - (works even with 0.35 μm technology)



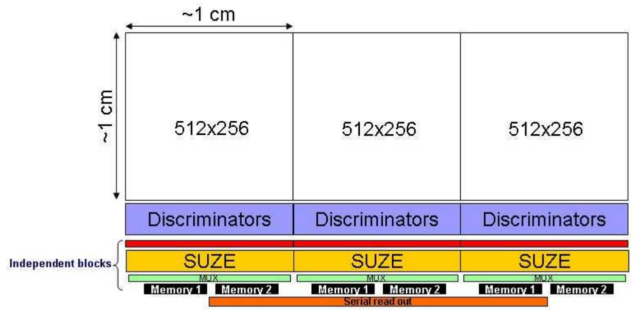
0.18 μm Technology Prototyping

- **MIMOSA-32 : technology exploration**
  - ⋇ fabricated in Q4/2011 with high resistivity epitaxial layer ▷ ▷ ▷
  - ⋇ numerous different pixels (sensing syst., pre-ampli., elongated pix.), etc.
  - ⋇ lab tests under way (^{55}Fe source) :
    - good charge coll. eff. observed (high-res epi)
    - no parasitic charge coll. seen with Deep P-well
    - N $\sim$ 15-18 e^{-} ENC
    - irradiation up to 3 MRad has marginal impact
    - difficult to model in-pixel circuitry
  - ⋇ beam tests foreseen in June-July '12





- **Next steps**
  - ⋇ Q4:
    - MIMO-22THR1 $\equiv$ MIMO-30 translation
    - MIMO-22THR2 $\equiv$ id. but 2-discri/col.
    - AROM-1 $\equiv$ Accelerated Read-Out MIMOSA sensor
      $\rightarrowtail$ prototype with in-pixel discrimination
    - SUZE-02 $\equiv$ Zero-Suppression & output buffer circuit
      $\rightarrowtail$ sparsification: 4 rows simultaneous r.o.
  - ⋇ 2013: first full scale (1 cm^2) sensor fabrication
    $\Rrightarrow$ final full size proto. in 2014/15 (ALICE, CBM, AIDA)



Characteristics & Variants of MIMOSA & AROM Sensors

- **Assuming MIMOSA and AROM variants to equip innermost and outer layers**

  ⋇ MIMOSA-in and AROM-1 equip innermost layers ⋇ MIMOSA-out and AROM-2 equip outer layers

Sensor version	**MIMOSA-in**	**MIMOSA-out**	**AROM-1**	**AROM-2**
Active area dimensions [mm^2]	8.7×31.0	19.6×31.0	10.9×31.0	20.8×31.0
Pixel dimensions [μm^2]	17×17	34×34	17×85	34×72
Single point resolution [μm]	$\lesssim$ 3	$\lesssim$ 4	5-7	$\sim$ 10
Read-out time [μs]	50	$\sim$ 100	1.5	7
Power consumption: instantaneous [W]	$\sim$ 1.8	$\sim$ 0.6	2.7	0.7
average [mW]	36	12	55	14

- **Expected VXD performances at 1 TeV (and 0.5 TeV)**

Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** 1 TeV (0.5 TeV)	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs (10 μs)	4.5(0.9) / 0.5(0.1)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs (100 μs)	1.5(0.3) / 0.2(0.04)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs (100 μs)	0.3(0.06) / 0.05(0.01)	200/4 W

SUMMARY

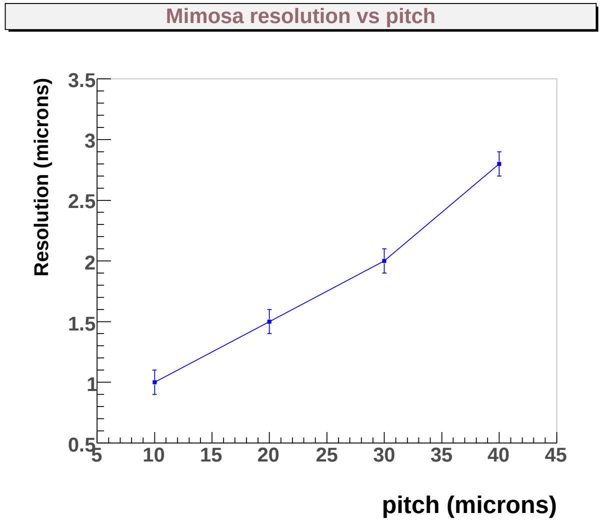
- **CPS architecture is ready to be adapted to all VXD sensor specifications at $\sqrt{s}$=500 GeV :**
  - architecture based on sensors realised for EUDET-BT and STAR-PXL (0.35 μm CMOS process)
  - relies on 2-sided ladder concept $\Rrightarrow$ hit resolution/timestamp on opposite ladder sides (PLUME project)
  - innermost layer : $<$ 3 μm and $\lesssim$ 10 μs (upgradable to $\lesssim$ 5 μs with 2 discri/col)
  - outer layers : $\lesssim$ 3.5 μm (ADCs not yet tested) and $\sim$ 100 μs
  - VXD power consumption : $<$ 700 W (inst.) / $<$ 15 W (average) $\rightarrowtail$ 20% less with 0.18 μm technology
  - final prototypes fabricated $\Rrightarrow$ tests under way : MIMOSA-30(in) & MIMOSA-31(out)
  - validation of concept $\pm$ completed in 2012 with 2-sided ladder (PLUME) offering 0.35 % X_0 (X-section)

- **Translation 0.35 $\mu m \rightarrowtail$ 0.18 μm CMOS under way for $\sqrt{s} \gtrsim$ 1 TeV :**
  - benefits: read-out $<$ 2/10μs (inner/outer layers), $>$ 20% less power, throughput, pixelated SIT ?, ...
  - exploratory chip (MIMOSA-32) under test
  - mid-scale prototypes validating architecture planned for submission in Q4/2012
  - Full Scale Basic Block (FSBB - 1cm^2 active area) expected to be fabricated in 2013

    $\Rrightarrow$ Final (full scale) prototype in 2014/15
  - synergy with AIDA-SALAT, ALICE-ITS & -MFT, CMB-MVD, ...

Measured Spatial Resolution

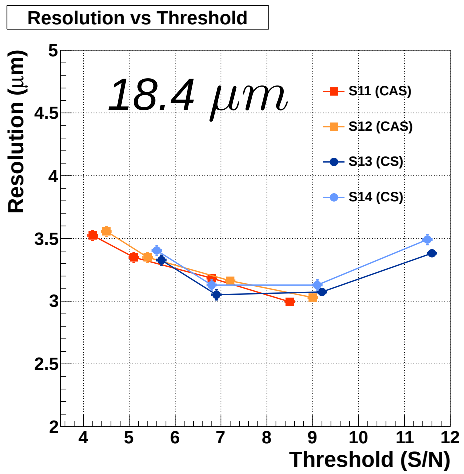
- **Compare position of impact on sensor surface predicted with BT to hit reconstructed with sensor under test :**
  clusters reconstructed with eta-function,
  exploiting charge sharing between pixels

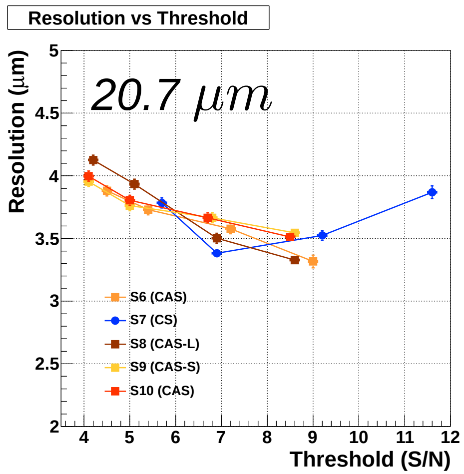


- **Impact of pixel pitch (analog output) :** ▷▷▷
  $\sigma_{\mathbf{sp}} \sim \mathbf{1}\ \boldsymbol{\mu}\mathbf{m}$ (10 μm pitch) $\longrightarrow$ $\lesssim \mathbf{3}\ \boldsymbol{\mu}\mathbf{m}$ (40 μm pitch)

- **Impact of charge encoding resolution :** ▷▷▷
  ▷ ex. of 20 μm pitch $\Rrightarrow$ σ_{sp}^{digi} = pitch/$\sqrt{12} \sim$ 5.7 μm

Nb of bits	**12**	**3-4**	**1**
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$



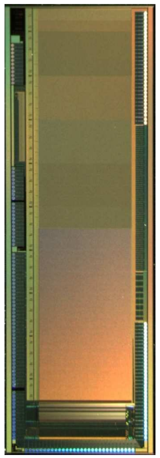


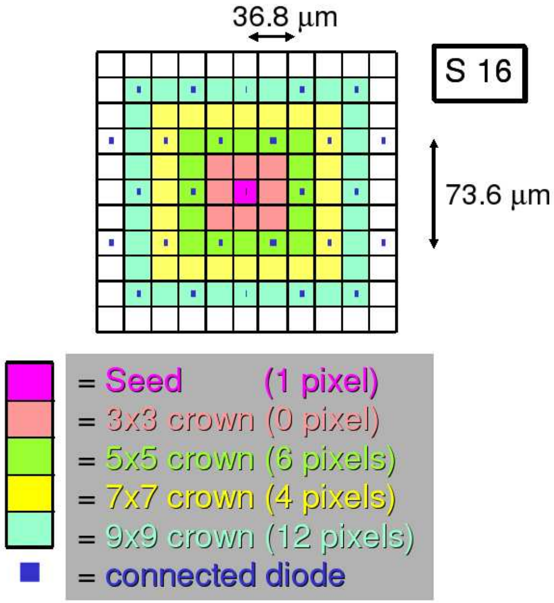
Towards a Large Pitch

- **Large pitch : Motivations**
  - ⋇ elongated pixels allow faster read-out
  - ⋇ trackers (e.g. ILD-SIT) require $\sigma_{sp} \gtrsim 10\ \mu m$
  - $\Rrightarrow$ minimise number of pixels for the sake of power dissipation, integration time and data flow

- **Large pitch : Limitations (besides spatial resolution)**
  - ⋇ DANGER: increasing distance inbetween neighbouring diodes
    - $\Rrightarrow$ particles traversing sensor ”far” from sensing diodes may not be detected because of e$^-$ recombination
  - ⋇ ”fragile” detection efficiency, exposed to losses due to irradiation, high temperature operation & ”slow” read-out

- **Elongated pixels : Test results**
  - ⋇ elongated pixels allow minimising the drawbacks of large pitch
  - ⋇ concept evaluated with MIMOSA-22AHR prototype,
    composed of a sub-array with 18.4×73.6 μm^2 pixels ▷▷▷
  - ⋇ m.i.p. detection performances assessed at CERN-SPS (T ∼ 15°C)
    - ⊸ $\epsilon_{det} \sim 99.8$ %
    - ⊸ $\sigma_{sp} \sim$ 5-6 μm (binary charge encoding)

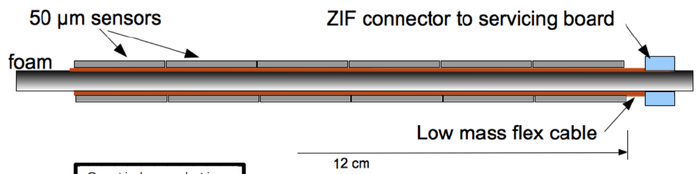


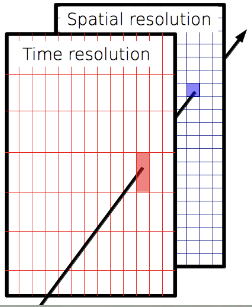


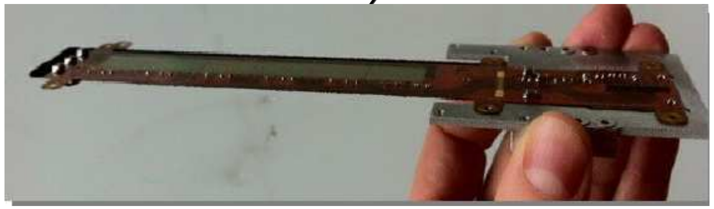
- **Square pixels : prototype back from foundry**
  - ⋇ MIMOSA-29 : fabricated on high-resistivity epitaxy in Summer ’11
  - ⋇ pixels of 64×16/32/64 μm^2 and 80×16/48/80 μm^2
  - ⋇ chips back from foundry $\Rrightarrow$ test preparation under way

Sensor Integration in Ultra Light Devices

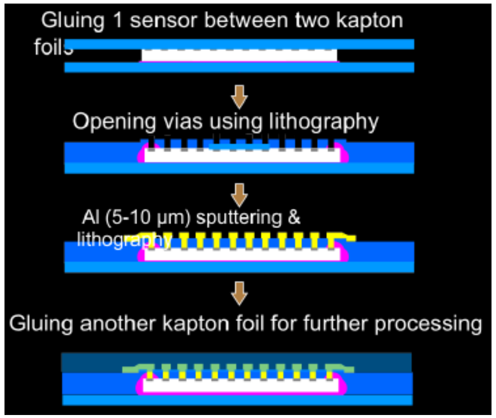
- **2-sided ladders with time stamping for the ILD-VXD :**
  - ⋇ manyfold bonus expected from 2-sided ladders:
    compactness, alignment, pointing accuracy (shallow angle), redundancy, etc.
  - ⋇ studied by PLUME coll. (Oxford, Bristol, DESY, IPHC) & AIDA (EU)
    $\hookrightarrow$ **P**ixelated **L**adder using **U**ltra-light **M**aterial **E**mbedding
  - ⋇ square pixels for single point resolution on beam side
  - ⋇ elongated pixels for 4-5 times shorter r.o. time on other side
  - ⋇ correlate hits generated by traversing particles
  - ⋇ expected total material budget $\sim$ 0.3 % X_0
    $\hookrightarrow$ 1st proto. (0.6 % X_0) fabricated & operationnal
    $\triangleright$ beam tests at CERN-SPS (traversing m.i.p.) in Nov. '11

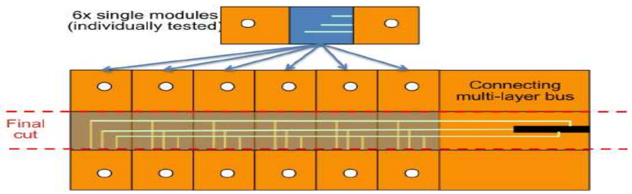






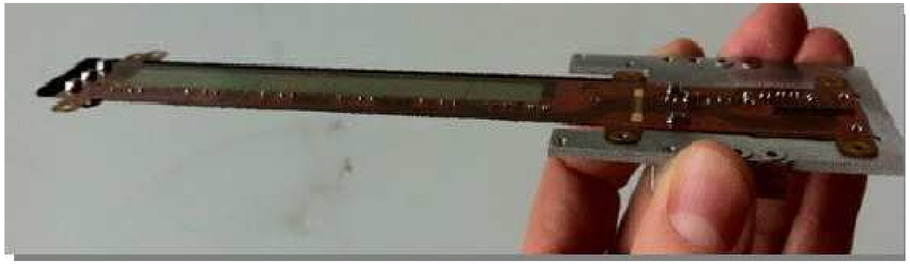
- **Unsupported ladders (Hadron Physics 2 / FP-7)**
  - ⋇ 50 μm thin CMOS sensors embedded in thin kapton and cabled
    with redistributed connections $\rightarrowtail$ suited to curved surfaces ?
  - ⋇ expected total material budget $\lesssim$ 0.15 % X_0
  - ⋇ 1st single sensor mechanical prototype fabricated
  - ⋇ 1st 3-sensor electrical proto. expected by Summer 2012

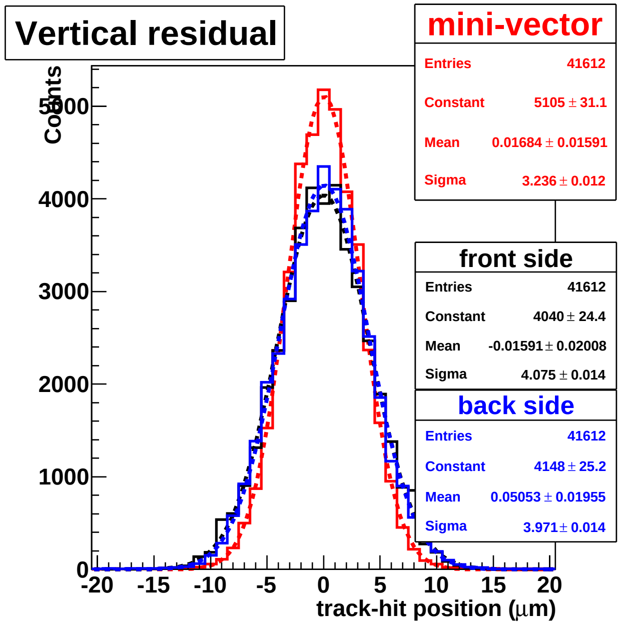


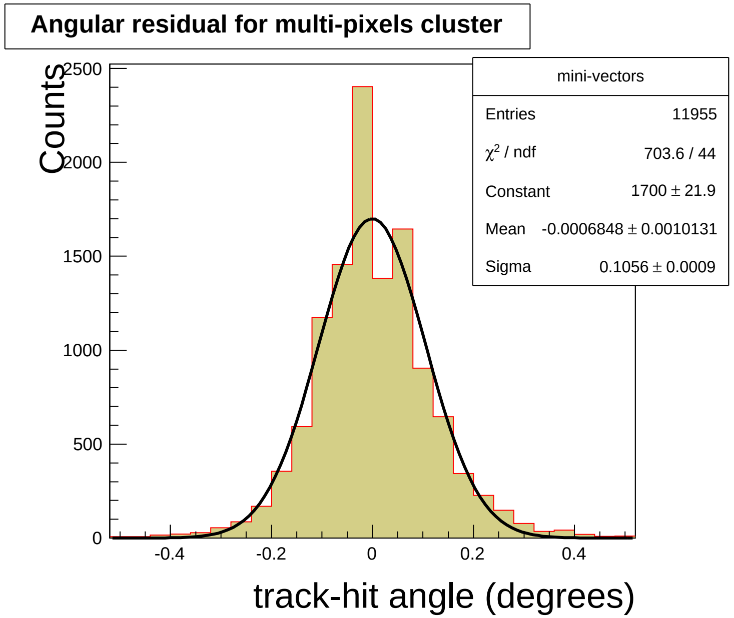


2-Sided Ladder Beam Test Results

- **PLUME prototype-2010 tested at SPS in Nov. 2011:**
  - ⋇ *Beam telescope : 2 arms, each composed of 2 MIMOSA-26 sensors*
  - ⋇ *DUT : 1 PLUME ladder prototype (0.6 % X_0)*
    - $\hookrightarrow$ *6 MIMOSA-26 sensors on each ladder face ($>$ 8 Mpixels)*
  - ⋇ *CERN-SPS beam : $\gtrsim$ 100 GeV "π^-" beam*
  - ⋇ *BT (track extrapolation) resolution on DUT $\sim$ 1.8 μm*
  - ⋇ *Studies with PLUME perpendicular and inclined ($\sim$ 36°) w.r.t. beam line*
  - ⋇ *Preliminary results (no pick-up observed): combined impact resolution & pointing resolution*







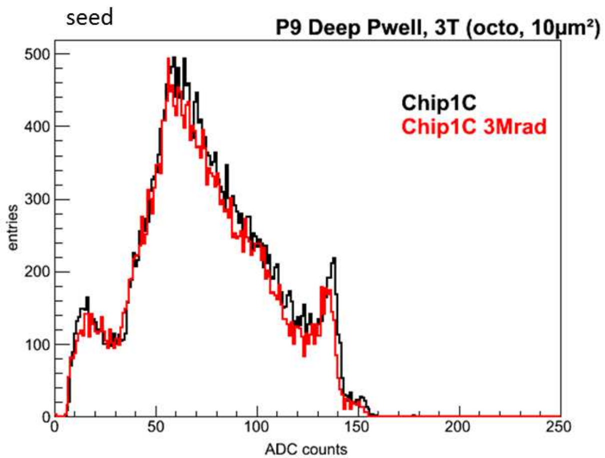
- **New PLUME proto. under construction with 0.35 % X_0** (X-sect.) $\longrightarrow$ **beam tests in Q4/2012** (SPS ?)

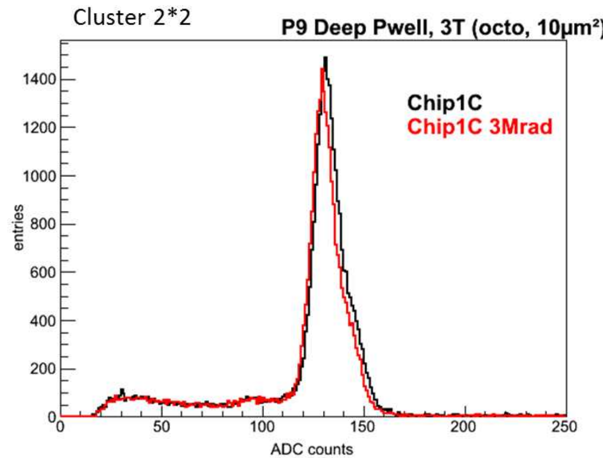
Preliminary 0.18 μm Process Test Results

- **MIMOSA-32 lab tests (^{55}Fe source) of pixel matrix with analog output** $\longrightarrow$ **Very preliminary results :**
  - ⋇ Read-out time of each sub-matrix = 32 μs
  - ⋇ Observed CCE (20$\times$20 μm^2 pixels) :
    - ∘ seed pixel : $\sim$ 40–50 % ▷ ▷ ▷ ▷
    - ∘ 2$\times$2 pixel cluster : nearly 100 % ▷ ▷ ▷ ▷

      $\Rrightarrow$ confirms Epi. layer 1-5 $k\Omega \cdot cm$
    - ∘ No parasitic charge coll. seen with Deep P-well
    - ∘ CCE of 20$\times$40 μm^2 pixels

      $\hookrightarrow$ seed $\sim$ 30 % and with 1st crown $\sim$ 75 %



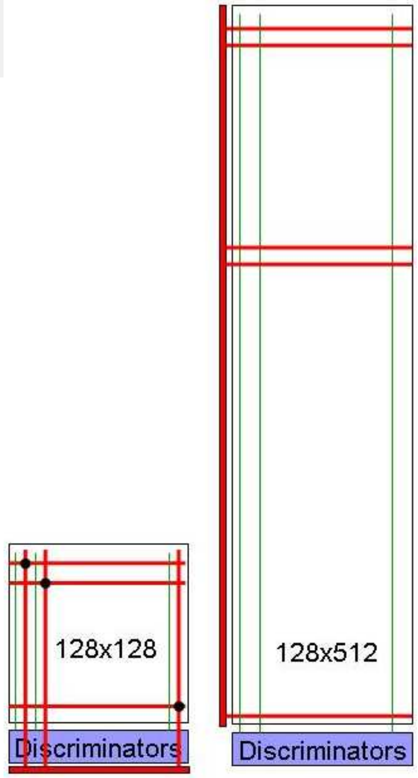


  - ⋇ Noise $\sim$ 16-18 e$^-$ ENC at 20°C
  - ⋇ Irradiation: 0.4/1/3 MRad $\longrightarrow$ $\sim$ no effect up to 35°C **(tbc !)**
  - ⋇ Difficult to find operating regime of in-pixel ampli. due to inaccurate simul. **models** $\Rrightarrow$ pixel design optimisation ?

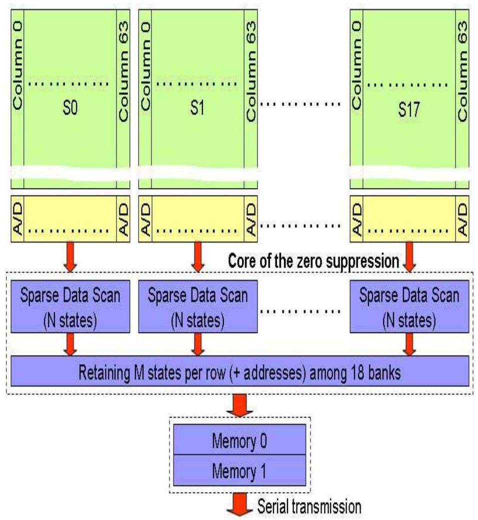
- **Next 2012 steps :**
  - ⋇ Beam tests of pixel matrix foreseen in June-July 2012 (incl. NI radiation tolerance assessment)
  - ⋇ Lab and beam tests of digital matrix through Summer 2012
  - ⋇ Lab tests of in-pixel discriminator array in Q3-Q4/2012 (tbc)
  - ⋇ **MIMOSA-32bis** fab. in Spring'12 with standard epitaxial layer $\longrightarrow$ lab tests in Summer 2012
  - ⋇ **Submission of MIMOSA-32ter** (July 2012) with alternative in-pixel amplification schemes

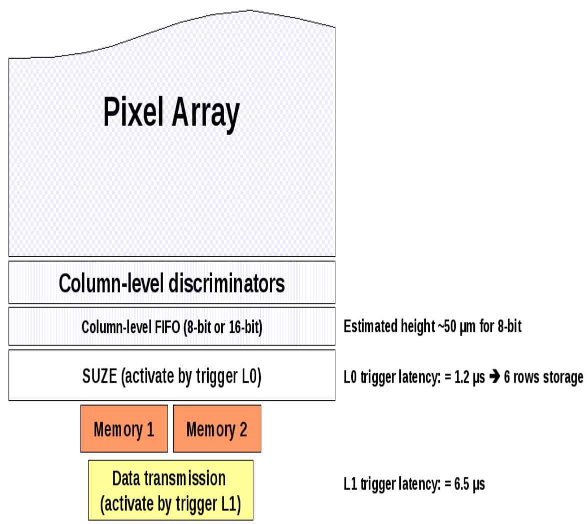
MISTRAL: 0.18μm Architecture Prototyping

- 1st step : MISTRAL $\equiv$ MIMOSA FOR THE INNER SILICON TRACKER OF ALICE
- MIMOSA-22THR (Upstream part of sensor) :
  - ⋇ Col. // pixel array with in-pixel ampli + pedestral subtraction (cDS)
  - ⋇ Each of 128 columns ended with discriminator + 8 columns without discri.
  - ⋇ Pixel array sub-divided in sub-arrays featuring different pixel designs (22$\times$22/44 μm^2)
  - ⋇ 2 options $\rightarrowtail$ submission in Octobre'12 :
    - ○ end of column discriminator $\equiv$ translation of MIMOSA-22AHR (0.35 techno.)
    - ○ simultaneous 2-row encoding & 2 discriminators/column $\Rrightarrow$ twice faster



- AROM-1 (Accelerated Read-Out Mimosa)
  - ⋇ in-pixel discri. & simultaneous 4-row encoding $\Rrightarrow$ 8 times faster than MIMOSA-22THR
  - ⋇ submission in Octobre'12
- SUZE-02 (Downstream part of sensor) :
  - ⋇ $\emptyset$ μ-circuits & output buffers ($\equiv$ SUZE-01)
  - ⋇ add filter L0 info after discriminators for data flow & power reduction
  - ⋇ add 2nd filter downstream of output buffers for further data flow & power compression
  - ⋇ submission in Octobre'12

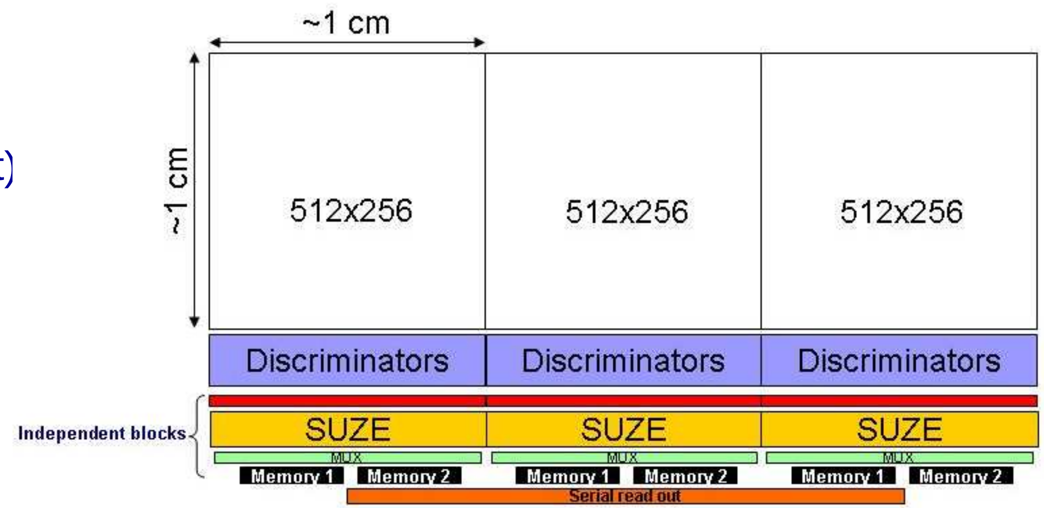




MISTRAL : Final Steps

- **FSBB (Full Scale Basic Block) : 2013**
  - ⋇ Composition :
    - ⊸ Pixel array with $\sim$ final pixel design ($\sim$ 1 cm^2)
    - ⊸ Final r.o. circuitry ($\emptyset$, filtering, data transmission, ...)
    - ⊸ All read-out circuitry split in elementary blocks
      according to **stitching** design rules $\longrightarrow$ AIDA-BT
  - ⋇ Submission : Summer 2013 (?)

- **MISTRAL : 2014 ?**
  - ⋇ Composition :
    - ⊸ 3 full-size adjacent FSBB (1-sided read-out)
      or 6 half FSBB (2-sided read-out)
    - ⊸ Complemented with serial r.o. circuitry
  - ⋇ Submission : Summer 2014 (?)

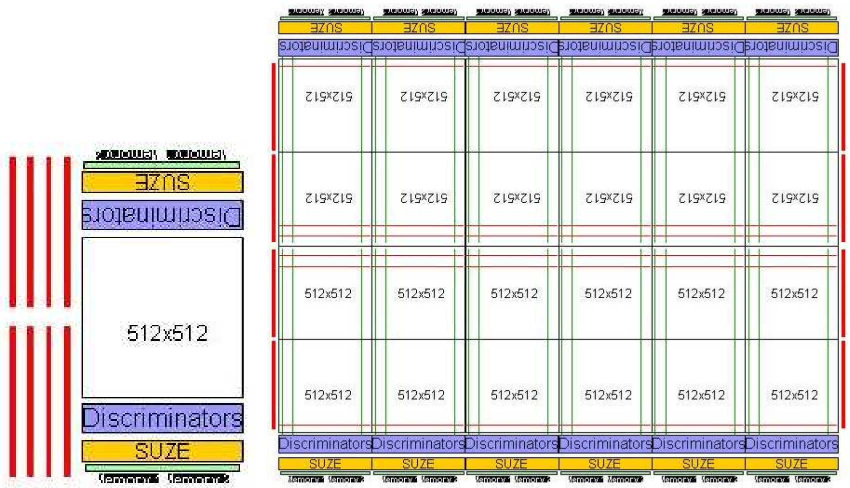


- **Start MIMAIDA & MIMOSIS designs (+ others ?) :**

  $\hookrightarrow$ submission in 2015

AIDA Project : Assessment of Stitching & 2-Sided Ladder

- **Single Arm Large Area Telescope (SALAT) :**



  ⁜ *2048$\times$3072 pixels ($\sim$ 20 μm pitch)*

  $\Rrightarrow$ *4$\times$6 cm^2 sensitive area, $\sim$ 3.5 μm spatial resolution*

  ⁜ *requires combining several reticules (based on FSBB)*

  $\Rrightarrow$ *stitching process* $\Rrightarrow$ *establish proof of principle*

  ⁜ *2-sided read-out of 1024 rows in $\sim$ 200 μs*

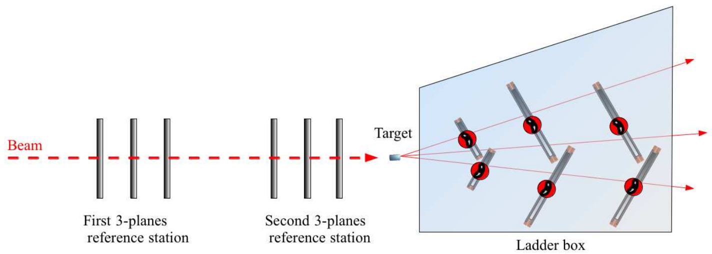
  $\Rrightarrow$ *3 planes of Large Area Telescope for AIDA project (EU-FP7)*

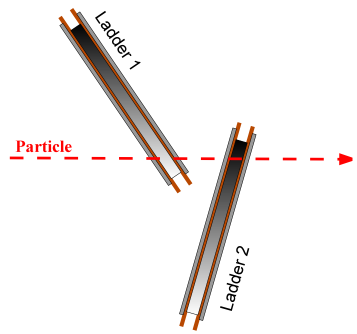
  ⁜ *windowing of $\lesssim$ 1$\times$6 cm^2 (collimated beam)*

  $\Rrightarrow$ *$\sim$ 50 μs r.o. time*

  ⁜ *50-100 μm pitch variants under consideration (trackers)*

- **Alignment Investigation Device (AID) :**





  ⁜ *box allowing to mount 3-4 pairs of ladders arranged in 3-4 consecutive layers $\equiv$ VTX sector*

  ⁜ *can be equipped with PLUME (2-sided) ladders*

  ⁜ *ladders mounted on movable micrometric supports*

  $\Rrightarrow$ *investigate alignment with particles traversing overlapping regions of neighbouring ladders*

  ⁜ *allows developing clustering, tracking & vertexing algo. with particle beams*

VXD - SIT Variant Composed of CPS

- **ILD-SIT : baseline assumes 2 double-sided μstrip detector layers**
  - ⋇ try understanding if CMOS sensors could improve performance with their high spatial resolution
  - ⋇ advantage : spatial resolution $\triangleright$ 4×4 μm^2 instead of 7×50 μm^2

    $\Rrightarrow$ improved soft track reconstruction (p) and TPC link

    potentially : material budget, cost
  - ⋇ disadvantage : time resolution $\triangleright$ 7 μs instead of O(100)ns – Is power a pb ?
- **Variant of VXD–SIT design made of CMOS pixel sensors (other variants give similar performances)**

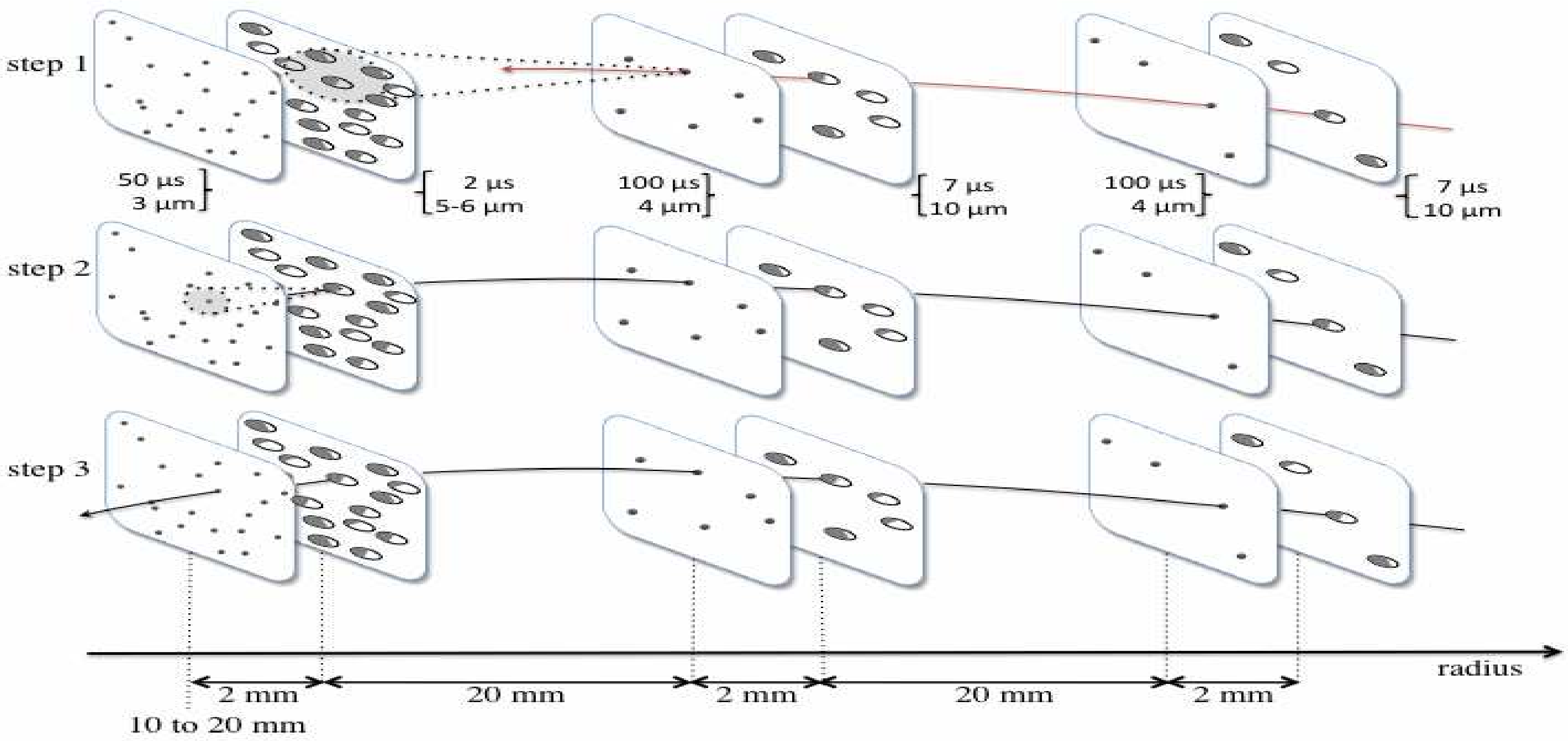
Layer	σ_{sp} MIMOSA/AROM	t_{int} MIMOSA/AROM	**Occupancy [%]** w/o safey factor	**Power** inst./average
VXD-1	3 / 5-6 μm	50 / 2 μs	0.9(2.6) / 0.1(0.3)	250/5 W
VXD-2	4 / 10 μm	100 / 7 μs	0.3(0.9) / 0.04(0.1)	120/2.4 W
VXD-3	4 / 10 μm	100 / 7 μs	0.06(0.2) / 0.01(0.03)	200/4 W
SIT-1	4 / 15 μm	100 / 7 μs	$\lesssim$ 0.01	$\sim$ 1.3 kW/26 W
SIT-2	4 μm	100 μs	$\lesssim$ 0.01	$\sim$ 2.5 kW/50 W

- **ILD-SIT : power consumption** (average $\lesssim$ 100 W for $\gtrsim$ 4 m^2 coverage) **seems affordable**

  $\Rrightarrow$ **need benchmark event study with beam BG to evaluate track reconstruction performance**

Tracking through ILD-VXD

- **Tracking from outside towards IP combining MIMOSA spatial resolution & AROM timestamp**
  - ⁜ MIMOSA provides < 3 or 4 μm spatial resolution
  - ⁜ AROM provides 2 or 7 μs time stamping



	M-in	A-1	M-out	A-2	M-out	A-2
Pixel occupancy [%] :	**0.9**	**0.1**	**0.3**	**0.04**	**0.06**	**0.01**
with safety factor 3 [%] :	**2.6**	**0.3**	**0.9**	**0.1**	**0.2**	**0.03**