

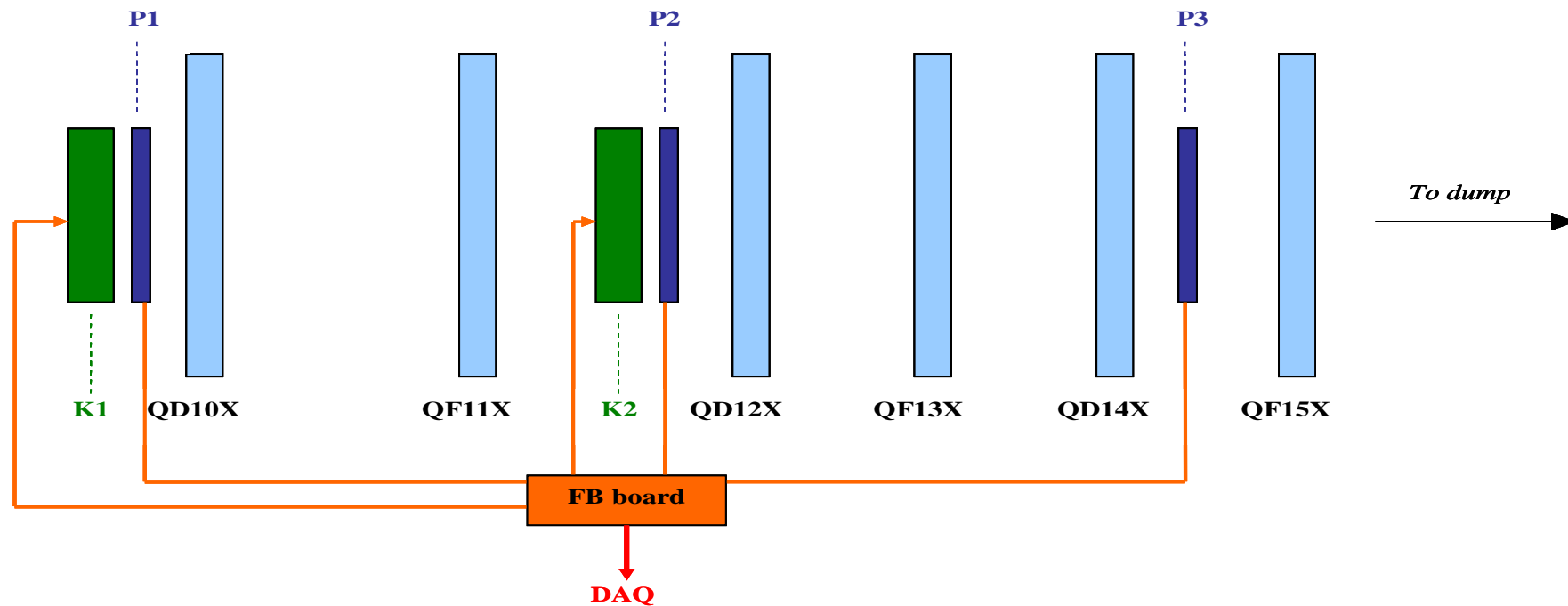
Update on recent results of FONT5 beam-tests at ATF

Glenn Christian

20 March 2012

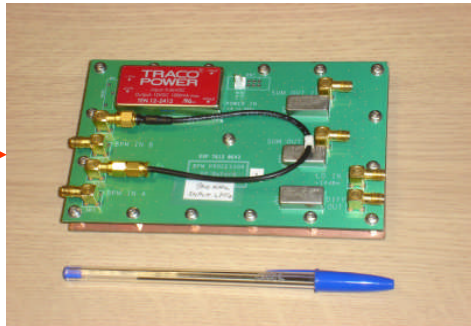
FONT5 upstream feedback system @ ATF2

- Bunch-by-bunch (two-phase) position and angle feedback: 3 stripline BPMs (on movers), 2 stripline kickers

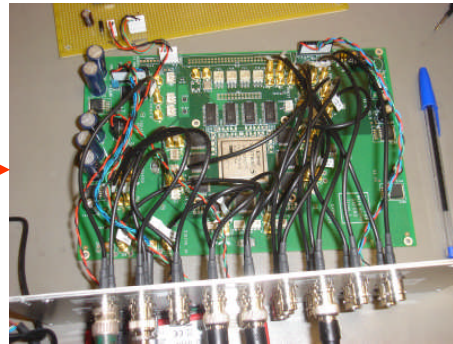


- Ideal: 2 loops, $\pi/2$ betatron phase advance between each loop. Loop1 (P2-K1) corrects position (angle) at P2 (P3); loop 2 (P3-K2) corrects angle (position) at P2 (P3).
- As phase advance is not exactly $\pi/2$ - loops coupled. Kicker drive signals linear function of both P2 and P3 measurements.
- **Correct correlated jitter at two phases – remain corrected at arbitrary location downstream**
- FB with two or three bunch per trains. Measure first bunch, correct subsequent bunches.

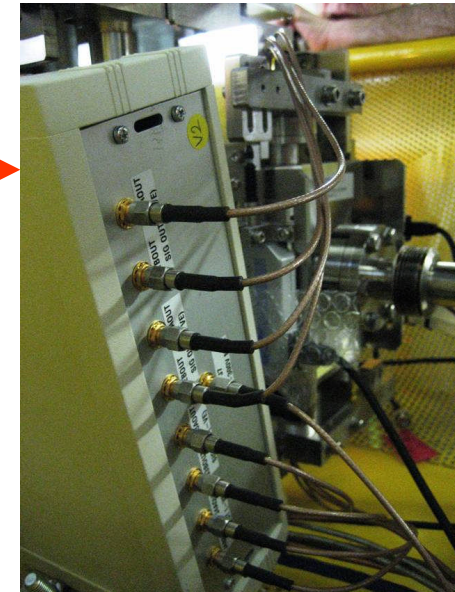
FONT5 Hardware



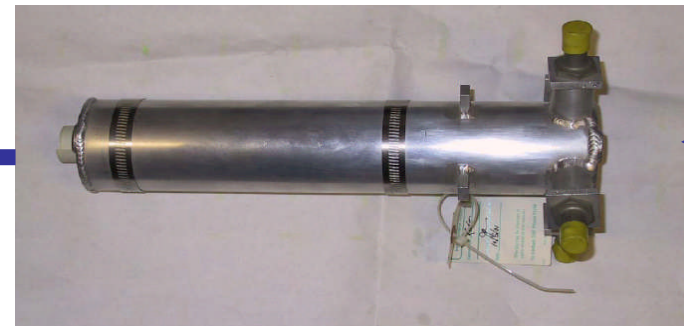
Analogue Front-end
BPM processor



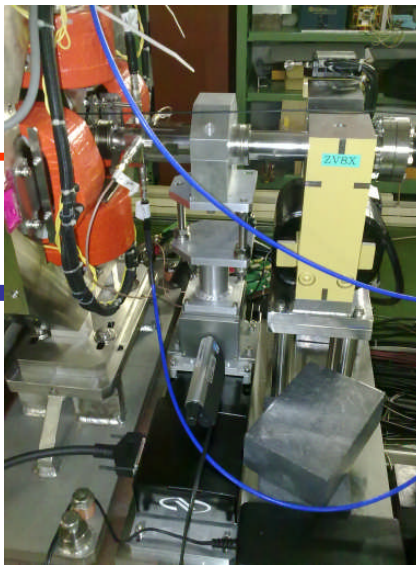
FPGA-based digital
processor



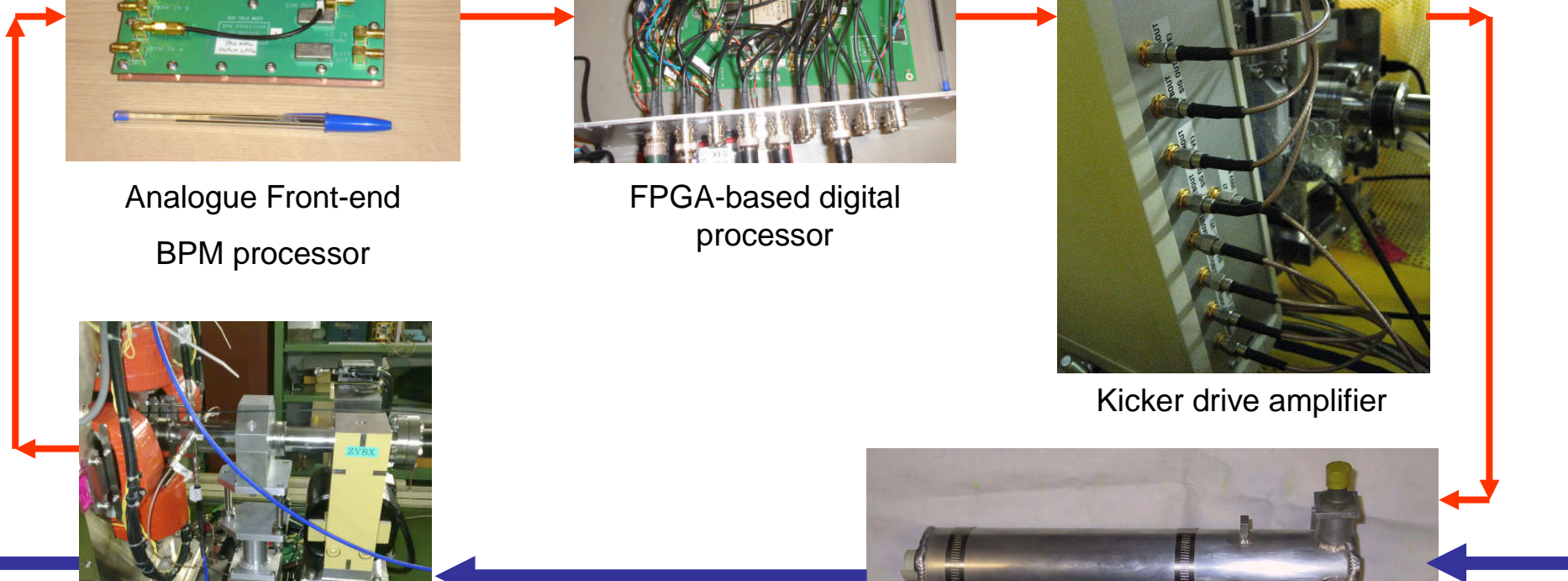
Kicker drive amplifier



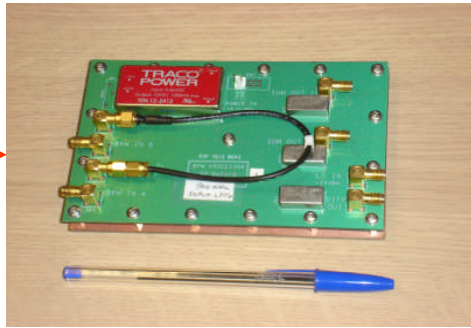
Strip-line kicker



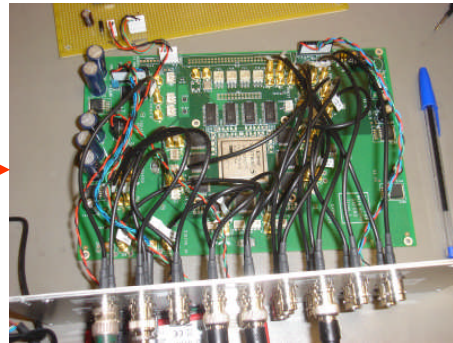
Strip-line BPM with
mover system



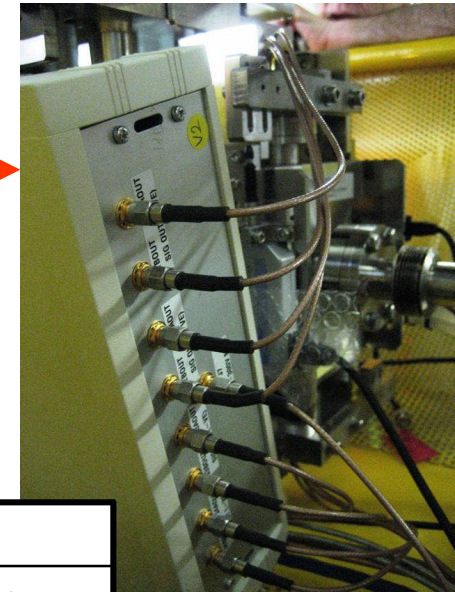
FONT5 Hardware



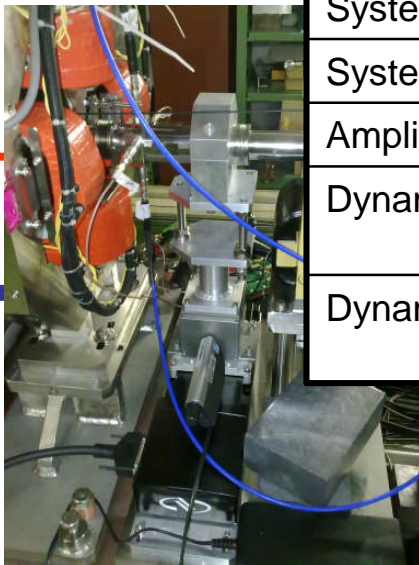
Analogue Front-end
BPM processor



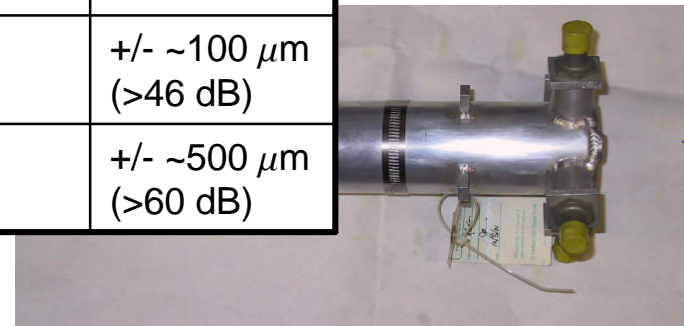
FPGA-based digital
processor



Kicker drive amplifier



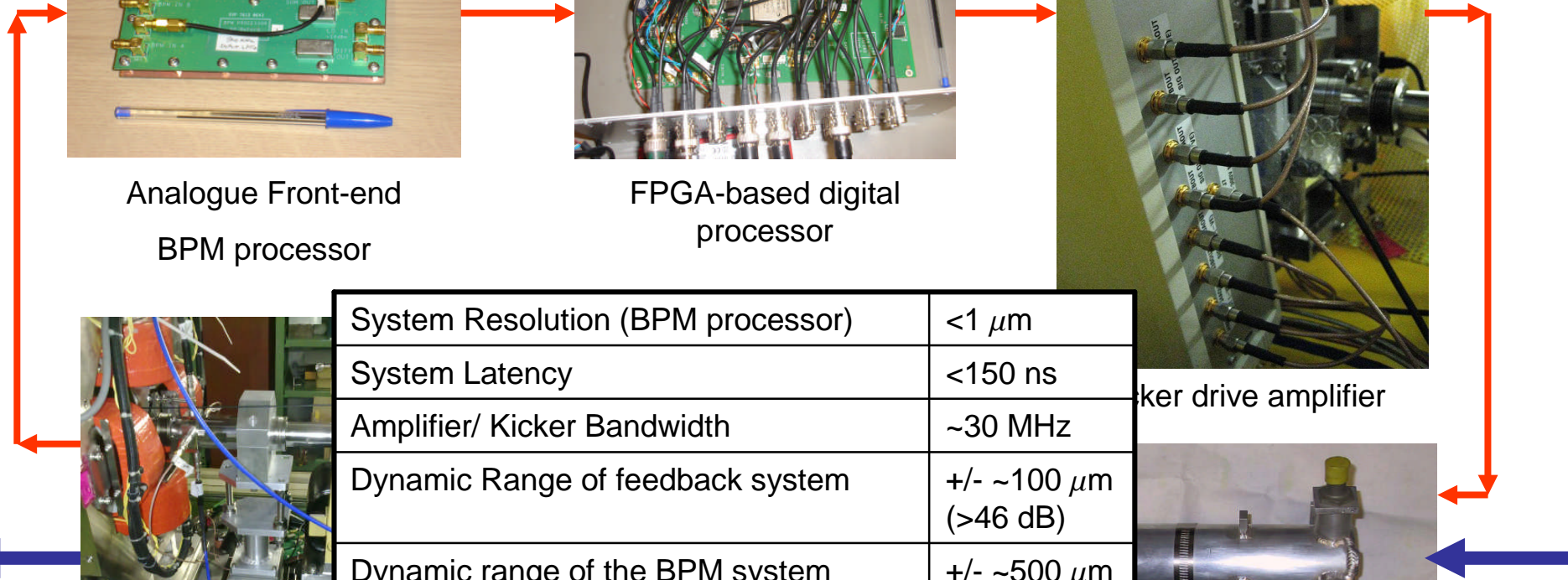
Strip-line BPM with
mover system



Strip-line kicker

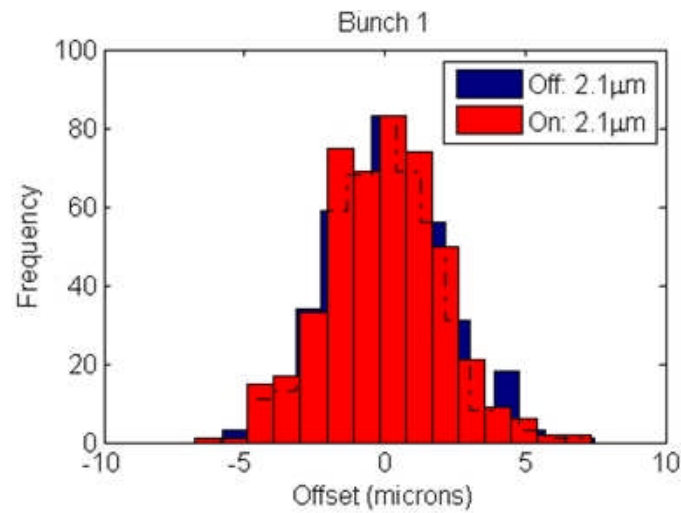
System Resolution (BPM processor)	$<1 \mu\text{m}$
System Latency	$<150 \text{ ns}$
Amplifier/ Kicker Bandwidth	$\sim 30 \text{ MHz}$
Dynamic Range of feedback system	$\pm \sim 100 \mu\text{m}$ ($>46 \text{ dB}$)
Dynamic range of the BPM system	$\pm \sim 500 \mu\text{m}$ ($>60 \text{ dB}$)

System parameters



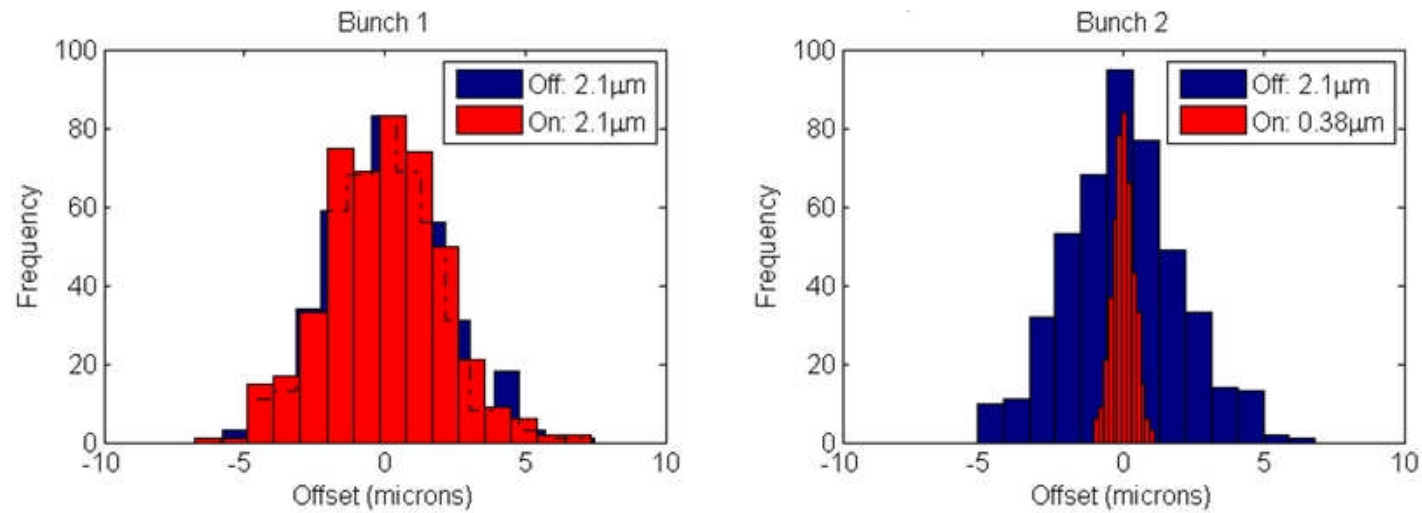
16 April 2010

Feedback Performance (2) – Jitter Reduction @ P2 (16 April 2010)



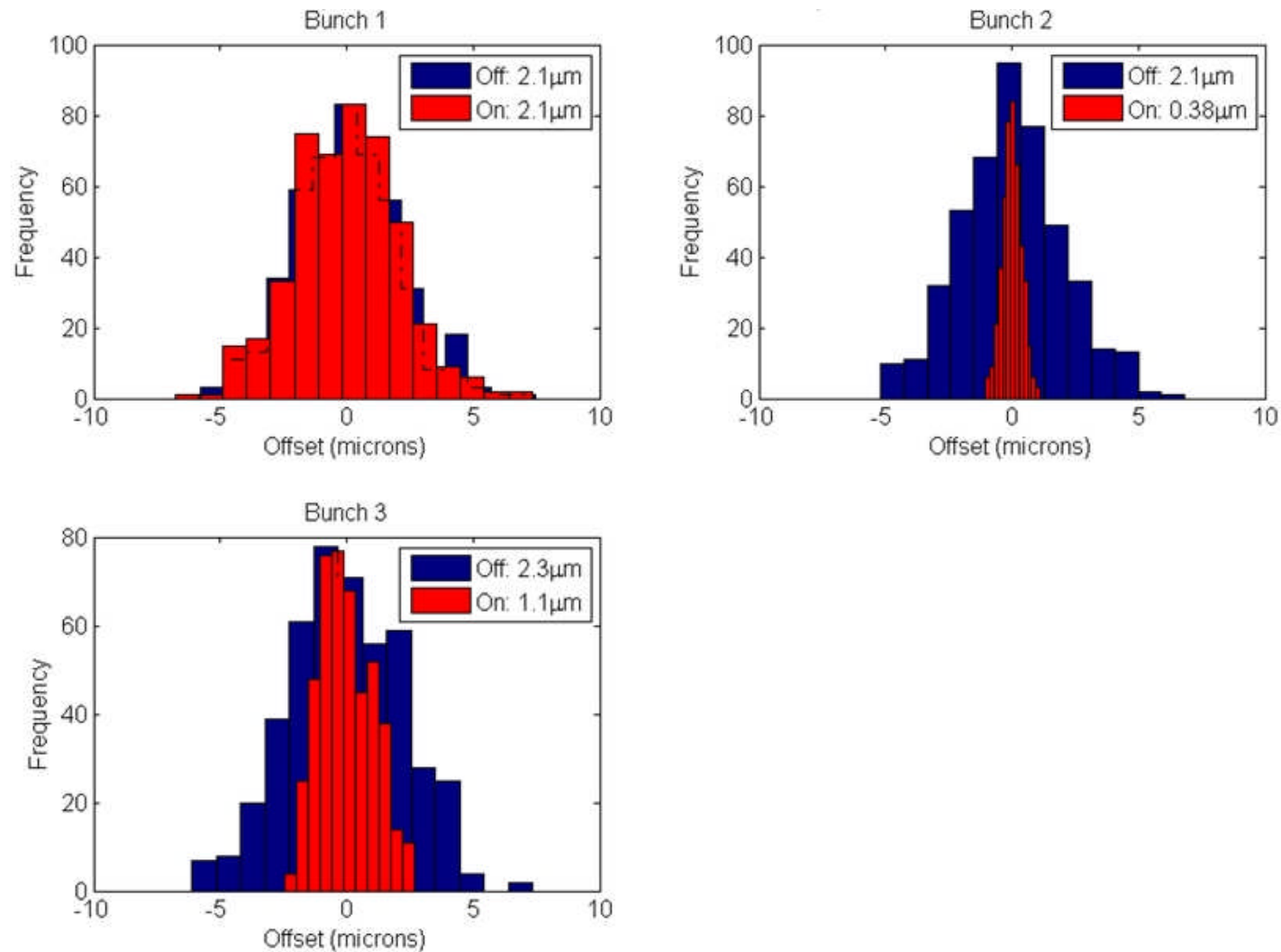
16 April 2010

Feedback Performance (2) – Jitter Reduction @ P2 (16 April 2010)



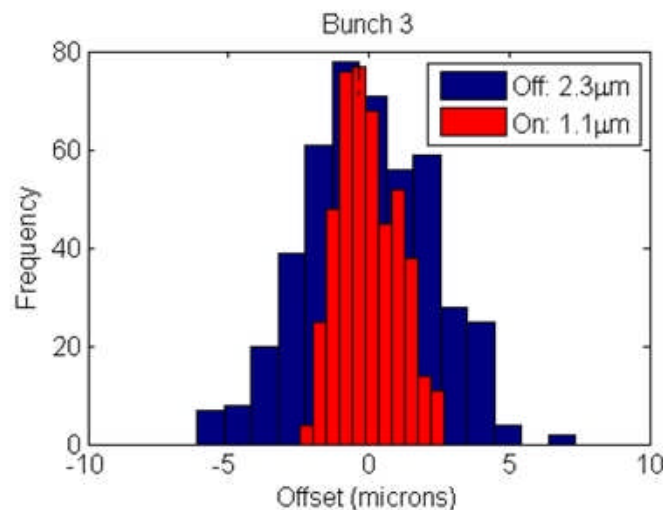
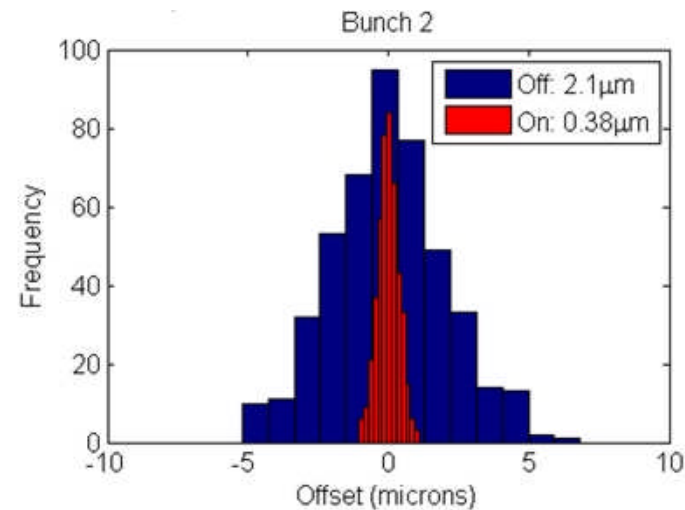
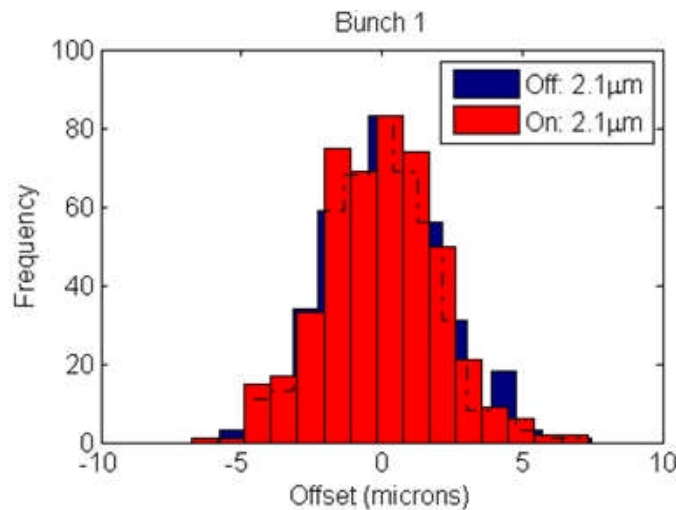
16 April 2010

Feedback Performance (2) – Jitter Reduction @ P2 (16 April 2010)



16 April 2010

Feedback Performance (2) – Jitter Reduction @ P2 (16 April 2010)



Measured bunch-to-bunch correlations:

Bunch 1 – Bunch 2 : 98 %

Bunch 2 – Bunch 3 : 89 %

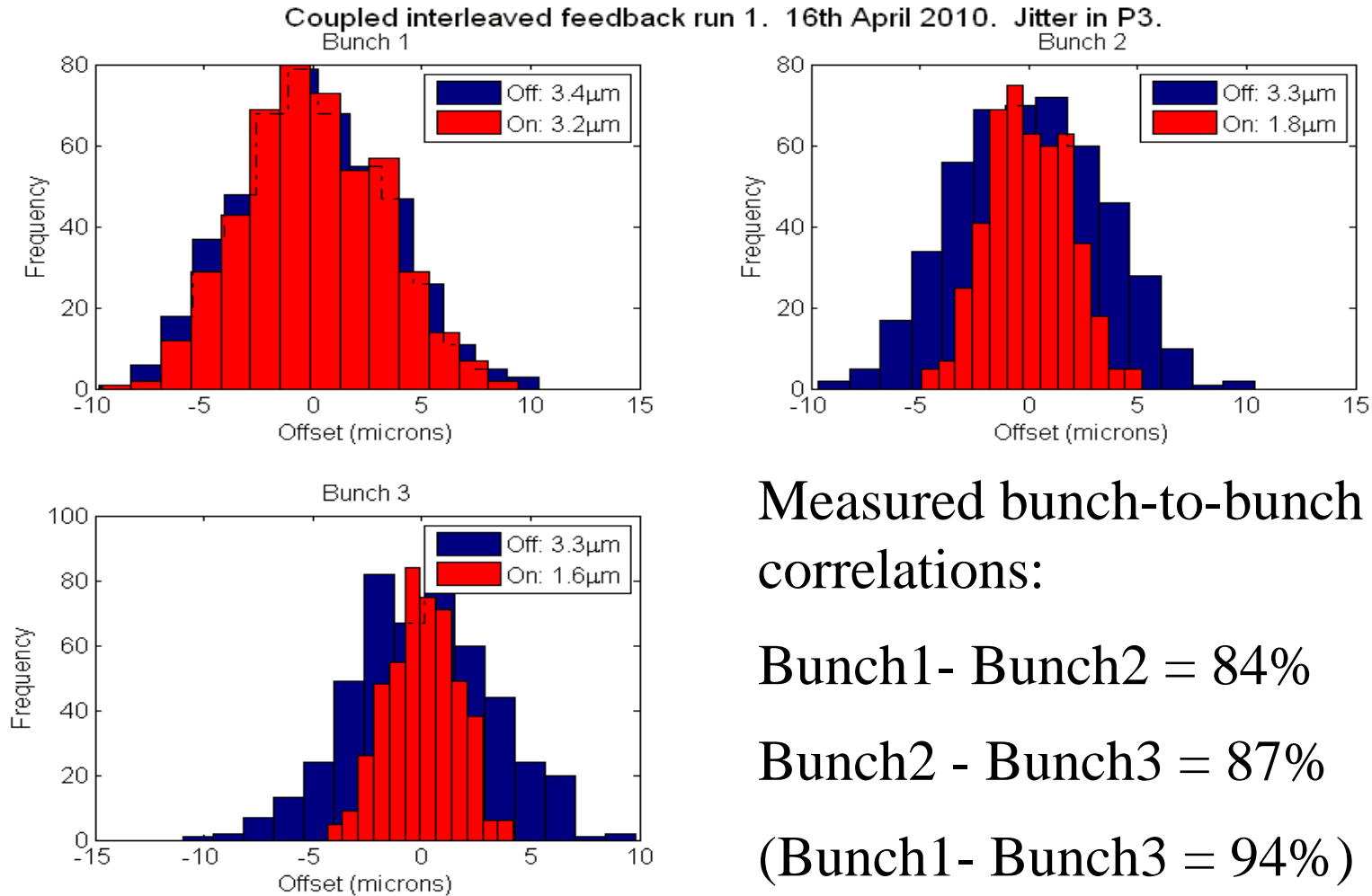
(Bunch 1 – Bunch 3 : 85 %)

$$\sigma_n'^2 = \sigma_n^2 + \sigma_{n-1}^2 - 2\text{cov}(n, n-1)$$

Bunch 2 result implies resolution of ~ 300 nm!

16 April 2010

Feedback Performance (3) – Jitter Reduction @ P3 (16 April 2010)



Processor Improvements (2011)

- Hypothesis that discrepancy between FB results and resolution due to sensitivity of measured position to LO phase jitter
 - All processors/BPMs exhibit different sensitivity to LO jitter wrt beam. (P2 just happens to be least sensitive.)
 - Effects cancel for measurements using just one BPM, for example FB, whereas measurements involving correlating positions across several BPM, appear to have poor resolution.
 - Largest effect due to path length imbalance to hybrid (unique for each processor) – larger residual from subtraction, more susceptible to LO jitter
- All processors optimised (summer 2011)
 - Input cables optimised for matched path length at hybrid
 - Sum loopback cables re-made to phase sum and difference channels
- Also, discovered and fixed problem with sampling jitter caused by noise pickup on ADC clocks from FPGA (affected correlated measurements across more than one BPM, hence contributed to effective resolution)

Summary of FONT data-taking visits 2011/2012

- June 2011 (Burrows, Perry, Apsimon, Bett, Davis)
 - 1 week, no shifts
 - Check-out of FB instrumentation post earthquake
- October 2011 (Perry, Bett, Davis)
 - 1 week, no shifts requested
 - Parasitic measurements of processor performance
- November 2011 (Christian, Bett)
 - 1 week, 2 shifts
 - Studies in DR and EXT of jitter and bunch phase stability wrt LO, and clock stability studies
- Nov-Dec 2011 (Burrows, Christian, Apsimon, Bett, Davis, Blaskovic)
 - 3 weeks, 2 shifts per week
 - 2 bunch feedback in EXT with BS 187.6 ns
- March 2012 – 1 week (Bett, Davis, Blaskovich)
 - 1 week, 2 shifts.
 - Further investigations of phase jitter effects.

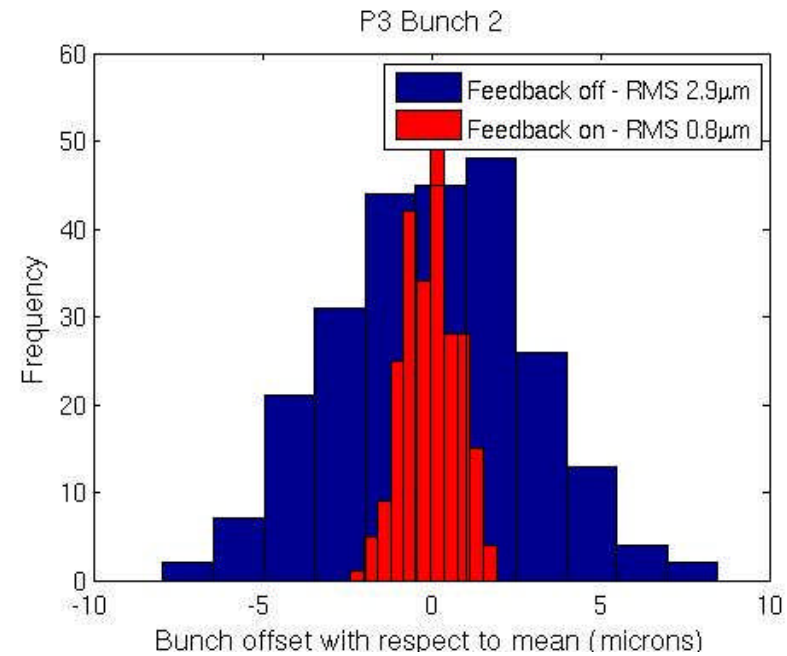
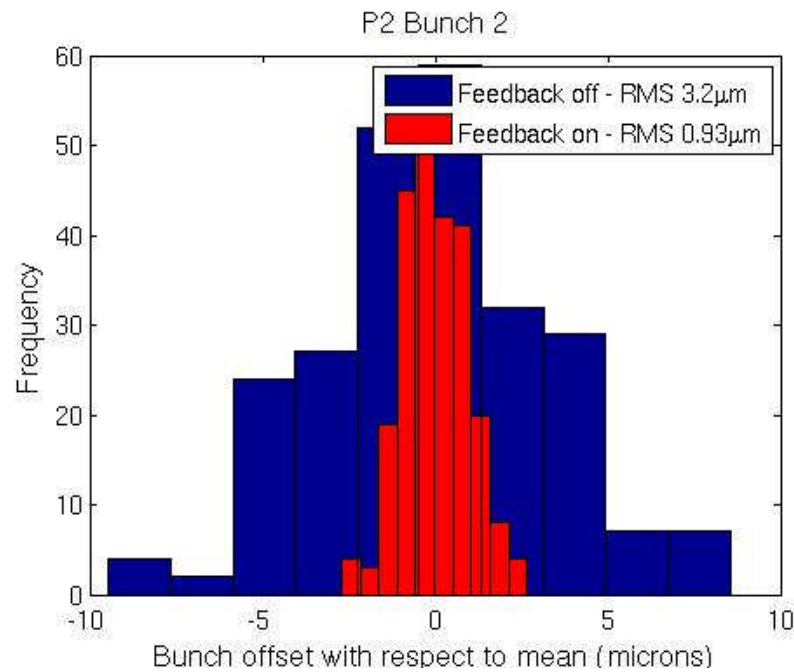
Summary of Nov-Dec data-taking

- Investigated 2 bunch extraction
 - Vary bunch spacing & extraction kicker timing
- Resolution studies (mostly parasitic)
- 2 bunch feedback @ 187.6 ns spacing
 - Instrumented MQF14X, MQD15X, and MFB1FF
 - ‘Standard’ set of measurements
 - BPM calibrations
 - LO-phase sensitivity scans
 - Single loop FB , P2-K1, P3-K2 and two loop coupled/uncoupled FB
 - Kicker calibrations (transfer function measurement -> FB gain)
 - FB gain scans (vary four loop gain values by +/- 20-40 % around nominal point)
 - FB loop latency measurements

Dec 2011

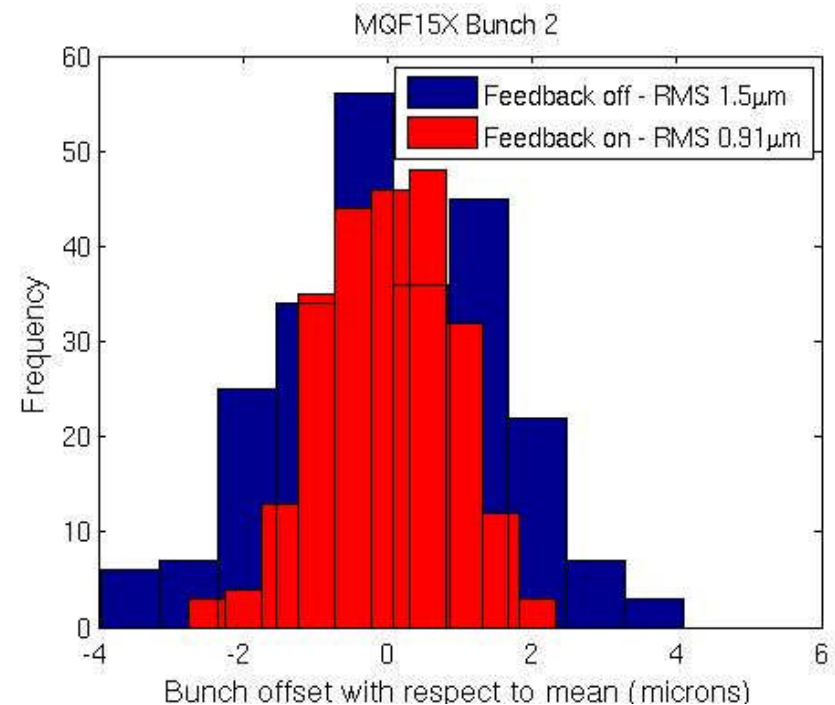
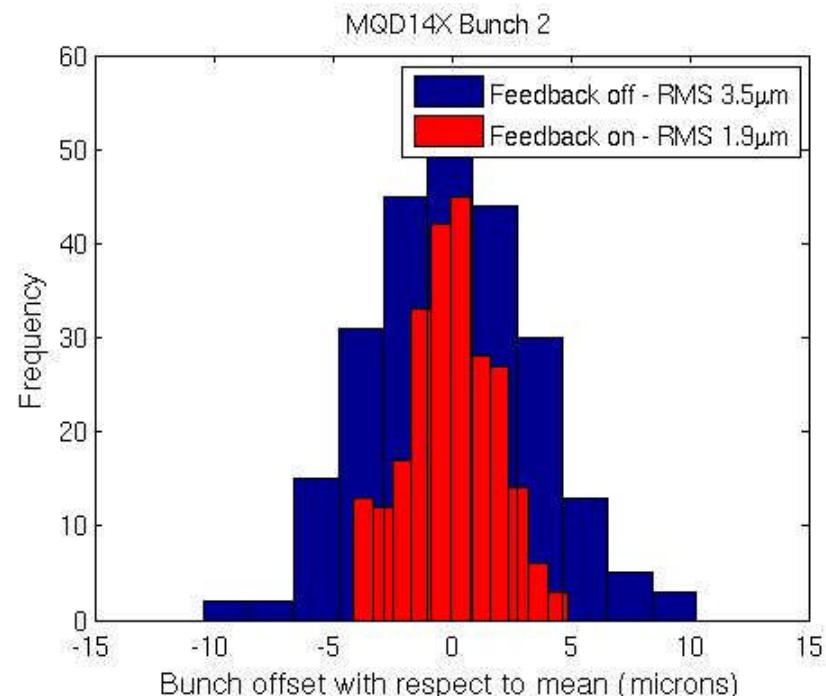
December 2011 FB results

Feedback BPMS



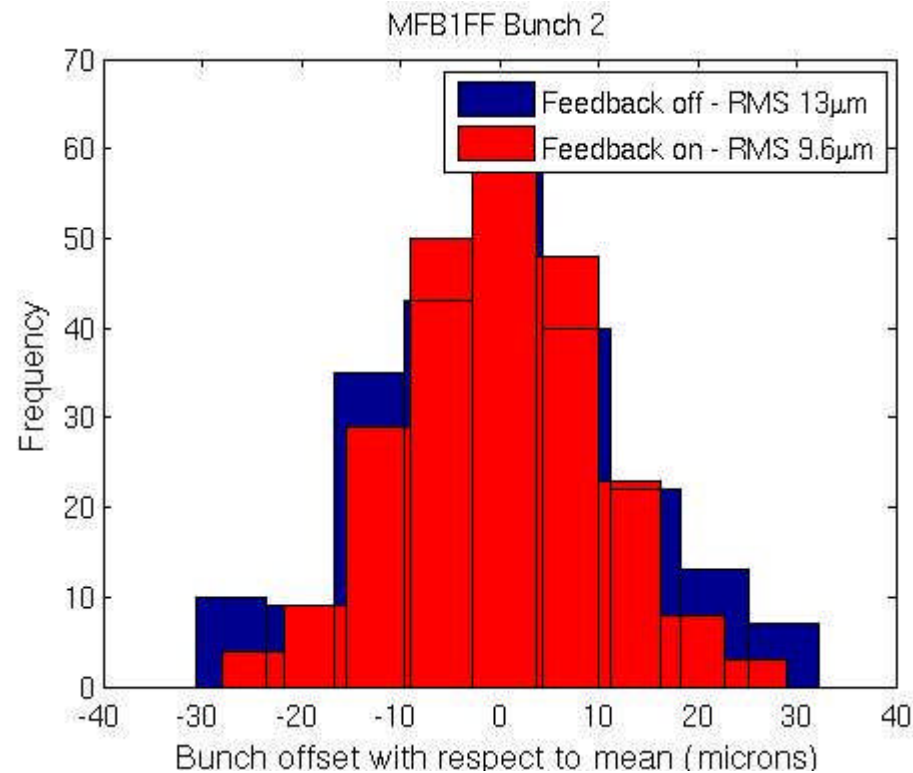
Dec 2011

December 2011 FB results Witness BPMS (1)



Dec 2011

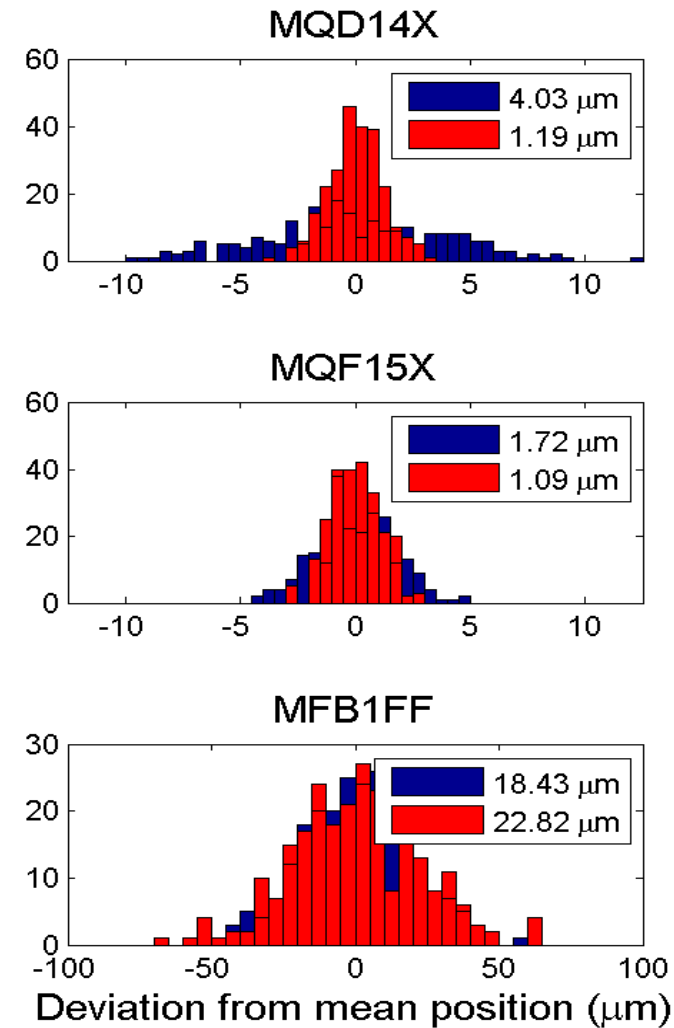
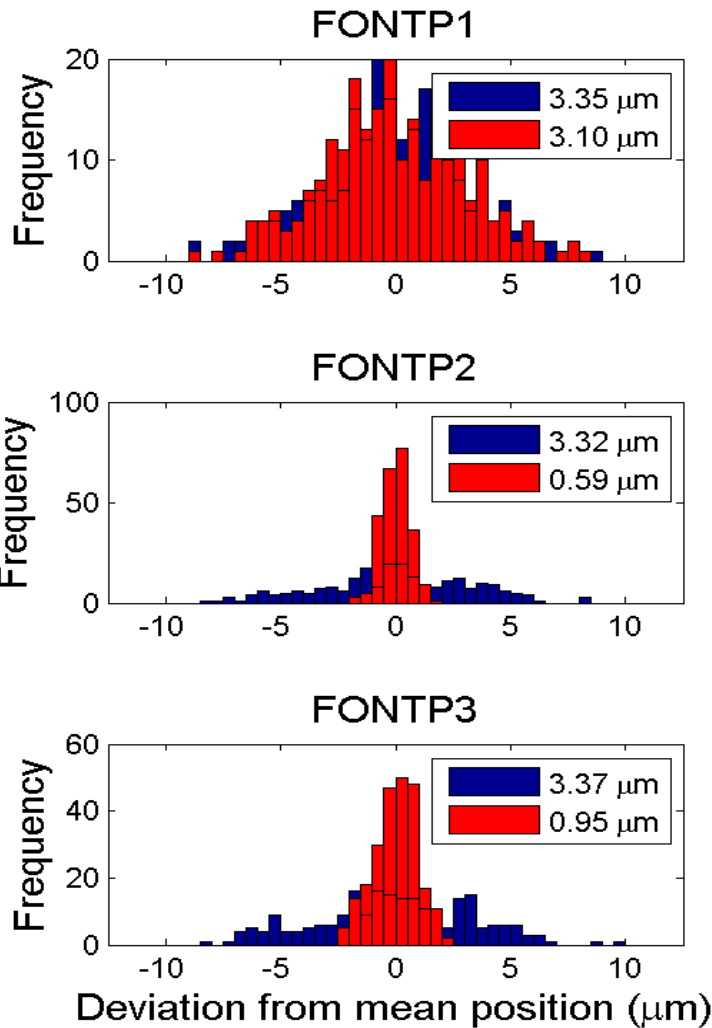
December 2011 FB results Witness BPMS (2)



Dec 2010

Feedback examples (14 Dec 2011)

Run6_141211



BPM resolution tests (parasitic)

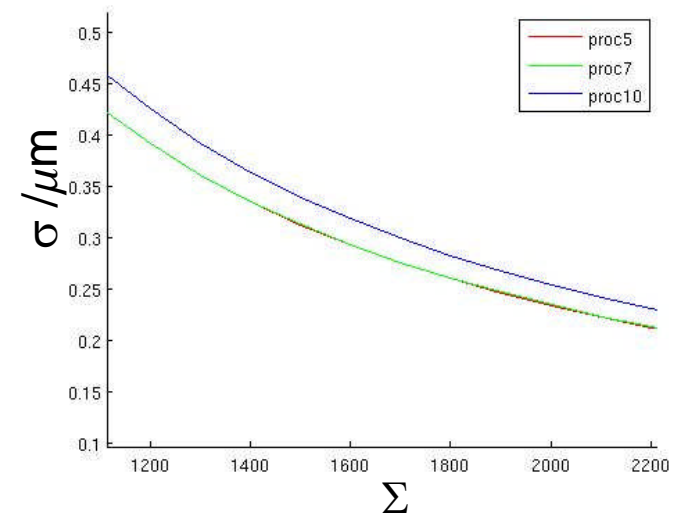
October 2011 – 3 processors on P2 (Charge ~1000-1500 cnts, Jitter 3-4 microns)

Proc1	0.55	0.56	0.53	0.50	0.45	0.50
Proc2	0.56	0.54	0.40	0.35	0.44	0.43
Proc3	0.60	0.51	0.35	0.33	0.35	0.36

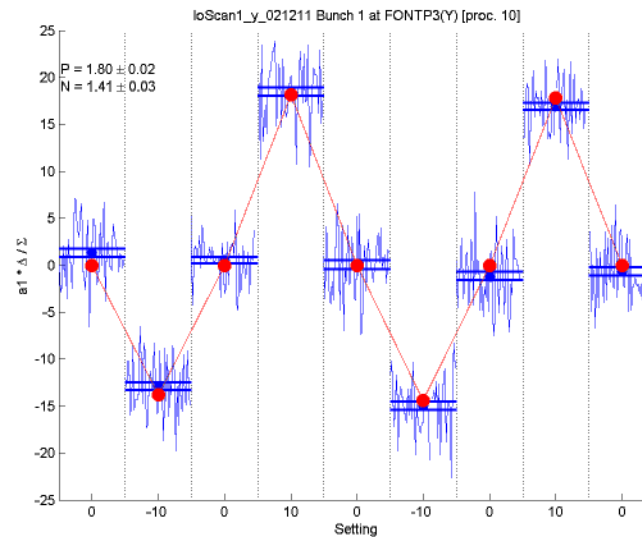
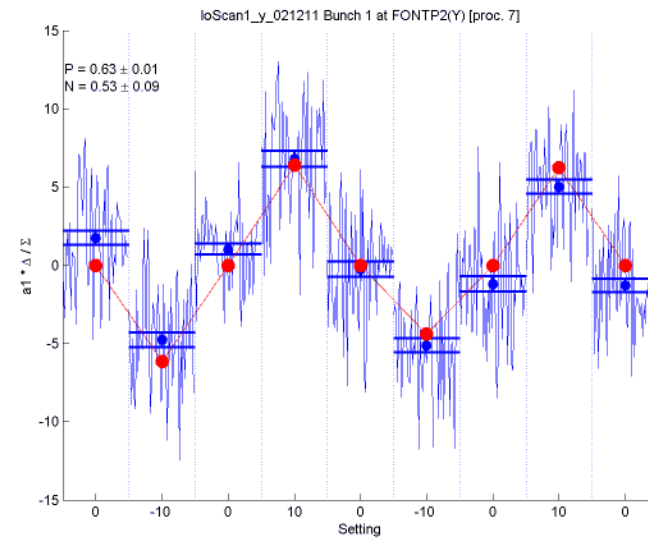
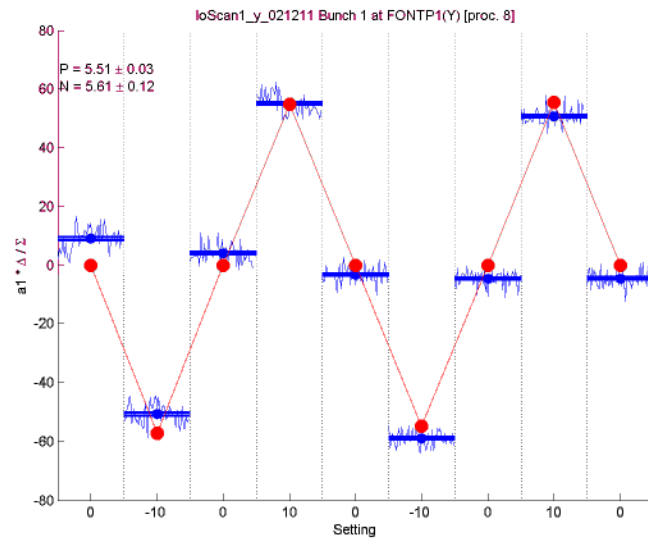
December 2011 – 2 processors on P1,P2,P3

Board #	Method	P1 soln	P2 soln	P3 soln
	1 3-BPM fit	3.01	0.61	0.61
	2 3-BPM fit	1.49	0.79	0.80
BOTH	2-on-1 pairwise	0.39	0.67	0.40
	1 3-BPM fit	3.38	0.70	0.70
	2 3-BPM fit	2.25	0.77	0.78
BOTH	2-on-1 pairwise	0.39	0.53	0.36

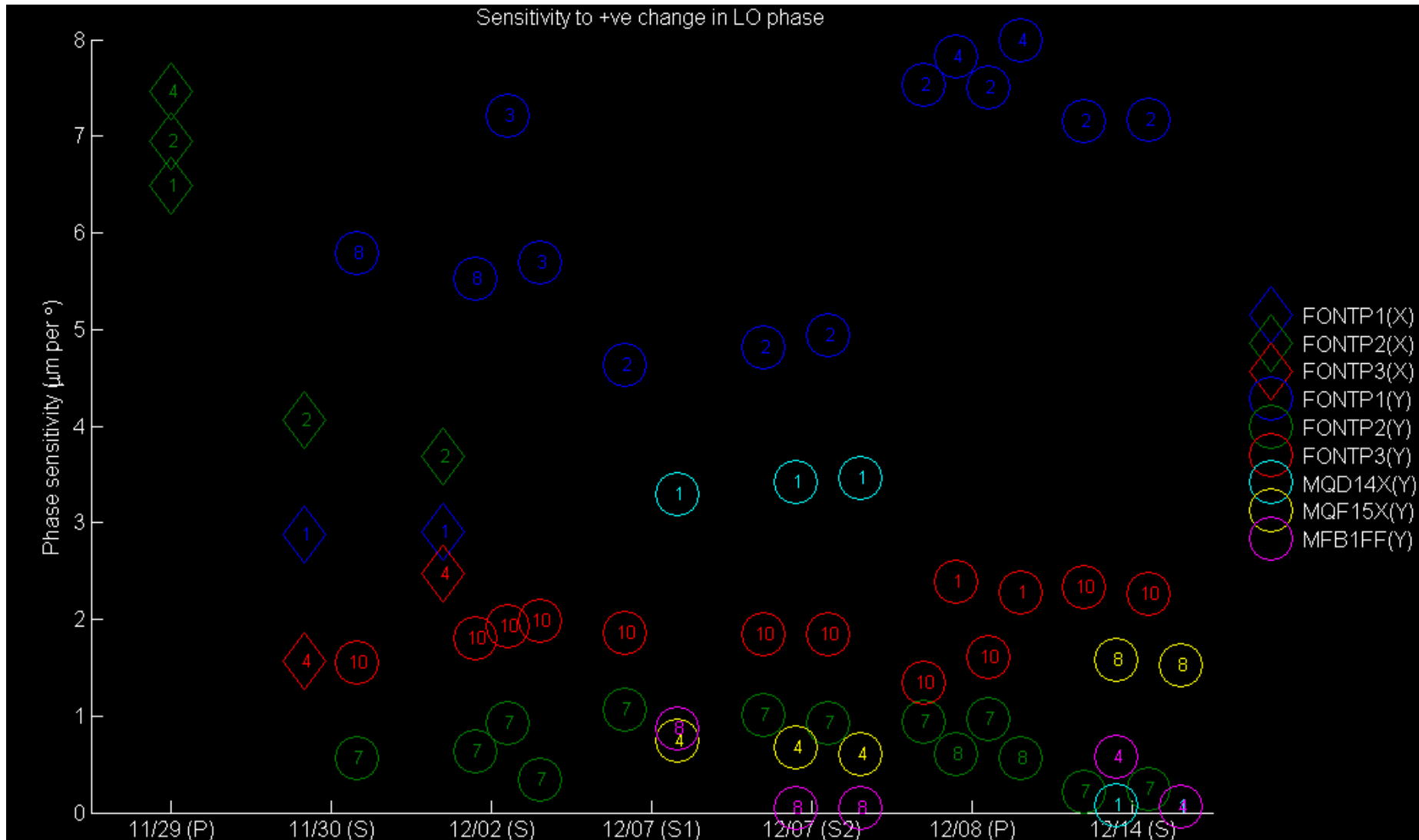
Minimum resolution based on ADC noise alone



LO phase scans example (02/12/11)

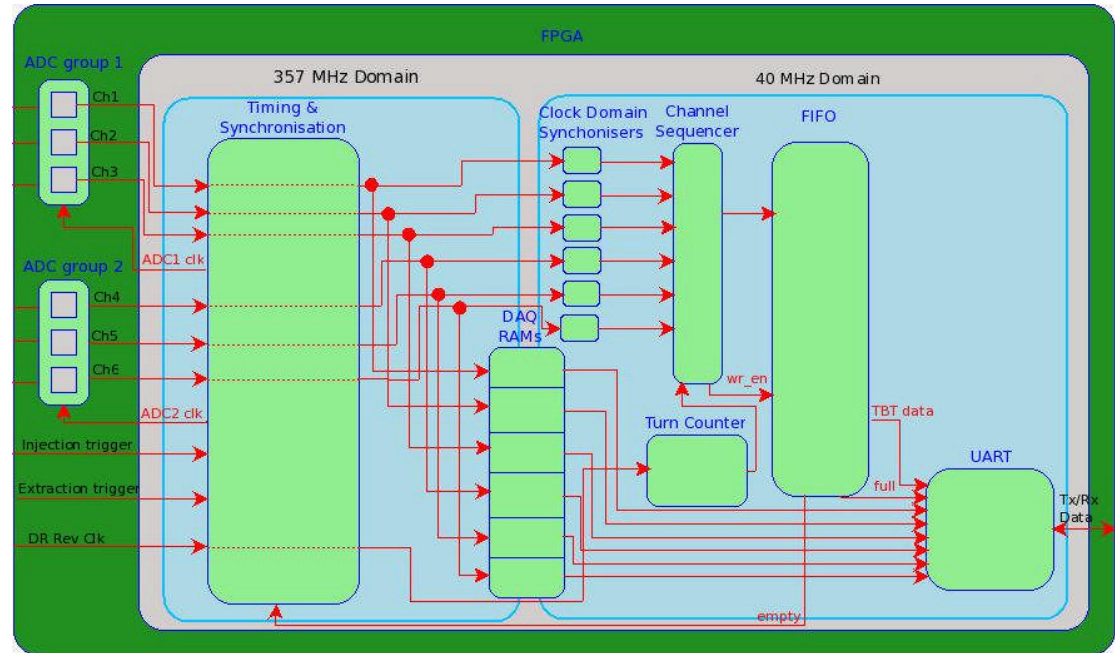
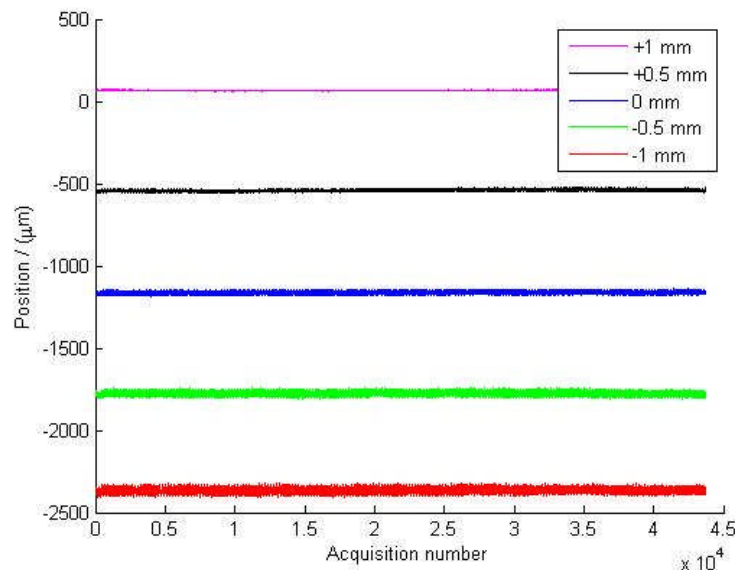
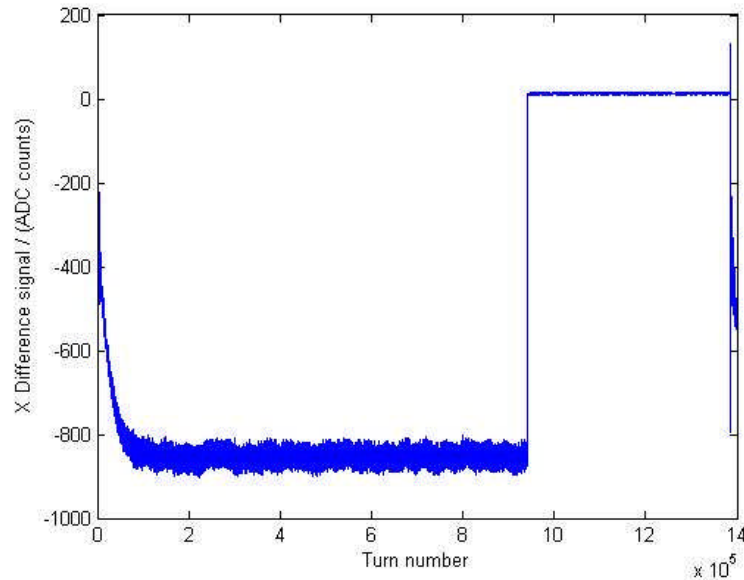


LO phase scans (Nov-Dec summary)



Oct 2010

ATF Damping Ring Multi-bunch Diagnostics



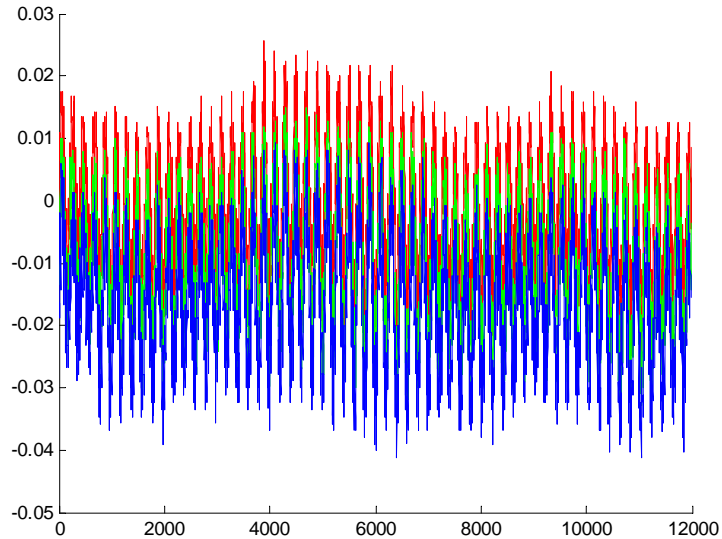
Modified feedback hardware for multi-bunch turn-by-turn DAQ from ATF damping ring

- Up to 3 bunches, 3 channels, from up to 2 BPMs
- Records 131,071 samples per pulse (up to 15% of damping period for single bunch, single channel)
- Can record to n-turns-in-m to vary time window and resolution

Nov 2011

Bunch phase oscillations at extraction wrt LO

SumQ/SumI – 'raw' data



3 distinct frequencies:

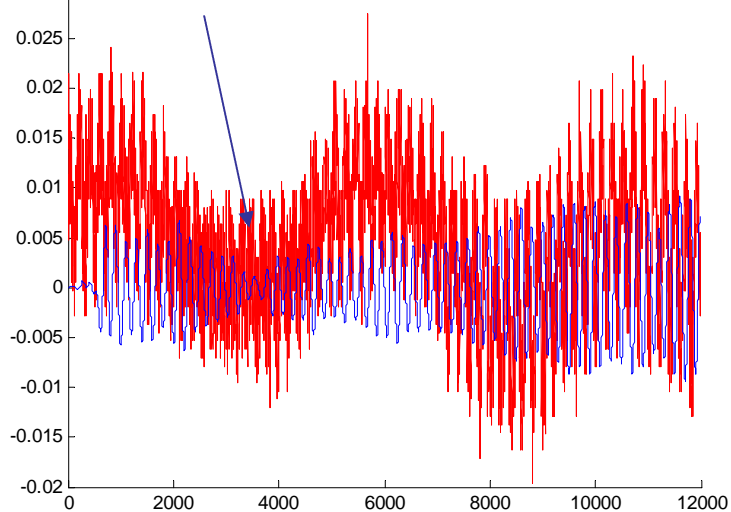
10.8 kHz – synchrotron

434 Hz slow oscillation (unknown)?

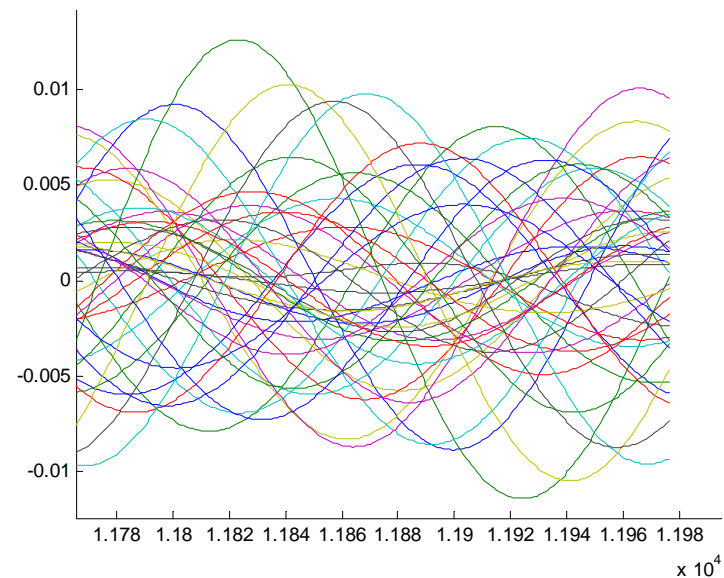
735 kHz fast oscillation – aliased?

Last 200 turns before extraction

5-15 kHz BPF



All pulses : Bunch 3

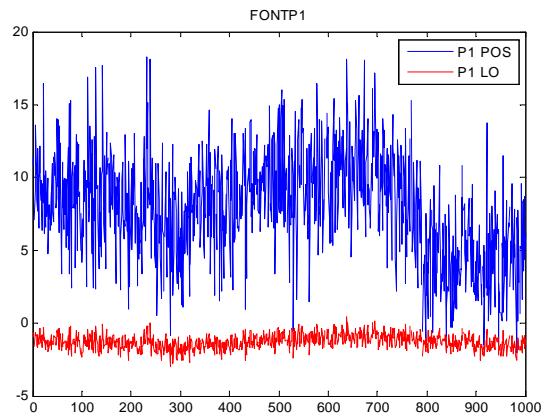


Dec 2011

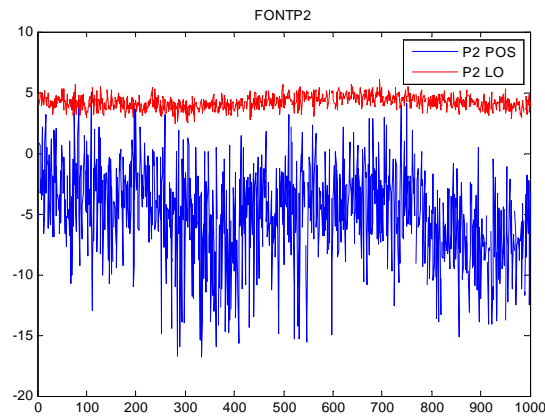
BPM/LO correlations

(1000 pulse parasitic dataset 13/12/11)

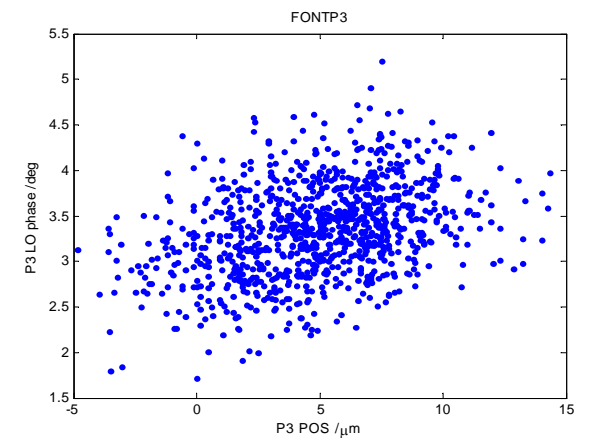
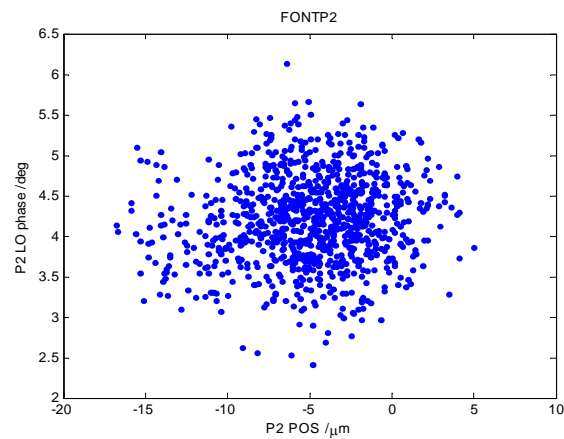
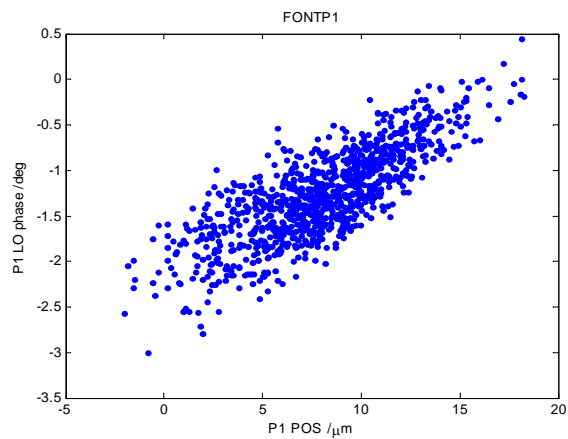
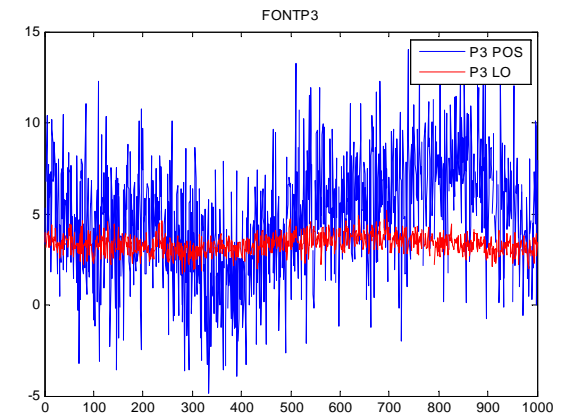
P1: $\rho=0.86$



P2: $\rho=0.01$

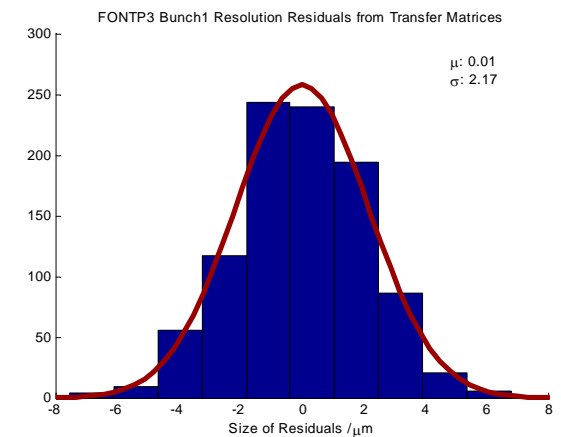
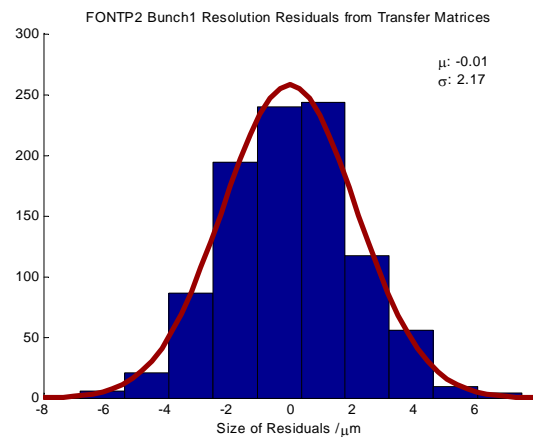
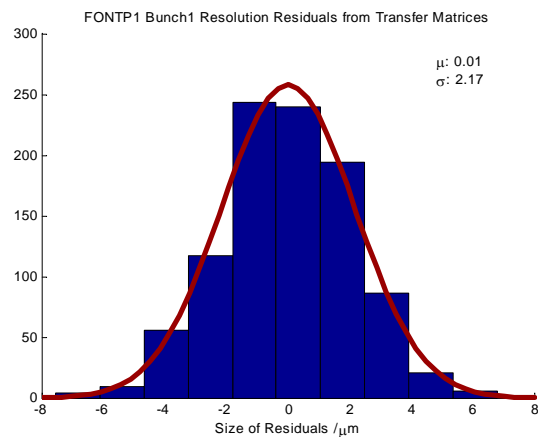
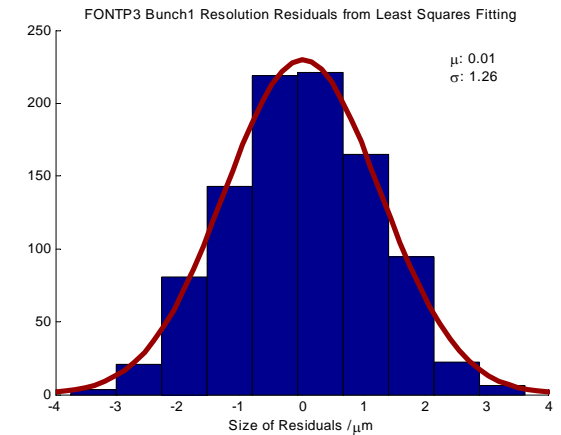
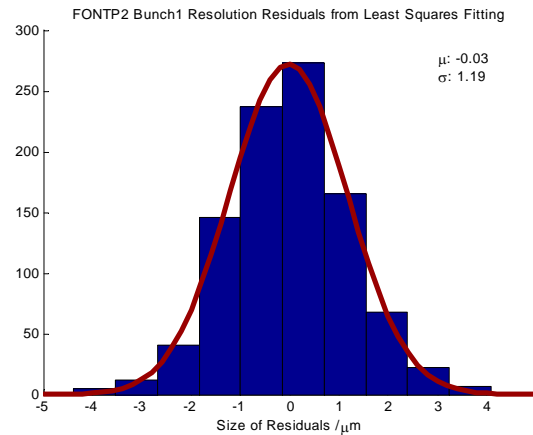
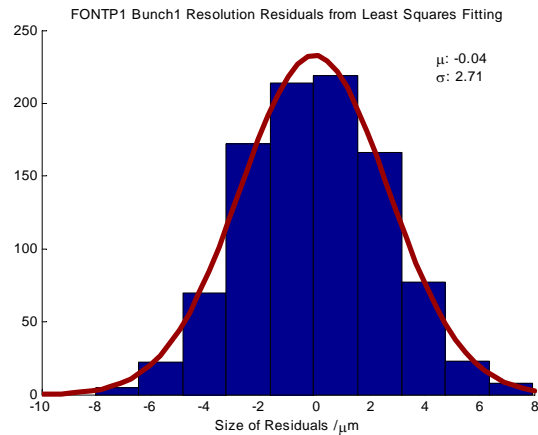


P2: $\rho=0.31$



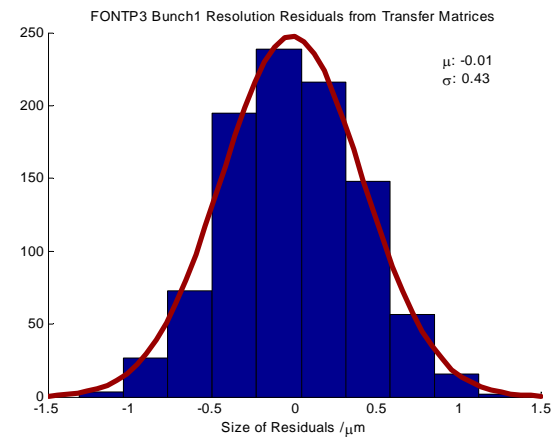
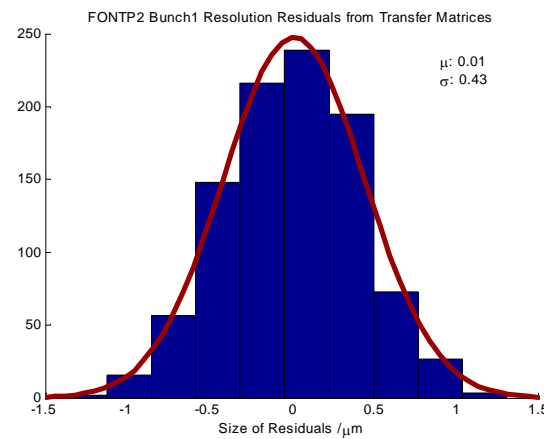
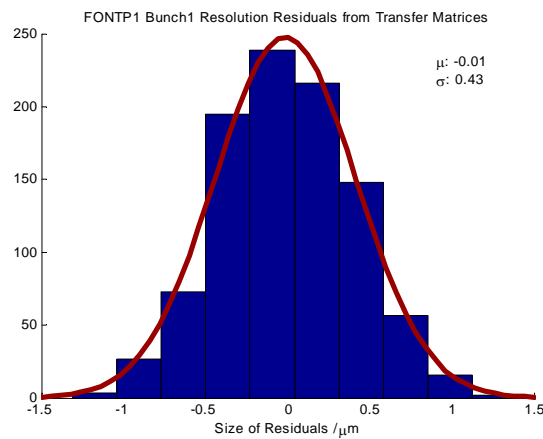
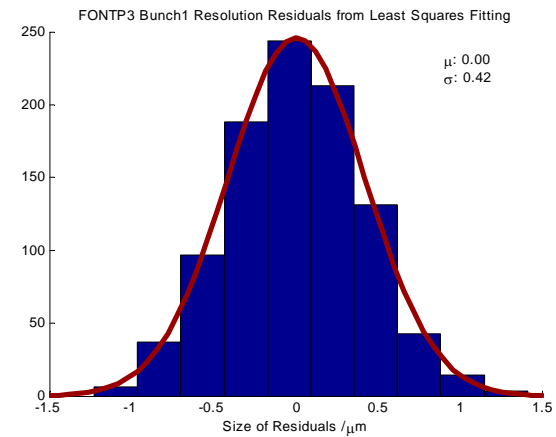
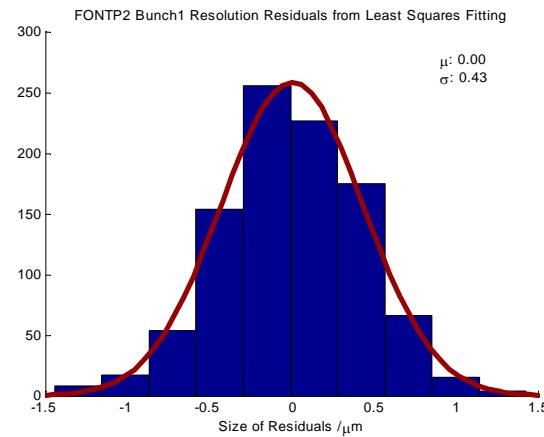
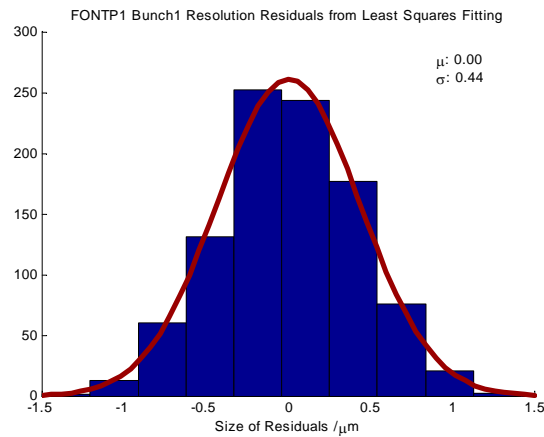
Dec 2011

Original residuals – drift subtracted (1000 pulse parasitic dataset 13/12/11)

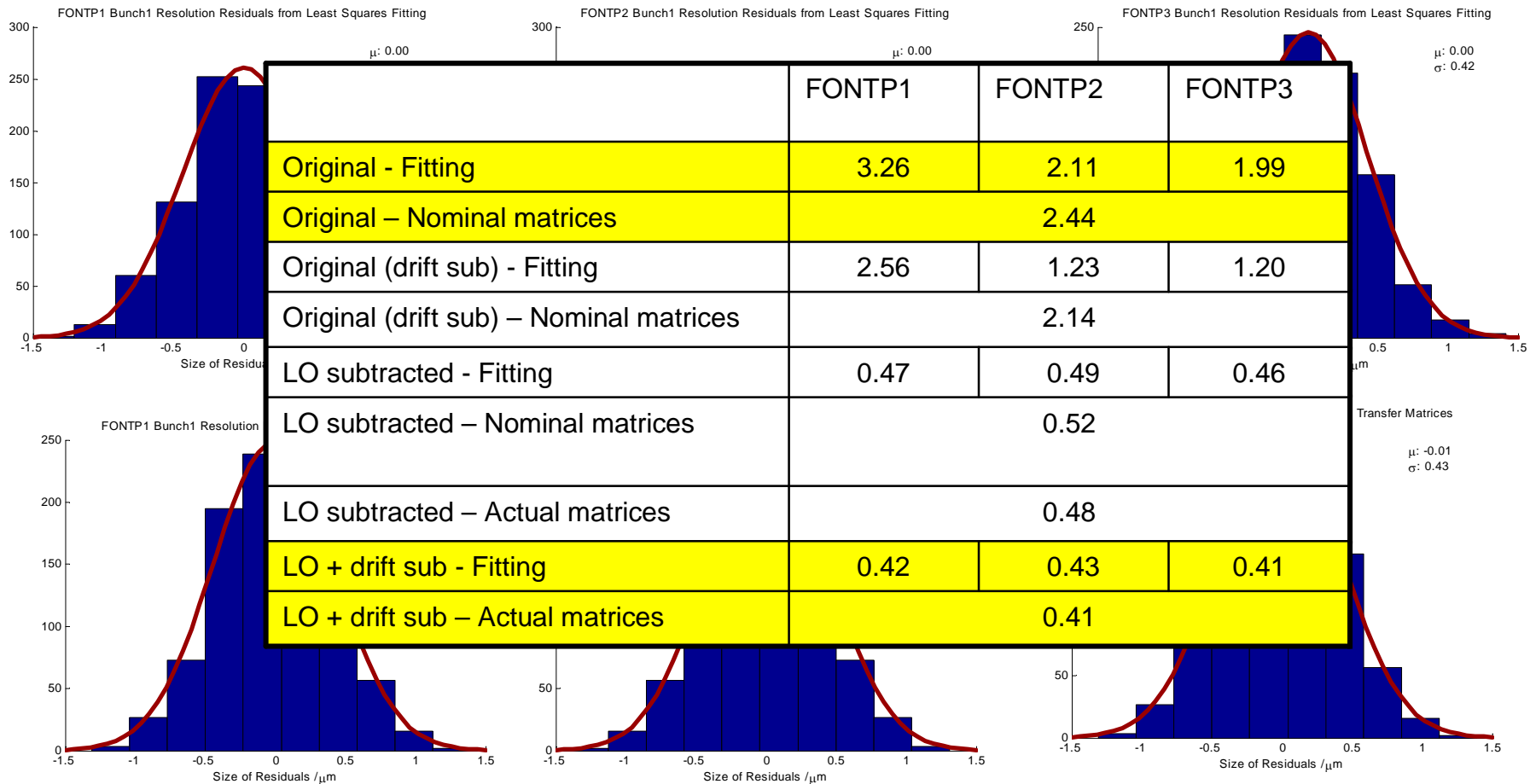


Dec 2011

Resolution residuals – LO phase jitter subtracted + drift removal



Resolution residuals – LO phase jitter subtracted + drift removal



Mitigating against bunch phase jitter wrt LO

- Understand why see good correction at FB control BPMS but not witness BPMs
 - FB system will couple relative phase jitter back into the beam (e.g. synchrotron motion turns into vertical beam jitter)
- Mitigation options
 1. Remove effects (eg synchrotron motion) in DR
 - Feed-back/forward on beam in DR **Hard**
 2. Immunise against effects in DR
 - Feed-forward on the LO to track the bunch phase **Easier**
 3. Subtract the phase jitter from position data OFFLINE, and correct the feedback signal ONLINE
 - **Conceptually even easier, OFFLINE already done, ONLINE requires firmware mods (being tested)**
 - **Proposed solution in first instance**

$$y = G \left(\frac{\Delta - k_\phi \Sigma_Q}{\Sigma_I} \right)$$

Summary

- Feedback performance determined by three quantities: bunch-to-bunch correlation (beam), resolution (processor), and gain (system)
- Over the past year or so spent a lot of time and effort in understanding and mitigating effects limiting resolution
 - Minimising processor sensitivity to LO phase jitter – optimising the path lengths to hybrid
 - Reducing ADC noise pickup – timing jitter on ADC clocks
 - Removing BPM sensitivity to phase jitter
 - Now see very good resolution ~400 nm, in all BPMs, and perfect agreement between machine model and fitting beam trajectory
- Feedback – goal has been to reproduce excellent correction previously seen in P2 at P3 also, and maintain this correct downstream
 - Very good results obtained for P2,P3 (down to ~500-600 nm) correction factor 3-5 , but in general not preserved at witness BPMs
 - Should be able to see better downstream corrections from the removing the phase sensitivity of the BPMs in the feedback correction.

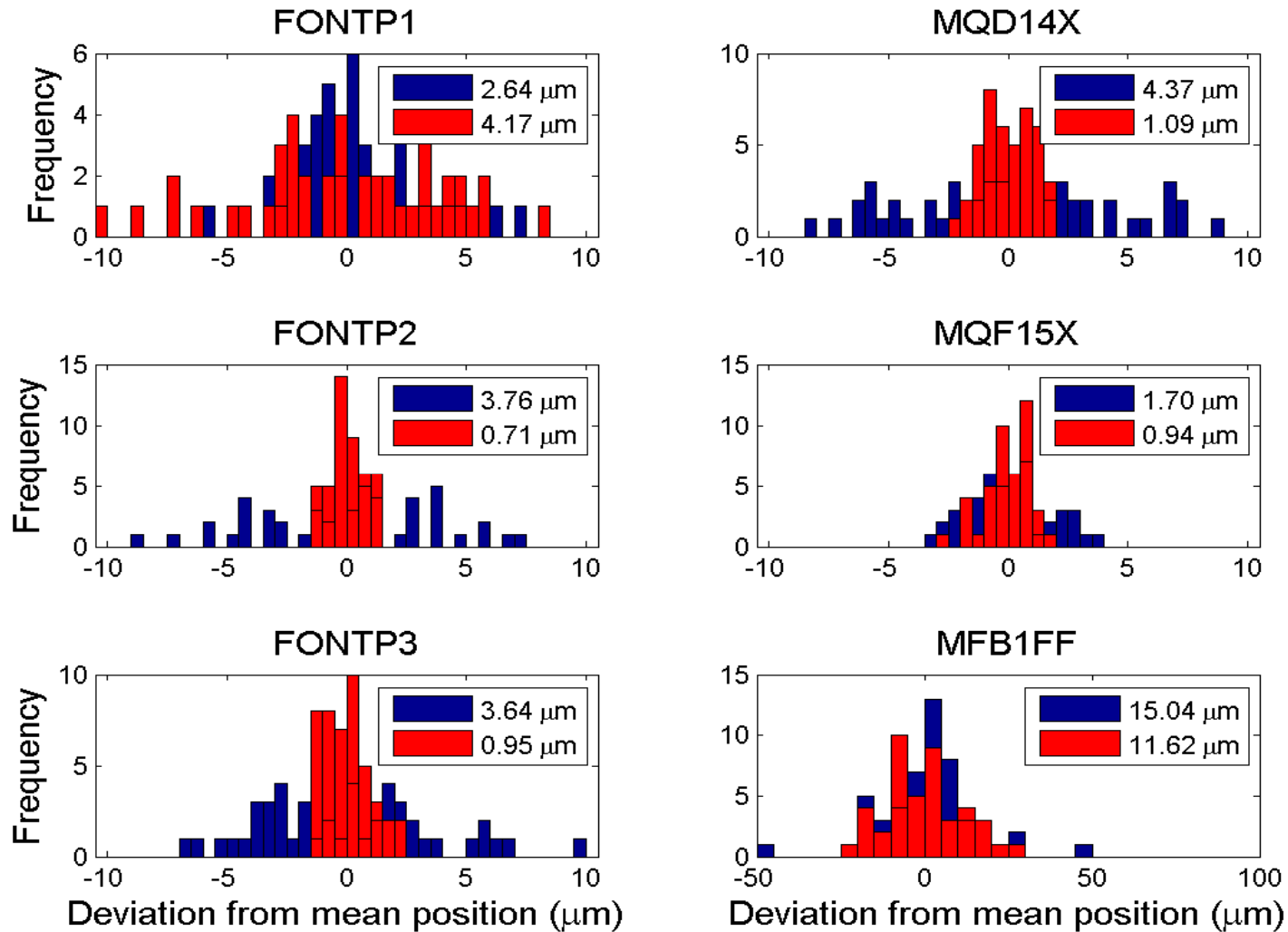
Spares

BPM processor resolution and FB performance limitations

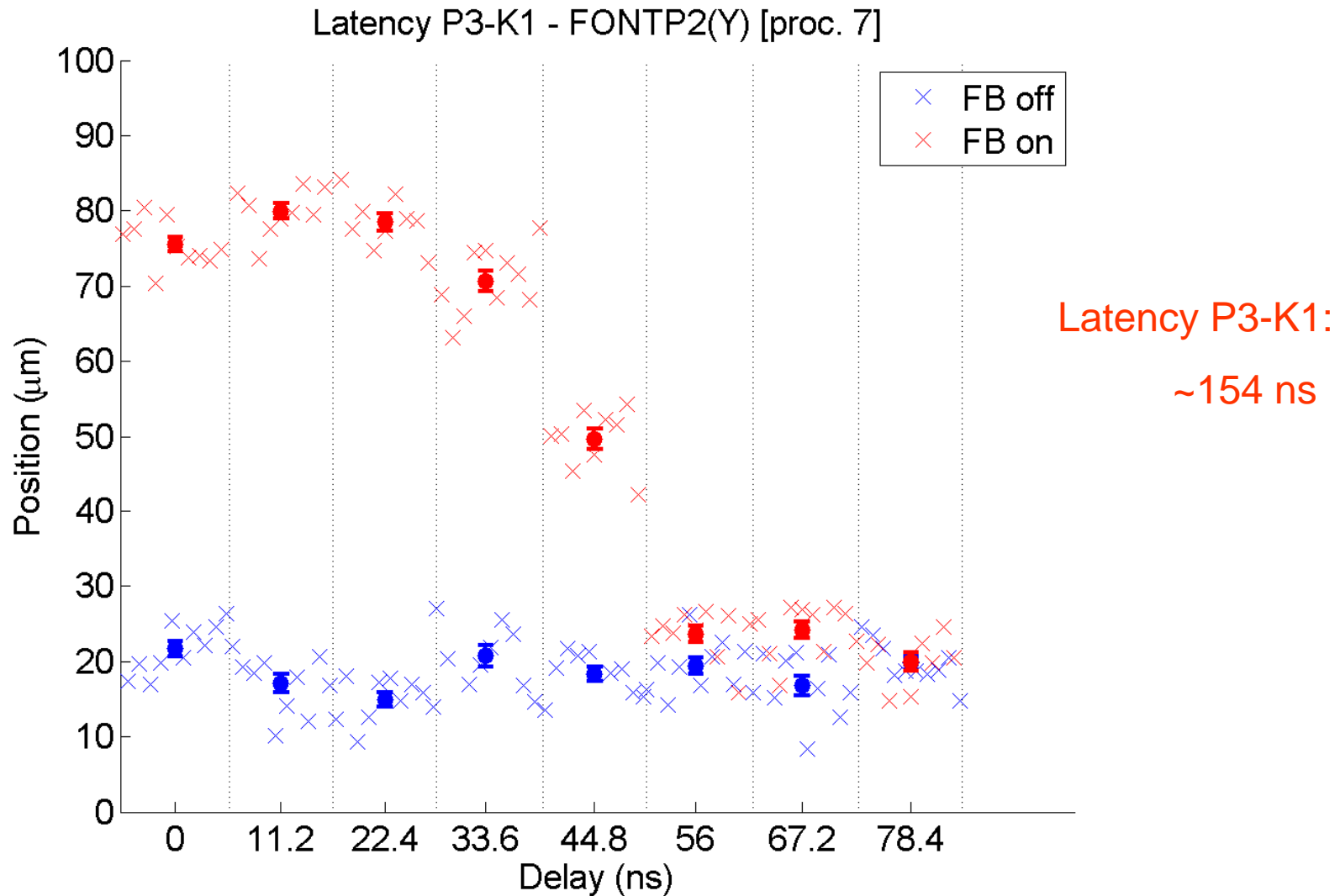
- Standard 3-BPM resolution method gives 'average' resolutions of 1 – 2 micron across 3-BPM system, however FB system performance in P2-K1 loop show ~300 nm.
 - Believe we were lucky with processor at P2, and that all processors have different resolutions due to different sensitivity to LO jitter
 - Largest effect due to path length imbalance to hybrid (unique for each processor) – larger residual from subtraction, more susceptible to LO jitter
 - All processors optimised, to be tested in Autumn
- Even if resolution 'perfect', system performance still determined by beam jitter conditions
 - Measured bunch-to-bunch correlations of >94% needed to make useful correction on ~3 micron beam jitter (50 % needed to break even)
 - Bunch 3 assumed to be on edge of ~310 ns EXT kicker pulse

Feedback examples (14 Dec 2011)

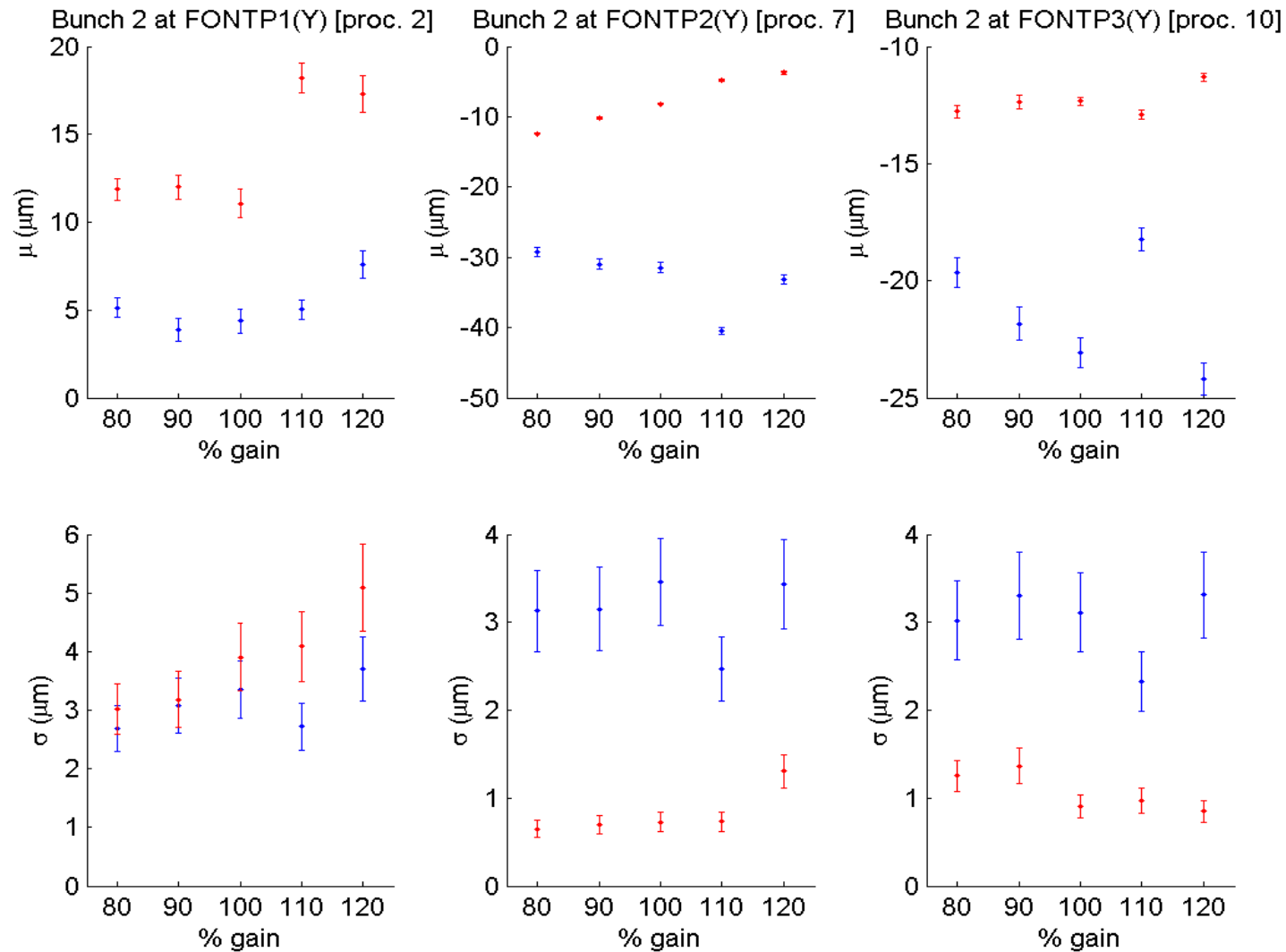
Run5_141211



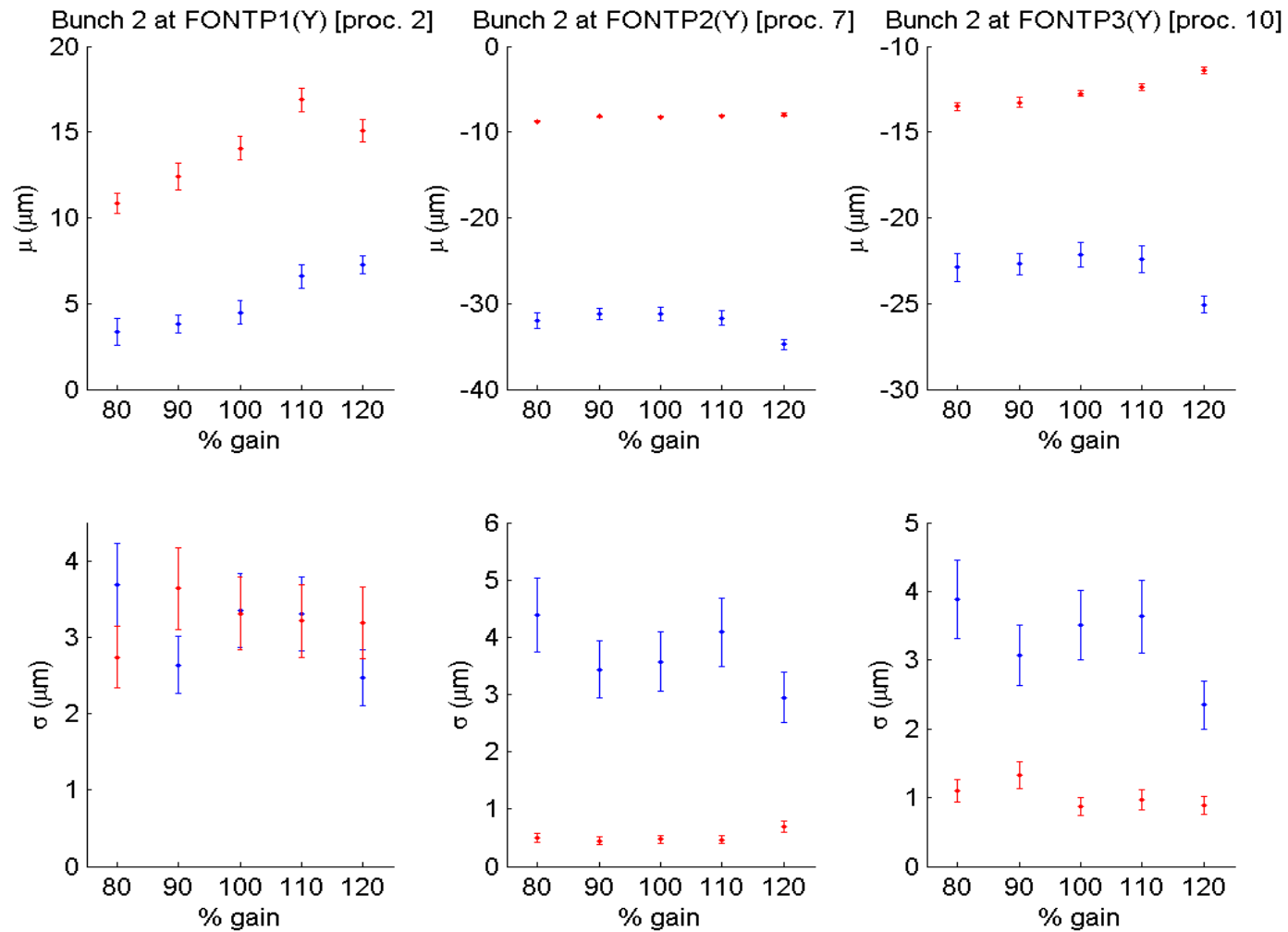
Latency (Dec 2011) – not-optimised



Kicker K1 gain scan (14/12/11)



Kicker K2 gain scan (14/12/11)



Dec 2011

Original residuals

(1000 pulse parasitic dataset 13/12/11)

