LLRF World Wide

LLRF Lecture Part 3.7

S. Simrock, Z. Geng

ITER / SLAC

Evolution of Hardware at SNS

1st Generation Control Chassis	2nd Generation Control Chassis	3rd Generation Field Control Module
		
MEBT Rebunchers	RFQ & DTL	CCL, SCL & HEBT
4 installed, 1 spare	7 installed, 3 spares	Retrofit to MEBT, RFQ & DTL
Retrofitted with FCM Nov 04	Retrofitted with FCM Jul 04	98 systems + spares

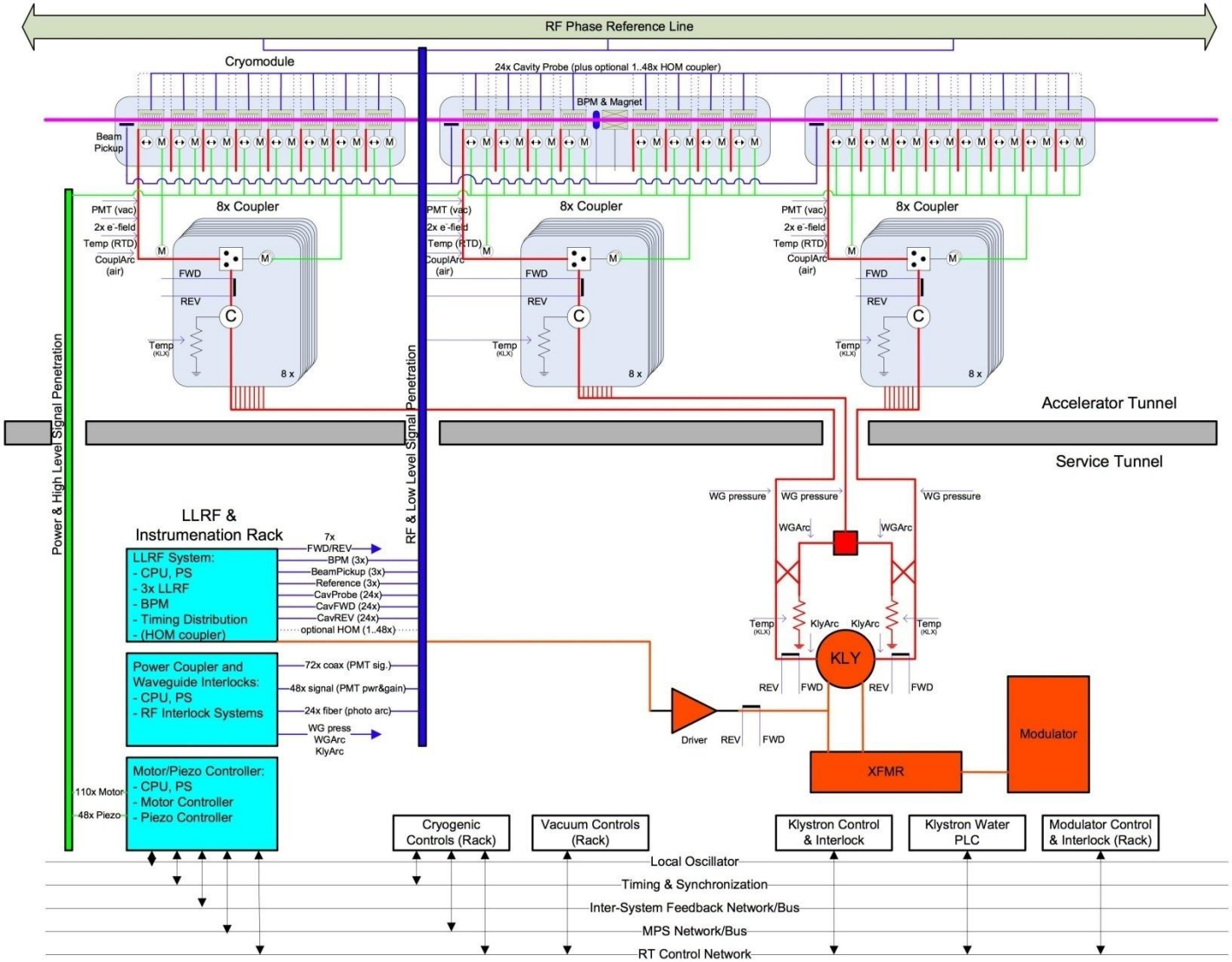
Evolutionary Development: build on proven concepts, hardware and software

October 10, 2005

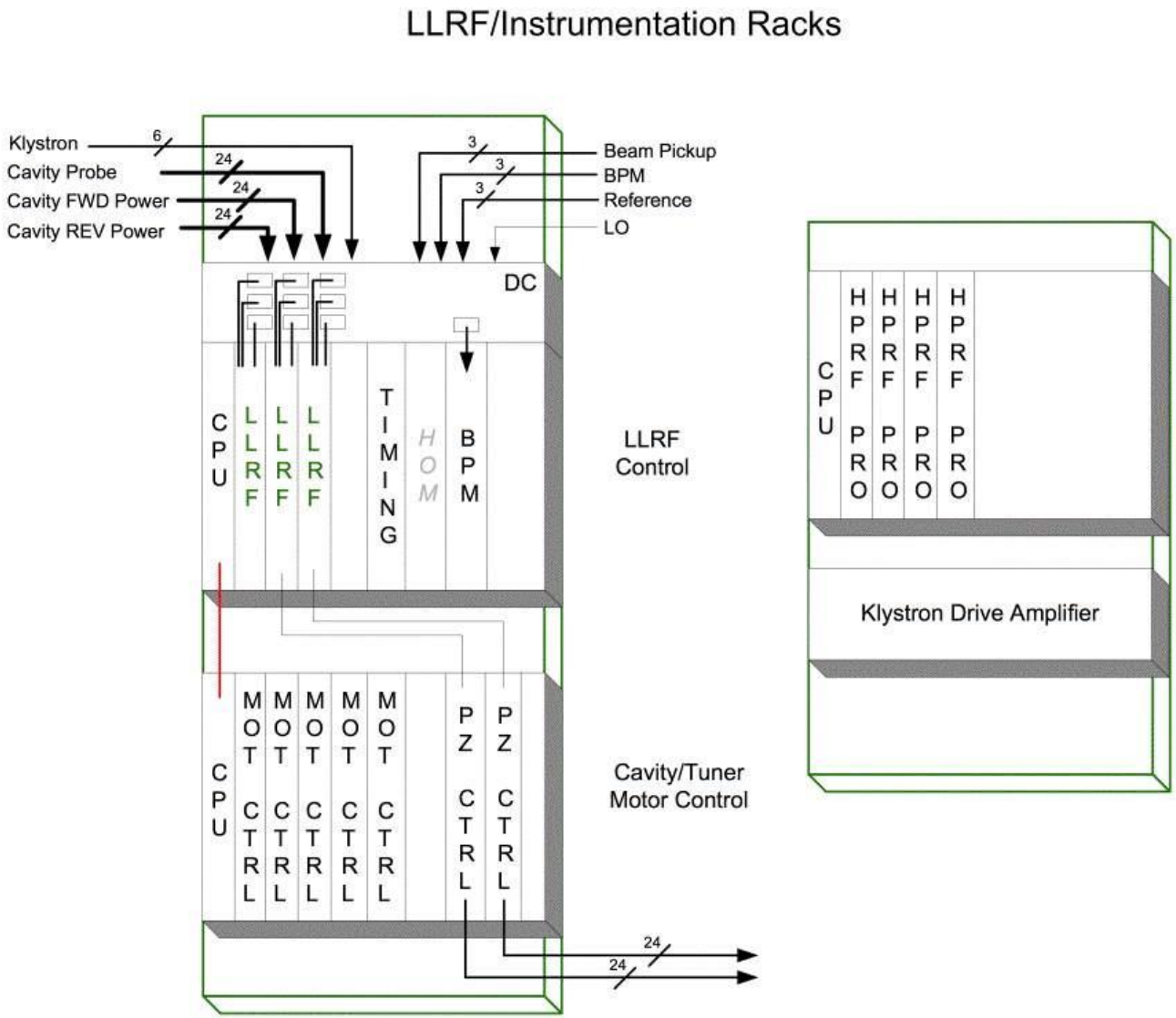
Lesson Learned at SNS

Advice for Hardware Development

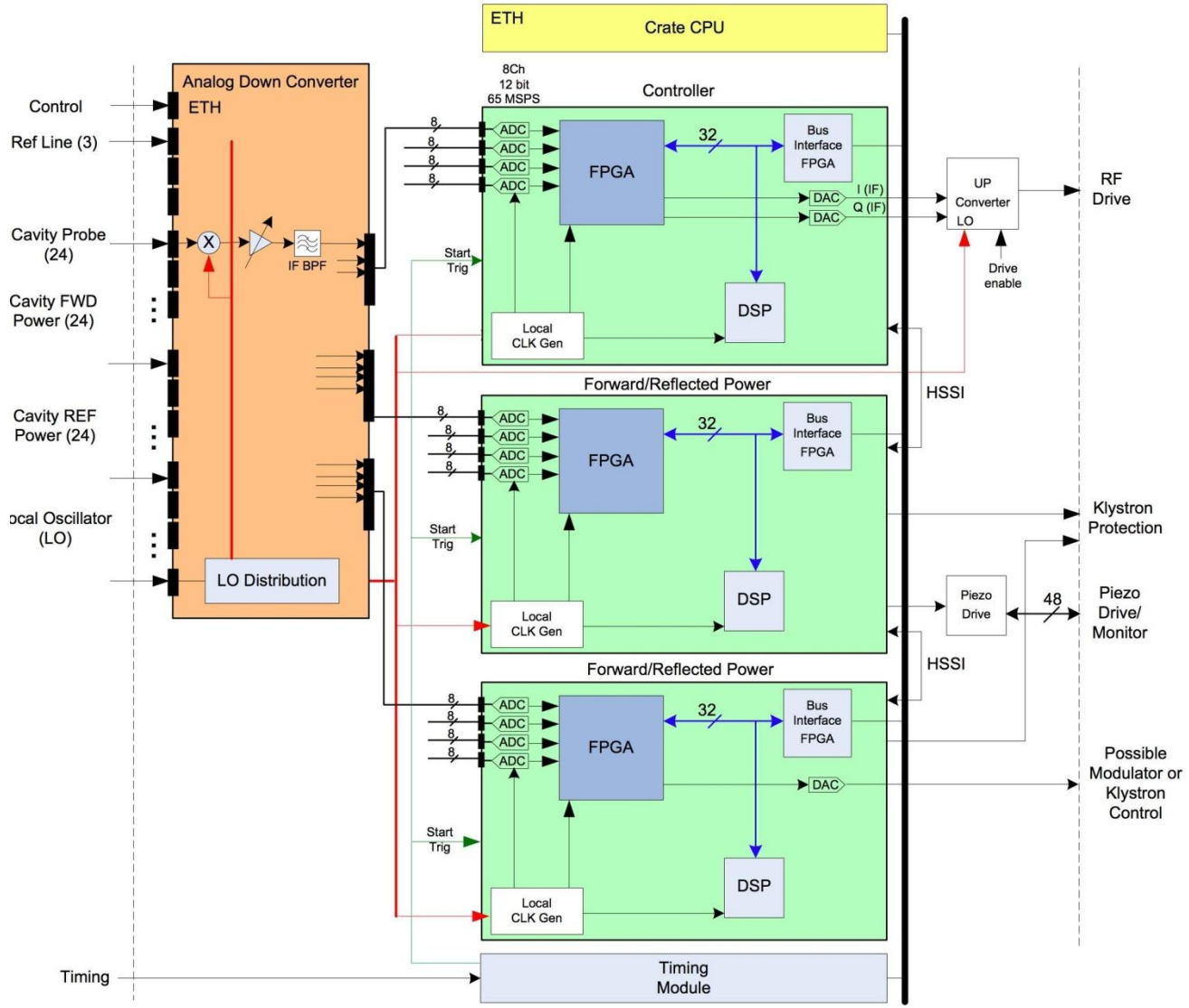
RF Station with 3 Cryomodules



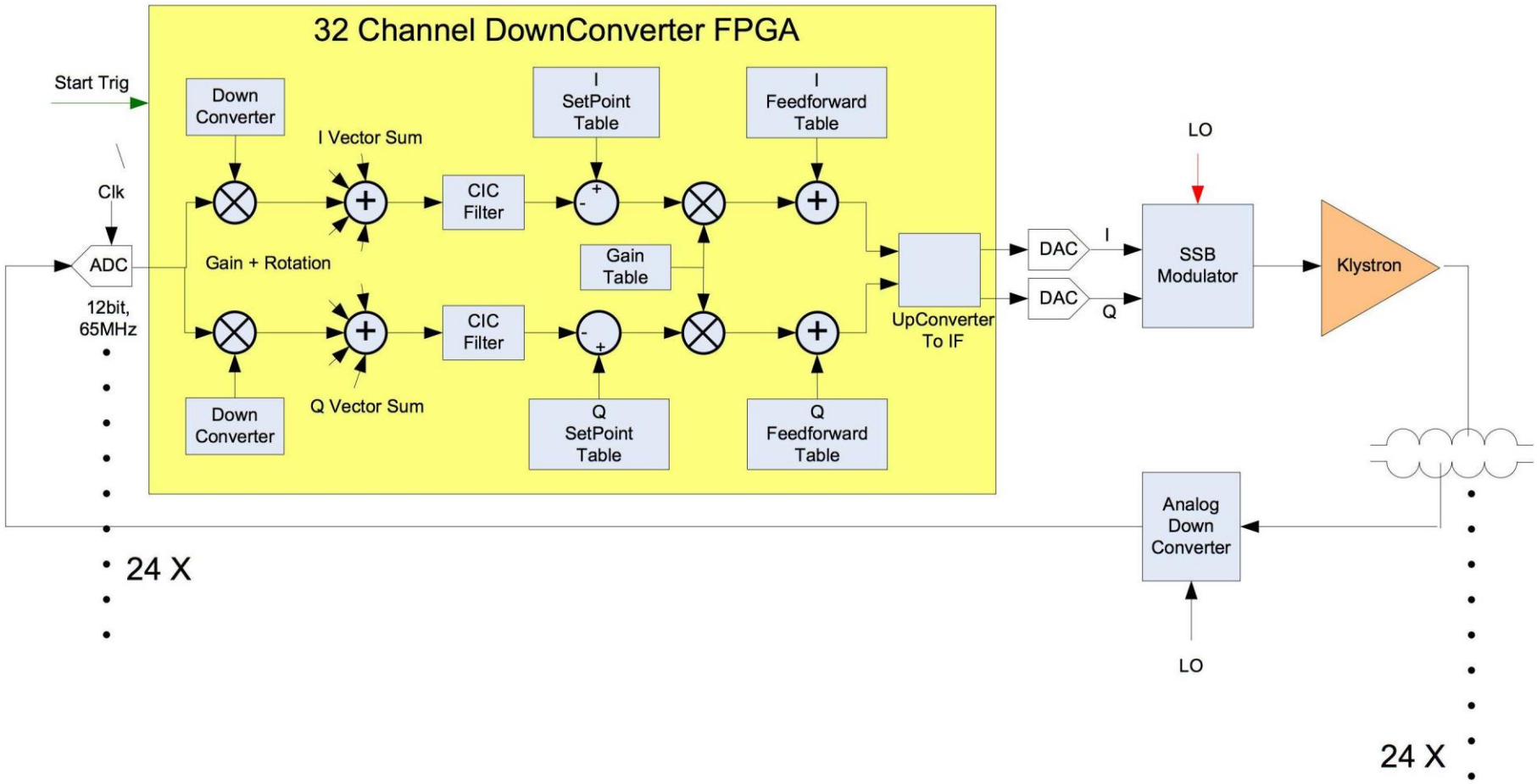
Rack Layout


LLRF/Instrumentation Racks
Klystron
Cavity Probe
Cavity FWD Power
Cavity REV Power
6
24
24
24
3
3
3
Beam Pickup
BPM
Reference
LO
DC
CPU
LLRF
LLRF
LLRF
TIMING
HOM
BPM
LLRF Control
CPU
MOT CTRL
MOT CTRL
MOT CTRL
MOT CTRL
MOT CTRL
PZ CTRL
PZ CTRL
Cavity/Tuner Motor Control
24
24
CPU
HPRF PRO
HPRF PRO
HPRF PRO
HPRF PRO
Klystron Drive Amplifier

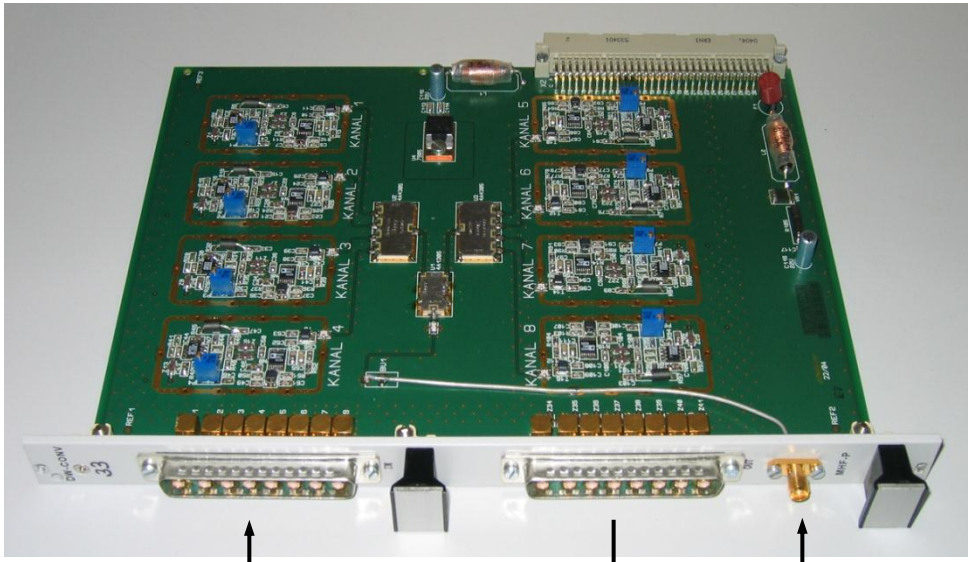
LLRF Rack Detail



LLRF Field Module Controller



Downconverter

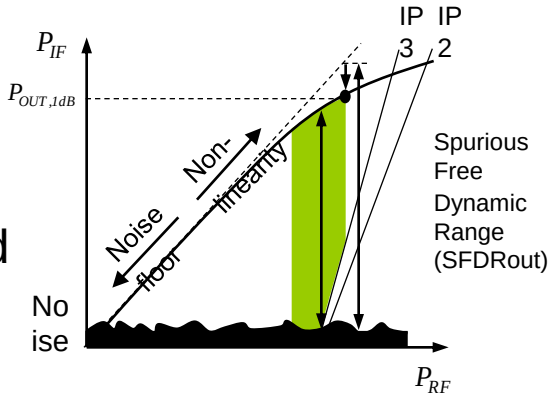


8-channels from cavity probe :

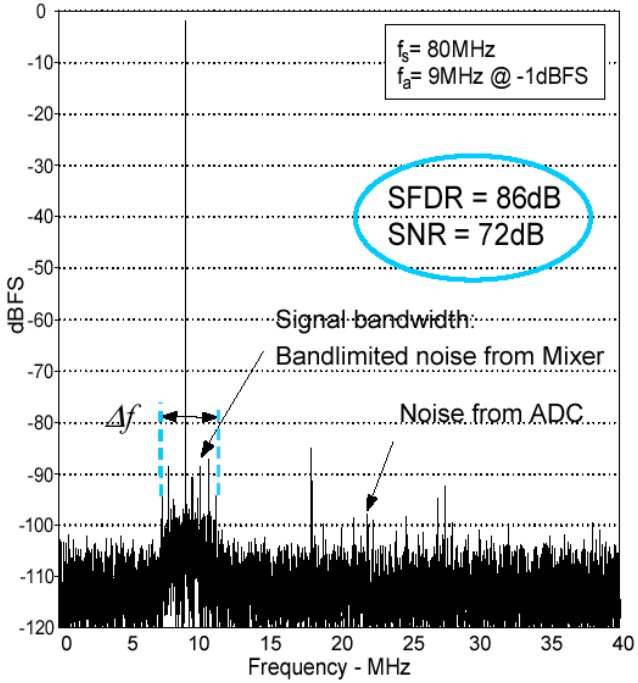
8-channels to ADC-Board :

LO-Input :

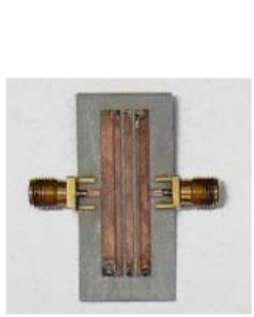
Compromise between noise and linearity

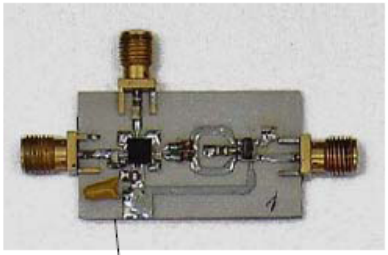


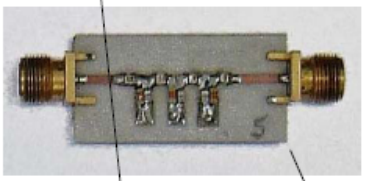
- **SNR for oversampling :**

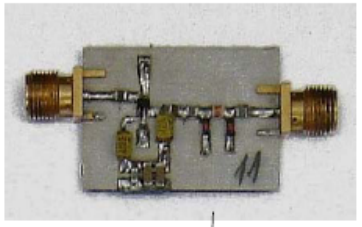


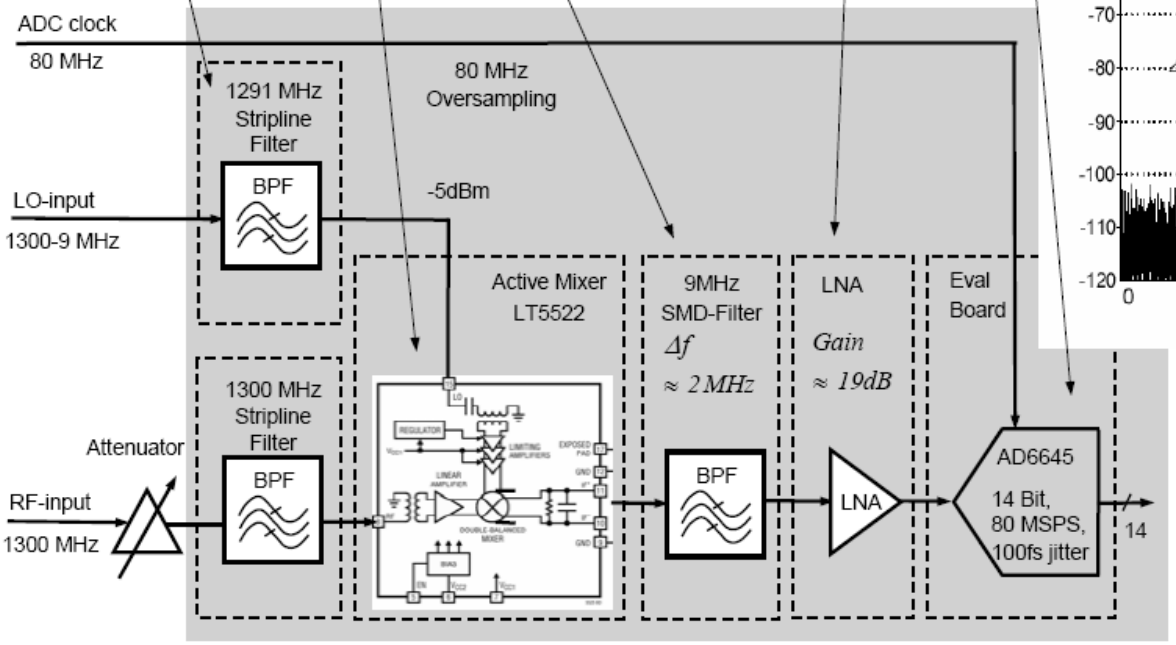
Gilbert Cell Mixer



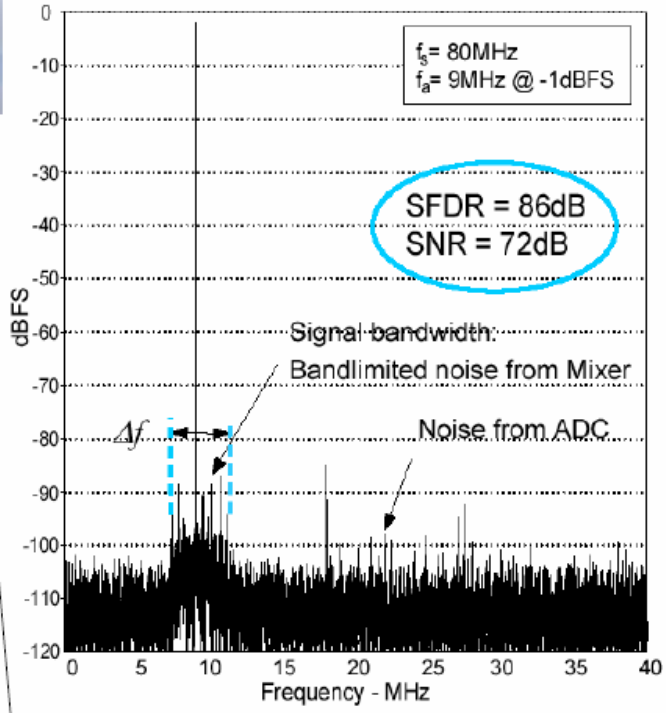








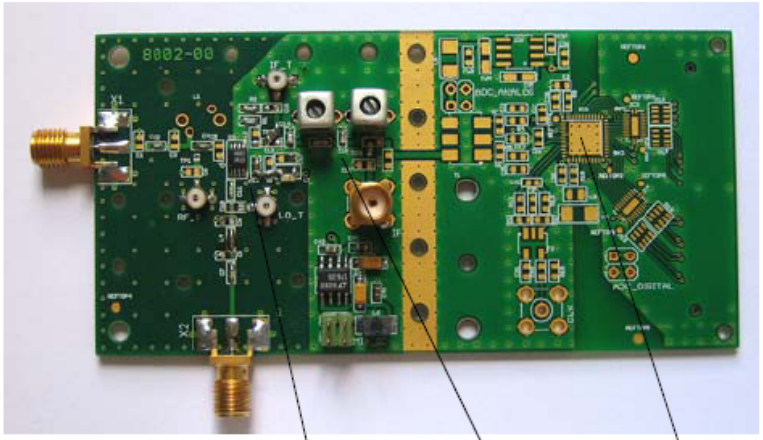
- **SNR for oversampling :**

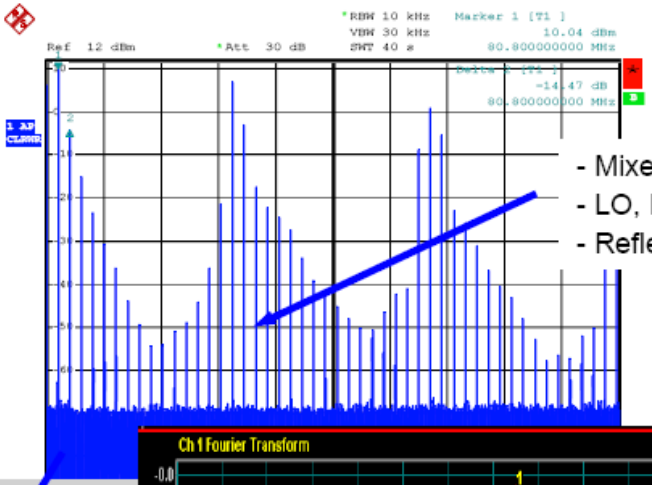


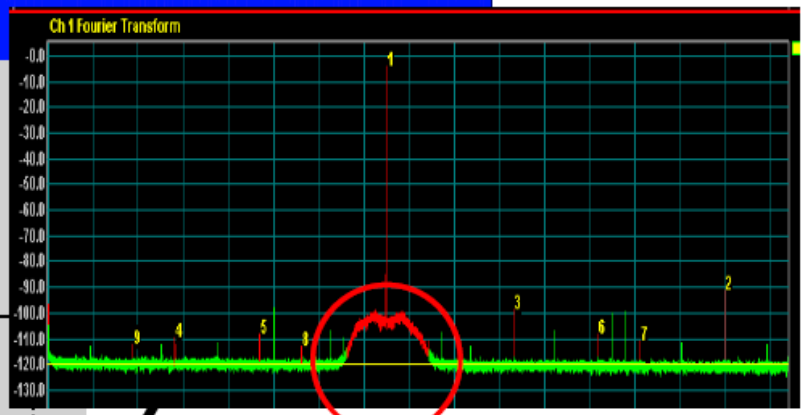
SNR is limited to 72dB by the NF of the front end mixer.

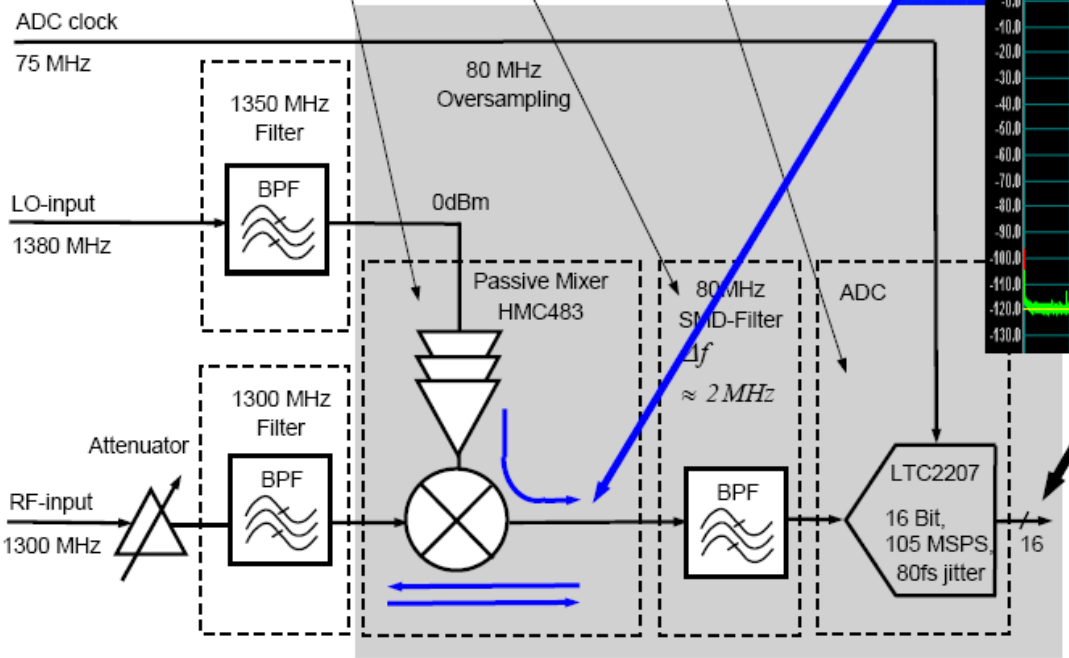
(SNR of about 70dB from JLAB using HMJ mixers.)

Passive Mixer





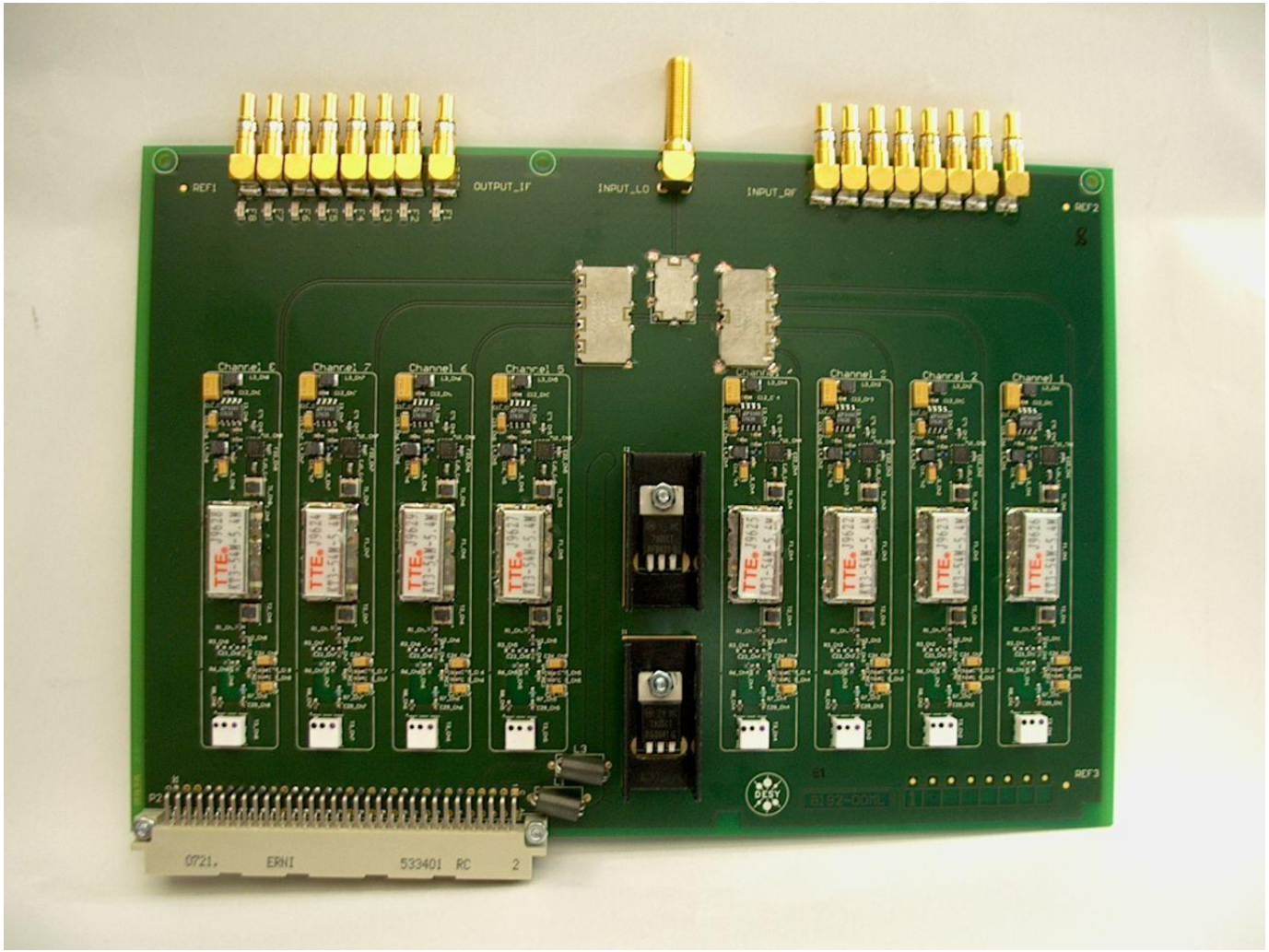




- SNR of 73dB is limited by the reference signal generation of RF and LO.

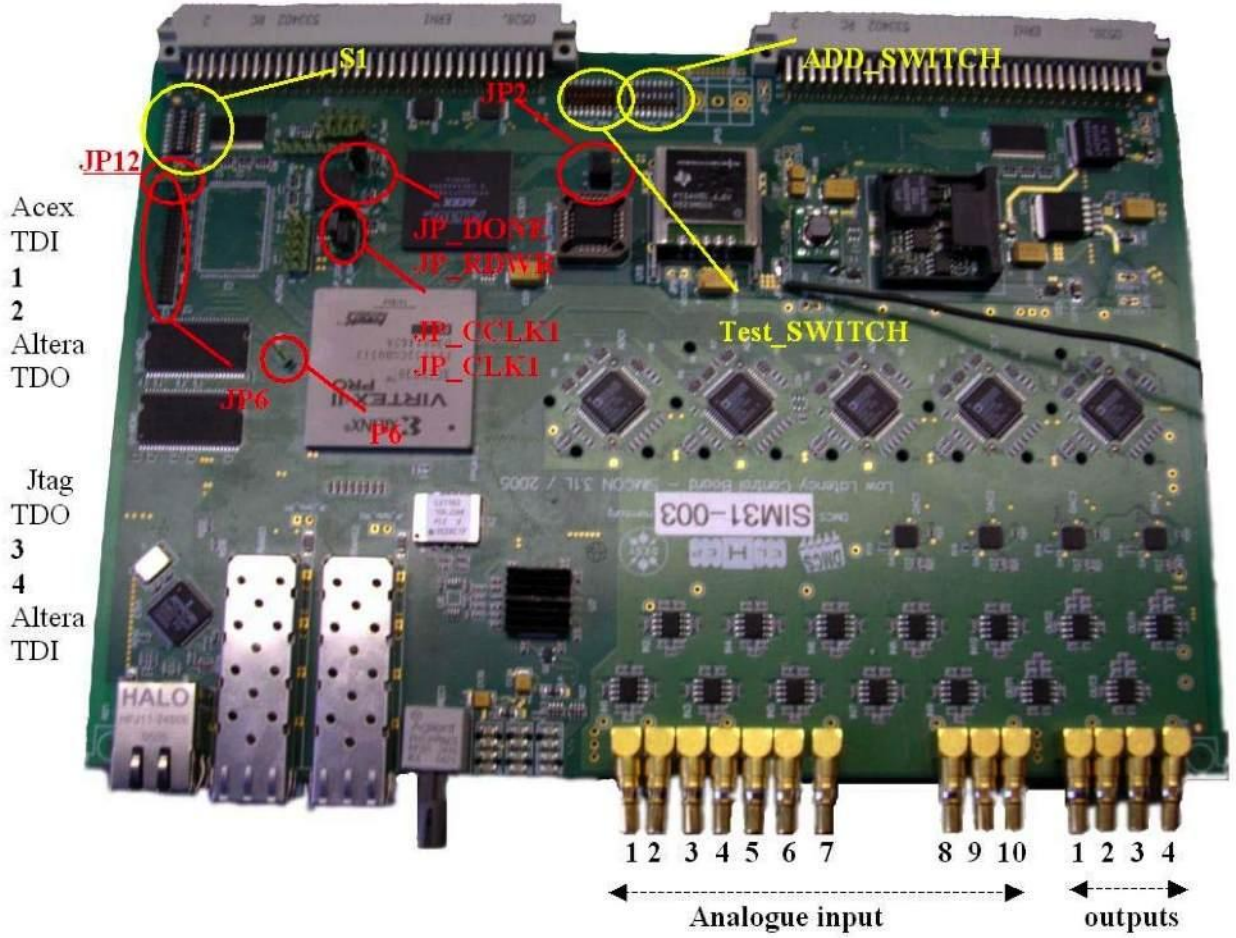
- Test setup with fs resolution.
- Diplexer design to reduce distortions.

8-channel downconverter



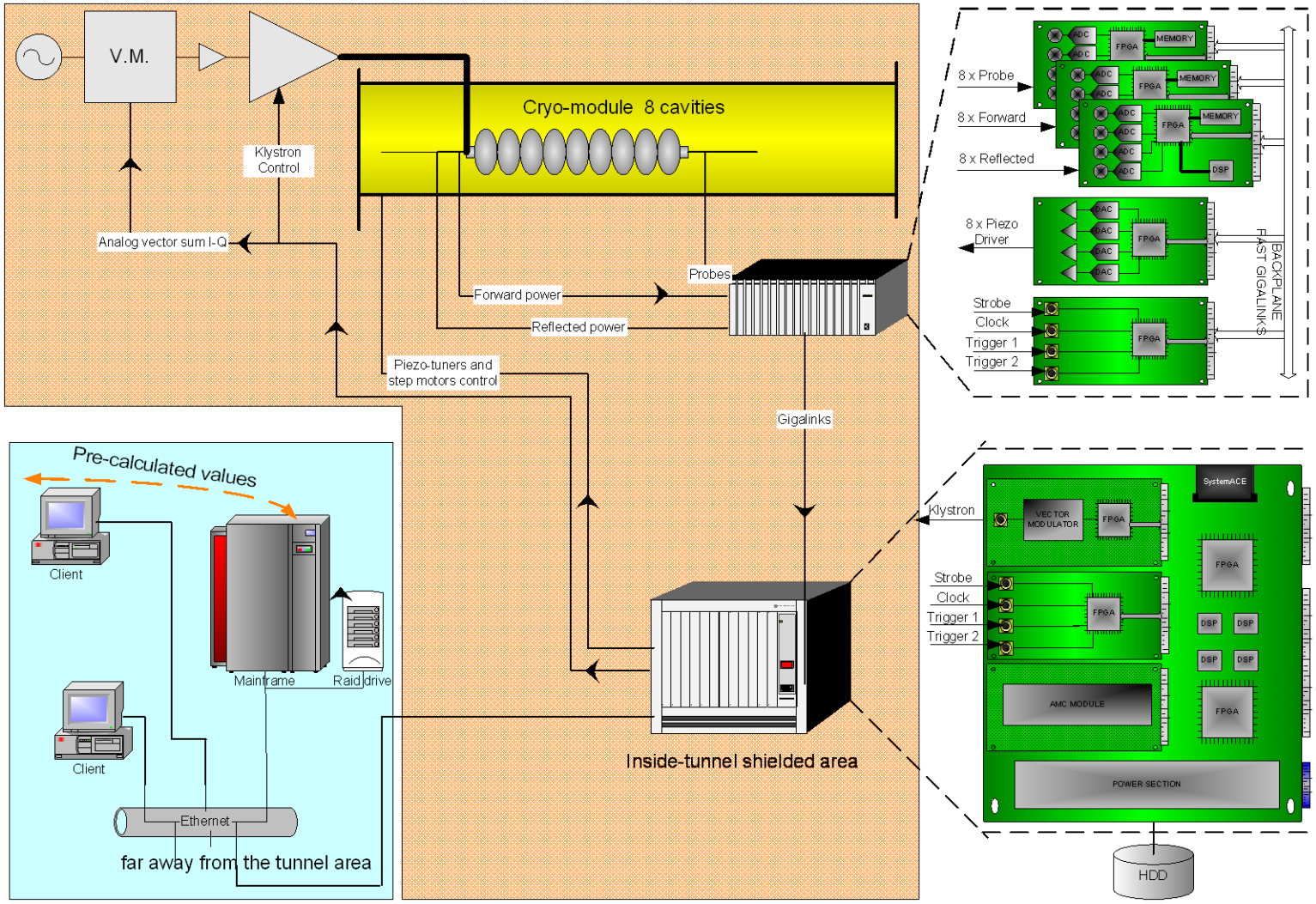
DESY SIMCON 3.1 Controller

2.SIMCON3.1 board description and schematics.

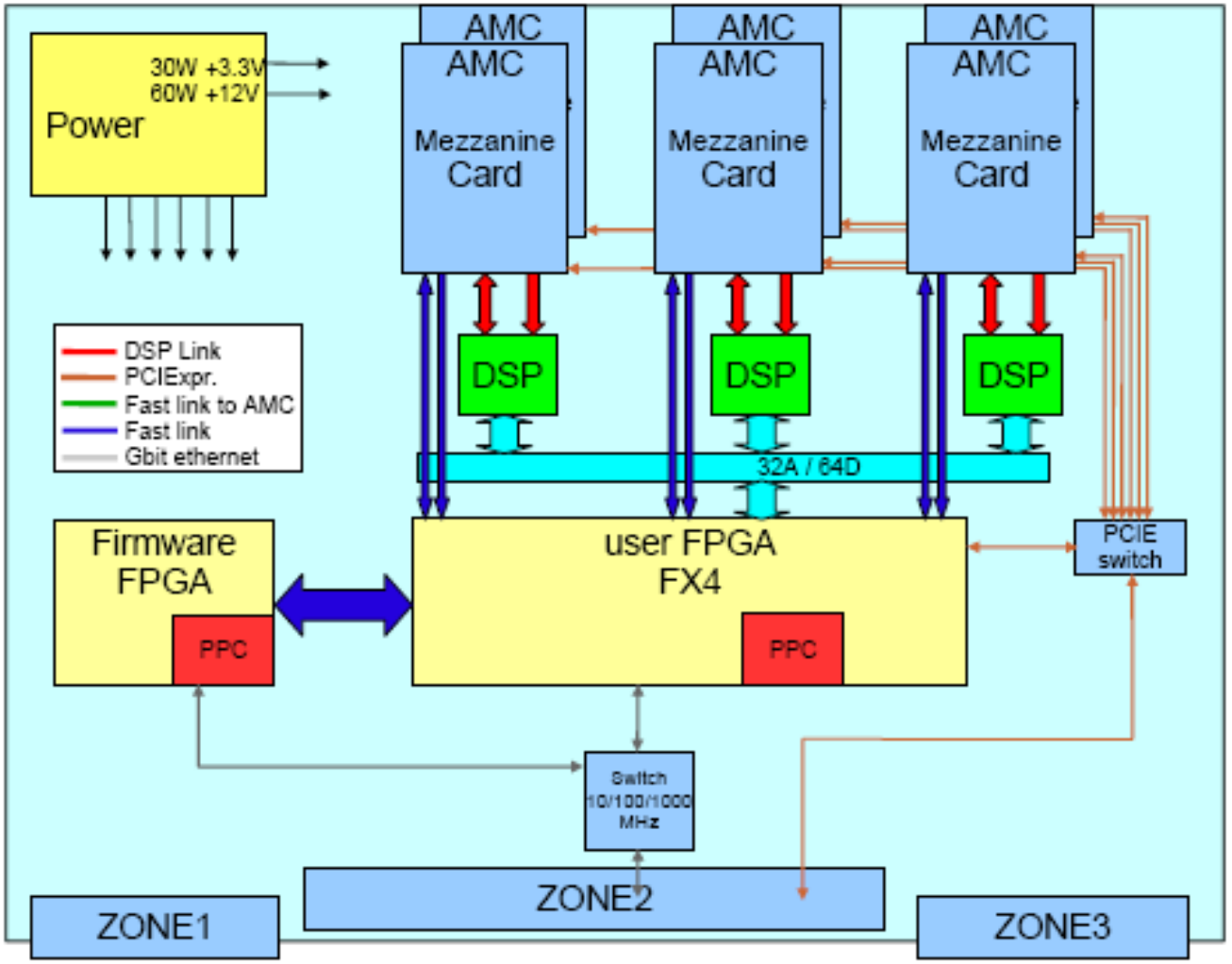


Next generation: SIMCON DSP

Next generation: ATCA

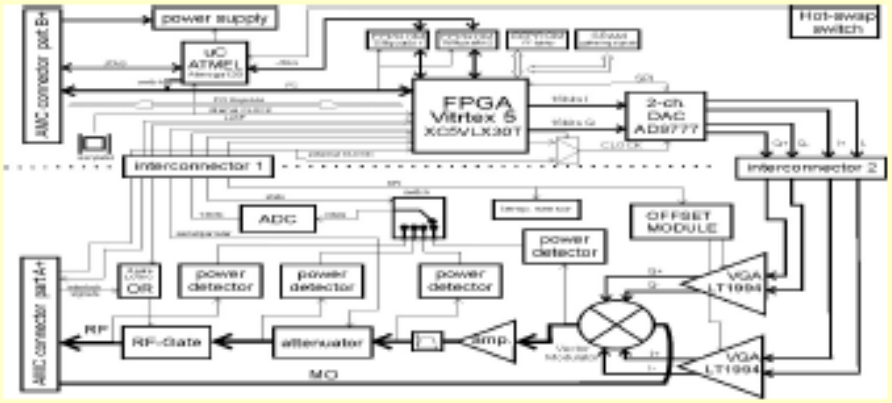


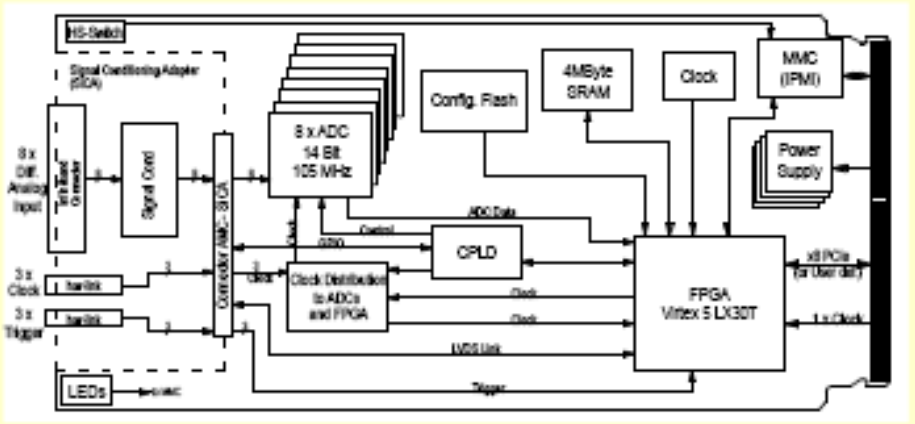
Architecture of Carrier Board



AMC Modules

- ***All modules:***
  - IPMI v. 1.5
  - PCIExpress
  - Fast link to the carrier (10 differential pairs)
  - Virtex 5
- ***8 channels "slow" ADC board***
  - 14 bits
  - BW 200 MHz
  - SF ext. & int. up 105 MHz
- ***2 channels. "fast" ADC board***
  - BW 1 GHz
  - 10 bits
  - SF 1-2.5 GHz
- ***Timing Module***
  - Receive coded clock signal, produces 6 different clocks
- ***Vector Modulator***
  - Digital input
  - 1.3 GHz, 0dBm





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[2] A. Regan et al., "The SNS Linac RF Control System", Proceedings of the 2002 Linac Conference, Gyeongju, Korea

[3] M. Champion et al , "The Spallation Neutron Source Accelerator Low Level RF Control System", Proceedings of the 2003 Particle Accelerator Conference, Portland

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