Status of the 2nd generation AHCAL prototype

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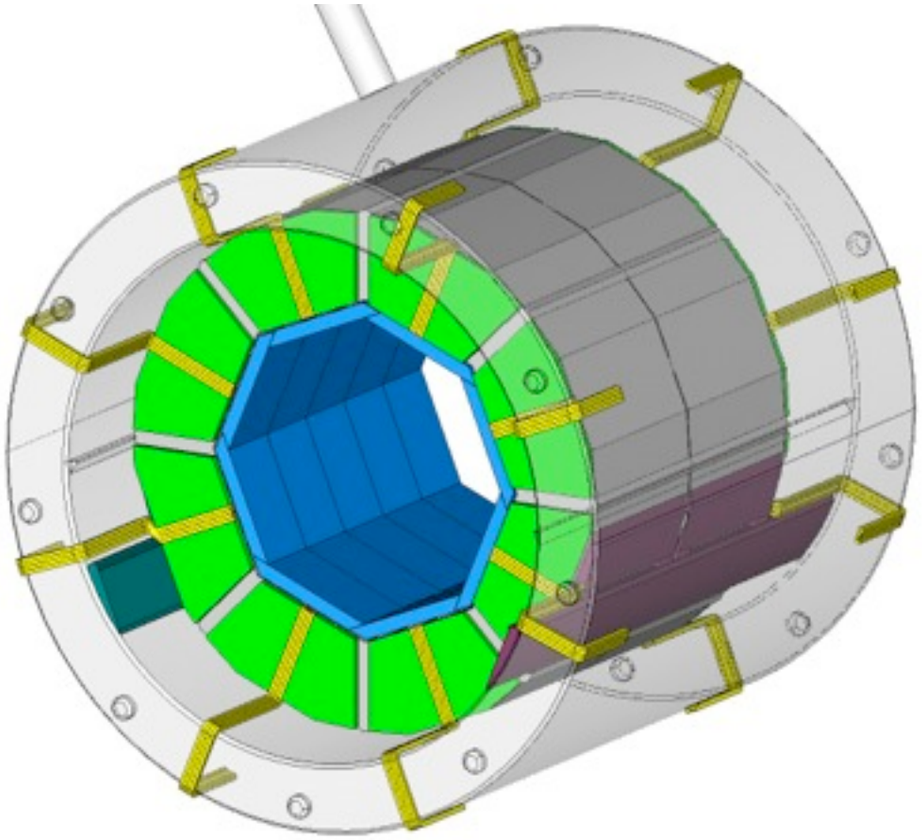
CALICE meeting - Cambridge

Outline

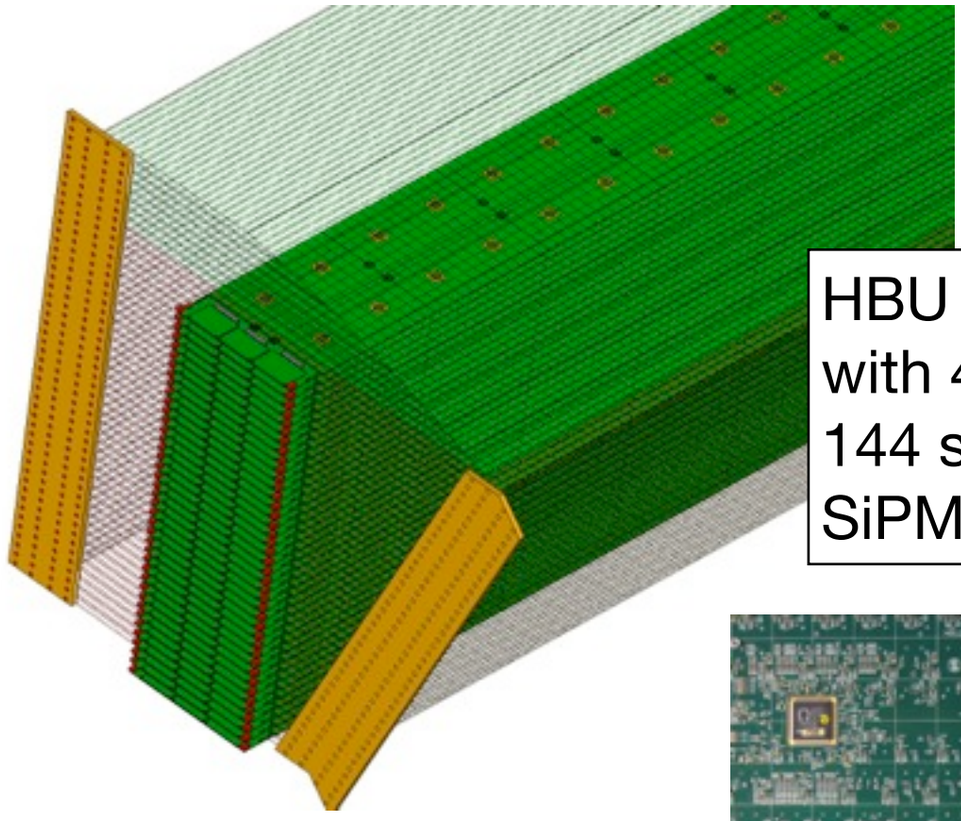
- General concept of the AHCAL
- Signal detection
    - Tiles with SiPM readout
    - Readout electronics
- Testbeam status

The engineering AHCAL prototype

Development of a **scalable LC detector** based on successful experience with physics prototype



octagonal shapes,
16 equivalent wedges,
segmented in two along z



HBU (HCAL Base Unit)
with 4 ASICs,
144 scintillator tiles,
SiPM readout

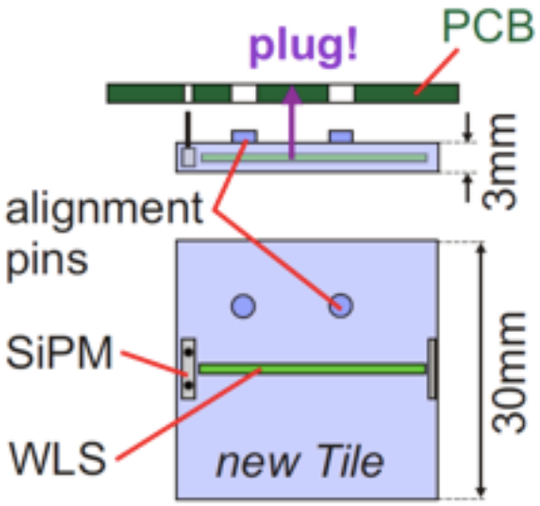
Challenges:

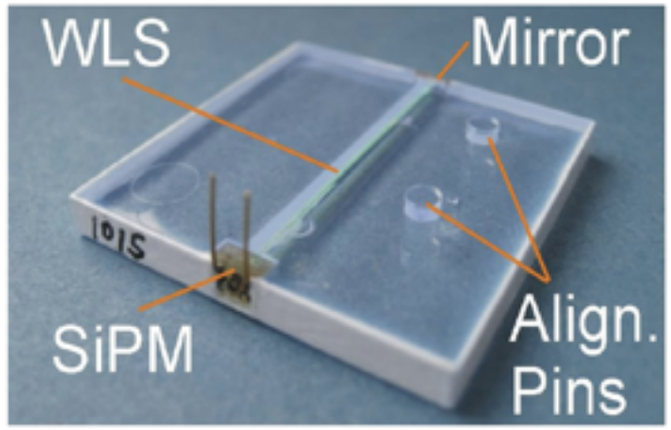
- No spacer between layers
- Minimize dead material between wedges
- Minimize gap between barrel and endcap

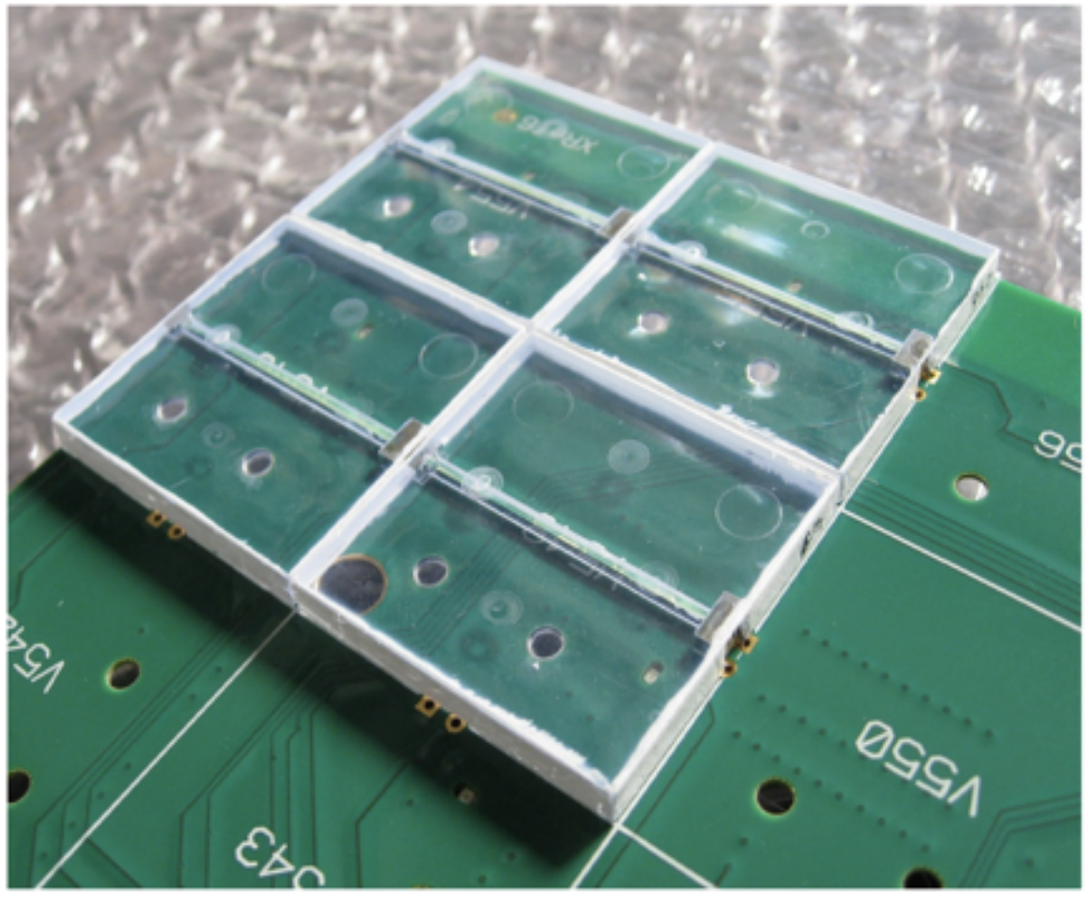
→ **Integrated readout electronics**

Scintillating tiles

- Signal sampled by scintillating tiles
- 3 x 3 x 0.3 cm^3, 2592 tiles per layer
- 576 tiles mounted below 4 new HBU2:
  - 3 HBUs equipped with tiles from newest batch
  - 1 HBU equipped with tiles from previous batch (slightly lower bias voltage, lower gain)
- Gain: 500k - 3000k
- Light yield = 15±2 Pixel/MIP







The readout chip - SPIROC2b

Specific chip for SiPM readout

- Input DAC for channel-wise bias adjustment (36 channels)

Designed for ILC operation:

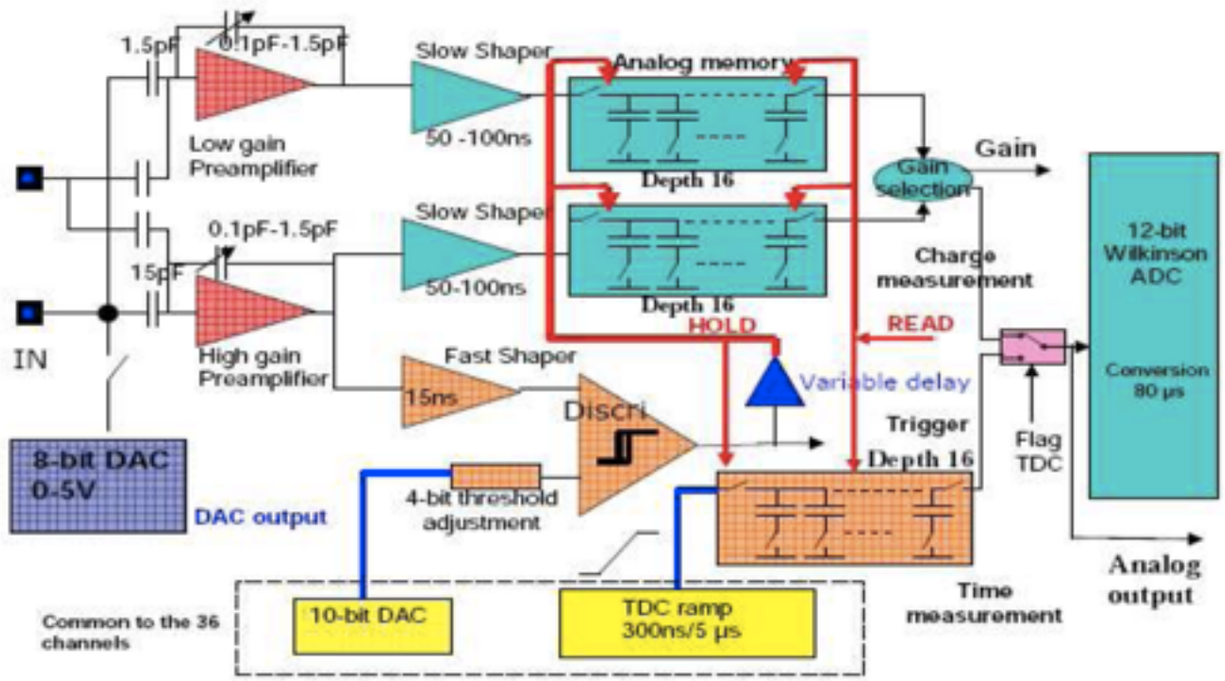
- Power pulsing 25 µW/ch
- Dual gain setup per channel

→ high gain/low gain ~10

- Auto-trigger mode (12-bit TDC)

→ channel-wise adjustable threshold

- Many aspects have already been tested and discussed and all issues will be fixed in **SPIROC2c**
  - Tests are still ongoing
  - But at the moment SPIROC2b is our working horse

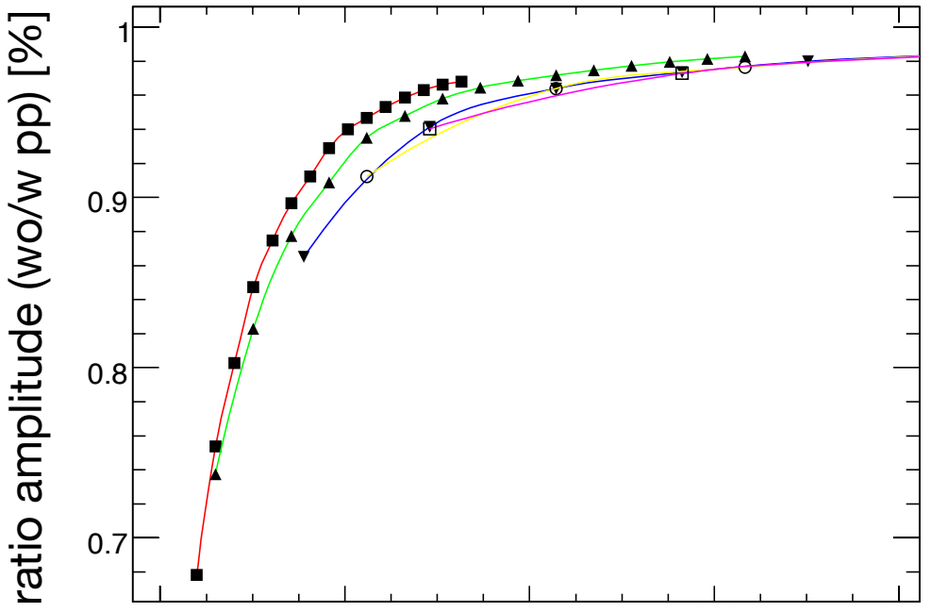


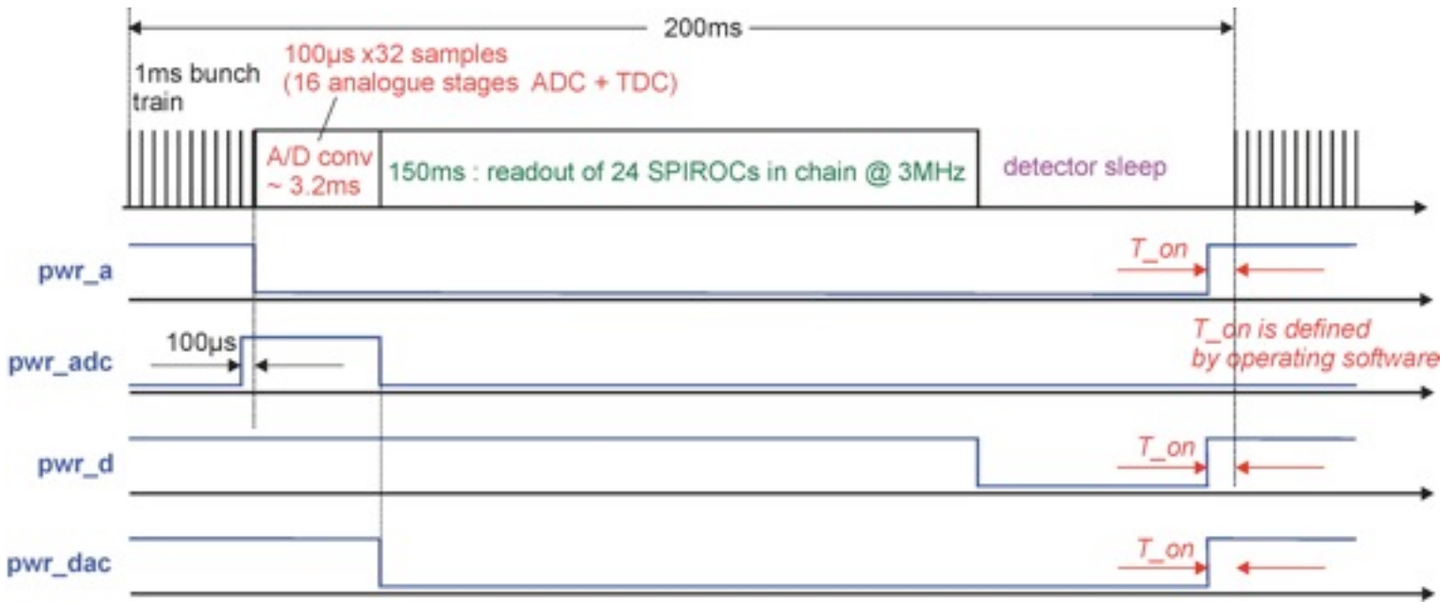
Power pulsing

- Necessary to avoid an extra cooling system

  → heat production limited to 40 µW/ch
- Electronics switched off between the bunch trains
- **Comparison w/wo power pulsing (pp):**
  With pp: reduced amplitude, depending on switch-on time (250 µs for 95% efficiency) (right slide)
- **Power consumption:** ~190 µW/ch (SPIROC2b + HBU2)

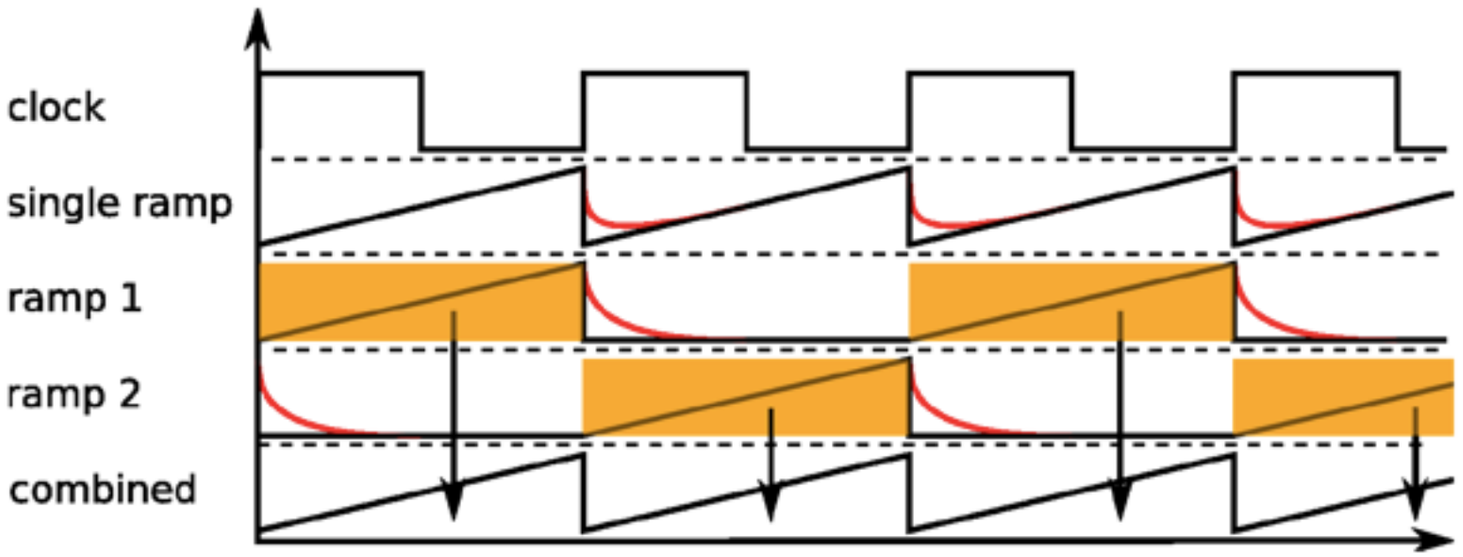
Improvement in SPIROC2c has to be checked!



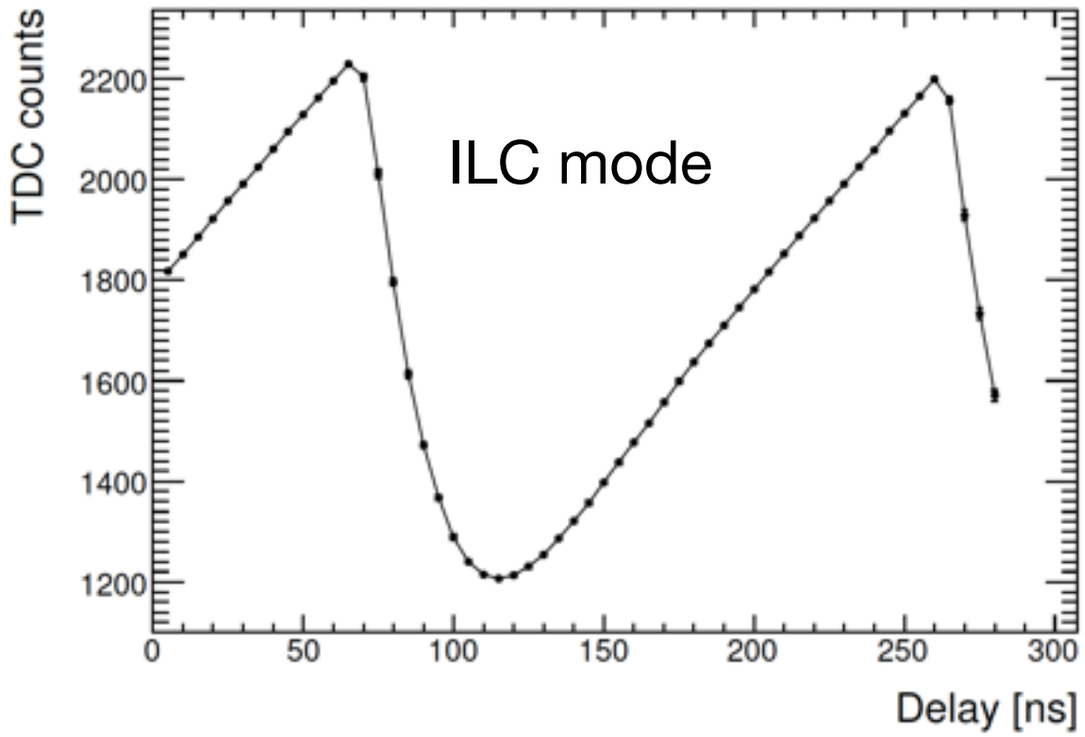


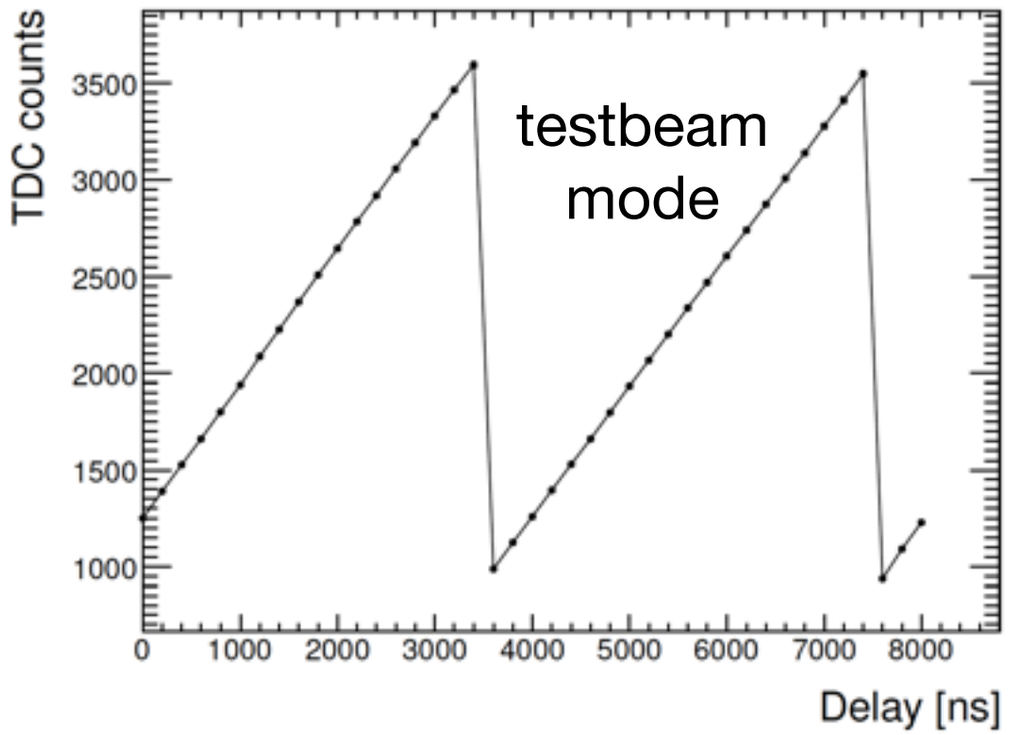
TDC time measurement

- SPIROC2b measures time in auto-trigger mode relative to bunch clock
- Dual TDC ramp in SPIROC switched by a multiplexer to reduce dead time due to ramp reset
- ILC mode = 200 ns ramp, testbeam mode = 5 µs ramp (less dead time) on the new HBU2



TDC time measurement

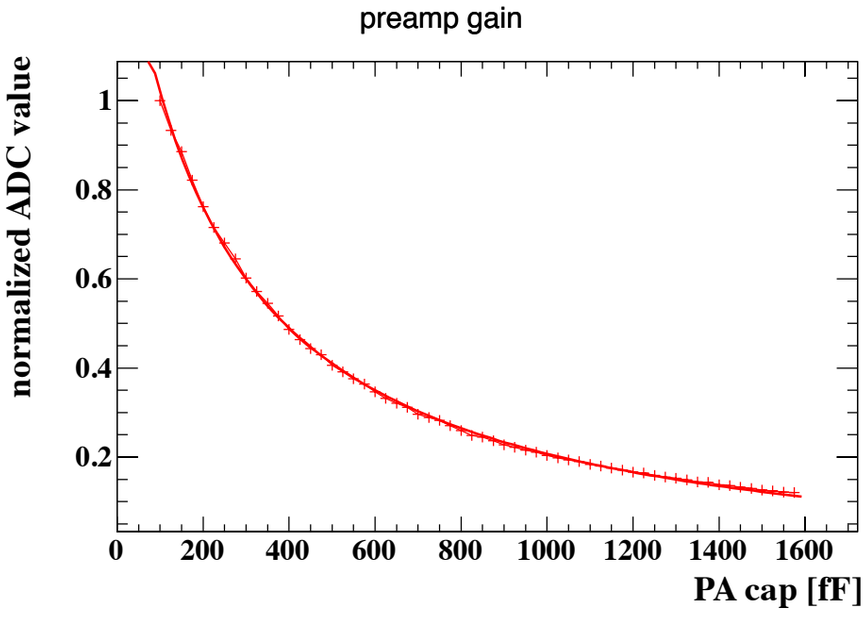


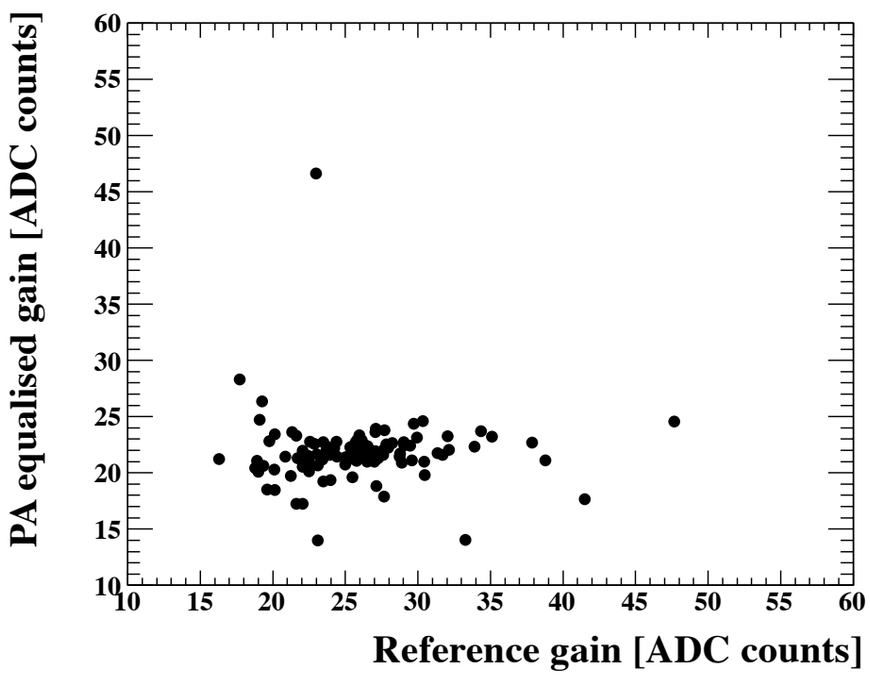


- ILC mode:
  - Resolution: ~100-250 ps
  - TDC measurement doesn't give reliable time information during ~30% of the time (dead time for TDC measurement, ADC information can be used)
- Testbeam mode:
  - Resolution: ~1-1.5 ns
  - Fraction of dead time much smaller

Channel gain equalization

- Idea: equalize MIP response by adjusting preamp gain per channel
  - Sorting tiles to HBUs by similar operating voltage
  - Setting proper operating voltage for all channels
  - Original gain measured with SPS (LED system)
  - Electronics gain dependence on preamplifier capacitance measured for each channel
  - Preamplifier capacitance adjusted for each channel
  - Preamplifier setting verified for each channel with SPS
- With this procedure just one global threshold without channel-wise adjustment is needed



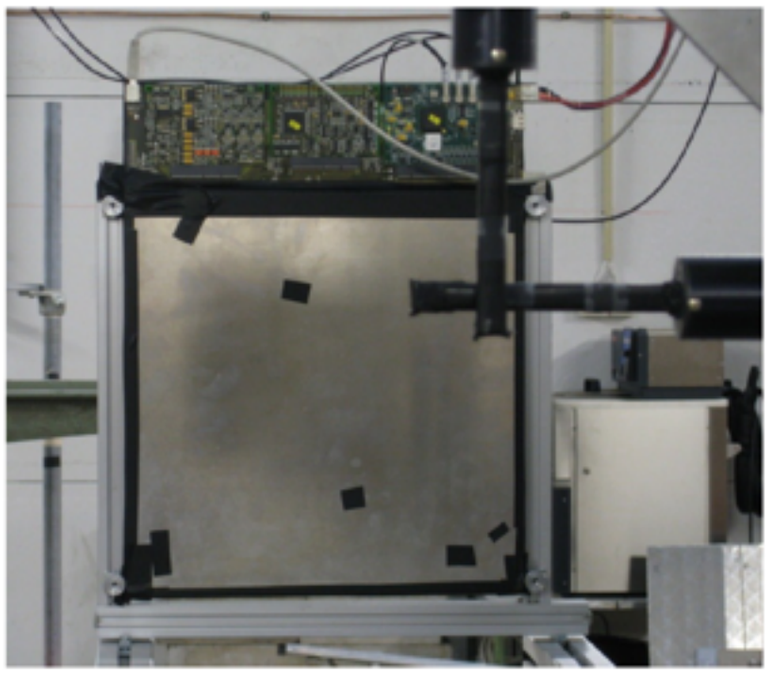


→ Original **gain spread** of about a factor 6 can be compensated to 5-10%

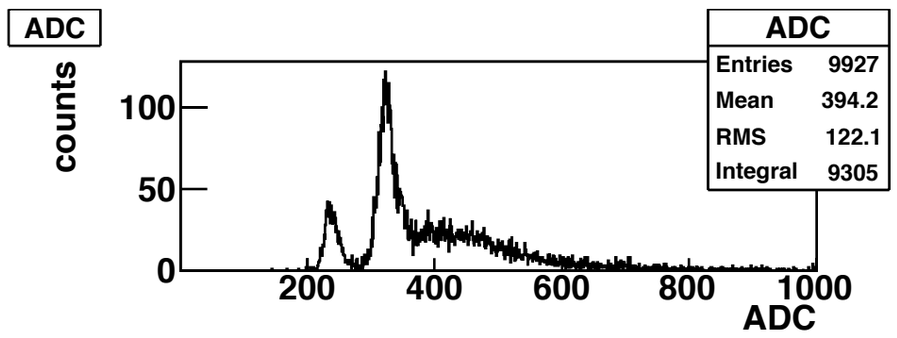
DESY testbeam

- Verify gain equalization by measuring a MIP signal in all tiles (3 GeV electron beam)
- Measure the MIP response in each channel in auto trigger mode

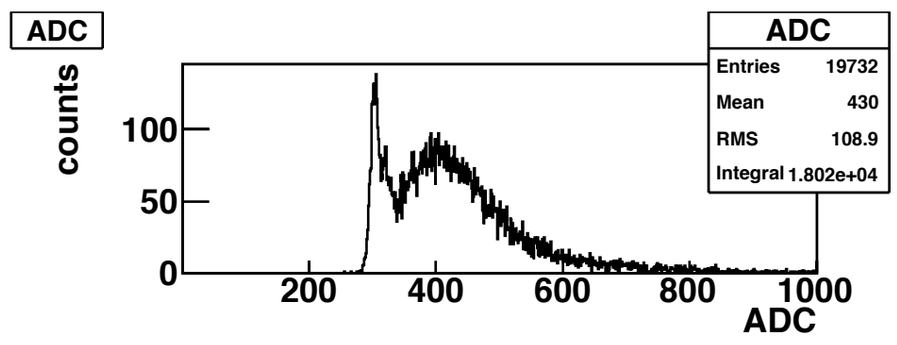
→ In progress for all 4 HBUs



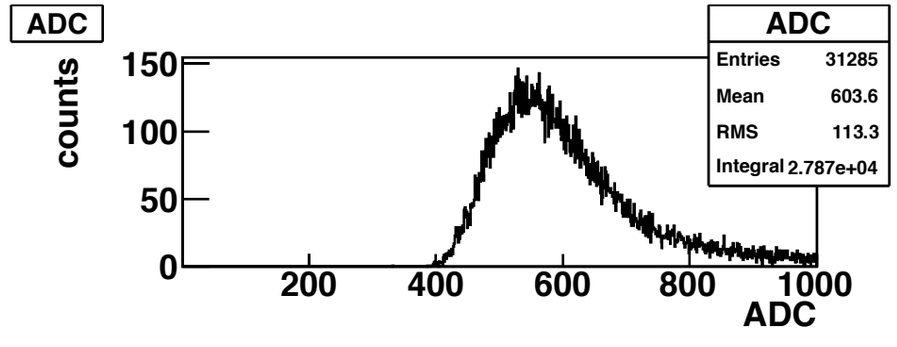
All HBUs and chips are working fine!



too low threshold



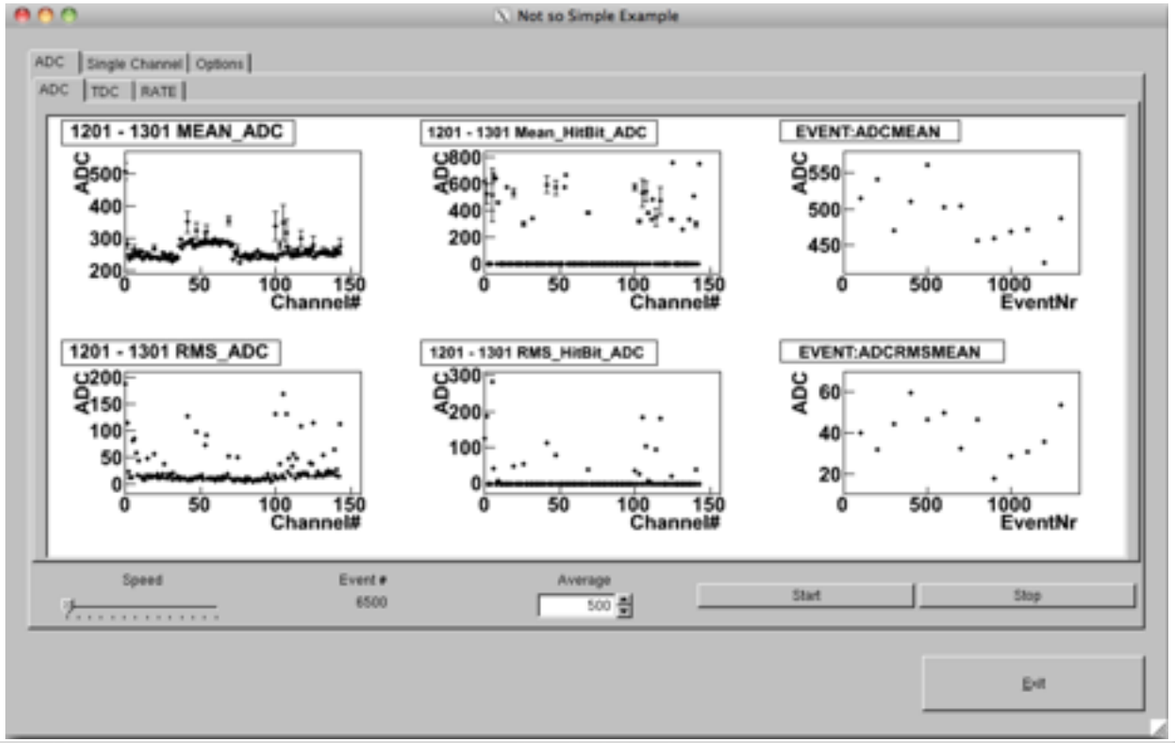
good threshold

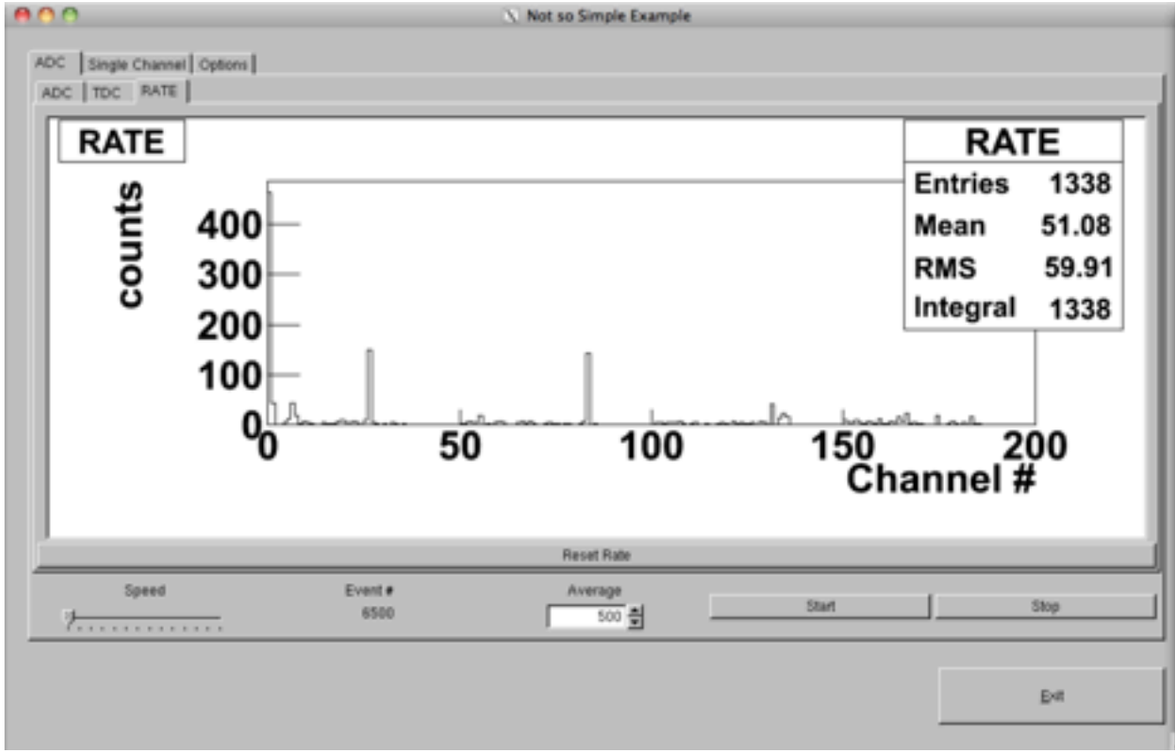


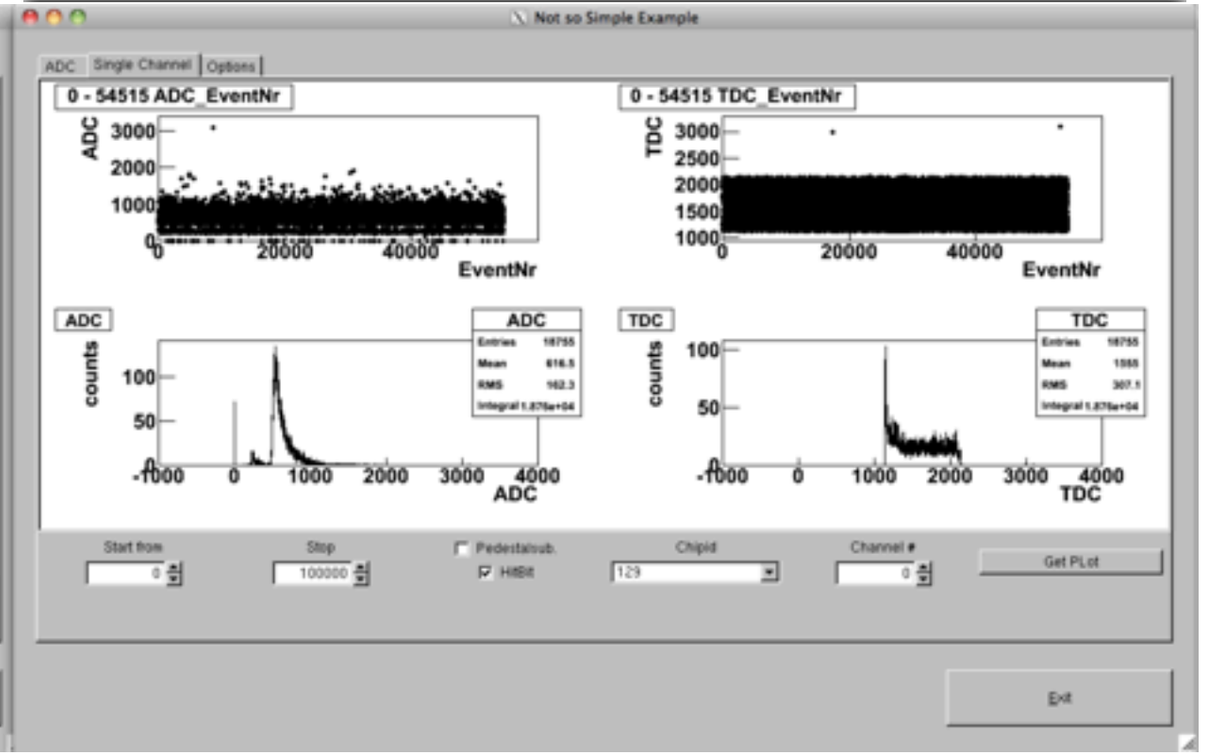
too high threshold

DESY testbeam

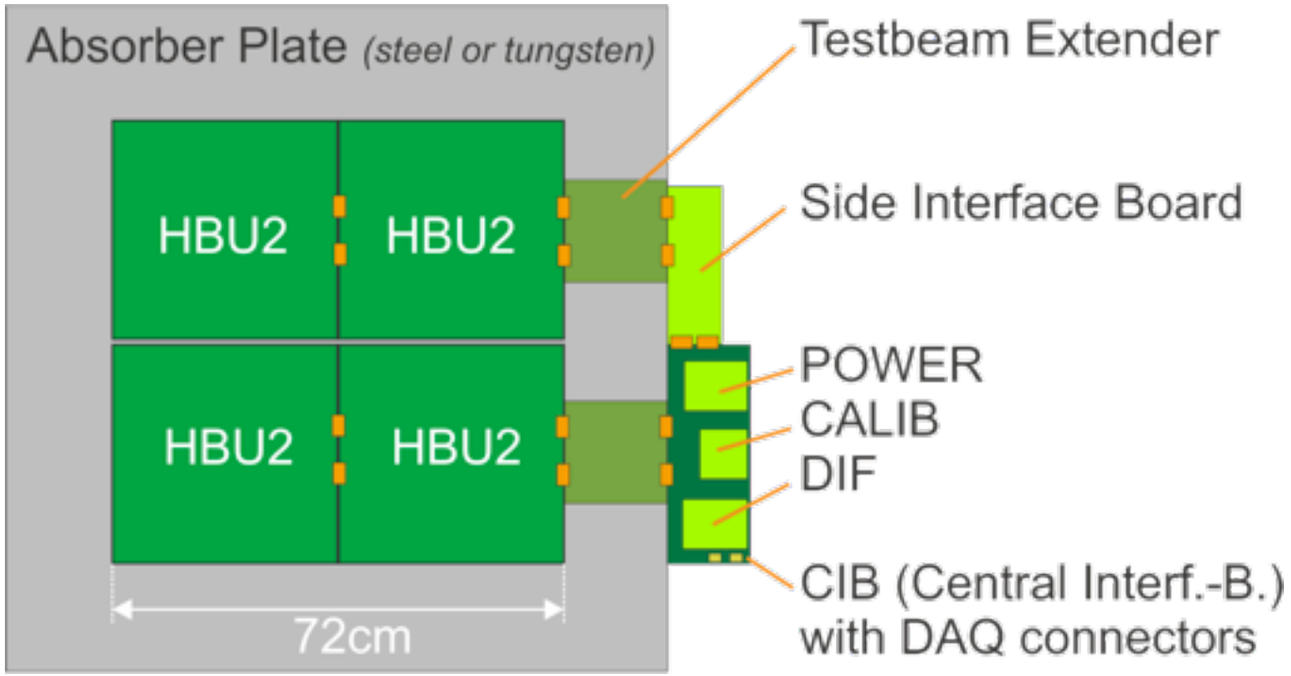
- New online monitor
  - Flexible to be used with single or multiple HBUs
  - Standard functionality used now, more histograms in development for CERN testbeam

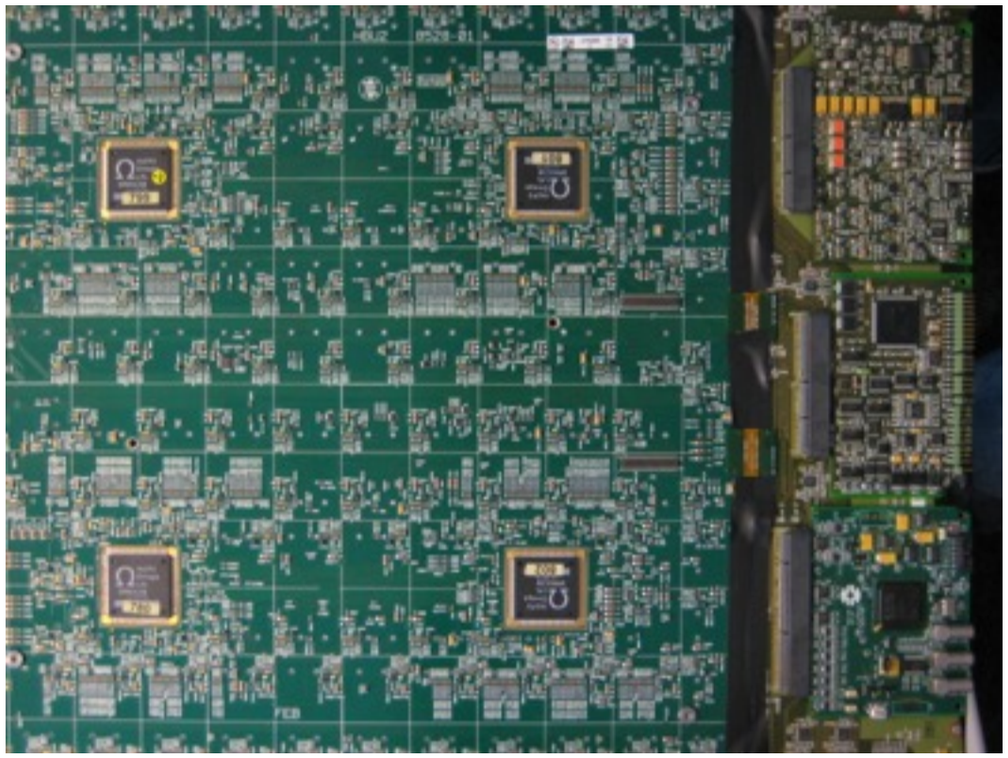






Preparation for CERN testbeam

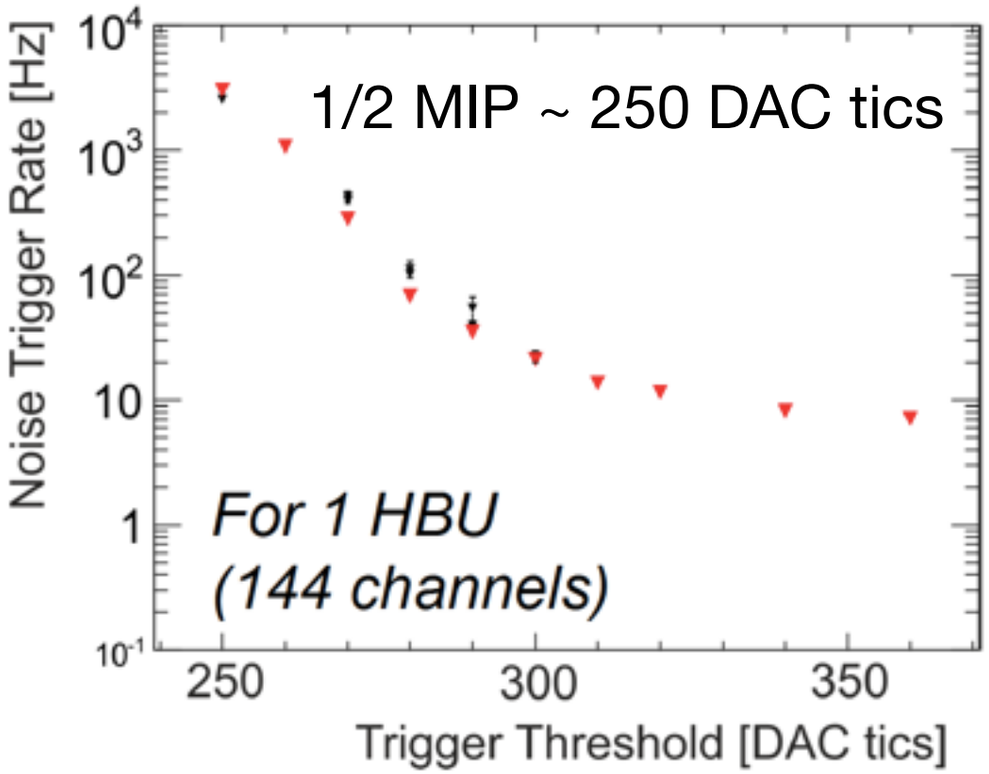




- Assemble 4 new HBUs to one full layer
  - Cassette in production
  - Side-Interface-Board is ready but not tested
  - Extender Board is ready and tested
- DIF reprogramming already finished
- Do first test at DESY testbeam
  - Calibration and readout studies for 576 channels

Preparations for CERN

- **Determine noise rate at 0.5 MIP threshold**
  - Dependence of rate on trigger threshold already measured in Lab
  - Noise is dominated by single channels (~5 channels per SPIROC off)
  - HBU noise rate is fine for ILC (SP2b:~2 of 16 cells filled by noise in 1 ms), in testbeam noise events are cancelled by **trigger validation:**
  - Would allow suppression of noise to negligible rate at CERN
  - In principle already tested successfully in Lab, want to cross check with signal from trigger scintillator



ITEP: noise of 1 SiPM @ 0.5 MIP: 7-70Hz

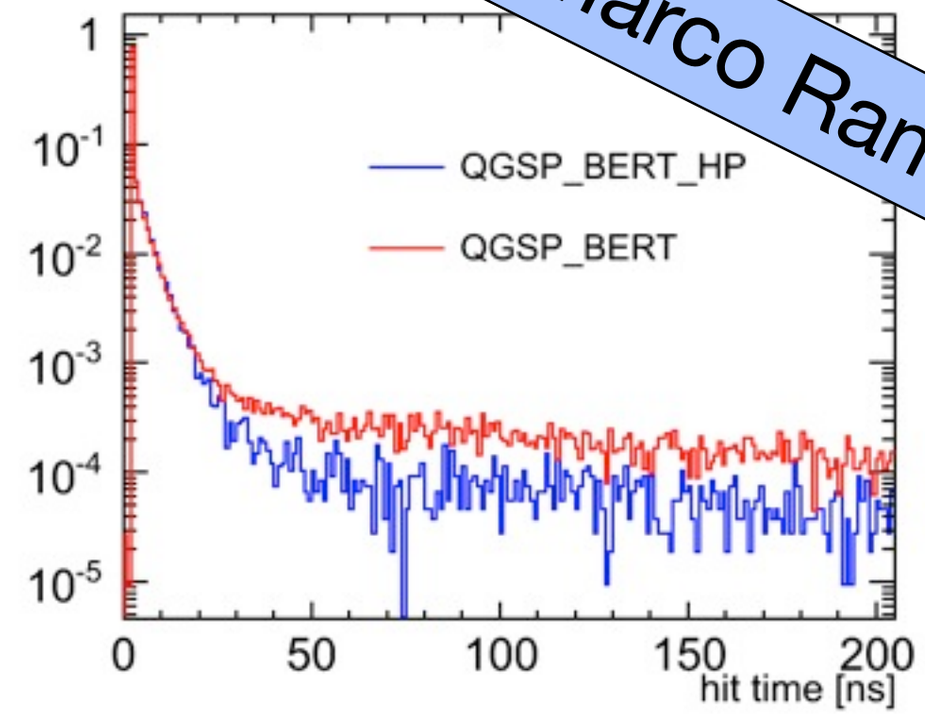
Goals for testbeam at CERN

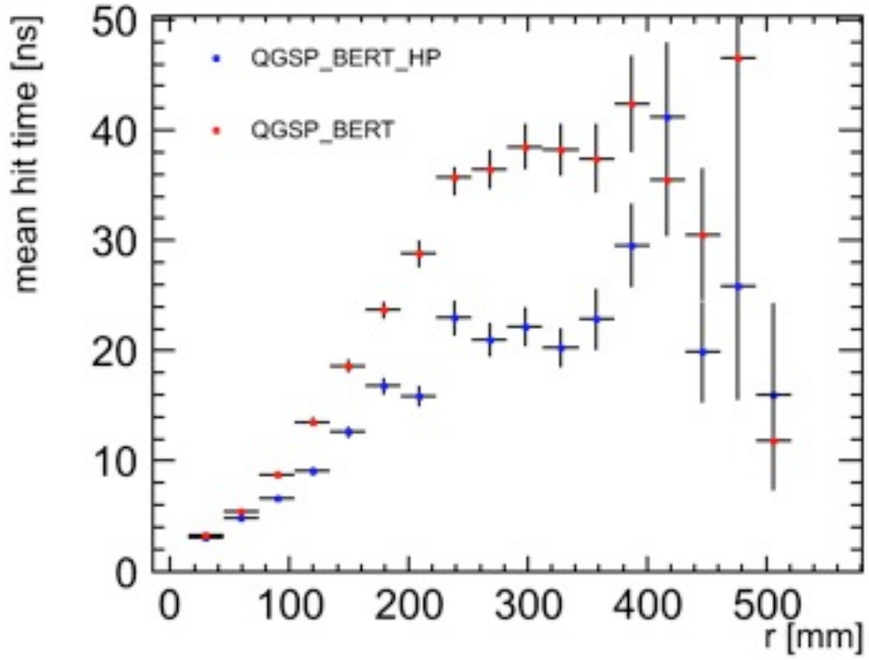
System test of prototype with 4 HBUs

Study time structure of hadron showers

- Expect differences in the time development of showers between the Geant4 physics lists
- Simulation: need O(50k) events to be able to distinguish between different physics lists

Marco Ramilli





Summary and outlook

Status:

- HBU2 plus SPIROC2b is in action and is working fine
- Function tests of multi HBUs are partially done (further tests are still on going, e.g. MIP measurements, readout studies, etc.)
- Simulation studies have started
- First tests started on SPIROC2c (still ongoing)

Plans:

- Full slab test (6 HBUs)
- Maybe small stack (~10 layers) in the future?
- Large layer test in fall at CERN

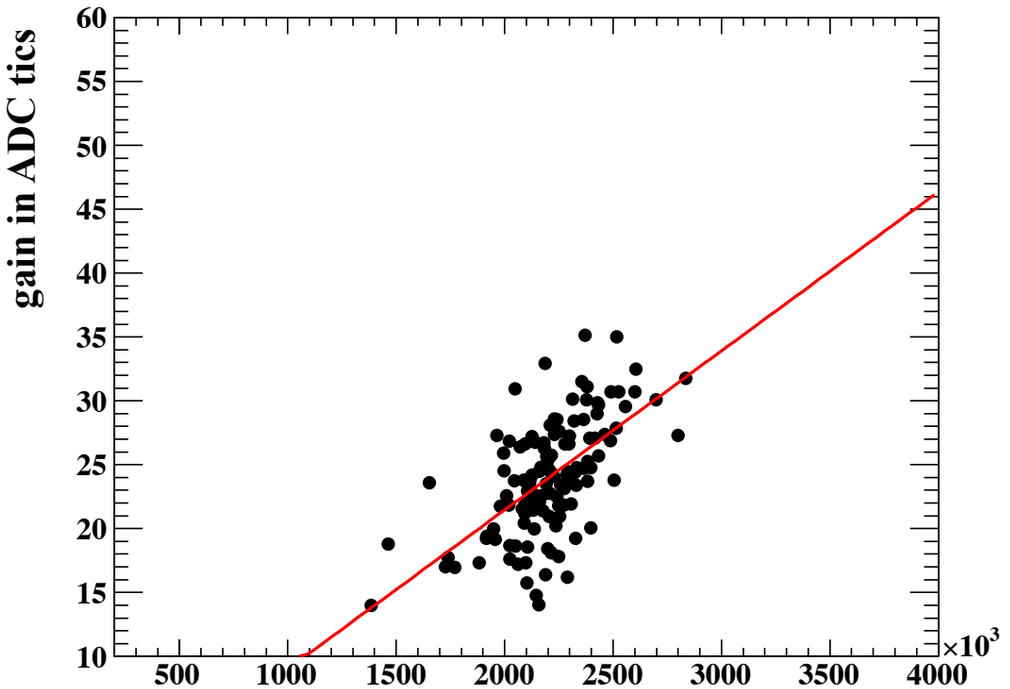
→ **Measure shower time development!**

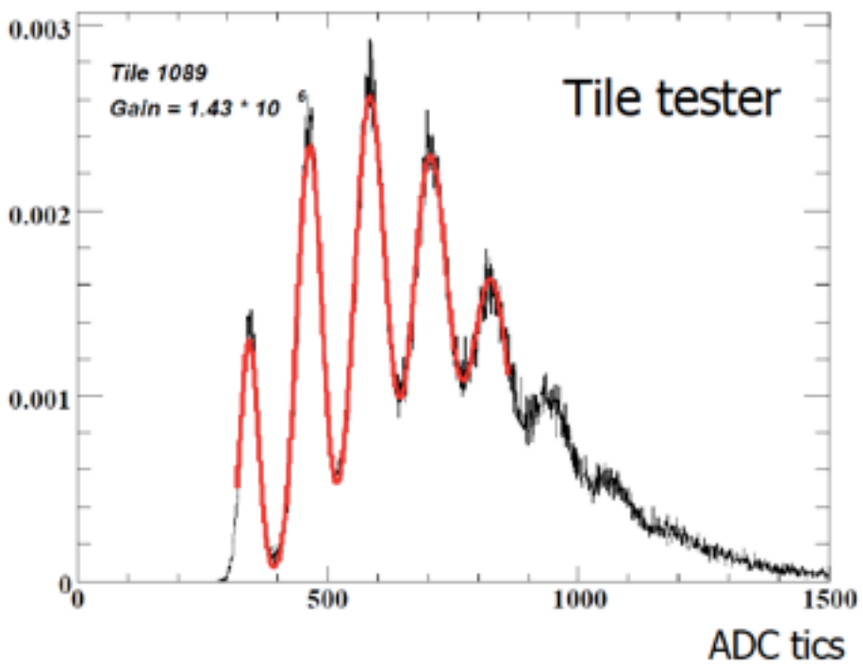
Backup

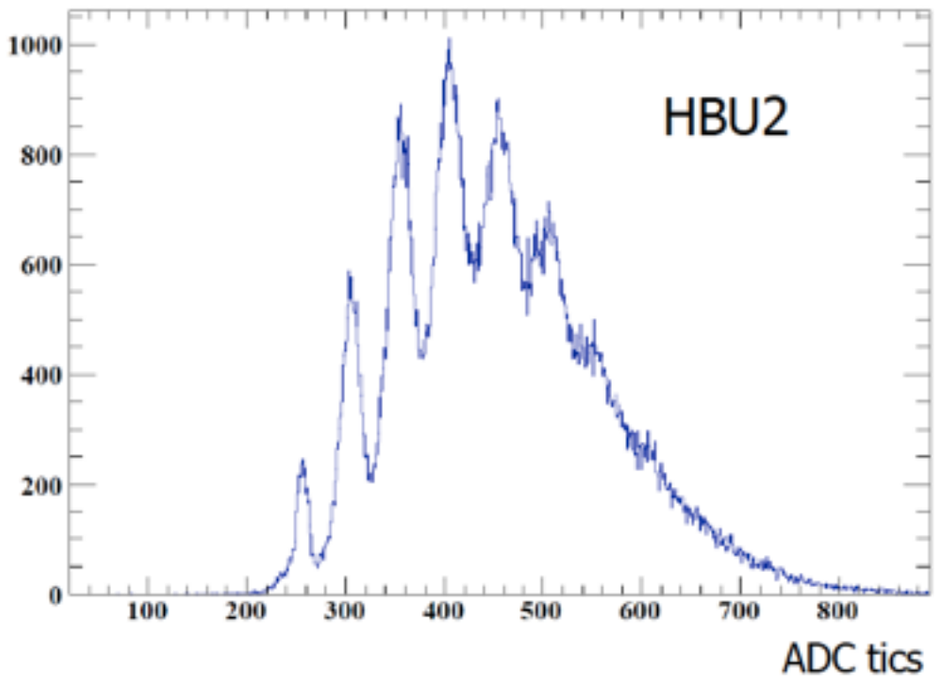
Scintillating tiles

- Single pixel spectra measured with dedicated tile tester and HBU2

→ comparable performance







Embedded LED calibration system

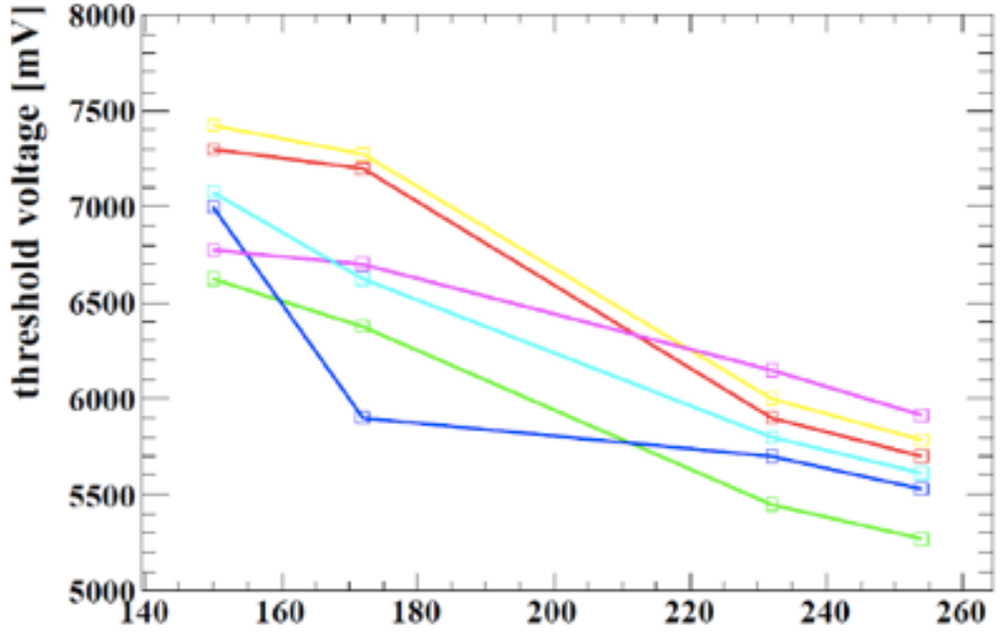
LED light output equalization:

- 4 bias capacitor combinations tested:

→ 150pF, 172pF, 252pF and 254 pF

- Measured V_{calib} where light output starts

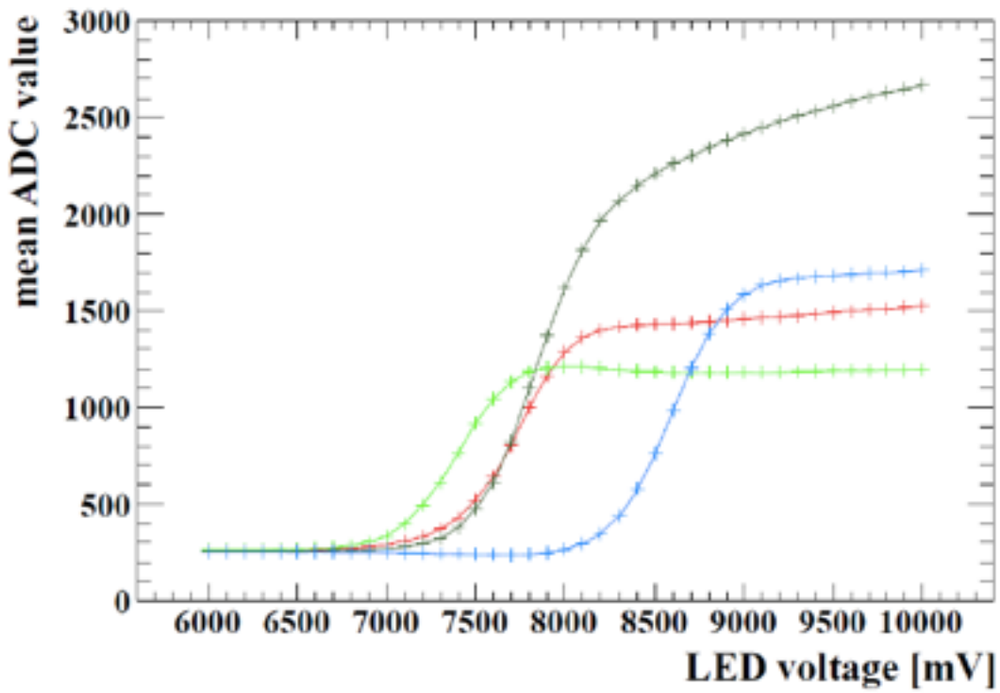
→ Improvement of LED uniformity possible!



SiPM saturation:

- Can the integrated LED system be used for SiPM saturation monitoring?

→ Tests with the new DESY electronics prove capability!



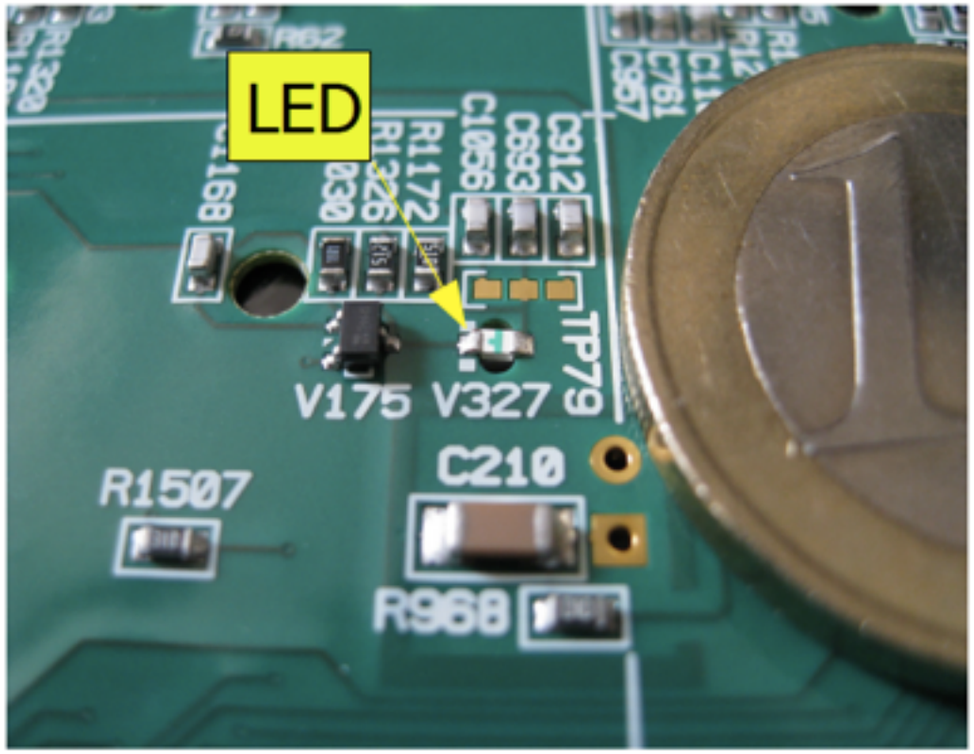
Scintillating tiles

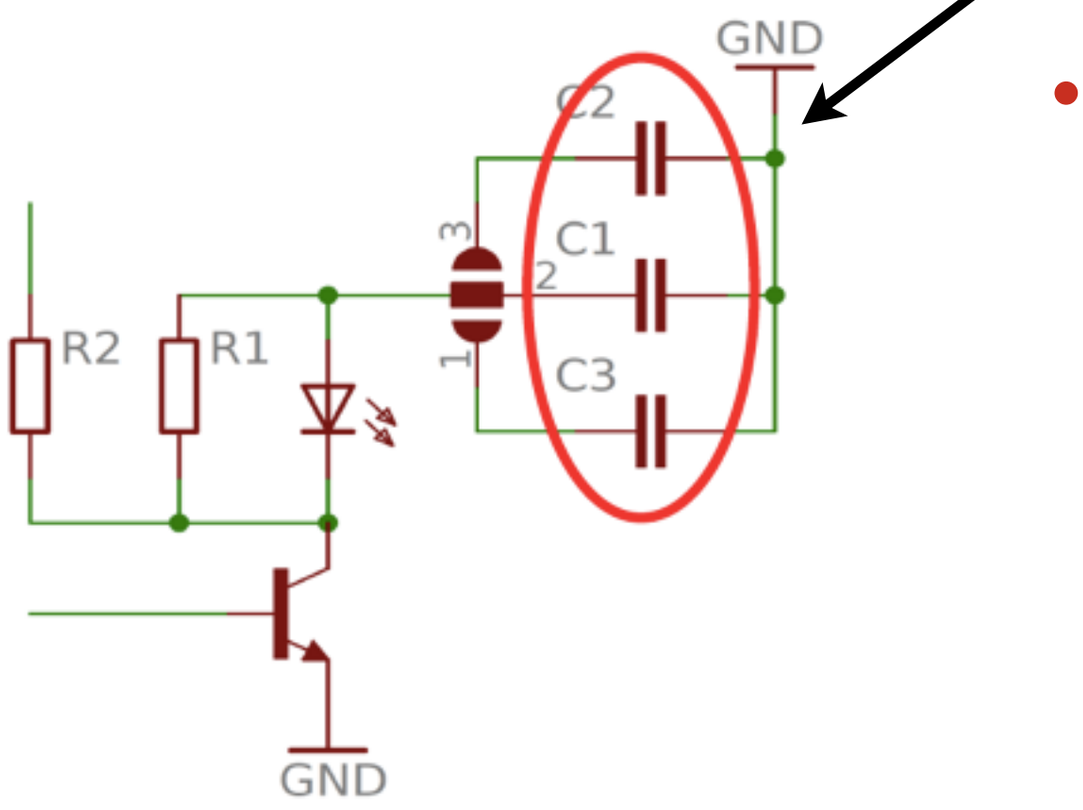
- ~600 tiles mounted below 4 new HBU2

→ Larger tests of calibration system and SiPM gain in HBU2 environment

→ Test of equalized gain and MIP measurements at DESY testbeam

LED calibration system

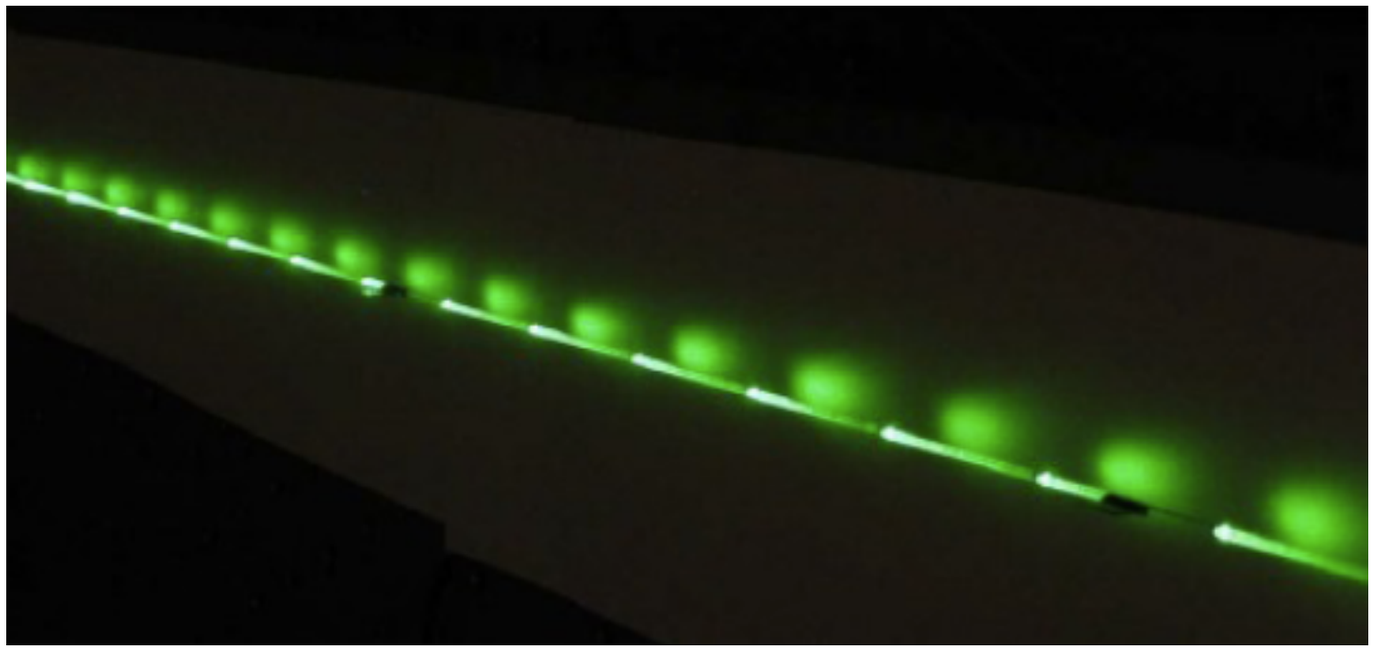




Wuppertal solution:

- Light directly coupled into tile by 1 integrated LED per channel
- Light output equalization via capacitors C1-C3 (default: 150 pF, plus: 22 pF, 82 pF)
- New design implemented in HBU2 and is currently tested extensively

LED calibration system



Prague solution:

- Light coupled into tile by notched fiber
- Mechanical integration difficult
- First test performed in DESY lab with new electronics and new tiles

Reflector foils

- New reflector foils realized (laser cutting), 4x top and bottom types
- Both types look promising:
  - → Quality
  - → Fit to HBU2