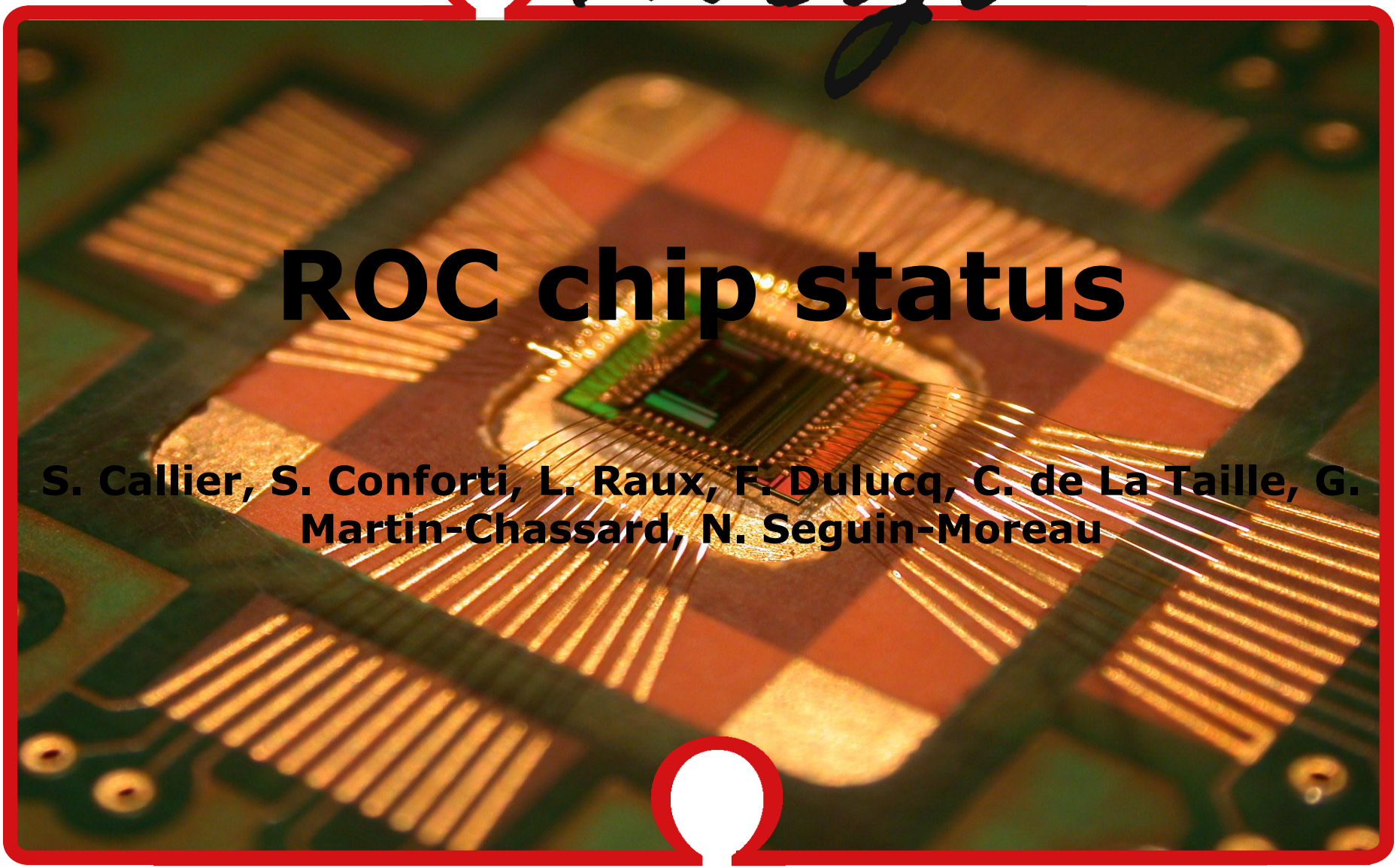


ROC chip status

S. Callier, S. Conforti, L. Raux, F. Dulucq, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau

Orsay MicroElectronics Group Associated

SUBMISSIONS SCHEDULE

- **HARDROC3**
  - First of the "3rd generation ROC chip" to be submitted
  - **independent channels**, one register/channel, I2C link for SC parameters(@IPNL), triple voting, circular memory, temperature sensor
  - Digital part finished in July 2012
  - Analog part: No major modifications in the analog part. Extension of the dynamic range to set Vth0=100fC Vth1=5pC and Vth2 > 15 pC
  - HR3 won't be pin to pin compatible with HR2 and packaged in TQFP208 instead of TQFP 160 (same size and thickness)

  ⇒ New 1 m2 RPC chamber to be built to test HR3 at the system level
  - Die size ~30 mm2
  - Chip design in its final stage. Submission in November 2013 => reception in March 2013. Aida report to be delivered in August 2013

- **SPIROC3/SKIROC3:**
  - **More complex chips (internal SCA, ADC, TDC):** many parts still to be tested on test bench and at the system level
  - Hardroc3 test feedback necessary before submitting Spiroc3/skiroc3

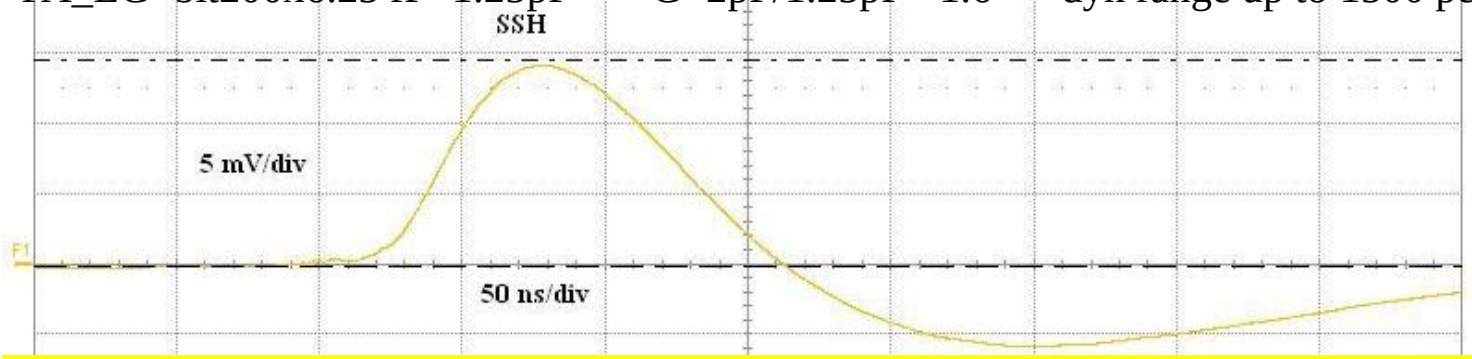
SPIROC2C towards SPIROC3

Spiroc2c: before submitting SPIROC3. Pin to pin compatible with spiroc2b so measurements can be performed at the system level using the existing HBUs

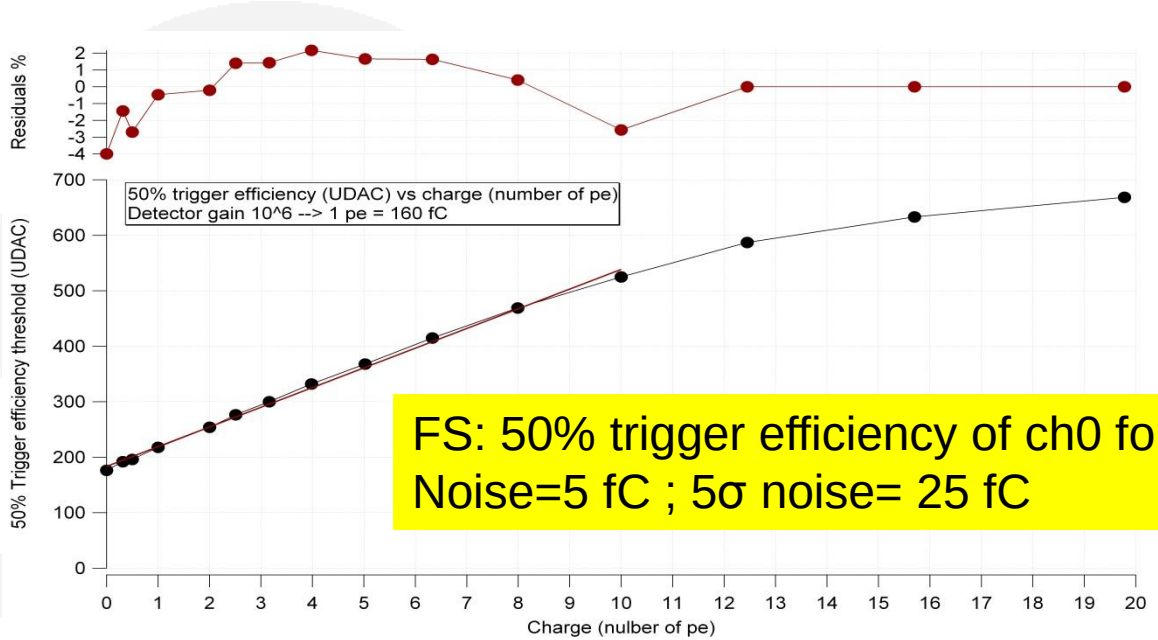
- Spiroc2c received in June 2012 and under test
- **New input preamp** (NMOS transistor instead of PMOS):
  - **pedestal shift problem in spiroc2b : CORRECTED in spiroc2c**
  - **Rate dependency in 2b: CORRECTED in 2c**
  - **Coupling HG/LG: CORRECTED in spiroc2c**
  - LG and HG preamp gain **can be changed independently in 2c**
    - HG: Cin=20pF, Cf = 6.25 fF x (1 to 255)
    - LG: Cin=2pF, Cf= 6.25 fF x (1 to 255)
- **"zero" events** pb in 2b: **CORRECTED in 2c**
- **4-bit Channel wise threshold** tuning: difficult in 2b as the tuning of one channel depends on the others. **CORRECTED in 2c**
- **New TDC** to decrease deadtime: **done**
- **New Delay box**
- Input 8-bit DAC: layout redone to improve the slope uniformity: **no difference…**

SPIROC2C: HG slow sh and FS trigger efficiency

PA_HG=bit100 x 6.25fF= 625fF => G=20pF/625fF= 32 => dyn range up to 100 pe-
PA_LG=bit200x6.25 fF=1.25pF => G=2pF/1.25pF= 1.6 => dyn range up to 1500 pe-



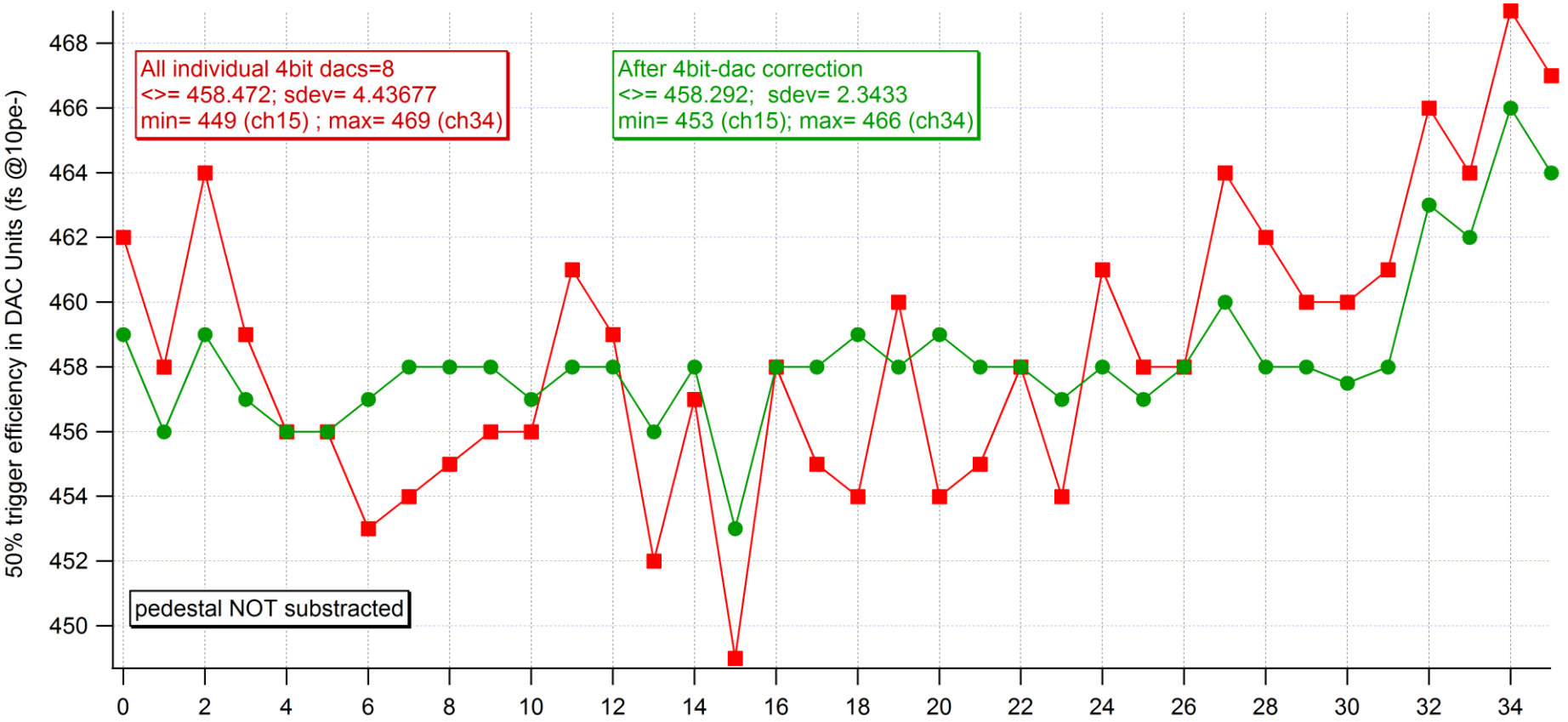
HG SSh: Vmax= 14.65 mV/pe (1pe=160 fC) RMS noise = 1.2mV = > SNR ~ 12



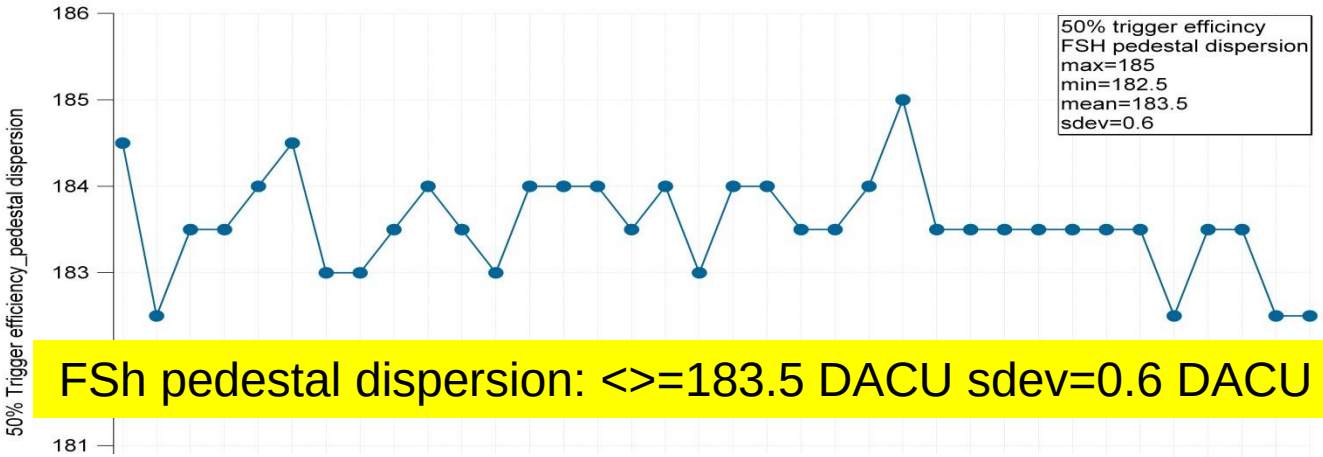
FS: 50% trigger efficiency of ch0 for various injected charge.
Noise=5 fC ; 5σ noise= 25 fC

SPIROC2C: 4 bit DAC channel wise tuning

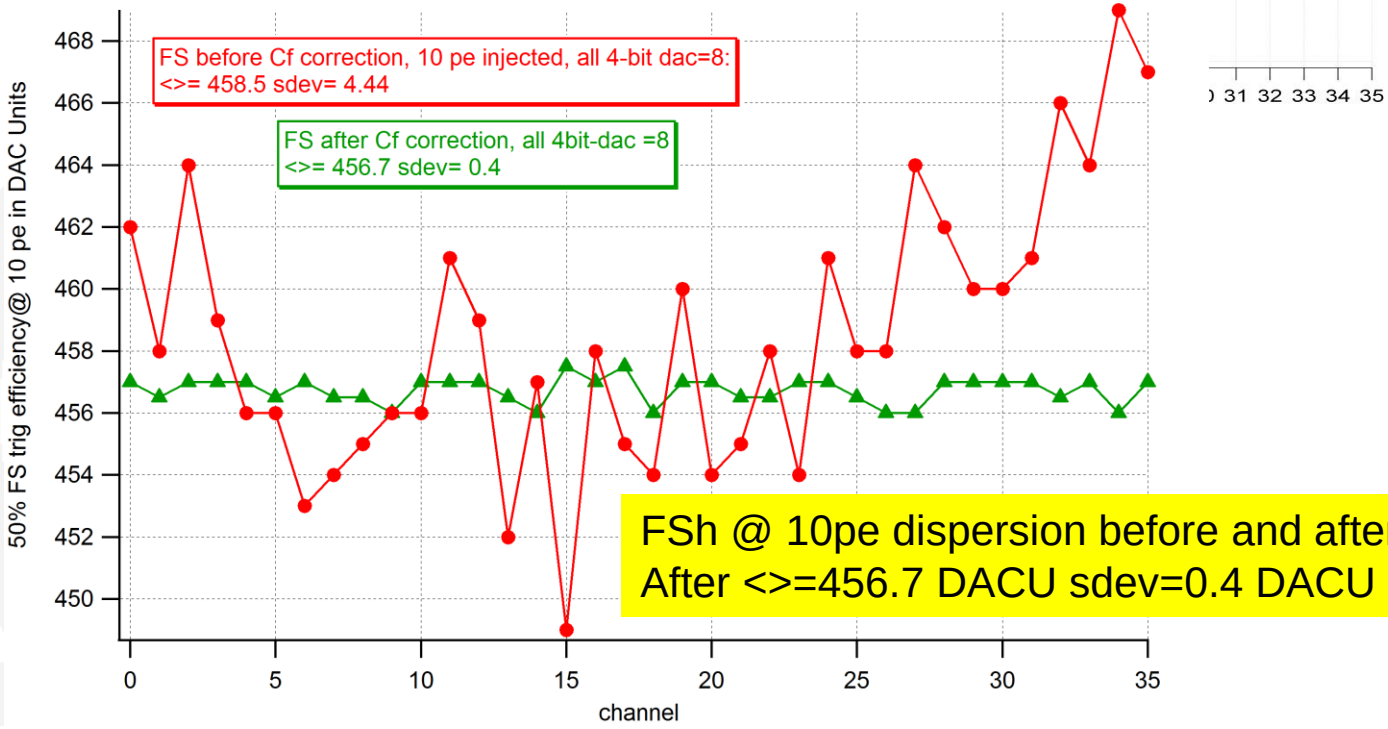
FS@ 10 pe injected



SPIROC2C: FS Uniformity and Cf correction



FSh pedestal dispersion: <>=183.5 DACU sdev=0.6 DACU



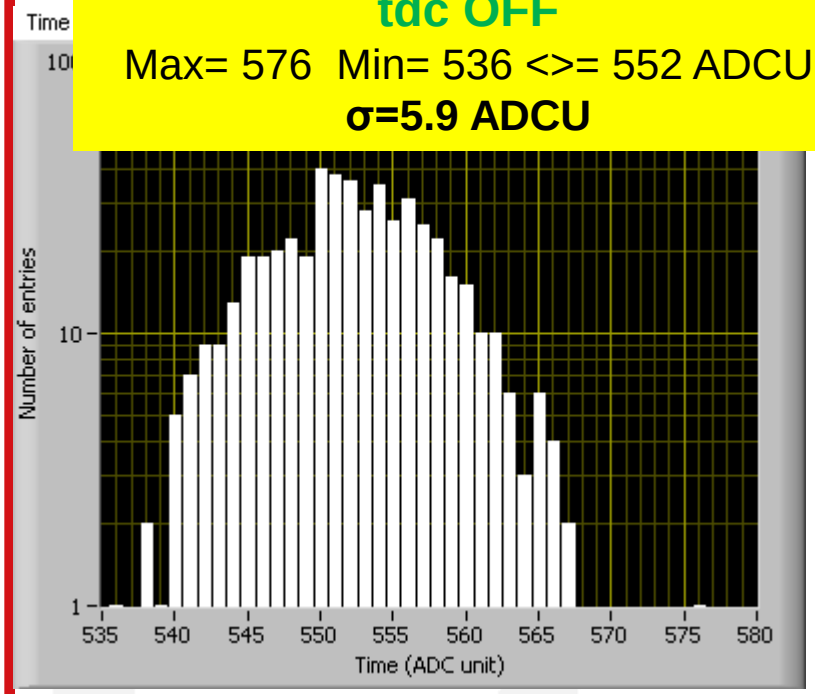
FSh @ 10pe dispersion before and after Cf correction:
After <>=456.7 DACU sdev=0.4 DACU

Spiroc2c: Digital coupling

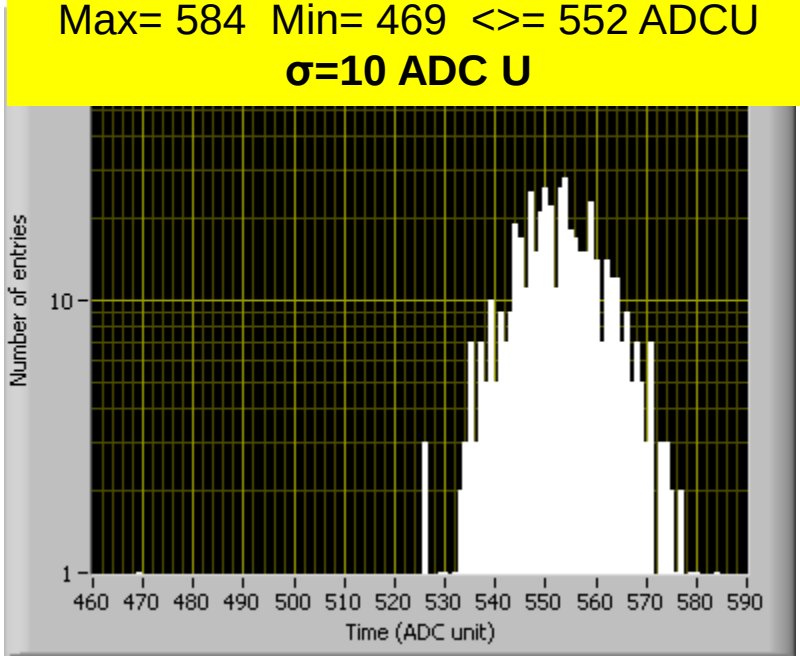
Acquisition using the autotrigger mode

Injection through 100pF, **1 pe-** (1.6V@60dB), HG Ssh @ 50ns
Cf=200fF (32x 6.25fF => G=100) for all the channels,
Vth=230 (=0.5 pe-)

tdc OFF
Max= 576 Min= 536 <>= 552 ADCU
σ=5.9 ADCU



tdc ON
Max= 584 Min= 469 <>= 552 ADCU
σ=10 ADC U



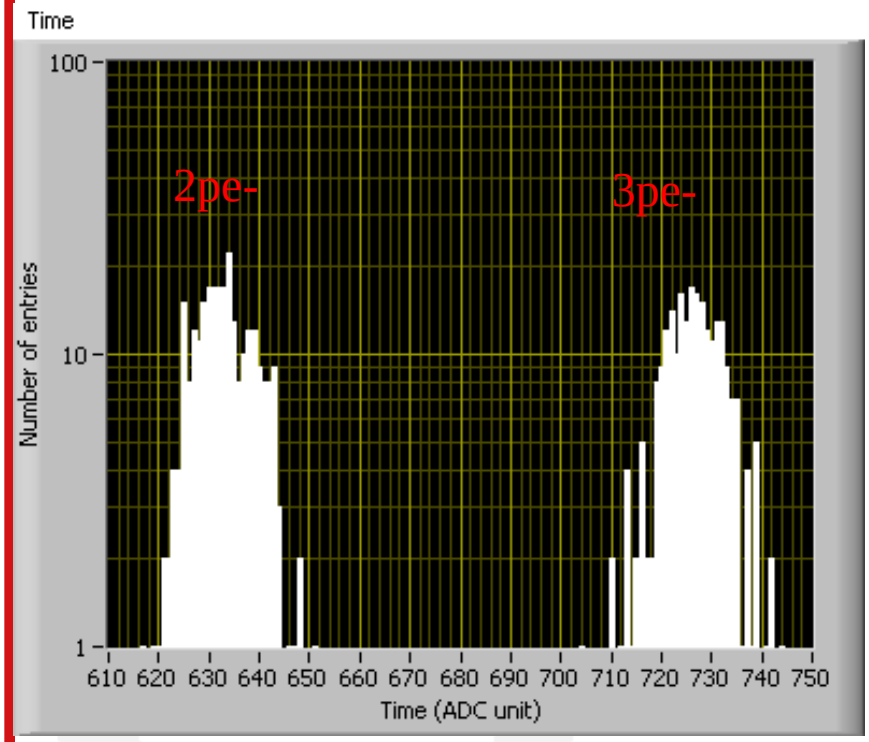
Pedestal~ 450 ADC Units

TDC => digital coupling in spiroc2c through the substrate (NMOS preamp connected to gnd)
There is no digital coupling in spiroc2b (PMOS transistor connected to vdd)

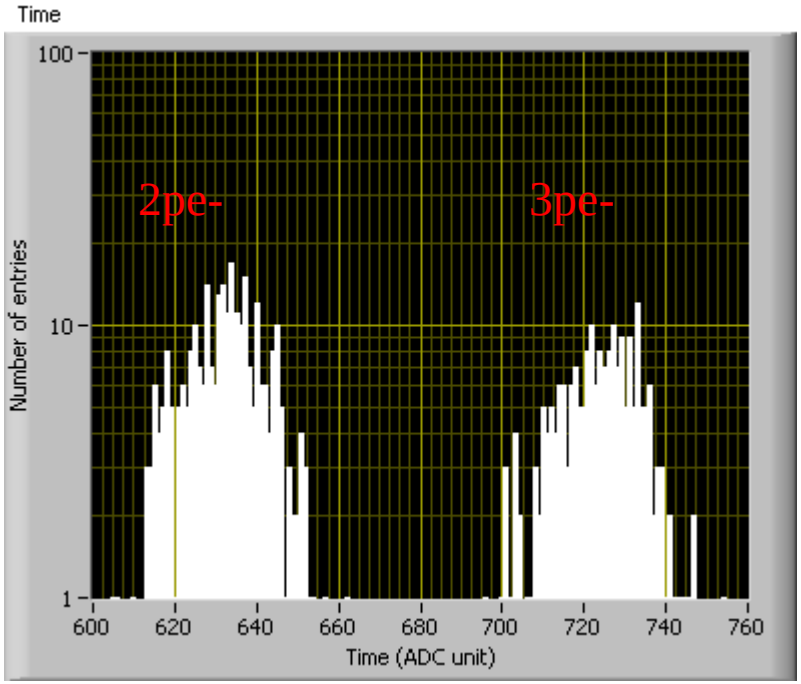
Digital coupling in Spiroc2c

Injection through 100pF, **2 and 3 pe-** , Cf=200fF (G=32) for all the channels, ssh@50ns Vth=260 (~1pe-)

HG ssh, tdc OFF



HG ssh, tdc ON



TDC coupling in Spiroc2c doesn't prevent to distinguish 2 and 3 pe-

CONCLUSION

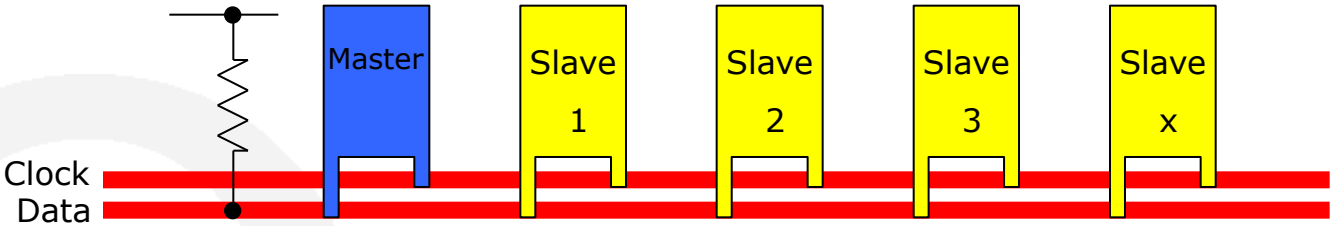
- HARDROC3: submission in November 2012

- Spiroc2c:
  - Spiroc2b “bugs” corrected
  - Very good performance of Spiroc2c when the TDC is OFF
  - BUT DIGITAL COUPLING through the substrate which prevents to set the threshold < to 1pe.
  - Anyway it would be interesting to equip HBUs with spiroc2c and check the performance in TB conditions
  - Many measurements to be done on testbench

BACK UP Slides

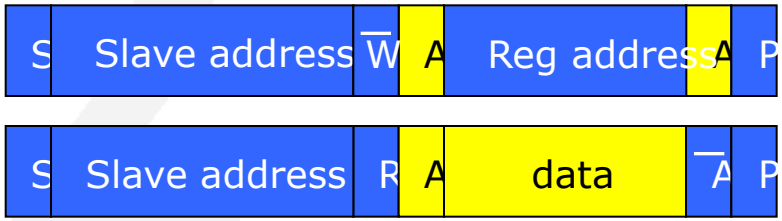
3Gen ROC chips: common features

- Slow control parameters:
  - Backward compatibility with 2Gen ROC chips slow control
    - Use of classical shift register slow control
  - Embedded I2C
    - 7-bit address + 1 general call address (127 chips can be addressed)
    - Access port doubled
    - Bidirectional data line with open collector (Driver will be the same as Dout)
  - Read back capability of SC bits (non destructive)



- Write frame:

- Read frame:



3Gen ROC chips: common features

- Extra pin needed for I2C / SC:

HARDROC 2		HARDROC 3	
ShiftReg_In	1	ShiftReg_In	1
ShiftReg_Out	1	ShiftReg_Out	1
ShiftReg_Clk	1	ShiftReg_Clk	1
ShiftReg_Rst	1	ShiftReg_Rst	1
		ShiftReg_Loadb	1
		ShiftReg_ReadBack	1
		Error_Triple_Voting	1
		7-bit I2C @	7
		2 x (SCL / SDA)	4
		Select_I2C_Port	1
		Clk_I2C_SR	1
		Rstb_I2C	1
		Select_I2C_SR	1
Total	4	Total	4+18

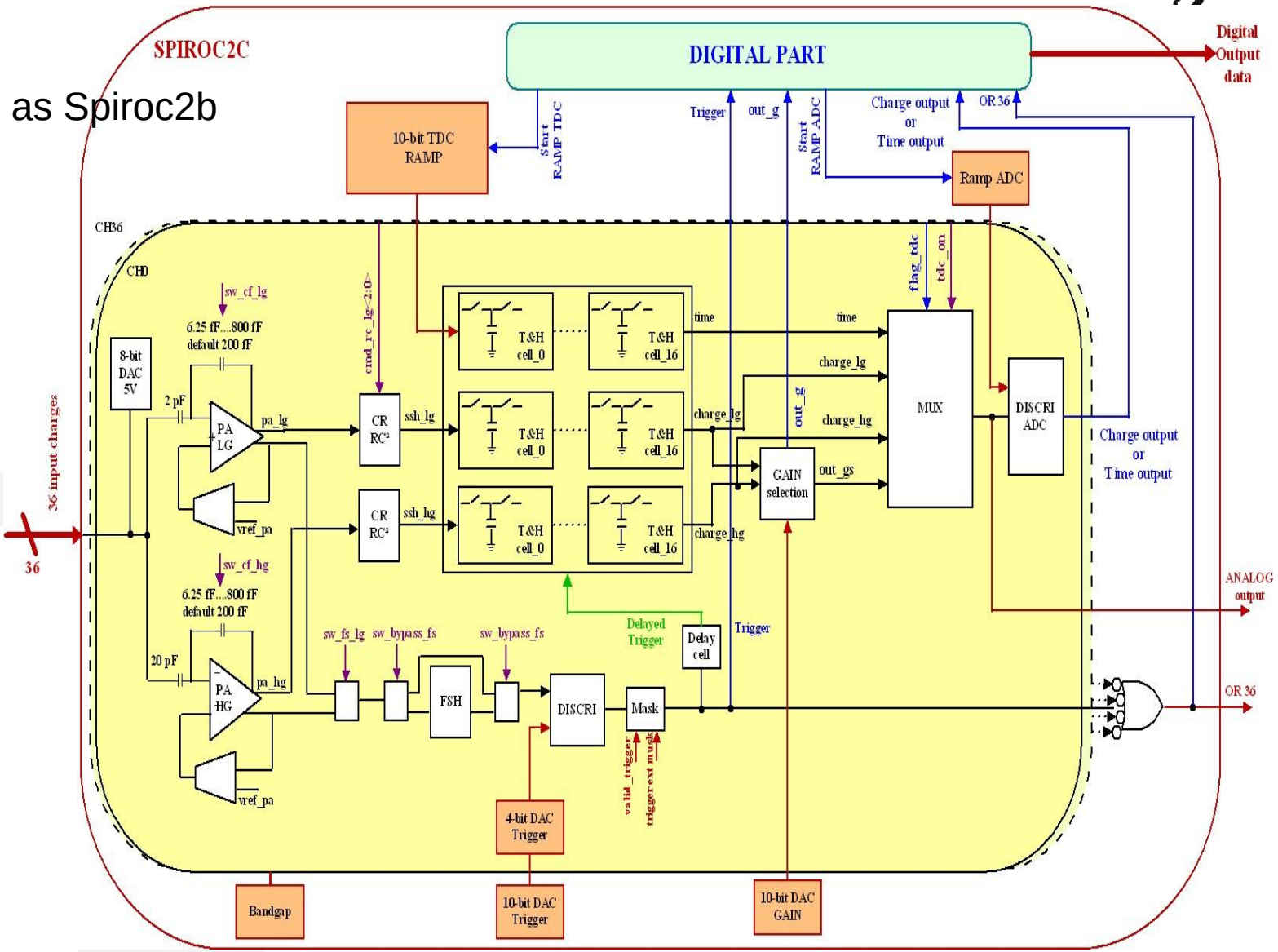
Standard SC

SC with triple voting

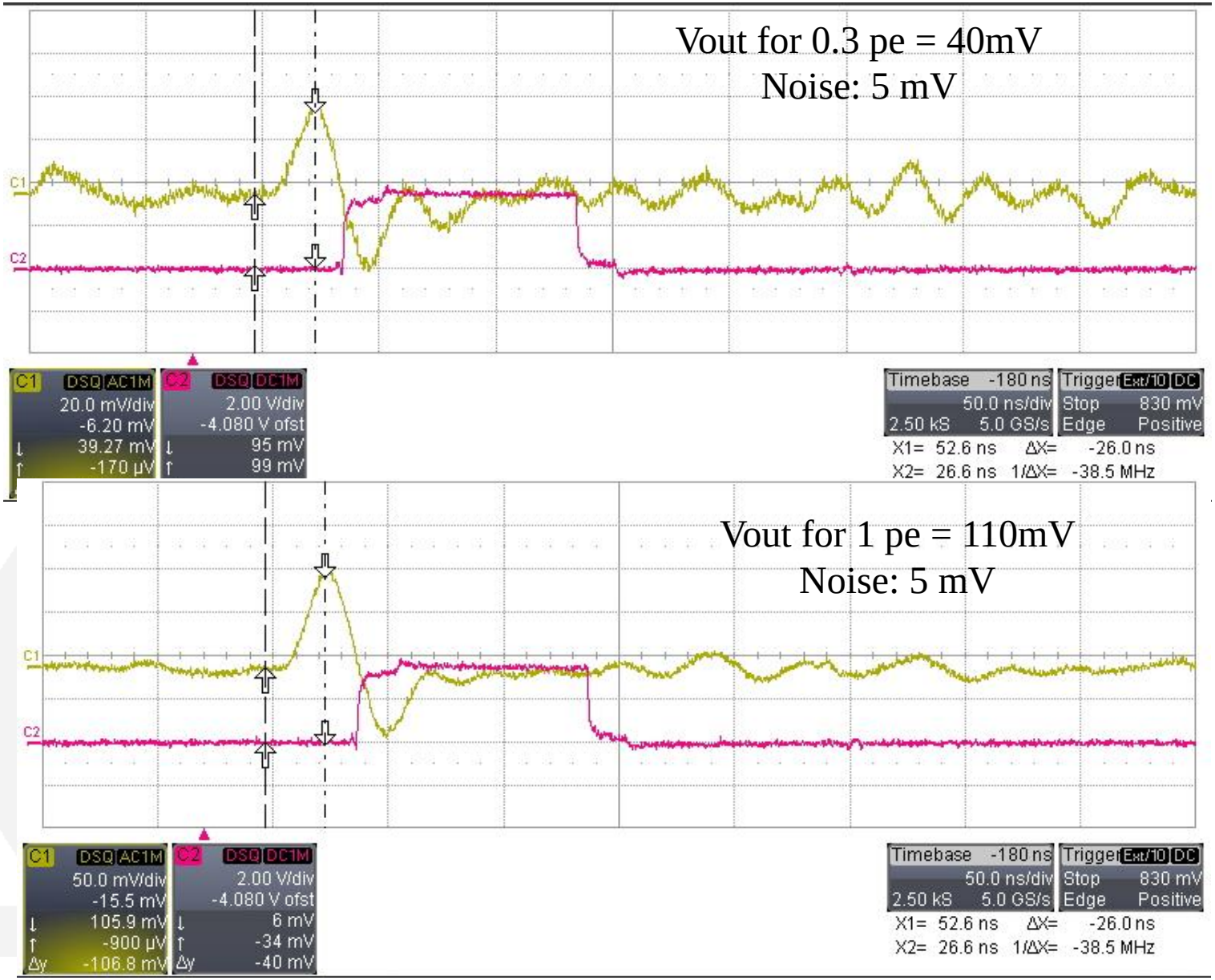
I2C

Selection I2C or std SC

Same pinout as Spiroc2b



FS @1/3 and 1pe, Cf=32x6.25fF=200fF



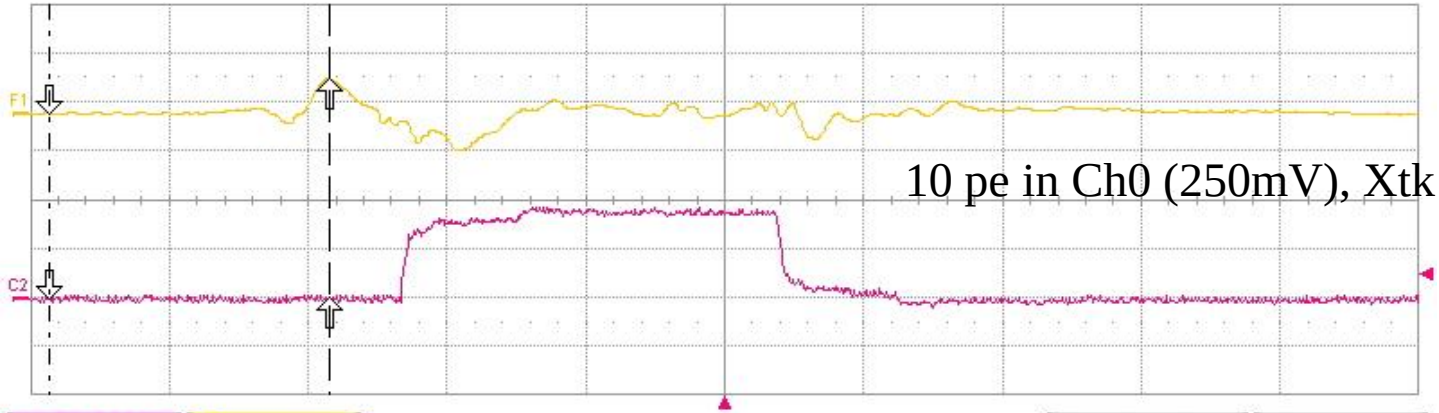
« Pedestal shift » due to coupling on Vdda_pa on spiroc2b

Spiroc2c: Injection of 10, 100, 300 and 1000pe- in ch0 and measurement of the charge (HG) seen on the neighbours (all preamp on but all discris masked except of ch<0>:

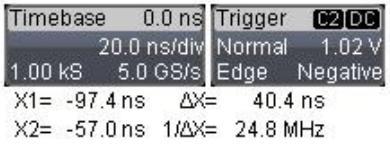
	10pe-	100pe-	300pe-	1000pe-
Ch<0>	950 UADC	3500	3500	3500
Ch<1>	470	470	450	450
Ch<2>	470	460	440	440
Ch<3>	460	463	446	446
Ch<20>	460	457	450	450
Ch<35>	455	457	455	455

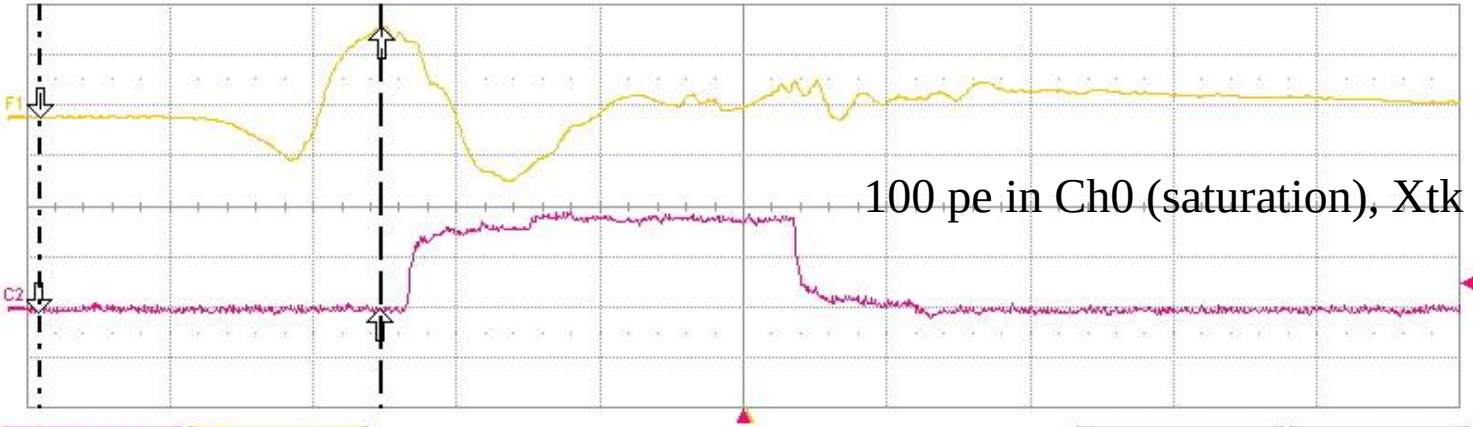
When discris of the other channels are ON => we measure Xtk in the neighbours

SPIROC2C: Xtk

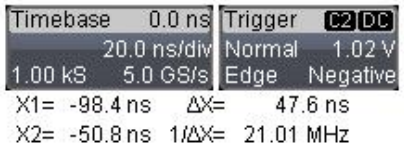


10 pe in Ch0 (250mV), Xtk in Ch1=3.5mV

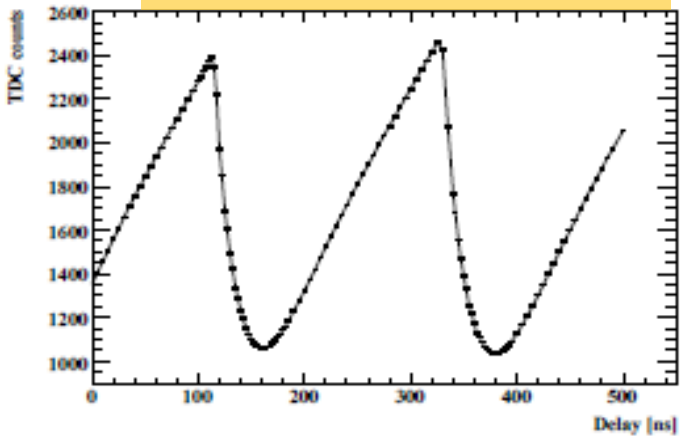


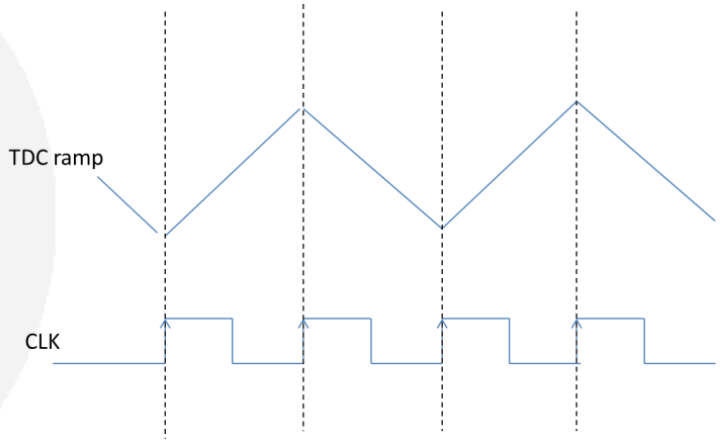


100 pe in Ch0 (saturation), Xtk in Ch1=10 mV

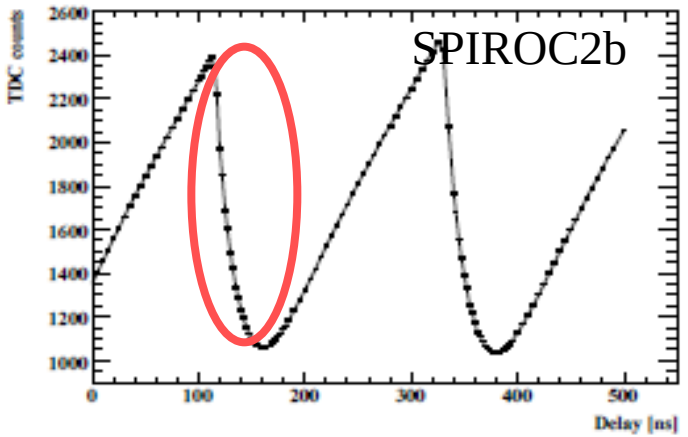


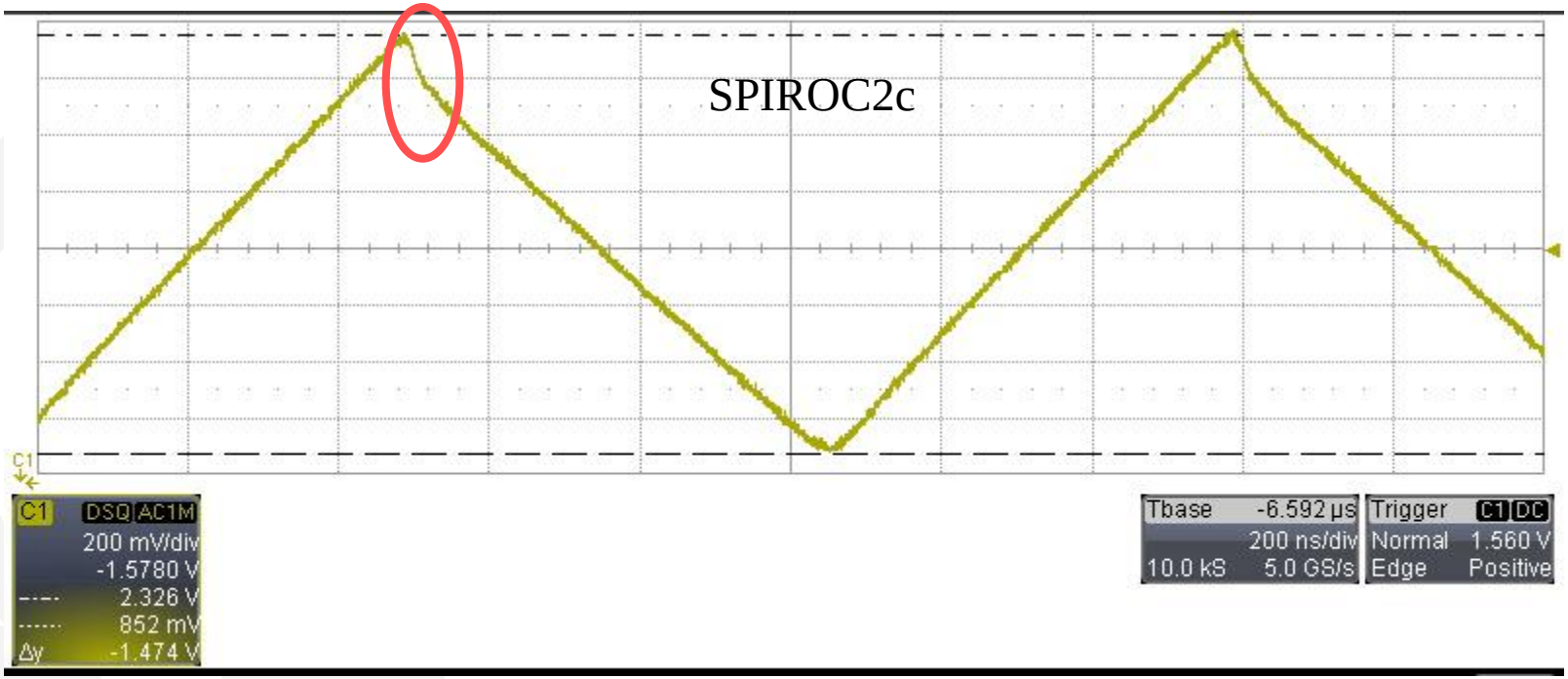
- Modifications of the TDC
  - To decrease dead time during transition => alternation of a rising and a falling ramp implemented
  - Conservative modification
  - a new TDC has to be re-designed in SPIROC 3



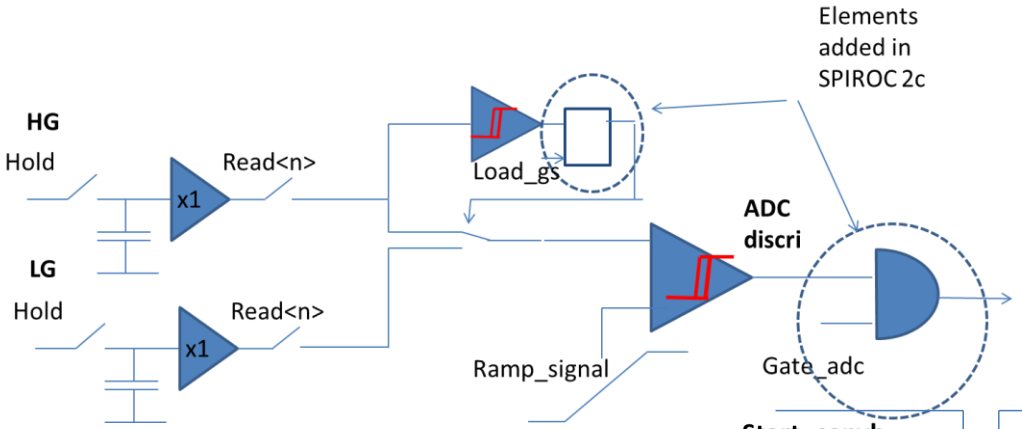


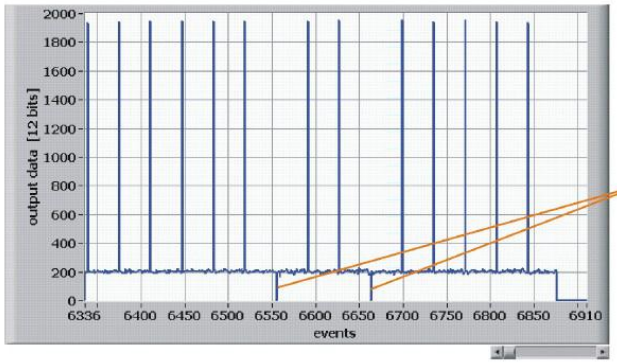
- Deadtime reduce with the tdc integrated in spiroc2c



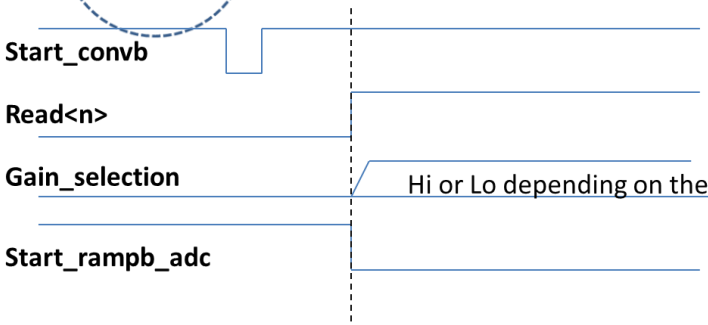


SPIROC 2c: Zero event bug

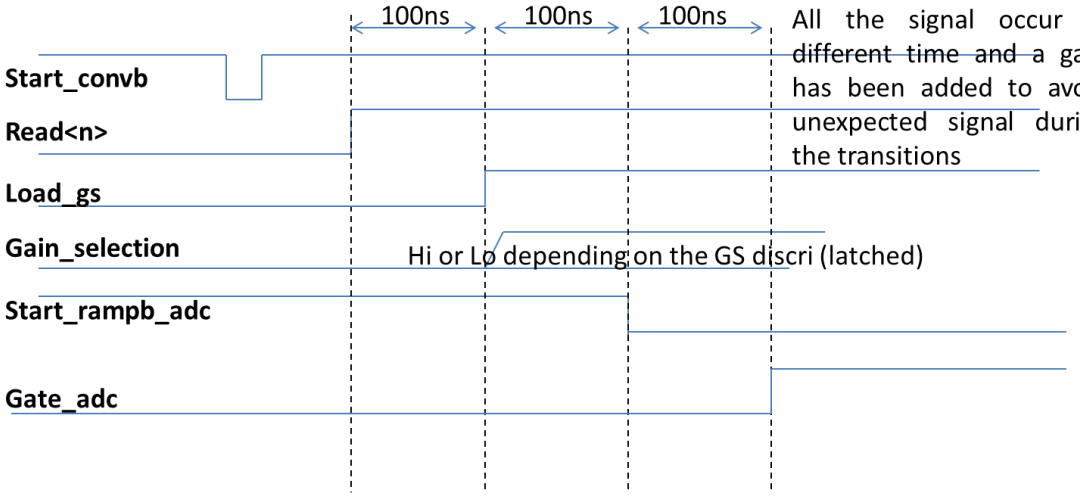




- "zero event" occurs randomly
- **Problem solved in SPIROC 2c**
- No major change in the digital part D-flip-flop, a gate on ADC discri and delays on control signals

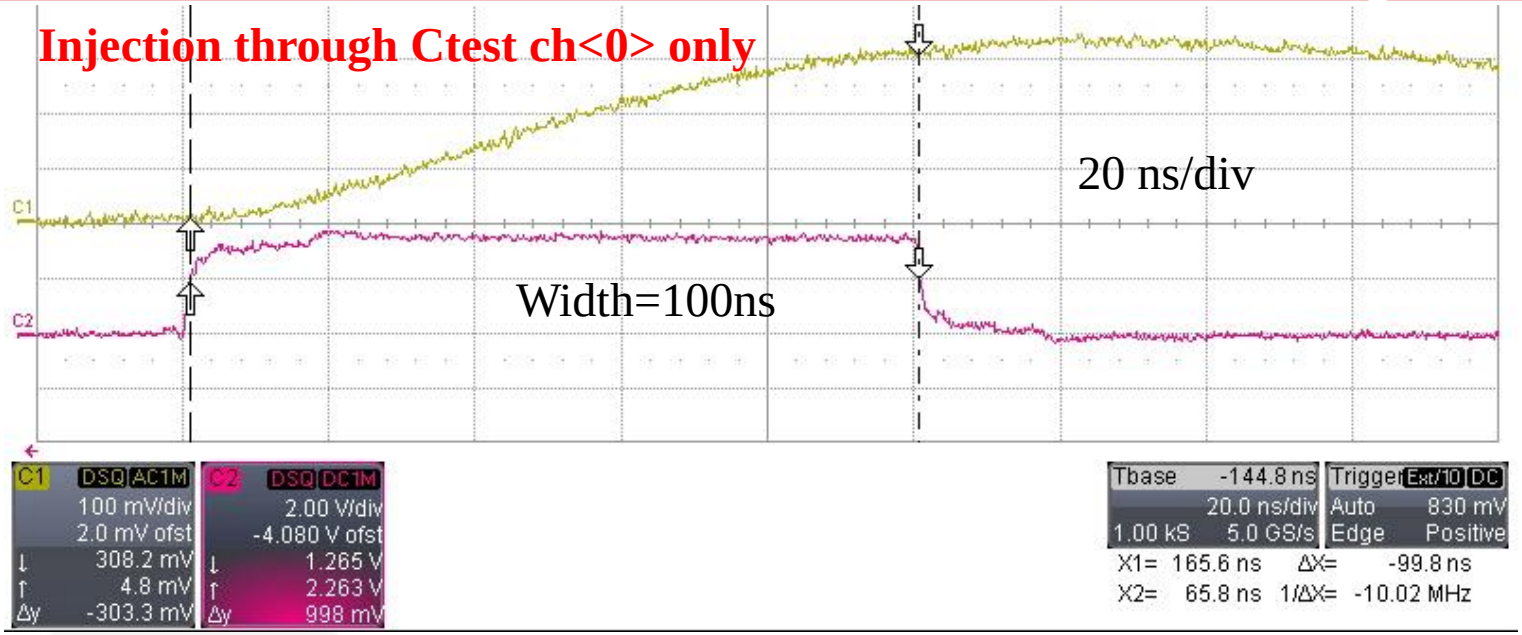


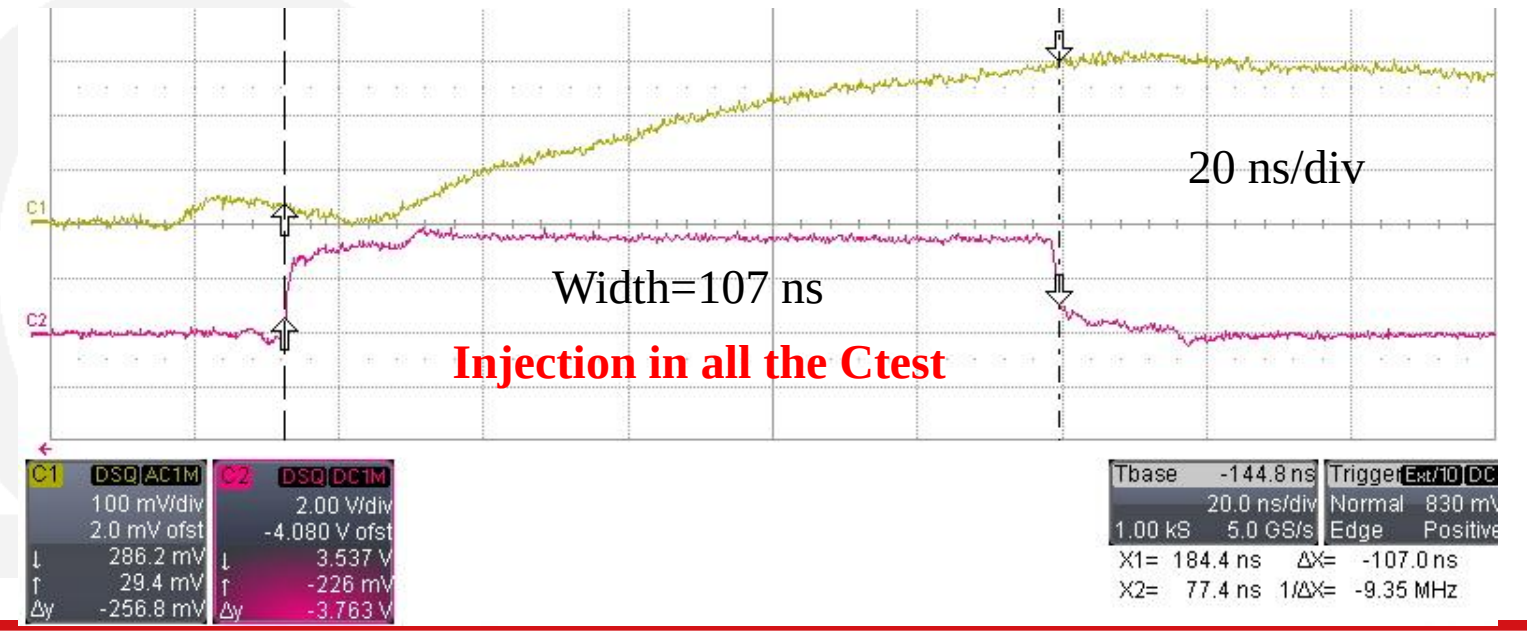
Situation in SPIROC 2b
All the signal occur at the same time



Situation in SPIROC 2c
All the signal occur at different time and a gate has been added to avoid unexpected signal during the transitions

SPIROC2C: New Delay box





SPIROC2C: HG SSh linearity using the acquisition mode