AHCAL LDA Concept

André Welker

Bruno Bauß, Volker Büscher, Reinhold Degele, Lucia Masetti, Uli Schäfer, Rouven Spreckels, Stefan Tapprogge, Rainer Wanke

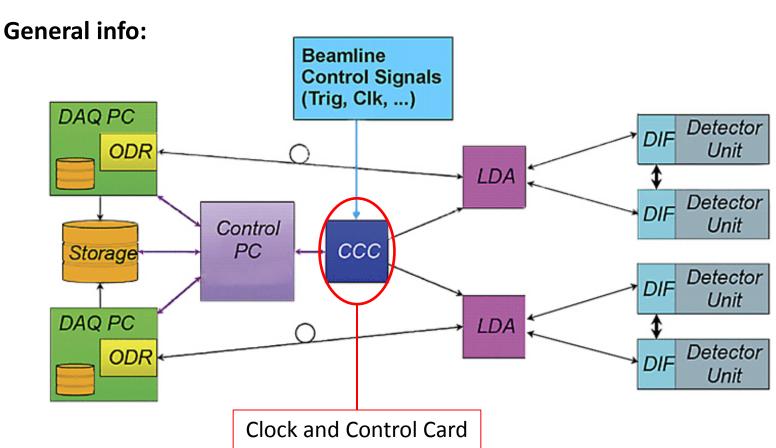
CALICE Collaboration Meeting Cambridge, Sept. 18, 2012





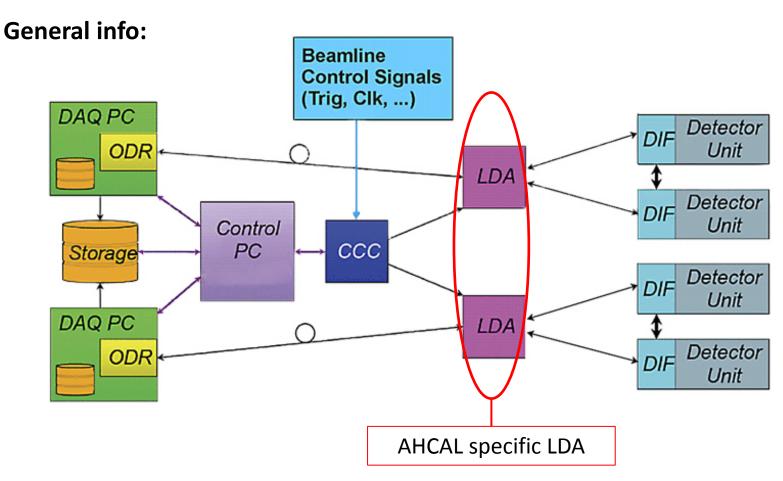
Readout chain





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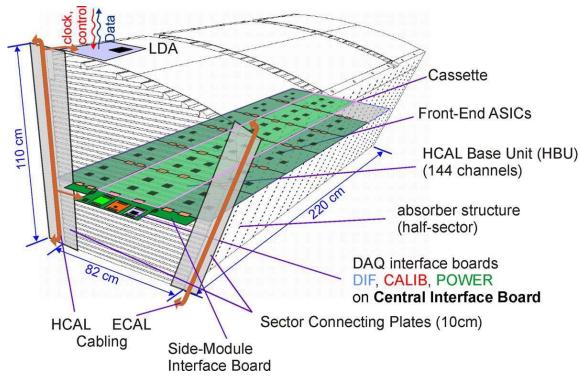


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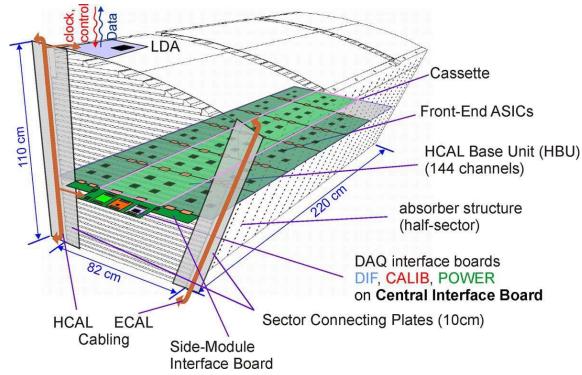
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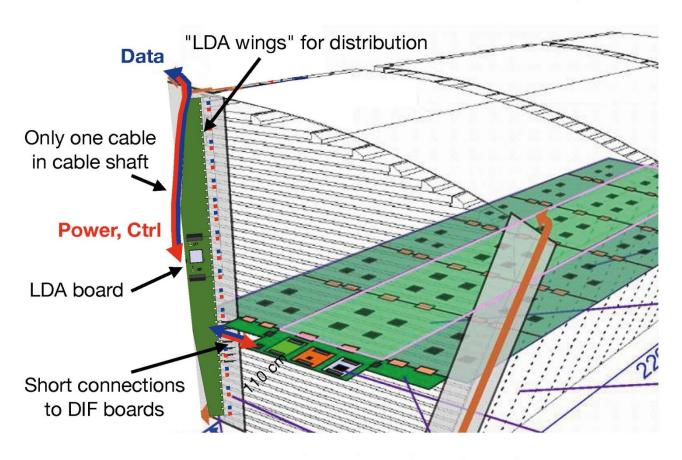
Disadvantages of the current layout:

- 1. Very limited space between AHCAL and coil for the LDA:
- 2. Many HDMI cables need to be routed through the cable shaft:





Proposal: Put LDA board inside or on the top of the cable shaft:





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1. Three passive PCBs:

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mezzanine to simplify upgrades of FPGA/processor.



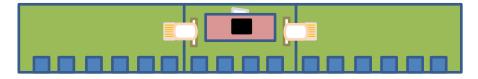
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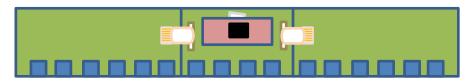
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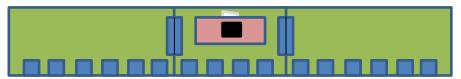
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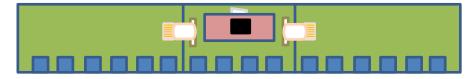
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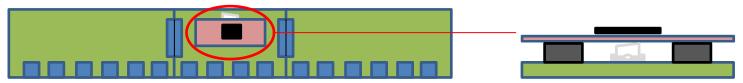
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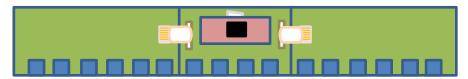
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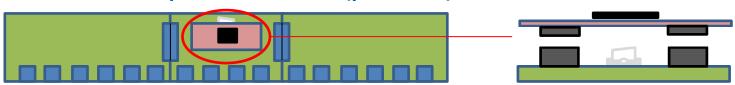
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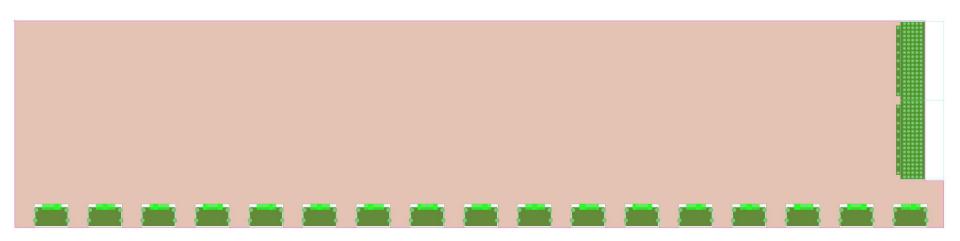
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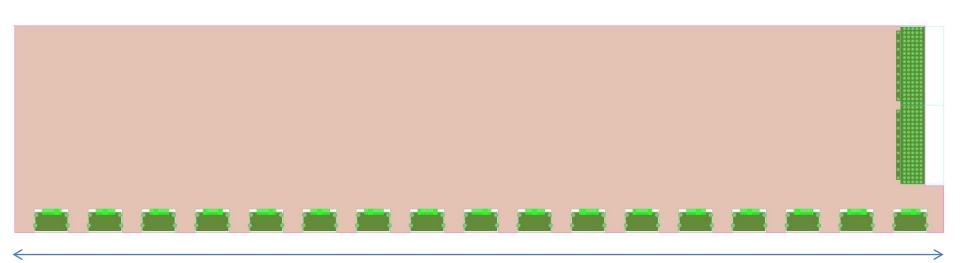
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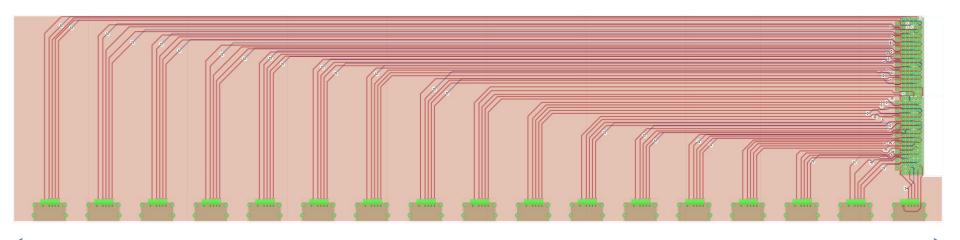


450mm



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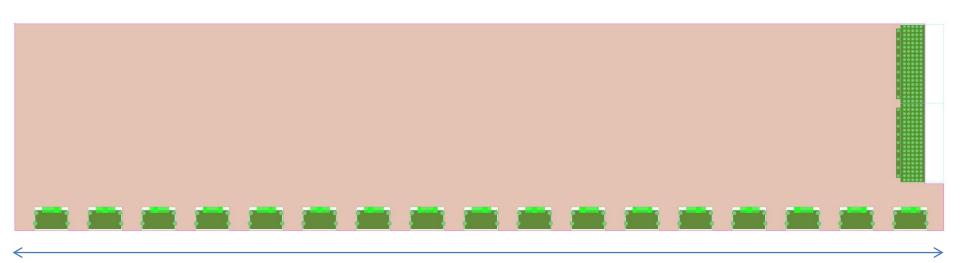


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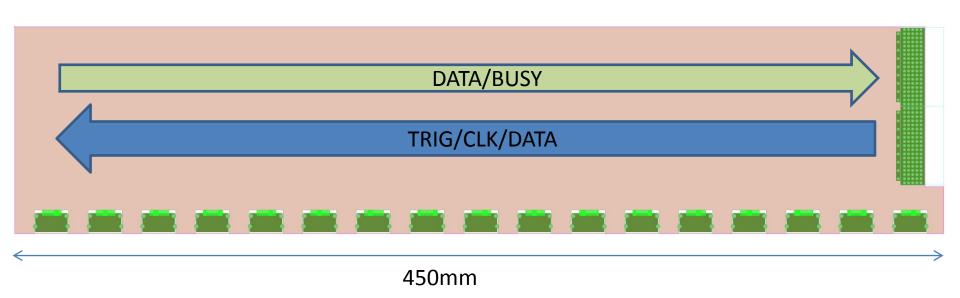
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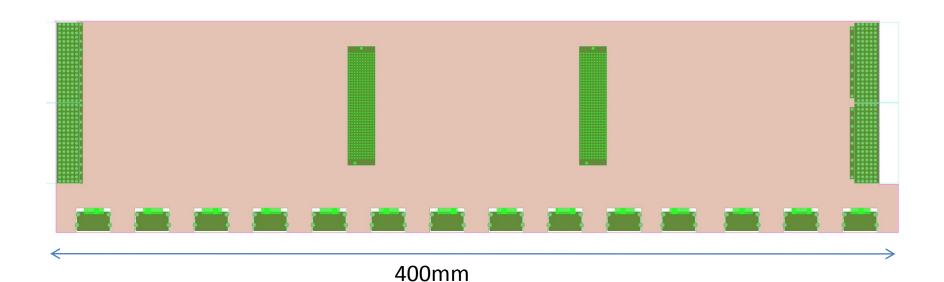
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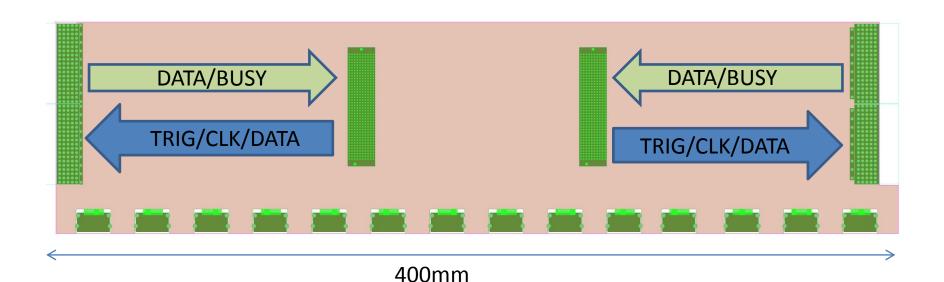
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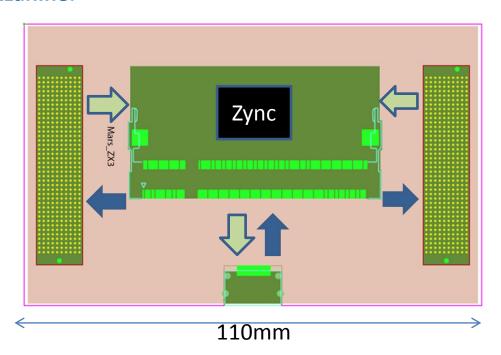
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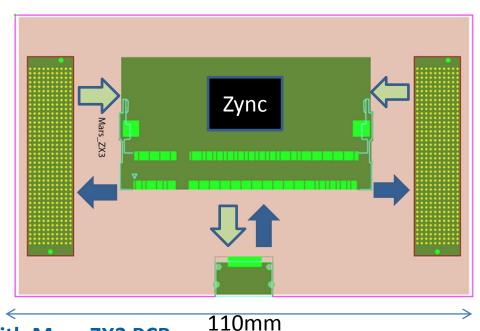
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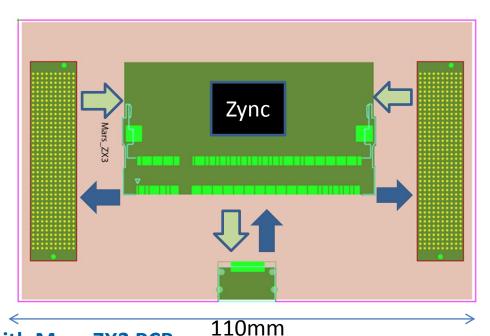
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New Xilinx FPGA/processor (108 I/Os), needed 490



The three PCBs:

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- 1. First test with Mars-ZX3 PCB:
 - New Xilinx FPGA/processor (108 I/Os), needed 490
- 2. Later with a FPGA/processor who can handle more I/Os:



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 - Where are the screw holes?
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- 7. Install and operate in AHCAL test beam.

The goal is to be ready before Christmas and for the next test beam.